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Analysis and design of DC-link capacitor in cascaded H-bridge multilevel active front-end converter

Muhammad Shehroz Malik

Department:

ANALYSIS AND DESIGN OF DC-LINK CAPACITOR IN CASCADED H-BRIDGE MULTILEVEL ACTIVE FRONT-END CONVERTER

by

MUHAMMAD SHEHROZ MALIK

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Approved by:

Dr. Jonathan Kimball, Advisor
Dr. Mehdi Ferdowsi
Dr. Pourya Shamsi

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ABSTRACT

Medium-voltage grid-tied systems often use a cascaded H-bridge multi-level active front-end. In this converter, dc link bus capacitors play an important role in stabilizing the converter and enabling both active and reactive power injections. The present work provides analytical expressions for the capacitor current, which are essential for optimizing system design (especially capacitor size vs. lifetime). Then, the expression is incorporated into the grid connected bidirectional power system model. Consequently, this work contributes to the guiding principles to choose accurate dc link capacitor ratings against grid-side power delivery requirements.

DC-link capacitors come with an expiration date which is dependent on the operating power and voltage values. Lack of information about the lifetime of the dc-link capacitor creates uncertainty in the duration of online operation of the converter, thus increasing the probability of a contingency outage. The lifetime of the capacitor can range from only a few seconds of online operation of the station due to under-sizing, to a compromised quality of power flowing through other solid state devices which may not have been designed for the transients that are caused by over-sizing of the dc-link capacitor. A better estimate of the lifetime of these capacitors can help maximize usage and maintain scheduled outages more efficiently, without disruption in service.

ACKNOWLEDGMENTS

This thesis was made possible with help from a number of people. I want to thank my parents for their relentless support and patience in getting me to where I am today. I would thank my sisters who turn bad days into good ones.

I am thankful for my thesis committee members, Drs. Ferdowsi and Shamsi for their teaching and encouragement. I am grateful for my colleagues and friends in and out of the lab at S&T. Thanks to Kartik and Angshuman, who continue to inspire me academically. I am grateful for Michele and Gideon for their fireside chats and traits that I will always look up to.

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Lastly, perhaps this page is a way of marking the time I spent with my advisor. I am grateful for his expertise and kindness, which associate me with him beyond time.

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1. INTRODUCTION

This thesis is motivated by a research project at Missouri S&T, called Extreme Fast Charging (XFC) enabled by Energy Storage. There are multiple industry and academic partners in the team working towards developing a faster off-board electric vehicle charging station.

In efforts towards planet sustainability, in the past decade battery-powered electric vehicles have become globally abundant. With growing number of electric vehicles (EVs), the need for infrastructure that supports these vehicles has become equally important. This infrastructure spans from vehicle charging stations to compatible road networks down to system operational costs for stakeholders. An EV end-user wants recharging times at least equivalent of the amount of time it takes to refill gasoline cars to travel the same amount of miles in a reliable manner. On the other hand, there are significant unanswered questions from the utility operations side as a significant financial investment is drawn from load-forecast. The load forecast data for EVs is still being compiled. Therefore, research efforts are being made to strengthen the adoption of EVs.

For electric vehicles market to be a durable business, it is imperative that the infrastructure be upgraded systematically. While electric sedan market has exploded in the past five years, the commercial electric vehicles, which are majority of the fuel consumers, have only been seen in the advanced customer orders of EV manufacturing companies.

One major reason why electrification of vehicles is experiencing more lab-to-market time is because of its charging needs. Either, electric vehicles demand an inconveniently large amount of power from generation sources or, the charging times are impractically long. From an operational standpoint, for an electric-vehicle based business, like a bus fleet, critical questions about when to repair and maintain the powertrain are still being answered.

The research project at Missouri S&T is focused on developing an off-board charger. A less common type of charger can be categorized as an on-board charger. An on-board charger comes in variants of wireless and wall-outlet based wired chargers whose power electronics sits inside the vehicle. An off-board charger is referred to as the type of charger which has dedicated power electronics outside the vehicle and only the pack is housed inside the vehicle, so called the XFC station. The overall aim of the project is to develop a medium-voltage and high power (1.15 kV / 1 MW) three phase charging station that demonstrates charging of regular-vehicle sized battery packs under 10 minutes. This target is an aggressive 75% reduction in charging time (empty to full) from today's fastest charging solution in the market. Today, the hard questions about manufacturing and supply of EVs in the gasoline-based market have been answered significantly. However, fast chargers are still only found in the lab testbeds. The "supercharger" of one of the leading EV companies today is rated at 350 kW, which has also been rolled back in various parts of US because of its brown-outs. From another point of view, a 500 kW induction motor found in the a traditional gas-fired power plant is a known load to the grid since half a century but a 350 kW charger is not.

Therefore, this project approaches the problem by research in all domains. The mechanical design of the battery pack is being reconsidered to explore thermal flexibility in various charging schemes at higher charging rates. Since the charging station is drawing power from the grid, the power systems team is looking at worst-case scenario of the stress on the grid at full load to inform the compensation commands to the power electronics system.

Not only does the introduction of EVs and their grid-connected chargers create the upgrade problem, but it also offers solutions to those problems. The power electronics group is focused on designing the converters that drive the power back and forth of the vehicles, energy storage, and the grid in a stable manner to achieve the objectives.

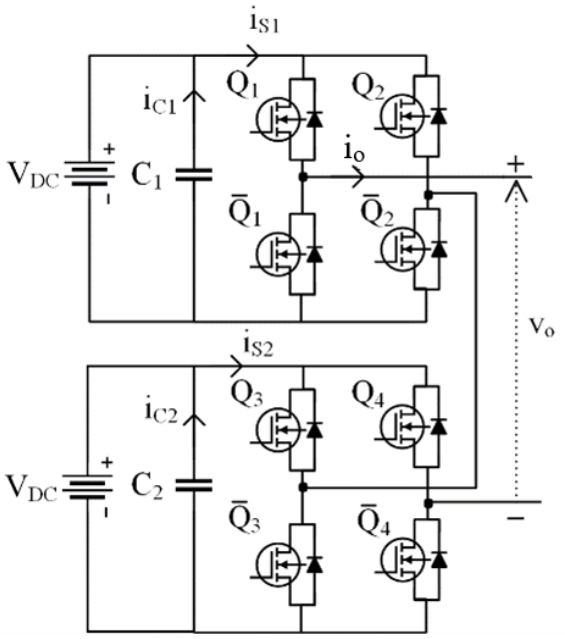


Figure 1.1. Two modules cascaded to form a five-level ac-dc converter

The station has an active front-end, which includes a cascaded H-bridge multilevel ac-dc converter, and an isolated dc-dc dual active bridge (DAB) converter. As an alternative to the DAB dc-dc converter, research is also being carried out in resonant dc-dc converters.

This thesis is focused on the active front-end and specifically the dc-link capacitor in the cascaded H-bridge multilevel ac-dc converter as illustrated in Figure 1.1.

The illustration shows the cascaded converter with two H-bridges with their ac and dc sides. (The full-scale topology of the converter used for the station has seven H-bridges per phase). The multilevel voltage output is shown on the right as v_o, depicting the ac-side of the converter. The dc-side on the left is modelled by battery and dc-link capacitor. The battery can be replaced with the DAB extension that actually connects with the pack and the ac-side's voltage v_o can be further visualized to extend its connection with the grid. A two-converter topology is useful not only because of the isolation advantages of using the DAB, but also because if it were a single ac-dc converter based charger, the stress on the dc-link capacitor could be impractically high. The dc-dc stage shares the stress that would

otherwise be on the dc-link capacitor against the same amount of power. Similarly, using more than one H-bridge distributes the V_{DC} into multiple modules, thus offering flexibility for application-specific bus-voltage configuration.

Cascaded H-bridge multilevel ac-dc converters are well suited for this application. On one hand, each H-bridge module provides independent dc-service to the energy storage thereby making it reliable in case one of the modules goes out of operation. On the other hand, the converter is capable of providing services on the ac-side, like reactive power compensation while active power is being drawn from the grid. The dc-link capacitors, shown in Figure 1.1 as C_1 and C_2, play a central part in enabling these features and stabilizing the operation. If the capacitor is not sized appropriately, design requirements like dc-bus voltage ripple may be violated which carries its effects onto unexpected saturation of the high frequency transformer and violation of ratings of other solid state devices. So the question that is setup in this thesis is, what is the appropriate rating of the dc-link capacitors against grid-side power delivery requirements.

This work comprises of two research papers. The first paper quantifies the dc-link current in those capacitors assuming that the ac-side current, i_o, is sinusoidal. Then, the derivations are used to map the grid's active and reactive power to the stress on these capacitors. These derivations are based on natural sampling of the phase-shifted carrier PWM, which is an ideal version of the modulation.

In the second paper, the exact expression for the dc-link current is again derived and the grid's active and reactive powers are mapped to the stress on dc-link capacitors. The derivations are based on symmetric and regularly sampled phase-shifted carrier PWM, which is implementable on the digital processor in contrast to the natural sampling PWM. Furthermore, the assumption that i_o is sinusoidal is discarded. Therefore, the second paper provides a more accurate framework for quantifying the dc-link current because i_o is typically not sinusoidal due to the filter cut-off frequency. A complete framework has been

provided that provides contributions of each ac-side harmonic towards the dc-link current. Consequently, true rms of the current in the dc-link capacitor can be calculated against a grid power command.

PAPER

I. ANALYTICAL EXPRESSION FOR DC LINK CAPACITOR CURRENT IN A CASCADED H-BRIDGE MULTI-LEVEL ACTIVE FRONT-END CONVERTER

Muhammad Shehroz Malik, Jonathan W. Kimball
Department of Electrical & Computer Engineering
Missouri University of Science and Technology
Rolla, Missouri 65409
Email: mm2c2@mst.edu, kimballjw@mst.edu

ABSTRACT

Medium-voltage grid-tied systems often use a cascaded H-bridge multi-level active front-end. In this converter, dc link bus capacitors play an important role in stabilizing the converter and enabling both active and reactive power injections. The present work provides analytical expressions for the capacitor current, which are essential for optimizing system design (especially capacitor size vs. lifetime). Then, the expression is incorporated into the grid connected bidirectional power system model. Consequently, this work contributes to the guiding principles to choose accurate dc link capacitor ratings against grid-side power delivery requirements. The analytical results have been validated with detailed simulations and hardware results.

1. INTRODUCTION

A cascaded H-bridge ac-dc converter consists of more than one full-bridge, depending on the number of voltage levels needed on the ac side. Therefore, to begin with, the building block of the converter alone is illustrated in Figure 1 and is referred to as a module in the cascaded system ahead.

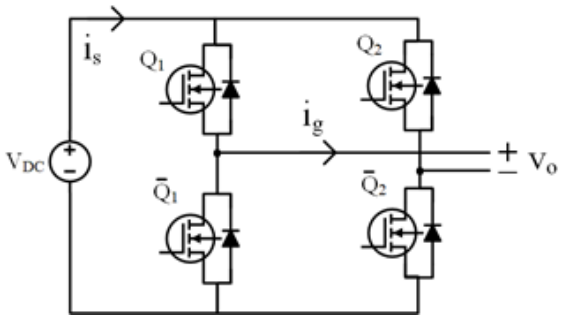


Figure 1. Defined quantities in a full bridge circuit

Throughout this paper, the dc-link current is referred as i_s, the voltage of the ac side of the full-bridge as v_o and the current, also through the ac side of the full-bridge, as i_g. If i_g is modeled by a sinusoidal current source, then i_s depends on how the switches Q_1, Q_2, $\overline{Q_1}$ and $\overline{Q_2}$ are driven. It is valuable to accurately express i_s so that when such a system is realized on the dc side by a battery and a shunt aluminium electrolytic capacitor, to take a typical example, the amount of current going through the capacitor can be quantified. The portion of i_s going through the dc bus capacitor will inherently contain harmonics naturally caused by the switching.

These switching harmonics impact the lifetime of the capacitor. The frequency dependent ESR of the bus capacitor dictates the heat dissipated inside it causing the electrolyte to evaporate and the component itself to age. For typical aluminium electrolytic capacitors, the life of the capacitor halves for every 10 °C rise above the rated temperature as dictated by Arrhenius Law [1, 2]. The capacitor lifetime's dependency on temperature has been an important concern for reliability of ac-dc converters both in literature as well as field operations [3, 4, 5].

Therefore, various approaches have been used in literature to quantify the dc-link current (instantaneous and rms). One method is to rely on a passive solution (i.e., simulations). While simulations are an effective way of finding the dc-link current in a particular circuit, the results do not reveal the underlying mathematical relationship which is essential

for studying the overall system. Later in this paper, the results show how a mathematical framework helps choose the capacitor with optimal current ratings, instead of a trial-and-error approach.

In [6], the authors present expression for dc-link current for a three phase two-level voltage source converter in compressed integral form. Although the measurement and calculation results have been presented, the solution of integrals or a method of calculation is not reported.

Another approach to calculate dc-link current in H-bridge based converters is to use analytical estimation techniques, which can simplify analysis at the cost of accuracy and more importantly, are limited to associated application. A recent work in [7] evaluates dc-link current for a single phase H-bridge converter by ignoring high frequency harmonics for computational convenience. In the current paper, a mathematical argument illustrates that in a generic case, the rms sum of the higher order harmonics can be equal, or even greater, than the rms of the highest magnitude harmonic.

Fundamental work by McGrath and Holmes [8] expresses the dc-link current in a carrier-based PWM driven half-bridge using the double Fourier Series analysis method introduced in [9]. The former reference applies the derived results of a cosine-triangle PWM based half-bridge converter under sinusoidal ac-side current on to two-level three phase VSI and on a three-level flying capacitor inverter. The same authors have utilized their framework to derive three-level flying capacitor converter's voltage balancing dynamics [10] and dc-link current harmonics in dual active bridge dc-dc converters [11].

In [12], the focus is on the dc link capacitor current for a three phase cascaded H-bridge converter connected with a diode rectifier. A closed form expression for the instantaneous dc link current is given for the three phase system but a (mathematical) argument of why it is applicable to their three phase application has not been discussed. For instance, the presented equation shows that in a three phase, multilevel cascaded H-bridge system, the dc-link current does not depend on modulator and carrier signals' phases.

However, it does not reveal the dependence of dc-link current on the modulation and carrier phases in the individual H-bridge of the cascaded system. A modular relationship is useful in various ways including control for voltage balancing in unbalanced loads. Moreover, an expression for the dc-bus capacitor's rms current is also presented in the same paper. Even though an instantaneous dc-link current expression is available, it serves the authors better to use the formula proposed in [13]. The formula has been developed based on graphical observation method after drawing waveforms for a particular load angle and carrier frequency value, which can not be used arbitrarily in a closed form.

This paper presents a precise analytical model for calculating dc-link current in a multi-phase cascaded H-bridge multilevel converter on a modular level with detailed analysis and reporting. The modular results help mathematically explain behavior of the converter, such as the natural voltage balancing property of the converter, and also provide a framework that can be utilized in a straightforward manner to study its interaction on a system level. This leads to the second contribution which is in expressing dc-bus capacitor's rms current in terms of active and reactive power at the grid in a bidirectional configuration.

2. ANALYTICAL BACKGROUND

Consider a full-bridge circuit with a dc voltage source and ac load in Figure 1. The first step is to accurately quantify the dc-link current in a single H-bridge and then apply the result to the cascaded system later. To solve for the exact dc-link current in Figure 1, the modulated voltage on the ac-side of the H-bridge is defined as

$$v_o(t) = M\cos(\omega_o t + \theta_o) \tag{1}$$

where M is the modulation index, i.e., the percentage of the amplitude of maximum possible v_o that is targeted, while ω_o and θ_o are the modulation angular frequency and phase of v_o respectively. The current in the ac side of the H-bridge is modeled by a current source as,

$$i_g(t) = I_g \cos(\omega_o t + \theta_o + \phi) \tag{2}$$

where ϕ is the relative phase between i_g and v_o. Next, the relationship between the switching functions of the respective half-bridges, $s_1(t)$ and $s_2(t)$, and the ac-side current, i_g, is explored. In this case, the dc-link current is a superposition of the products of switching function and the ac-side current. The dc link current can be expressed as

$$i_s(t) = [s_1(t) - s_2(t)] i_g(t) \tag{3}$$

where $s_1(t)$ and $s_2(t)$ are the switching functions of Q_1 and Q_2 respectively, as derived for naturally sampled phase shifted cosine-triangle PWM. $\overline{Q_1}$ and $\overline{Q_2}$ are complementary switches of the Q_1 and Q_2. These switching functions have been derived in [9] and are categorized into carrier and modulator harmonics in Eqs. (4)-(5) below.

$$s_1(t) = \frac{1}{2} + \frac{M}{2}\cos(\omega_o t + \theta_o) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{m\pi}\left[J_n(m\frac{\pi}{2}M)\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\right] \tag{4}$$

$$s_2(t) = \frac{1}{2} + \frac{M}{2}\cos(\omega_o t + \theta_o + \pi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{m\pi}\left[J_n(m\frac{\pi}{2}M)\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o] + \pi)\right] \tag{5}$$

Here, m is the harmonic number for the fundamental carrier (triangle) frequency, w_c, and n is the harmonic number for the fundamental modulation (cosine) frequency, w_o. Moreover, θ_c is the carrier phase in radians, defined for a cascaded phase-shifted-carrier

PWM system as follows.

$$\theta_c = \left[\frac{y-1}{(N-1)/2}\right] 2\pi \tag{6}$$

In (6), y is the module number and N is the total number of levels in v_o. Here, the denominator in the bracketed term is equal to the number of modules in the cascaded N-level converter. Additionally, note that in (5), π is added to create the anti-phase for the modulation signal in the half-bridge on the right side in Figure 1. π has been separated to avoid confusion in case the modulation signal is non-symmetric. This implies that θ_o is not only defined as the modulation angle of the overall multilevel voltage on the ac-side, but also as the modulation angle of the left half-bridge in each module. Finally, J_n is the Bessel function of the first kind with order n. In a cascaded converter, each half-bridge would have its unique switching function. Therefore, the equations have been set up to obtain intra-modular dynamics to investigate the individual dc-link currents.

2.1. DERIVATION OF DC-LINK CURRENT IN THE IDEAL MODEL AND ITS VALIDATION

The derivation strategy is as follows. To obtain the exact harmonic expression for the dc link current for the circuit in Figure 1, first, the Fourier transform is applied to (3). The multiplication in the time domain indicated in (3) becomes convolution in the frequency domain. The inverse Fourier transform is applied to the subsequent result. This process is carried out for each half-bridge of the module separately and then the contributions are superposed. The contributions from the left and right half-bridges towards the dc-link current, i_s of Figure 1 is summarized in (7) and (8) and then the results are substituted in (3) respectively, to obtain the dc link current for the module in (9) below.

$$\mathcal{F}^{-1}\left[S_1(\omega) * I_g(\omega)\right](t) = \frac{MI_g}{4}\cos(\phi) + \frac{I_g}{2}\left[\cos(\omega_o t + \theta_o)\cos(\phi) - \sin(\omega_o t + \theta_o)\sin(\phi)\right] + \frac{MI_g}{4}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{I_g}{2}\alpha \tag{7}$$

$$\mathcal{F}^{-1}\left[S_2(\omega) * I_g(\omega)\right](t) = -\frac{MI_g}{4}\cos(\phi) + \frac{I_g}{2}\left[\cos(\omega_o t + \theta_o)\cos(\phi) - \sin(\omega_o t + \theta_o)\sin(\phi)\right] - \frac{MI_g}{4}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] - \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{I_g}{2}\alpha \tag{8}$$

$$i_s(t) = \frac{MI_g}{2}\cos(\phi) + \frac{MI_g}{2}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} I_g\alpha \tag{9}$$

$$: \alpha = (K_{m,n+1} + K_{m,n-1})\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\cos(\phi)$$
$$+ (K_{m,n+1} - K_{m,n-1})\sin(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\sin(\phi)$$

$$: K_{mn} = \frac{2}{m\pi}J_n(m\tfrac{\pi}{2}M)\sin([m+n]\tfrac{\pi}{2}).$$

Each half-bridge generates a fundamental modulation frequency component which is effectively canceled in the superposition. Whereas, the dc component and remaining modulation and carrier harmonics add up to twice the magnitudes. The elimination of the fundamental modulator harmonic is because of the redistribution of harmonic energy (amplitude) to higher frequencies. Therefore, for dc-link capacitor, a full-bridge modulation is harmonically more efficient as compared to that in a half-bridge converter as the ESR of the capacitor is relatively lower at higher frequencies.

Eq. (9) is associated to dc-link current in one independent module. The topology of cascaded H-bridge converters is such that this equation can be applied to each module (due to the series connection) separately to provide information about all the modules. Therefore, this equation is applicable to any H-bridge as in Figure 1 driven by a naturally sampled cosine-triangle pulse width modulation strategy.

Now, the validity of the equation is carried using comparison with simulation of Figure 1 by modeling i_g as a sinusoidal current source defined in (2) in a single phase five-level unidirectional system. The simulation parameter are mentioned in Table 1. In this table, I_g stands for the peak value of the ac-load current and other modulation parameters have already been defined.

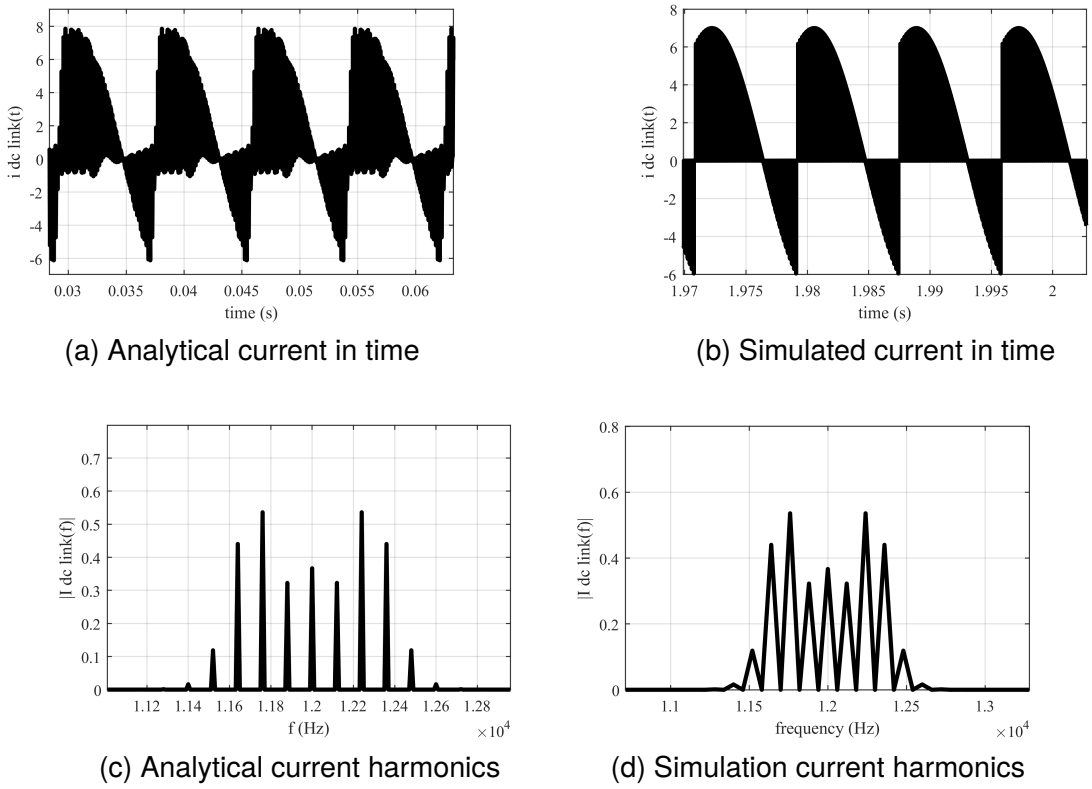
Table 1. Simulation parameters for validation of dc-link current

I_g (A)	ϕ (rad)	f_c (Hz)	M	N	f_o (Hz)
7	$\pi/3$	3000	0.9	5	60

Figure 2 shows a comparison of the simulation and analytical results in time and frequency domain. The difference between Figure 2(a) and Figure 2(b) is because in numerical implementation of (9), the double series sum is for finite indices of m and n. In this implementation, maximum value of m = 10 and n ranges between -500 and 500. The waveform corresponding to the numerical implementation of the analytical result exhibits the Gibbs phenomenon. Note that this trade-off is more efficient than ignoring the higher order harmonics as observed in literature. A random frequency band is chosen for comparison in Figure 2(c) and Figure 2(d) and the results show a close match in all of the finite frequency bands up to three decimal places, thereby permitting to move ahead.

Next, a two-module (five-level) system is studied. It is observed that within one phase, each module has the same rms dc-link current even though each half-bridge is switched differently from the three remaining half-bridges. In this way, the natural voltage

balancing property is mathematically illustrated for the cascaded multilevel converter. These conclusions motivate hardware implementation and results are evaluated while studying a grid-tied system in the next section.



(a) Analytical current in time

(b) Simulated current in time

(c) Analytical current harmonics

(d) Simulation current harmonics

Figure 2. (a)-(d) Validation of the ideal dc-link current model

3. ANALYSIS OF A GRID-TIED SYSTEM, AND EVALUATION OF RESULTS IN THREE DOMAINS

3.1. MAPPING GRID POWER TO $I_{CAP,RMS}$

A system overview in Figure 3 shows a typical active front-end configuration where the grid is modeled by a voltage source and a five-level cascaded H-bridge converter is connected to the grid through an LCL filter. It is now possible to map the the grid's active and reactive power flow (P_g, Q_g) to the dc-link current rms of the bus capacitor. Utilizing (9), the rms current flowing through the bus capacitors is obtained and is shown in (10).

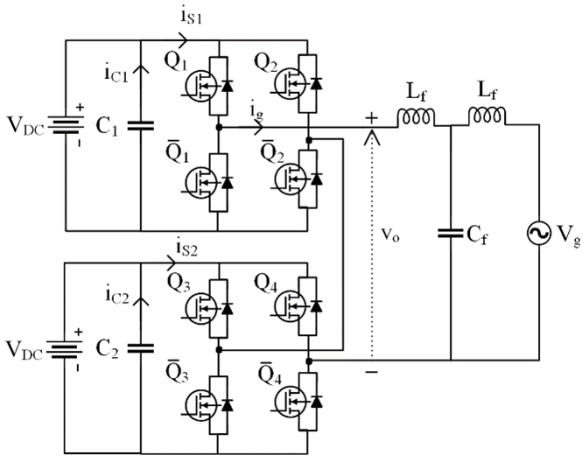


Figure 3. The grid-tied cascaded H-bridge converter

$$I_{cap,rms}^2 = \left[\frac{1-\omega^2 L_f C_f}{2\left|\hat{V}_g\right|}\right]^2 \left[P_g^2 + \left(Q_g - \frac{\omega C_f \left|\hat{V}_g\right|^2}{1-\omega^2 L_f C_f}\right)^2\right] \times \left[\frac{\beta}{2V_{DC}^2} + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{4}{m\pi}\sin([m+n]\frac{\pi}{2}) J\left(\frac{m\pi}{V_{DC}}\sqrt{\beta}\right)^2\right]$$

$$: \beta = \left(\frac{P_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f)\right)^2 + \left(\frac{Q_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f) + \left|\hat{V}_g\right|(1-\omega^2 L_f C_f)\right)^2 \quad (10)$$

In (10), $|\hat{V}_g|$ is the line-to-neutral rms of the grid voltage shown in Figure 5. All other parameters are constant or running sum indices. L_f and C_f are the filter inductance and capacitance, J stands for the Bessel function as defined earlier, V_{DC} is the dc-bus voltage of each module, ω is the grid's fundamental frequency, while P_g and Q_g are the grid's active and reactive power using generator sign convention. Because of the symmetry within and between balanced phases, the equation is applicable to a multi-phase and multilevel system. A contour plot is shown for (10) in Figure 4. Close examination shows that the round contours are not centered at the origin and do not form an exact ellipse, as is identified by the equation. For a specific contour, as P_g goes higher, the amount of Q_g decreases

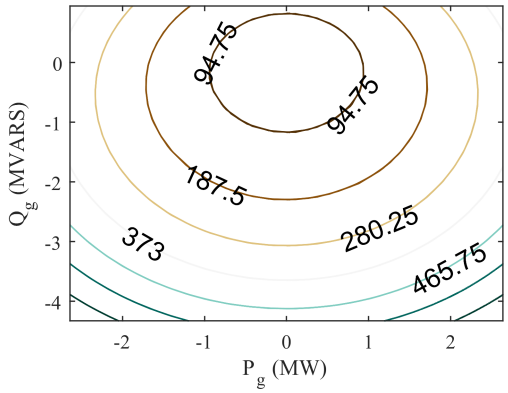


Figure 4. DC link capacitor's rms current contours

according to the described relationship. The area enclosed by a contour would depict the complex power operating points supported by the corresponding rms rating of the capacitor installed in the hardware.

The relationship between the dc-link capacitor's rms current and grid power P_g and Q_g is examined using a surface plot in Figure 5. Using 10, the graph shows that as operating power levels are increased, the stress on the dc-link capacitor increases non-linearly. It is observed that this plot is not symmetric around the grid's active and reactive power. This fact is most visible by shifting the discussion focus back to the contours in Figure 4. Consider the two points where the 94.75 A contour crosses zero P_g. In this case, the reactive power being supplied *to* the grid, positive Q_g, is 0.9 MVAR and in another operating scenario, the reactive power being drawn *from* the grid is around 1.2 MVAR, a point below the chosen contour. In other words, there is more stress on the capacitor when the same amount of reactive power is being consumed by the grid as compared to when it is being supplied by the grid. The LCL filter demands additional reactive power beyond the amount being fed to the grid.

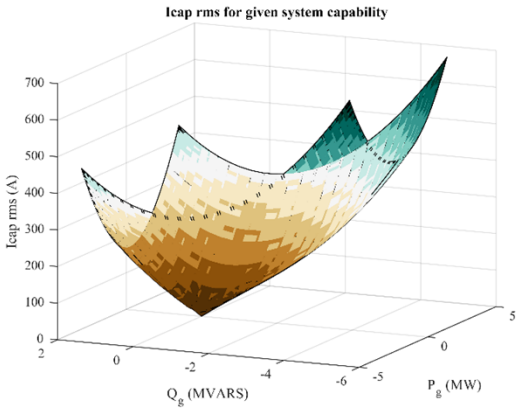


Figure 5. Relationship of $I_{cap-rms}$ with grid power

Table 2. Configuration parameters

Parameter		Value
V_{DC_a}	(V)	20
V_{DC_b}	(V)	1800
$f_{cut-off}$	(kHz)	6
L_f	(mH)	20.63
C_f	(nF)	34.11
R_f	(Ω)	22.35
f_c	(kHz)	3
L_h	(mH)	1.8
V_g l-n rms	(V)	7200

3.2. DISCUSSION OF VARIOUS RESULTS

A combination of hardware and simulation results were compared with analytical model to validate the derived equations. A single phase five-level cascaded converter was developed and its configuration parameters are shown in Table 2. This table contains specific parameters selected for corresponding discussion. Other parameters like modulation frequency, f_o, are not mentioned.

3.2.1. Evaluation of Analytical and Simulation Results. The analytical model was compared with a simulation setup following the circuit in Figure 3. All the parameters from Table 2 were used except L_h, V_{DC_a} and R_f. V_{DC_b} was used in the analysis of analytical and simulation results of the grid-tied system. The analytical model has been developed based on a sinusoidal current source model whereas its results are to be compared with Figure 3 which contains the LCL filter. The filter was designed for a cut-off frequency of 6 kHz to best accommodate the Bode gain and phase plots in the desired operating point. L_f was set to 0.05 p.u. of base impedance. Figure 6 shows a comparison between the analytical model and the simulation results.

Table 3. Test Points to Compare Simulation and Analytical Capacitor Stresses

	1	2	3	4	5	6	7	8
P_g (kW)	321	0	-321	0	-183	183	166	-167
Q_g (kVAR)	5	338	5	-363	168	168	-161	-141

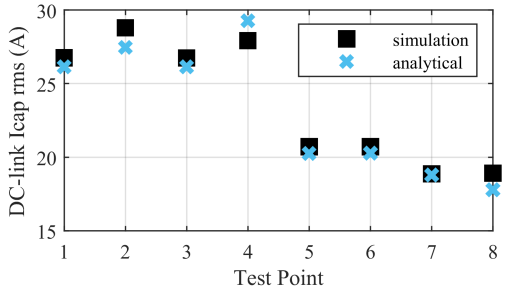


Figure 6. Simulation and analytical comparison for the capacitor stresses

The worst case error in simulation and analytical comparison is noted to be about 4.8%. The difference can be explained based on a few factors. The first reason lies in the difference between the analytical model of (10), which assumes sinusoidal ac-side current, and the simulation which has an LCL filter with a cut-off frequency of 6 kHz. The 6 kHz range allows for multilevel voltage harmonics to propagate in the system, thus causing ac-side current harmonics. This in-turn effects the dc-link current which is a sampled version of the ac-side current. Therefore, the bus capacitor's rms current will have a different rms

than the sinusoidal ac-load case. Another source of error is evident from the fact that the simulation implements regularly sampled PWM whereas the analytical model is based on naturally sampled PWM. Besides explaining errors, the results show that for all the sampled points in Table. 3, the rms portion of the 120 Hz harmonic was close to the sum of rms contribution from non-120 Hz harmonics (i.e., within 1 A).

3.2.2. Hardware and Simulation Results Evaluation. For hardware results, a single phase five-level H-bridge converter is operated in the inverter mode with an RL load. Therefore, V_{DC_a}, R_f, L_h and f_c are hardware and simulation parameters in this case. For this setup, the dc-link current was measured and compared with simulations. The five-level voltage, the RL load current and the voltage output from both half-bridges of one module can be seen in Figure 7.

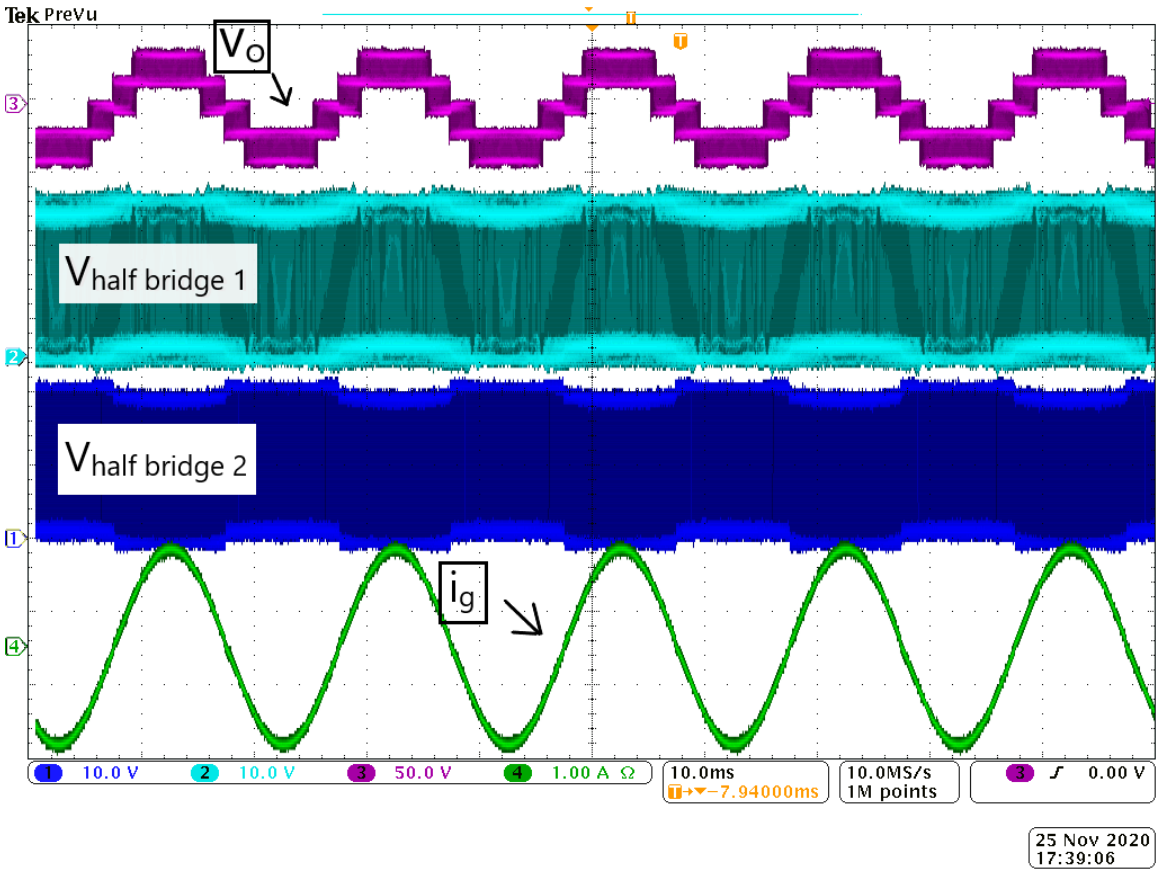


Figure 7. Hardware results for the five-level cascaded H-bridge converter

The ac-side current through the RL load and the output voltage of the half bridges were measured directly as seen in Figure 7. Since the dc-link current is of discontinuous nature, a regular Hall-effect based current probe cannot be used to measure it directly. Therefore, the method recommended in [14] was used. The method is described as follows. As illustrated in the referred work, the half-bridge outputs were multiplied with the ac-side load current to obtain the hardware dc-link current. This hardware result was then compared with the simulation results as shown in Figure 8 and Figure 9 respectively.

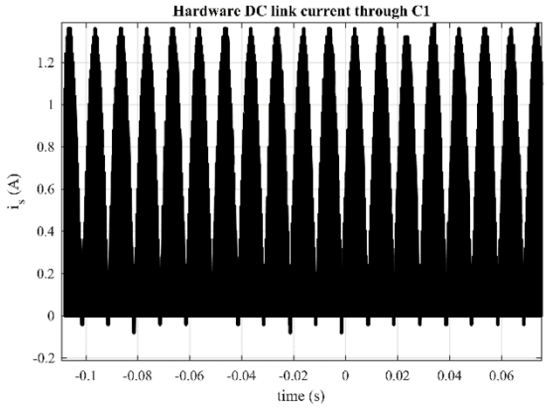


Figure 8. Hardware dc-link current in one module

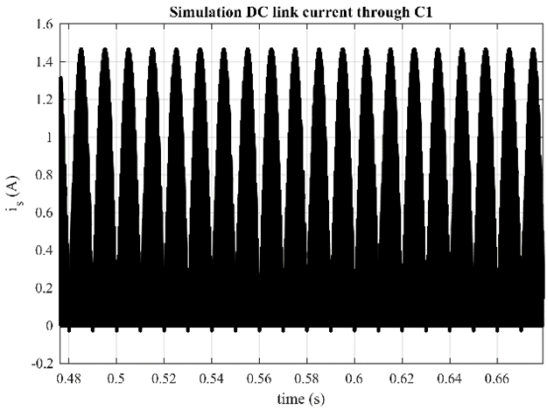


Figure 9. Simulation dc-link current in one module

The rms current measured in the hardware and that in the simulation had a worst case difference of 9.2%. This difference is explained in two parts. The switching functions from the ideal simulation blocks are not the same as those coming from the microcontroller. The

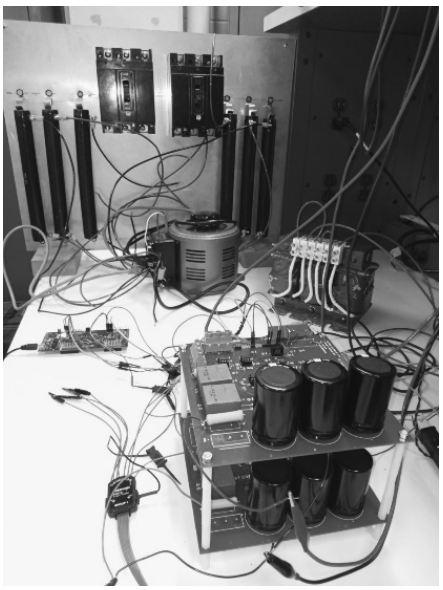


Figure 10. Hardware prototype of the cascaded H-bridge system

code implemented in the microcontroller contains deadtime which has not been incorporated in to the simulation blocks. This difference has direct impact on the hardware data-processing of the dc-link current as the pulse widths are not the same in the microcontroller as the simulation.

However, this is only partially contributing to the deviation in pulse widths as it is a difference due to voltages but load current does not exist. When the load is turned on, a dynamic behavior between the body diode and IGBT-based half-bridge causes the pulse width to deviate as well. This deviation is evident from Figure 7. The conduction of body diode is initiated during deadtime. Based on the polarity of the load current, corresponding body diodes will conduct. Due to the body diode's forward voltage drop, the pulses seen in Figure 7 are slightly above and below V_{DC} as well as slightly below and above the 0 voltage level. Therefore, the overall pulse width profile in the hardware, which is used to calculate dc -link current, is significantly different than that in the simulation. The hardware prototype is finally shown in Figure 10 with two modules for the five-level converter, micrcontroller and RL load.

4. CONCLUSION AND FUTURE WORK

In this paper, a detailed and exact mathematical model has been developed for the dc-link current in a cascaded H-bridge multilevel converter. The detail of the model has been used to study the converter's interaction with a grid-tied system. The grid's active and reactive power commands have been mapped to the dc-link current stress in the bus capacitors. The analytical, simulation and hardware results have been evaluated in a variety of setups and these show a good match thereby validating the work. For future work, the derivations motivate deriving a framework for capacitor sizing against the dc-bus voltage specifications. Overall, this work contributes to estimating the lifetime of the dc-link capacitors in an accurate manner which in-turn adds to system reliability by avoiding contingency outages and improving scheduled outages in power systems.

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II. ANALYSIS AND DESIGN OF DC-LINK CAPACITOR IN CASCADED H-BRIDGE MULTILEVEL ACTIVE FRONT-END CONVERTER

Muhammad Shehroz Malik, Jonathan W. Kimball
Department of Electrical & Computer Engineering
Missouri University of Science and Technology
Rolla, Missouri 65409
Email: mm2c2@mst.edu, kimballjw@mst.edu

ABSTRACT

Medium-voltage grid-tied systems often use a cascaded H-bridge multi-level active front-end. In this converter, dc link bus capacitors play an important role in stabilizing the converter and enabling both active and reactive power injections. The present work provides analytical expressions for the capacitor current, which are essential for optimizing system design (especially capacitor size vs. lifetime). Then, the expression is incorporated into the grid connected bidirectional power system model. Consequently, this work contributes to the guiding principles to choose accurate dc link capacitor ratings against grid-side power delivery requirements. The analytical results have been validated with detailed simulations and hardware results.

DC-link capacitors form a fundamental part of cascaded H-bridge multilevel ac-dc converters found in grid-connected power systems. These capacitors come with an expiration date which is dependent on the operating power and voltage values. Lack of information about the lifetime of the dc-link capacitor creates uncertainty in the duration of online operation of the converter, thus increasing the probability of a contingency outage. A better estimate of the lifetime of these capacitors can help maximize usage and maintain scheduled outages more efficiently, without disruption in service.

A cascaded H-bridge ac-dc converter can consist of more than one H-bridge, depending on the number of voltage levels required on the ac-side of the bridge. A single H-bridge is illustrated in Figure 1 and is referred to as a *module* in the cascaded system ahead.

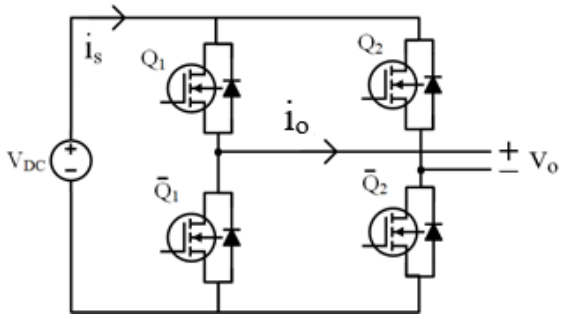


Figure 1. Defined quantities in a full bridge circuit

Throughout this paper, the dc-link current is referred as i_s, the voltage of the ac side of the full-bridge as v_o and the current, also through the ac side of the full-bridge, as i_o. If i_o is modeled by a sinusoidal current source, then i_s depends on how the switches Q_1, Q_2, $\overline{Q_1}$ and $\overline{Q_2}$ are driven. It is valuable to accurately express i_s so that when such a system is realized on the dc side by a battery and a shunt aluminium electrolytic capacitor, to take a typical example, the amount of current going through the capacitor can be quantified. The portion of i_s going through the dc bus capacitor will inherently contain harmonics naturally caused by the switching.

These switching current harmonics impact the lifetime of the capacitor. The frequency dependent ESR of the bus capacitor dictates the heat dissipated inside it causing the electrolyte to evaporate and the component itself to age. For typical aluminium electrolytic capacitors, the life of the capacitor halves for every 10 °C rise above the rated temperature as dictated by Arrhenius Law [1, 2]. The capacitor lifetime's dependency on temperature has been an important concern for reliability of ac-dc converters both in literature as well as field operations [3, 4, 5]. Therefore the phrases, dc-link capacitor lifetime and dc-link

capacitor current are used interchangeably in this article ahead. Once the instantaneous and rms current expressions are obtained, the grid power requirements can be translated to the stress on dc-link capacitors.

Various approaches have been used in literature to quantify the dc-link current (instantaneous and rms). One method is to rely on a passive solution (i.e., simulations). While simulations are an effective way of observing the dc-link current in a particular circuit, the results do not reveal the underlying mathematical relationship which is essential for studying the overall system. When mathematical dependencies are not available, open-loop properties of the converter, like the natural voltage balancing property of the cascaded H-bridge converter, are not evident. Later in this paper, the derivations provide the relationship that maps grid's active and reactive power to the rms current stress rather than using a sweep-and-observe approach in the simulation.

In [6], the authors present expression for dc-link current for a three phase two-level voltage source converter in compressed integral form. Although the measurement and calculation results have been presented, the solution of integrals or a method of calculation is not reported.

Another approach to calculate dc-link current in H-bridge based converters is to use analytical estimation techniques, which can simplify analysis at the cost of accuracy and more importantly, are limited to associated application. A recent work in [7] evaluates dc-link current for a single phase H-bridge converter by ignoring high frequency harmonics for computational convenience. In the current paper, a mathematical argument illustrates that in a generic case, the rms sum of the higher order harmonics can be equal, or even greater, than the rms of the highest magnitude harmonic.

Fundamental work by McGrath and Holmes [8] expresses the dc-link current in a half-bridge driven by carrier-based PWM (for both natural and regular sampling) using the double Fourier Series analysis method introduced in [9]. The former reference applies the derived results of a sine-triangle PWM based half-bridge converter under sinusoidal ac-side

current on to two-level three phase VSI and on a three-level flying capacitor inverter. The same authors have utilized their framework to derive three-level flying capacitor converter's voltage balancing dynamics [10] and dc-link current harmonics in dual active bridge dc-dc converters [11].

In [12], the focus is on the dc link capacitor current for a three phase cascaded H-bridge converter connected with a diode rectifier. A closed form expression for the instantaneous dc link current is given for the three phase system but a (mathematical) argument of its validity in the three phase application has not been discussed. For instance, the presented equation shows that in a three phase, multilevel cascaded H-bridge system, the dc-link current does not depend on modulator and carrier signals' phases. However, it does not reveal the dependence of dc-link current on the modulation and carrier phases in the individual H-bridge of the cascaded circuit. A modular relationship is useful in various ways including control for voltage balancing in unbalanced loads. Moreover, an expression for the dc-bus capacitor's rms current is also presented in the same paper. Even though an instantaneous dc-link current expression is available, a formula proposed in [13] is used. The formula has been developed based on the assumption that the switching function is the same as the modulation function as the switching frequency is typically very high as compared to the modulation signal's frequency. This assumption discards the high frequency switching harmonics for dc-link rms current calculation. Furthermore, the rms calculation is based on the assumption that the dc-link current repeats after every one-sixth of the fundamental cycle. Therefore, the reported rms current expression cannot be used arbitrarily in a closed form. In contrast, the present paper uses its instantaneous dc-link current expression such that each harmonic's contribution to the rms current is evident and shows that the range of double Fourier Series sum indices controls the accuracy of the current.

This paper presents a precise analytical model for calculating dc-link current in a multi-phase cascaded H-bridge multilevel converter on a modular level with detailed analysis and reporting. The modular results help mathematically explain behavior of the

converter, such as the natural voltage balancing property of the converter, and provide a framework that can be utilized in a straightforward manner to study its interaction on a system level. This leads to the second contribution which is in expressing dc-bus capacitor's rms current in terms of active and reactive power at the grid in a bidirectional configuration.

The authors of the current article have previously presented analytical results for a naturally sampled phase-shifted carrier PWM assuming sinusoidal current in the ac-side of the full-bridge. The present article analyzes the regularly sampled and symmetric phase-shifted carrier PWM which is commonly implemented on a digital processor. Moreover, in this work, the authors consider that the ac-side current can be non-sinusoidal and therefore provide a framework that utilizes all the harmonics on the ac-side that impact the dc-link current.

1. ANALYTICAL BACKGROUND

Consider a full-bridge circuit with a dc voltage source and ac load in Figure 1. The first step is to accurately quantify the dc-link current in a single H-bridge and then apply the result to the cascaded system later. To solve for the exact dc-link current in Figure 1, the modulated voltage on the ac-side of the H-bridge is defined as

$$v_o^*(t) = M\cos(\omega_o t + \theta_o) \tag{1}$$

where M is the modulation index, i.e., the percentage of the amplitude of maximum possible v_o^* that is targeted, while ω_o and θ_o are the modulation angular frequency and phase of v_o^* respectively. For clarity, v_o refers to the multilevel voltage.

Next, the relationship between the switching functions of the respective half-bridges, $s_1(t)$ and $s_2(t)$, and the ac-side current, i_o, is explored. In this case, the dc-link current is a superposition of the products of switching function and the ac-side current. The dc link

current can be expressed as

$$i_s(t) = [s_1(t) - s_2(t)]i_o(t) \tag{2}$$

where $s_1(t)$ and $s_2(t)$ are the switching functions of Q_1 and Q_2 respectively, as derived for regularly sampled phase shifted sine-triangle PWM. $\overline{Q_1}$ and $\overline{Q_2}$ are complementary switches of the Q_1 and Q_2. These switching functions have been derived in [9] and are categorized into carrier and modulator harmonics in Eqs. (3)-(4) below.

$$\begin{aligned} s_1(t) = \frac{1}{2} + \sum_{n=1}^{\infty} K_{mn}\cos(n[\omega_o t + \theta_o]) + \sum_{m=1}^{\infty} K_{mn}\cos(m[\omega_c t + \theta_c]) \\ + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o]) \end{aligned} \tag{3}$$

$$\begin{aligned} s_2(t) = \frac{1}{2} + \sum_{n=1}^{\infty} K_{mn}\cos(n[\omega_o t + \theta_o + \pi]) + \sum_{m=1}^{\infty} K_{mn}\cos(m[\omega_c t + \theta_c]) \\ + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o + \pi]) \end{aligned} \tag{4}$$

$$: K_{mn} = \tfrac{2}{q\pi} J_n(q\tfrac{\pi}{2}M)\sin([q+n]\tfrac{\pi}{2}),\ q = m + n\tfrac{w_o}{w_c}$$

Here, m is the harmonic number for the fundamental carrier (triangle) frequency, w_c, and n is the harmonic number for the fundamental modulation (cosine) frequency, w_o. Moreover, θ_c is the carrier phase in radians, defined for a cascaded phase-shifted-carrier PWM system as follows.

$$\theta_c = \left[\frac{y-1}{(N-1)/2}\right] 2\pi \tag{5}$$

In (5), y is the module number and N is the total number of levels in v_o. Here, the denominator in the bracketed term is equal to the number of modules in the cascaded N-level converter. Additionally, note that in (4), π is added to create the anti-phase for the modulation signal in the half-bridge on the right side in Figure 1. This implies that θ_o is not only defined as the modulation angle of the overall multilevel voltage on the ac-side, but also as the modulation angle of the left half-bridge in each module. Finally, J_n is the Bessel function of the first kind with order n.

The current in the ac side of the H-bridge is modeled as,

$$i_o(t) = I_o \cos\Big(a[\omega_c t + \theta_c] + b[\omega_o t + \theta_o] + \phi_{ab}\Big) \tag{6}$$

where $b\theta_o + \phi_{ab}$ is the arbitrary phase of a particular harmonic. It is justified to represent i_o in this way due to the following. The multilevel voltage, v_o, contains carrier harmonics with a multiple of m and modulator harmonics with a multiple of n. When these harmonics are connected to a load or a low pass filter, the resulting i_o will contain the same harmonic numbers as v_o but with the adjusted magnitude, I_o, and phase offset, ϕ_{ab}. However, it is important to differentiate between the harmonic number in voltage and that in current. Therefore, the carrier and modulator harmonic numbers in i_o are represented by a and b respectively.

2. DERIVATION OF THE DC-LINK CURRENT AND ITS VALIDATION

The derivation strategy is as follows. To obtain the exact harmonic expression for the dc link current for the circuit in Figure 1, first, the Fourier transform is applied to (2). The multiplication in the time domain indicated in (2) becomes convolution in the frequency domain. The inverse Fourier transform is applied to the subsequent result. This process is carried out for each half-bridge of the module separately and then the contributions are

superposed. The contributions from the left and right half-bridges towards the dc-link current, i_s of Figure 1 is summarized in (7) and (8) and then the results are substituted in (2) respectively, to obtain the dc link current for the module in (9) below.

$$\begin{aligned}\mathcal{F}^{-1}\Big\{S_1(\omega) * I_o(\omega)\Big\}(t) = \frac{I_o}{2}\cos\Big(a[\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)+\\ \sum_{n=1}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big(a[\omega_c t+\theta_c]+[b-n][\omega_o t+\theta_o]+\phi_{ab}\Big)\\ +\cos\Big(a[\omega_c t+\theta_c]+[b+n][\omega_o t+\theta_o]+\phi_{ab}\Big)\Bigg]+\\ \sum_{m=1}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big([a-m][\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)\\ +\cos\Big([a+m][\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)\Bigg]\\ +\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big([a-m][\omega_c t+\theta_c]+[b-n][\omega_o t+\theta_o]+\phi_{ab}\Big)\\ +\cos\Big([a+m][\omega_c t+\theta_c]+[b+n][\omega_o t+\theta_o]+\phi_{ab}\Big)\Bigg]\end{aligned} \tag{7}$$

$$\begin{aligned}\mathcal{F}^{-1}\Big\{S_2(\omega) * I_o(\omega)\Big\}(t) = \frac{I_o}{2}\cos\Big(a[\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)+\\ \sum_{n=1}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big(a[\omega_c t+\theta_c]+[b-n][\omega_o t+\theta_o]-n\pi+\phi_{ab}\Big)\\ +\cos\Big(a[\omega_c t+\theta_c]+[b+n][\omega_o t+\theta_o]+n\pi+\phi_{ab}\Big)\Bigg]+\\ \sum_{m=1}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big([a-m][\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)\\ +\cos\Big([a+m][\omega_c t+\theta_c]+b[\omega_o t+\theta_o]+\phi_{ab}\Big)\Bigg]+\\ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{K_{mn}I_o}{2}\Bigg[\cos\Big([a-m][\omega_c t+\theta_c]+[b-n][\omega_o t+\theta_o]-n\pi+\phi_{ab}\Big)\\ +\cos\Big([a+m][\omega_c t+\theta_c]+[b+n][\omega_o t+\theta_o]+n\pi+\phi_{ab}\Big)\Bigg]\end{aligned} \tag{8}$$

Therefore, the net dc-link current in the module would be the sum of the individual contributions from the half-bridges. The result summarized below.

$$
\begin{aligned}
i_s(t) = \sum_{\substack{n=1 \\ n=odd}}^{\infty} K_{mn} I_o \Bigg[& \cos\Big(a[\omega_c t + \theta_c] + [b-n][\omega_o t + \theta_o] + \phi_{ab}\Big) \\
& + \cos\Big(a[\omega_c t + \theta_c] + [b+n][\omega_o t + \theta_o] + \phi_{ab}\Big)\Bigg] \\
+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} K_{mn} I_o \Bigg[& \cos\Big([a-m][\omega_c t + \theta_c] + [b-n][\omega_o t + \theta_o] + \phi_{ab}\Big) \\
& + \cos\Big([a+m][\omega_c t + \theta_c] + [b+n][\omega_o t + \theta_o] + \phi_{ab}\Big)\Bigg]
\end{aligned}
\tag{9}
$$

The harmonics in i_o are called $a\omega_c + b\omega_o$ and the harmonics in v_o are called $m\omega_c + n\omega_o$. Together, these show up in various combinations as harmonics of the dc-link current in the module, i_s.

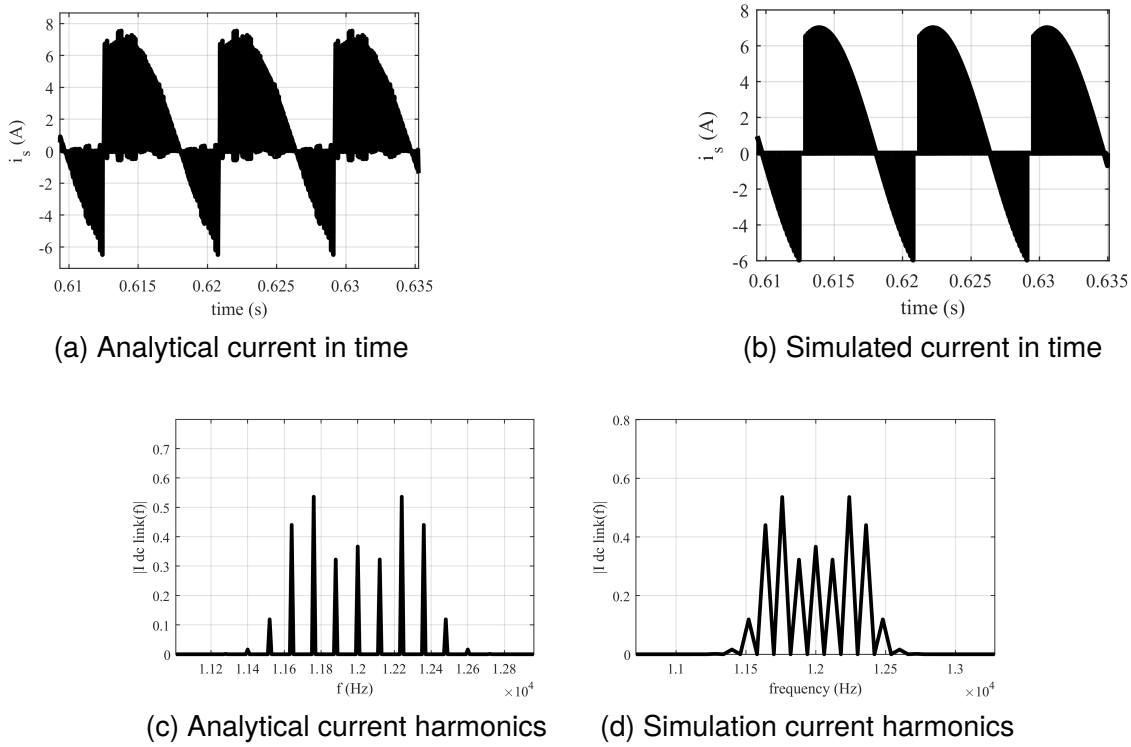
When (7) and (8) are substituted in (2), the first terms cancel out on their own. The third terms also cancel out on their own since in these terms, n is zero and consequently, the $n\pi$ factor of (4) that convolves with i_o is zero.

The second and fourth terms in (7) and (8) are different due to the $n\pi$ in the arguments of the sinusoids. This difference is again created by how the switching functions are defined in (3) and (4). When n is even, the second and fourth terms are the same and therefore cancel each other out. The resulting expression is then shown in (9). The harmonic energy of first, third and even-n harmonics of second and fourth terms in (7) and (8) is redistributed as twice the amplitudes and lesser number of harmonics in (9).

Eq. (9) is associated to dc-link current in one independent module. The topology of cascaded H-bridge converters is such that this equation can be applied to each module (due to the series connection) separately to provide information about all the modules. Therefore, this equation is applicable to any H-bridge as in Figure 1 driven by a symmetric and regularly sampled sine-triangle pulse width modulation strategy.

Table 1. Simulation parameters for validation of the dc-link current

I_o (A)	ϕ (rad)	f_c (Hz)	M	N	f_o (Hz)
7	$\pi/3$	3000	0.9	5	60



(a) Analytical current in time

(b) Simulated current in time

(c) Analytical current harmonics

(d) Simulation current harmonics

Figure 2. (a)-(d) Validation of the ideal dc-link current model

Now, the validity of the equation is carried using comparison with simulation of Figure 1 by modeling i_o as a sinusoidal current source defined by setting $a = 0$ and $b = 1$ in (6) in a single phase five-level unidirectional system. The simulation parameter are mentioned in Table 1. In this table, I_o stands for the peak value of the ac-load current and other modulation parameters have already been defined.

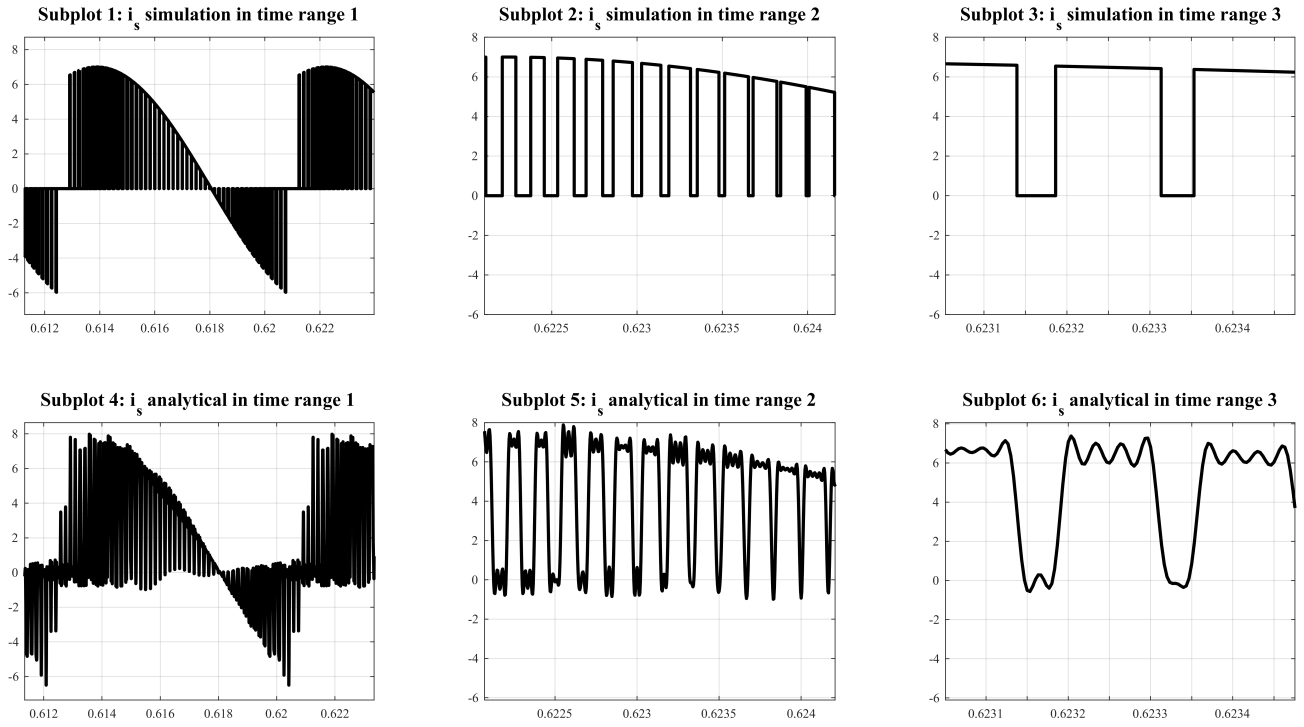


Figure 3. Zoomed-in view of instantaneous dc-link current in a module in various time ranges from left to right and simulation and analytical from top to bottom

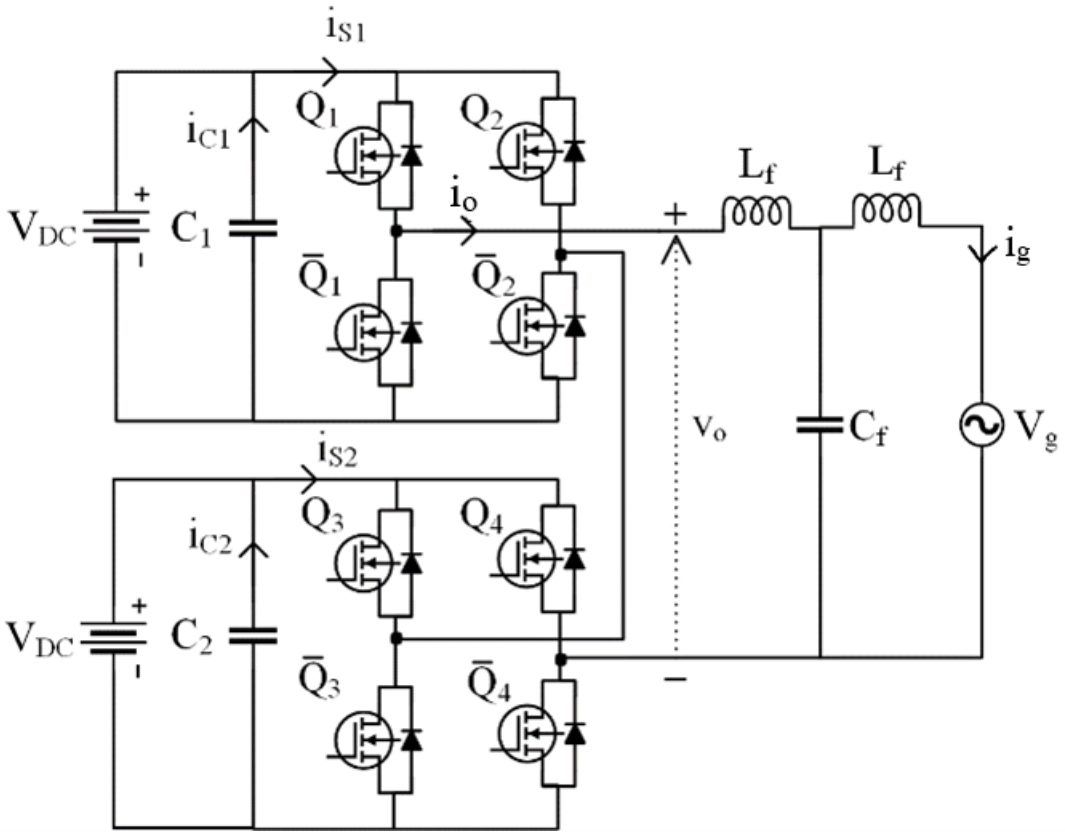


Figure 4. Cascaded H-bridge converter connected to grid with LCL filter

Figure 2 shows a comparison of the simulation and analytical results in time and frequency domain. The difference between Figure 2(a) and Figure 2(b) is because in numerical implementation of (9), the double series sum is for finite indices of m and n. In this implementation, maximum value of $m = 10$ and n ranges between -501 and 501. The waveform corresponding to the numerical implementation of the analytical result exhibits the Gibbs phenomenon. Note that this trade-off is more efficient than ignoring the higher order harmonics as observed in literature. A random frequency band is chosen for comparison in Figure 2(c) and Figure 2(d) and the results show a close match in all of the finite frequency bands up to three decimal places, thereby permitting to move ahead.

Within one phase, each module has the same dc-link current even though each half-bridge is switched differently from the three remaining half-bridges. In this way, the natural voltage balancing property is mathematically illustrated for the cascaded multilevel converter. These conclusions motivate hardware implementation and results are evaluated while studying a grid-tied system in the next section.

3. APPLICATION IN A GRID-TIED SYSTEM

3.1. MAPPING GRID POWER TO $I_{CAP,RMS}$

A system overview in Figure 4 shows a typical active front-end configuration where the grid is modeled by a sinusoidal voltage source and a five-level cascaded H-bridge converter is connected to the grid through an LCL filter.

Since v_g only has a fundamental harmonic, the corresponding harmonic in i_o that is responsible for P_g and Q_g will be the one with $a = 0$ and $b = 1$. Therefore, in this application, (9) reduces to (10). It is now possible to map the grid's active and reactive power flow (P_g, Q_g) to the dc-link current rms of the bus capacitor. Utilizing (10), the rms current flowing through the bus capacitors is obtained and is shown in (11).

$$i_s(t) = \sum_{\substack{n=1 \\ n=odd}}^{\infty} K_{mn} I_o \left[\cos\left([n-1][\omega_o t + \theta_o] - \phi_{01} \right) + \cos\left([n+1][\omega_o t + \theta_o] + \phi_{01} \right) \right] + \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} K_{mn} I_o \left[\cos\left(m[\omega_c t + \theta_c] + [n-1][\omega_o t + \theta_o] - \phi_{01} \right) + \cos\left(m[\omega_c t + \theta_c] + [n+1][\omega_o t + \theta_o] + \phi_{01} \right) \right] \tag{10}$$

Therefore, the rms dc-link current in this case reduces to the following equation.

$$I_{cap-rms}^2 = \left[\frac{1-\omega^2 L_f C_f}{2\left|\hat{V}_g\right|}\right]^2 \left[P_g^2 + \left(Q_g - \frac{\omega C_f \left|\hat{V}_g\right|^2}{1-\omega^2 L_f C_f}\right)^2\right] \times \left[\sum_{\substack{n=1 \\ n=odd}}^{\infty} K_{0n}^2 + \sum_{\substack{n=3 \\ n=odd}}^{\infty} K_{0n}^2 + \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} 2K_{mn}^2\right] \quad (11)$$

$$: K_{mn} = \frac{2}{q\pi} J_n\left(q\frac{\pi}{2}\frac{\sqrt{(2\beta)}}{V_{DC}}\right) \sin\left([q+n]\frac{\pi}{2}\right)$$

$$: q = m + n\frac{w_o}{w_c}$$

$$: \beta = \left(\frac{P_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f)\right)^2 + \left(\frac{Q_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f) + \left|\hat{V}_g\right|(1-\omega^2 L_f C_f)\right)^2$$

In (11), $|\hat{V}_g|$ is the line-to-neutral rms of the grid voltage shown in Figure 4. All other parameters are constant or running sum indices. L_f and C_f are the filter inductance and capacitance, J stands for the Bessel function as defined earlier, V_{DC} is the dc-bus voltage of each module, ω is the grid's fundamental frequency, while P_g and Q_g are the grid's active and reactive power using generator sign convention. Because of the symmetry within and between balanced phases, the equation is applicable to a multi-phase and multilevel system.

This equation is quantifying the amount of current going through dc-link capacitor due to the ac-side current harmonic that is responsible for P_g and Q_g. Therefore, while (11) quantifies the stress on the dc-link capacitor due to grid's active and reactive power requirements, it is not the only stress on it. Additional stress is caused by the LCL filter harmonics in i_o. Each harmonic in i_o (a and b) can be identified and (9) can be used to obtain equation similar to (10) to get the $I_{cap-rms}$ contribution due to the chosen harmonic. This process can be iteratively done to get the total $I_{cap-rms}$ in the capacitors C_1 in Figure 4. The total $I_{cap-rms}$ in C_2 will be the same as C_1 within one phase. A contour plot is shown for (11) in Figure 5. Close examination shows that the round contours are not centered at the origin and form an ellipse scaled by the Fourier coefficients, as is identified by the

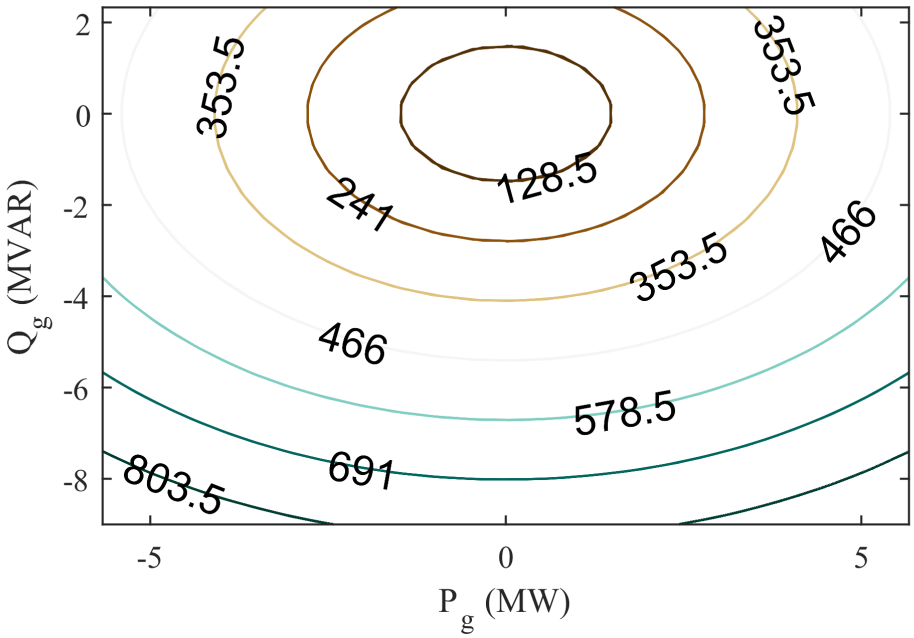
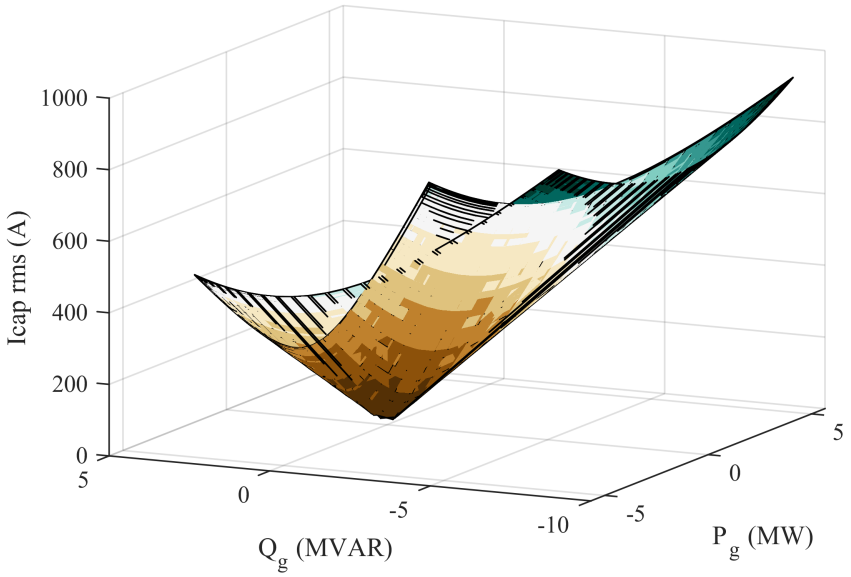


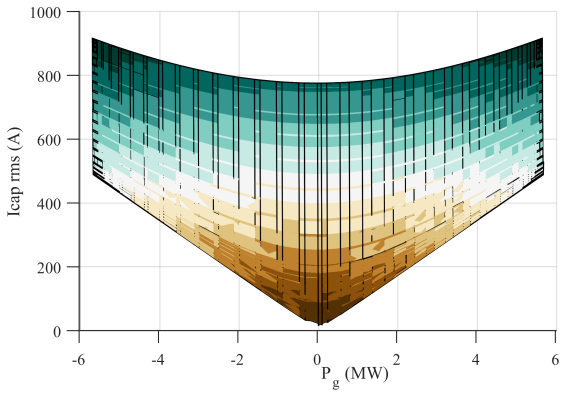
Figure 5. DC link capacitor's rms current contours in grid power plane

equation. For a specific contour, as P_g goes higher, the amount of Q_g decreases according to the described relationship. The points in the area enclosed by a contour would depict the complex power operating points supported by the corresponding rms rating of the capacitor installed in the hardware.

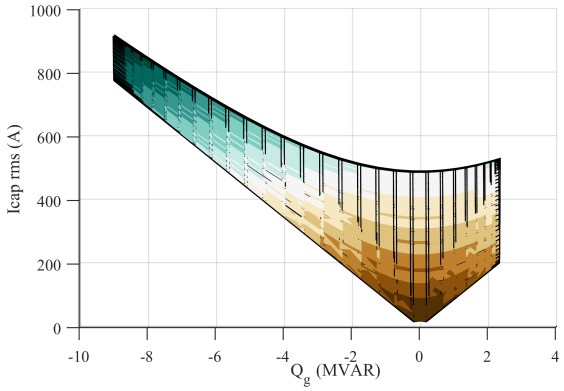
The relationship between the dc-link capacitor's rms current and grid power P_g and Q_g is examined using a surface plot in Figure 6. Figure 6a shows that as operating power levels are increased, the stress on the dc-link capacitor increases non-linearly. Using (11), Figs. 6b, 6c answer how the stress on the dc-link capacitor changes by changing P_g and Q_g individually, in cascaded multilevel converters. Also, Figure 6 is not symmetric around the grid's active and reactive power. There is more stress on the capacitor when the same amount of reactive power is being consumed by the grid as compared to when it is being supplied by the grid. The LCL filter demands additional reactive power beyond the amount being fed to the grid.



(a) $I_{cap-rms}$ in the complex power plane



(b) $I_{cap-rms}$ with P_g



(c) $I_{cap-rms}$ with Q_g

Figure 6. (a)-(c) Relationship of $I_{cap-rms}$ with grid power

3.2. DISCUSSION OF VARIOUS RESULTS

A combination of hardware and simulation results were compared with analytical model to validate the derived equations. A single phase five-level cascaded converter was developed and its configuration parameters are shown in Table 2. This table contains specific parameters selected for corresponding discussion. Other parameters like modulation frequency, f_o, are not mentioned.

3.2.1. Evaluation of Analytical and Simulation Results. The analytical model was compared with a simulation setup following the circuit in Figure 4. All the parameters from Table 2 were used except L_h, V_{DC_h} and R_f. V_{DC_s} was used in the analysis of analytical and simulation results of the grid-tied system. The filter was designed for a cut-off frequency of 6 kHz to best accommodate the Bode gain and phase plots in the desired operating point. L_f was set to 0.05 p.u. of base impedance. Figure 7 shows a comparison between the analytical model and the simulation results.

Table 2. Configuration parameters

Parameter		Value
V_{DC_h}	(V)	20
V_{DC_s}	(V)	1800
$f_{cut-off}$	(kHz)	6
L_f	(mH)	20.63
C_f	(nF)	34.11
R_f	(Ω)	22.35
f_c	(kHz)	3
L_h	(mH)	1.8
V_g l-n rms	(V)	7200

The worst case error in simulation and analytical comparison is noted to be about 5.5%. A few sources of this error are as follows. To compare simulation and analytical results, the simulation incorporating the LCL filter was used. The fundamental harmonic that interacts with the sinusoidal grid was manually identified from the FFT of the simulation

Table 3. Test Points to Compare Simulation and Analytical Capacitor Stresses

	1	2	3	4	5	6	7	8
S_g (MVA)	0.6	3.2	6.1	3.5	0.98	8.4	6.6	3.7
P_g (MW)	-0.3	3.1	4.6	3.4	0.2	-3.3	-4.8	-3.6
Q_g (MVAR)	0.5	0.75	-4	-0.74	-0.96	-7.7	-4.5	-1.0
$I_{cap,rms,sim}$(A)	37	211	408	549	605	564	435	245
$I_{cap,rms,ana}$(A)	39	222	427	567	622	582	454	258
$error$ (%)	3.5	5.5	4.6	3.4	2.8	3.2	4.3	5.2

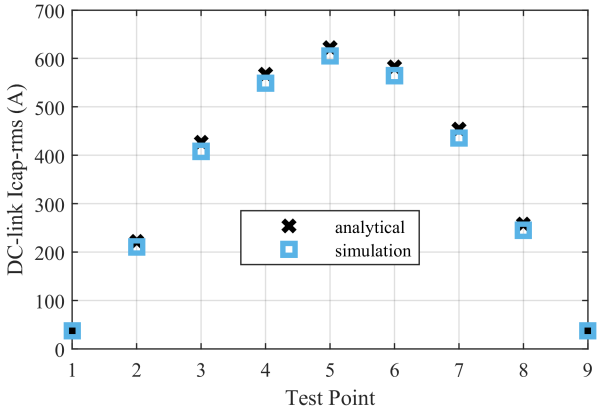


Figure 7. Simulation and analytical comparison for the capacitor stresses

against every test point case. Then, a separate simulation was conducted modeling the identified magnitude of the ac-side harmonic as the current source. In this manner, the contribution of the harmonic causing P_g and Q_g towards the total dc-link capacitor current in a module was recorded. The phase differences in the simulation were also manually observed (e.g. zero crossings of the multilevel signal) to calculate the amount of P_g and Q_g. Another source of error is the level of accuracy achieved by the finite m and n indices, which should theoretically be infinite. The damping resistors in the simulation have also not been incorporated in the analytical model.

Besides errors, the results show that for all the sampled points in Table. 3, the rms portion of the 120 Hz harmonic was close to the sum of rms contribution from non-120 Hz harmonics (i.e., within 1 A) in this application.

3.2.2. Hardware and Simulation Results Evaluation. For hardware results, a single phase five-level H-bridge converter is operated in the inverter mode with an RL load. Therefore, V_{DC_h}, R_f, L_h and f_c are hardware and simulation parameters in this case. For this setup, the dc-link current was measured and compared with simulations. The five-level voltage, the RL load current and the voltage output from both half-bridges of one module can be seen in Figure 8.

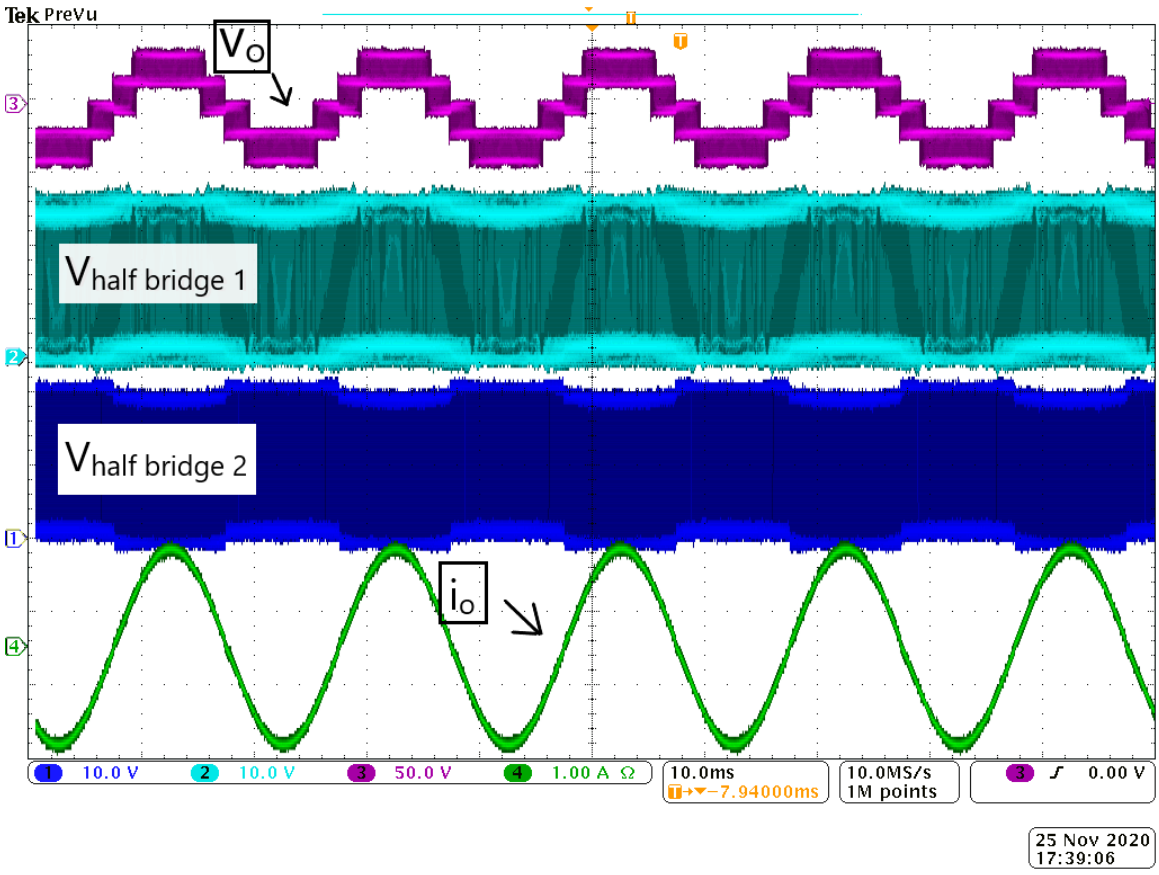
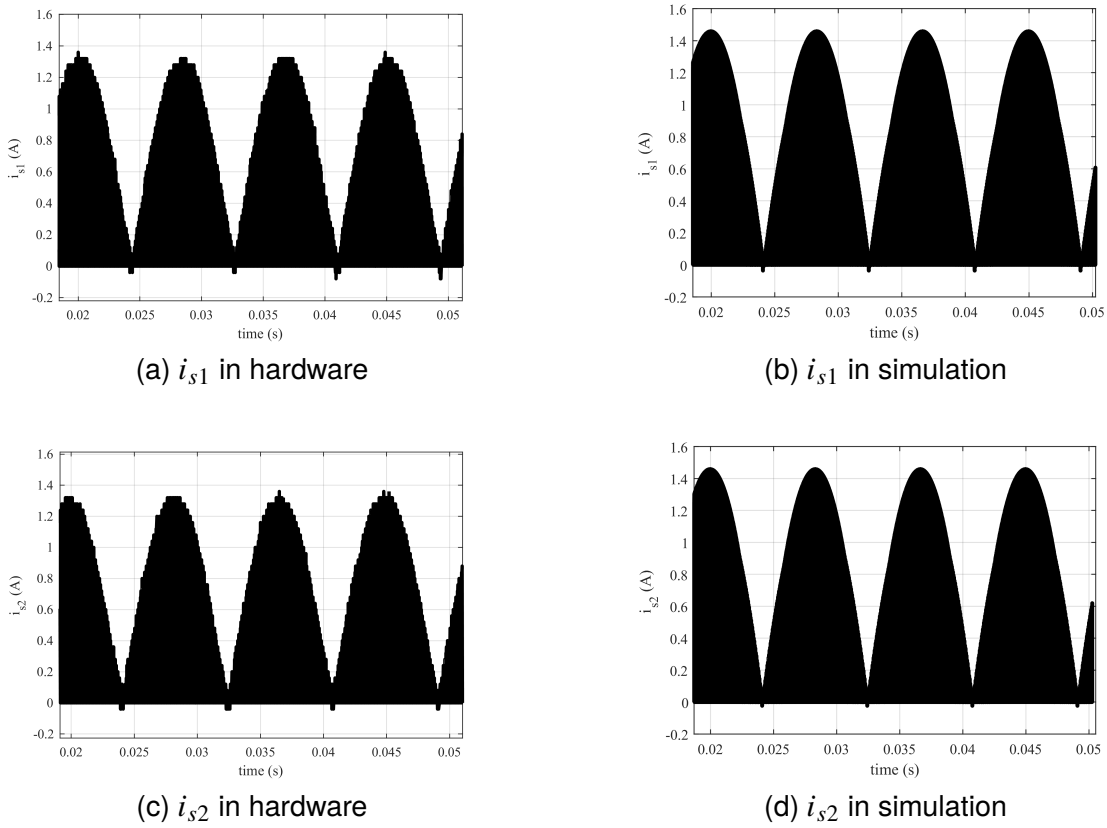


Figure 8. Hardware results for the five-level cascaded H-bridge converter

The ac-side current through the RL load and the output voltage of the half bridges were measured directly as seen in Figure 8. Since the dc-link current is of discontinuous nature, a regular Hall-effect based current probe cannot be used to measure it directly. Therefore, the method recommended in [14] was used. The method is described as follows.



(a) i_{s1} in hardware

(b) i_{s1} in simulation

(c) i_{s2} in hardware

(d) i_{s2} in simulation

Figure 9. (a)-(d) Comparison of dc-link currents in the two modules

As illustrated in the referred work, the half-bridge outputs were multiplied with the ac-side load current to obtain the hardware dc-link current. This hardware result was then compared with the simulation results as shown in Figure 9a and Figure 9b respectively.

The rms current measured in the hardware and that in the simulation had a worst case difference of 6.9%. This difference is explained in two parts. The switching functions from the ideal simulation blocks are not the same as those coming from the digital processor. The code implemented in the digital processor contains deadtime which has not been incorporated in to the simulation blocks. This difference has direct impact on the multiplication of i_o with individual half-bridge voltage outputs to calculate dc-link current as the pulse widths are not the same in the hardware as those in simulation. However, this is only partially contributing to the deviation in pulses as load current does not exist.

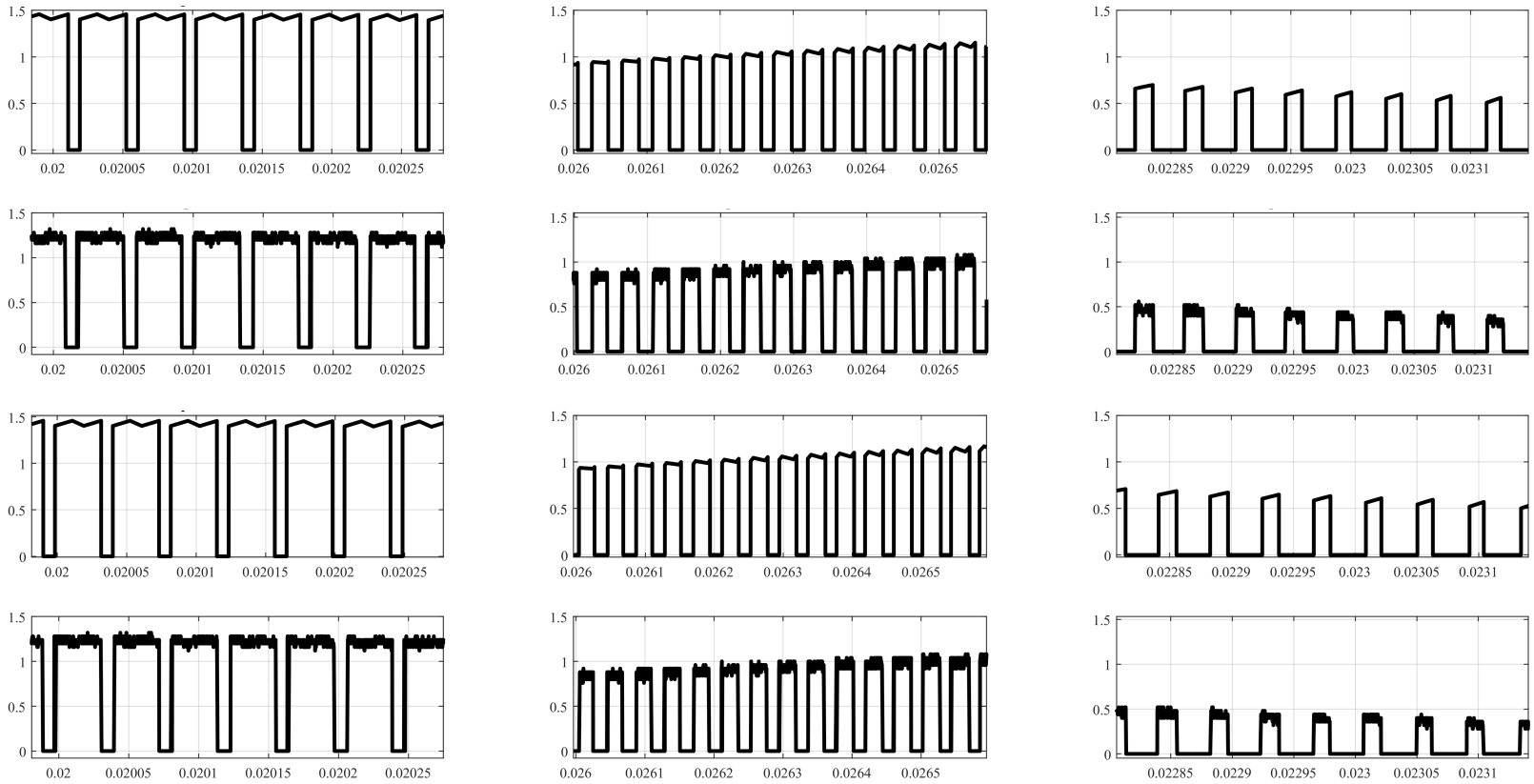


Figure 10. Zoomed-in comparison of the dc-link currents in different time ranges (from left to right), simulation i_{s1} and i_{s2} (as first and third rows) and hardware i_{s1} and i_{s2} (as second and fourth rows)

When the load is turned on, dynamic behavior between the body diode and IGBT-based half-bridge causes the pulse amplitudes to deviate as well. This deviation is evident from Figure 8. The conduction of body diode is initiated during deadtime. Based on the polarity of the load current, corresponding body diodes will conduct. Due to the body diode's forward voltage drop, the pulses seen in Figure 8 are slightly above and below V_{DC} as well as slightly below and above the 0 voltage level. Since the IGBT's body-diode forward voltage drop is comparable to V_{DC} (i.e., 0.7 V and 20 V respectively), the error in the amplitude of the pulses is high. As V_{DC} increases, the error in the pulse amplitude caused by body diode's conduction would decrease. The hardware prototype is finally shown in Figure 11 with two modules for the five-level converter, digital processor and RL load.

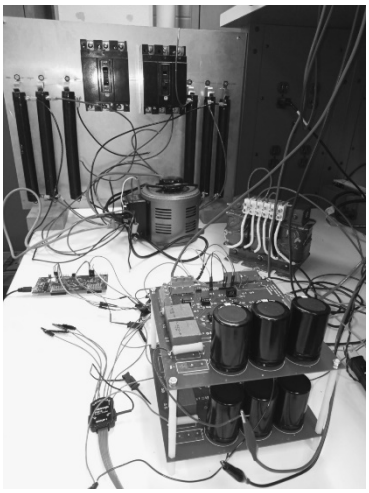


Figure 11. Hardware prototype of the cascaded H-bridge system

4. CONCLUSION

In this paper, a detailed and exact mathematical model has been developed for the dc-link current in a cascaded H-bridge multilevel converter. The detail of the model has been used to study the converter's interaction with a grid-tied system. The grid's active and reactive power commands have been mapped to the dc-link current stress in the

bus capacitors. The analytical, simulation and hardware results have been evaluated in a variety of setups and these show a good match thereby validating the work. For future work, the derivations motivate deriving a framework for capacitor sizing against the dc-bus voltage specifications. Overall, this work contributes to estimating the lifetime of the dc-link capacitors in an accurate manner which in-turn adds to system reliability by avoiding contingency outages and improving scheduled outages in power systems.

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SECTION

2. SUMMARY AND CONCLUSIONS

In this thesis, a detailed and exact mathematical model has been developed for the dc-link current in a cascaded H-bridge multilevel active front-end converter. In the first paper, the derivations quantified the contribution of ac-side current, which is a single harmonic of fundamental frequency, towards the dc-link capacitor's instantaneous and rms current. In the second paper, the assumption that the ac-side current is a sinusoid of the fundamental frequency is removed and the expression derived again. The front-end typically includes more than fundamental frequency sinusoid on the ac-side. Therefore, the framework derived in the second paper provides illustrations on how to use the equations to find the contribution of an arbitrary multilevel ac-side current harmonic towards the dc-link current, thereby differentiating the stress on the capacitor that is caused by the grid's active and reactive power commands, from the additional stress on these caused by filter harmonics. Consequently, a complete framework is provided to find true dc-link capacitor stress in a multiphase, multilevel cascaded H-bridge active front-end converter. Overall, this work contributes to estimating the lifetime of the dc-link capacitors in an accurate manner which in-turn adds to system reliability by avoiding contingency outages and improving scheduled outages in power systems.

This work also provides the platform for further inquiry. Based on the present work, the dc-link current in phase shifted carrier based PWM converters can be quantified easily. The results provided for the dc-link current contribution from each hard-switched half-bridge are portable and reusable to converters with similar drives. Moreover, since the expression for capacitor current is available, the expression for sizing the capacitor against bus voltage ripple requirements can be obtained. Once these expressions are available,

the dependencies of bus voltage and current ripple due to the system are observable. Consequently, the feedback between the PWM drive and bus voltage and current ripple can be established using complete theoretically offered parameters, thereby expanding design and control flexibility in PWM carrier-based power electronic converters.

VITA

Muhammad Shehroz Malik received his Bachelor of Science degree (B.S.) in Electrical Engineering from Lahore University of Management Sciences, Lahore, Pakistan in May, 2017. He received his Master of Science degree (M.S.) in Electrical Engineering from Missouri University of Science and Technology (formerly University of Missouri, Rolla) in December, 2021.

Shehroz studied Power Electronics as his research field. In his undergraduate school, his senior year project was on power electronic processing units for low-voltage and low-power off-grid microgrids. At S&T, he remained part of the research team enabling extreme fast electric vehicle off-board charging with advanced energy storage. During this time, he contributed to designing the dc-link capacitors for grid-connected multilevel ac-dc converter at the active front-end of the charging station.