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Modeling and control of cascaded bridgeless multilevel rectifier under unbalanced load conditions

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MODELING AND CONTROL OF CASCADED BRIDGELESS MULTILEVEL RECTIFIER UNDER UNBALANCED LOAD CONDITIONS

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ABSTRACT

The goal of this project is to model and control a novel unidirectional cascaded multilevel bridgeless rectifier as an active front end in medium and high voltage applications. This topology has many advantages over a conventional cascaded H-bridge rectifier, such as lower implementation cost, higher reliability, and greater flexibility with similar power quality. The complete design process of the proposed converter is developed step by step in order to meet all the desired objectives. The steady-state mathematical model is used to develop a method for the voltage balancing of dc cells. Power factor analysis is discussed to mathematically derive requirements for the number of partially controlled and fully controlled H-bridges in the proposed H-bridge converter. Power loss, efficiency, and cost comparison studies between the traditional cascaded H-Bridge converter and the proposed bridgeless converter demonstrate the advantages.

After exploring various well-established control methods, a novel control strategy is proposed to achieve dc voltage balancing, fast and robust grid synchronization, power factor correction, and elimination of zero crossing current distortion under both balanced and unbalanced load conditions. The converter can also be used for reactive power compensation in a grid tied power system if a sufficient number of fully controlled H-bridge modules are included. Processor-In-the-Loop (PIL) simulation has been the utilized to validate the performance of discrete control structure. Simulation and experimental results validate the models and control method.

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1. INTRODUCTION

Multilevel converters represent an interesting solution on the occasions of medium and high voltage power conversion applications[1; 2; 3]. Different topologies of multilevel converters like Neutral Point clamped (NPC), flying capacitor and Cascaded H-bridge converters (CHB) have been under research and development for five decades [4]. Multilevel converters today are used in wide range of single-phase and three-phase high power applications like conveyors, compressors, pumps, traction systems, propulsion systems, and renewable energy conversion. Despite their wide applicability, multilevel converters present a great deal of challenges which vary between different topologies used and for different applications.

This work is based on Cascaded H-bridge (CHB) converter technology because of its simplicity, modularity, bidirectional property, flexible regulation of output voltage and power quality [5]. Using a CHB converter as an active front end eliminates the need of a bulky and expensive line frequency transformer, thus increasing the efficiency and power density of the system. Each fully controlled switch, such as an IGBT or MOSFET, requires a gate driver and associated signal chain, complicating the hardware system when very high number of switches are used. IGBTs and MOSFETs involve switching losses which constitute significant percentage of losses in a power converter. Hence, the use of conventional CHB technology posed new challenges in high power applications. [6].

Figure 1.1 shows a simplified circuit of a single-phase N-cell CHB converter. All N cells are cascaded and connected in series. Each cell has four fully controlled switches and a dc link capacitor. Higher voltage levels are possible with the increase in number of cells. Unfortunately, a higher number of cascaded cells complicates the converter control

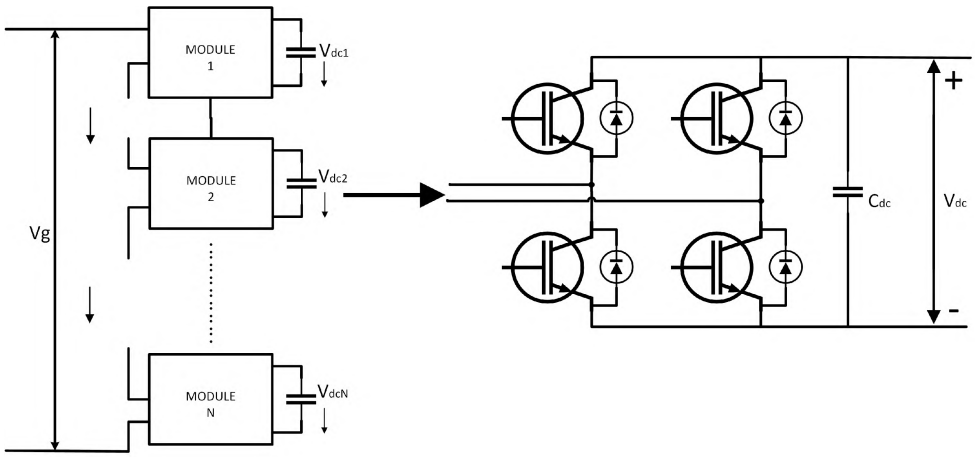


Figure 1.1. N-cell cascaded H-bridge converter

since a single current passing through all of the cells is responsible for dc voltage balancing in all the N H-bridge cells. At the same time, more voltage levels lower the total harmonic distortion (THD) of grid current [9].

The CHB converter is bidirectional and hence can be used as both an inverter and a rectifier. However, the majority of the applications like conveyors, pumps, electric vehicle charging just require unidirectional power flow [10], [11]. Figure 1.2 shows a simple 2-module version of the proposed Cascaded Bridgeless Rectifier topology (CBR) where some fully controlled switches in each module are replaced with simple uncontrolled switches (diodes). Reduction in the number of fully controlled switches greatly reduces the implementation cost, hardware and control complexity. Cost estimation, power loss and efficiency evaluation and THD of input grid current of both conventional Cascaded H-bridge converter and proposed Cascaded Bridgeless rectifier have been carefully studied. THD of input current is one of the very few disadvantages associated with CBR technology which is addressed in the subsequent sections.

Voltage Imbalance between multiple floating dc capacitors is a common challenge in CHB rectifier[7],[8]. The voltage imbalance has a variety of different causes like tolerances of passive components, unequal conducting and switching losses in semiconductor devices,

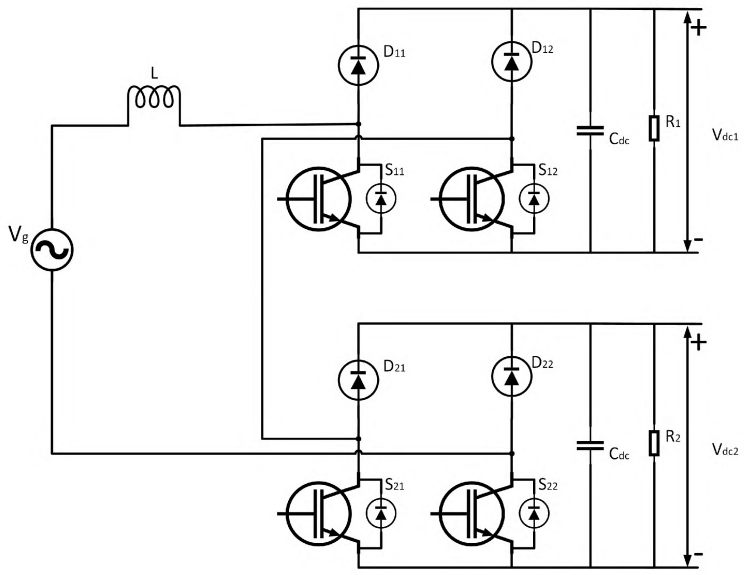


Figure 1.2. Two-module cascaded bridgeless rectifier

signal delay imbalance, and resolution issues in control circuit including voltage and current sensors as mentioned in [12]. The overall control of active rectifiers typically consists of grid current control, dc voltage balancing and grid voltage synchronization. The improved control strategy proposed in this work ensures balanced dc bus voltage, satisfactory power factor, and balanced active and reactive power between the H-bridges and also eliminates the zero-crossing distortion.

The synchronization of control with grid voltage is one of the important control objectives. Vector control methods (dq and PQ control) are mostly used for active rectifier control applications which involve Park transformation [15]. A typical PLL in a three-phase system also uses Clarke and Park transformation. However, the Clarke transformation cannot be used in single-phase systems. Orthogonal Signal Generation PLLs (OSG-PLLs) have gained a lot of importance in the field of power electronics and power systems [16],[18]. The Second-Order Generalized Integrator-PLL (SOGI-PLL) has become the most commonly used PLL in single-phase applications because of its low computational burden, high robustness and high filtering capability [17]. The SOGI part is used to obtain orthogonal

$\alpha\beta$ components from the single-phase grid voltage. These quadrature signals are sent to a Synchronous Reference Frame-based PLL (SRF-PLL). The estimated frequency of the SRF-PLL loop is fed back to the SOGI part to make SOGI-PLL frequency adaptive, thus ensuring accuracy under frequency fluctuation conditions.

Zero crossing input current distortion is a common problem when the power converters are forced to operate at unity power factor [19]. The single-phase dq decoupled control proposed in this work introduces a lagging phase angle ϕ to the grid voltage to eliminate zero crossing distortion. This control method considers all of the modules to be partially controlled Diode H-Bridge (DHB) modules. Voltage balancing can also be achieved by regulating the averaged voltage of all the dc cells using a PI regulator. However, this control cannot be used under input and load disturbances. An improved control strategy is then proposed where few DHBs are replaced by Fully controlled H-bridges (FHBs) which provide sufficient reactive power to the input filter inductor and thus are responsible for maintaining unity power factor in the system. In this way, reactive power compensation can be achieved by carefully choosing the number of FHB modules. The proposed improved control also maintains voltage balancing in all the cells under different load and input conditions. The proposed control strategies can be easily applied to three-phase systems. A five-module single-phase CBR has been used in this work for simulation and experimental validations. The complete simulation model has been developed in PLECS® [1]. The Processor-In-the-Loop (PIL) technique in PLECS has been utilized to validate the performance of discrete control structure.

The outline of the thesis is as follows. First we discuss different modes of operation in the proposed CBR. Mathematical modeling, power factor analysis, inductor sizing, cost and efficiency estimation of proposed CBR is discussed in Section 2. The SOGI-PLL technique for single phase grid synchronization, dq decoupled control and improved control strategy

[1] PLECS is a registered trademark of Plexim GmbH.

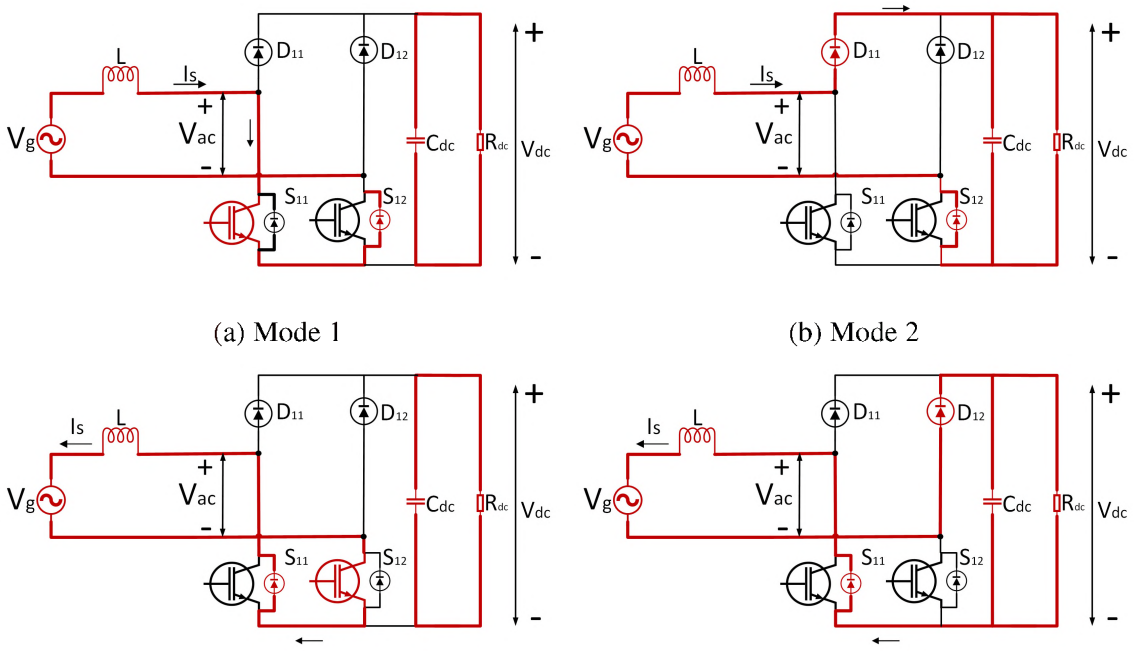
are discussed in detail in Section 3. Section 4 discusses the hardware implementation of the five-module CBR converter. Finally, simulation and experimental results validate the proposed control strategies.

2. MODELING OF MULTILEVEL CASCADED BRIDGELESS RECTIFIER (CBR)

This section describes the overall design of proposed CBR converter. The converter's modes of operation and corresponding mathematical models are discussed. The requirement for the number of FHB modules and partially controlled DHB modules is derived in Section 2.2. Power factor analysis is done using phasor diagrams and the inductor sizing is determined for unbalanced load conditions (that is, unbalanced dc-side load among the modules). Finally, power loss and efficiency evaluation for both conventional cascaded H-bridge converter and proposed cascaded bridgeless rectifier is done justifying the advantages of CBR over traditional CHB.

2.1. CONVERTER MODES OF OPERATION IN CBR

In this section, the modes of operation in one DHB module are analyzed. As previously discussed, each module has two fast recovery diodes D_{11} and D_{12} acting as substitutes for fully controlled IGBT/ MOSFET switches and two active switches S_{11} and S_{12} as shown in Figure 2.1. Since the two diodes D_{11} and D_{12} are uncontrollable and unidirectional in nature, the states of switches S_{11} and S_{12} and the polarity of the input current determine the resultant ac voltage V_{ac} across each module. A single module CBR (that is, a single DHB module) has four modes of operation as shown in Figure 2.1. The current polarity, conducting switches, and the value of ac voltage for each mode is given in Table 2.1.



(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

Figure 2.1. Four modes of operation in single module CBR

Table 2.1. Four modes of operation in single cell CBR

Parameter	Mode 1	Mode 2	Mode 3	Mode 4
Current polarity	$I_g > 0$	$I_g > 0$	$I_g < 0$	$I_g < 0$
Conducting Switches	S_{11}, S_{12}	D_{11}, S_{12}	S_{11}, S_{12}	D_{12}, S_{12}
AC voltage	$V_{ac} = 0$	$V_{ac} = V_{dc}$	$V_{ac} = 0$	$V_{ac} = -V_{dc}$

2.2. STEADY STATE MATHEMATICAL MODEL OF THE CBR

Figure 2.2 shows an N-module single-phase CBR converter. This section derives the relationship between the duty ratio of each module d_i and dc voltage balancing. As shown in Figure 2.2, the number of Diode H-Bridge modules (DHB) and Fully controlled H-Bridge modules (FHB) are defined to be l and m respectively. V_i and V_{dci} represent the net ac voltage and dc link voltage across i^{th} module. V_{DHB} and V_{FHB} represent the resultant ac voltage across all the DHB modules and FHB modules respectively. The expression for m, the minimum number of FHB modules will be derived in the subsequent section. When

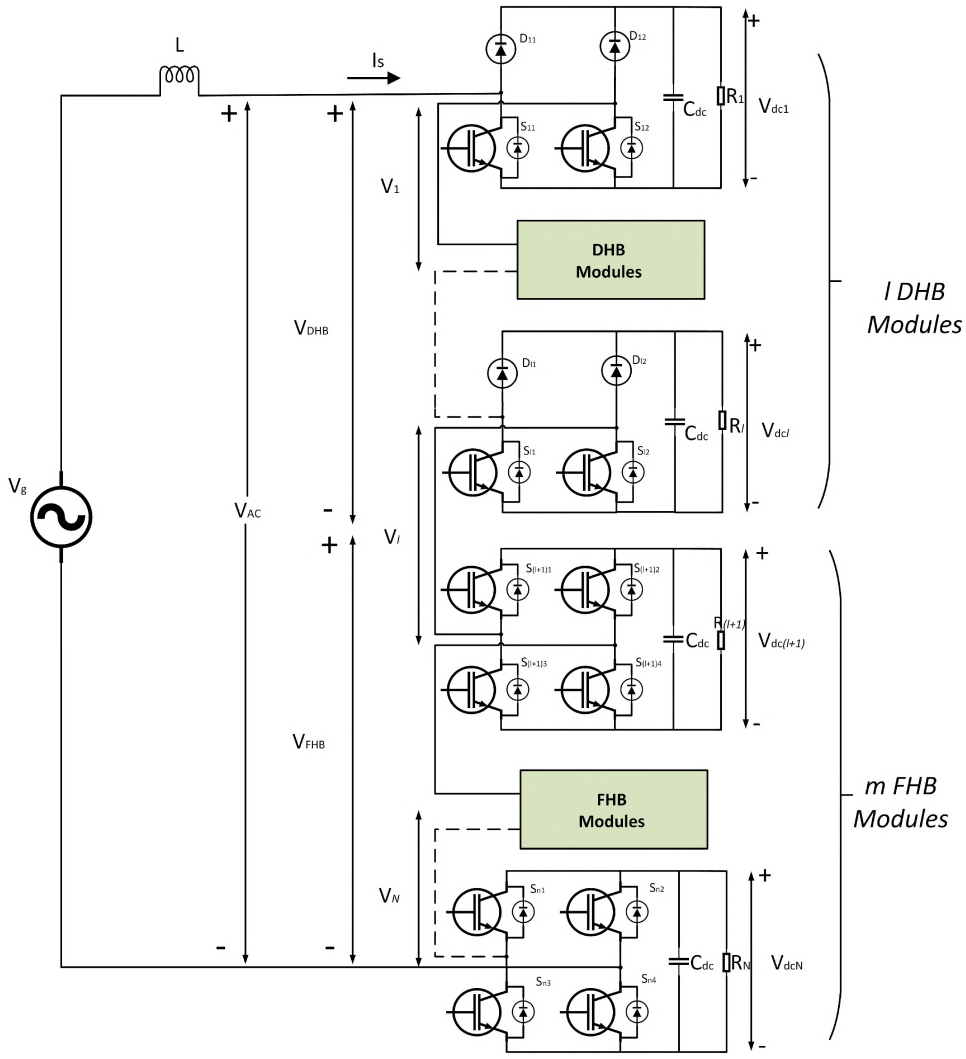


Figure 2.2. N-module cascaded bridgeless rectifier

$l = 0$, the CBR degenerates to a conventional CHB rectifier. S_i is defined to be the switching function of i^{th} module. Hence, the active switches are turned on when $S_i = 1$ and turned off when $S_i = 0$. The resultant ac voltage at i^{th} module, V_i depends upon the switching function and the direction of flow of input grid current as shown below,

$$V_i = \begin{cases} (1 - S_i)V_{dci} & i_s > 0 \\ -(1 - S_i)V_{dci} & i_s < 0 \end{cases} \tag{2.1}$$

The mathematical model under steady state conditions for the system shown in Figure 2.2 can be derived by applying KVL and KCL, resulting in

$$L\frac{di_g}{dt} = v_g - R_{ac}i_g - \sum_{i=1}^{N} S_i^* v_{dci} \tag{2.2}$$

$$C\frac{dv_g}{dt} = S_i^* i_g - \frac{v_g}{R_{ac}} \tag{2.3}$$

where

v_g, i_g	Input grid voltage and current.
L	Series inductance.
C	DC link capacitor at each module.
R_{ac}	AC side equivalent resistance.
R_i	Equivalent load resistance.
S_i^*	$(1 - S_i)$ for $i = 1, 2, 3, ..., N$.

The average voltage across an inductor in a periodic cycle is zero. Similarly, average current through a capacitor in a periodic cycle is zero. Applying these balance principles to equations 2.1, 2.2 and 2.3, we obtain the input-output characteristics of CBR converter as

$$\begin{aligned} i_g &= \frac{v_g}{R_{ac} + \sum_{i=1}^{N} R_i(1 - d_i^2)} \\ v_{dci} &= \frac{v_g R_i(1 - d_i)}{R_{ac} + \sum_{i=1}^{N} R_i(1 - d_i^2)} \end{aligned} \tag{2.4}$$

Equation 2.4 clearly indicates that the output dc voltage of i^{th} module can be controlled by modifying duty ratio d_i. A critical objective is to balance dc voltages in all the modules by employing a proper control to ensure safe and reliable operation [13].

2.3. POWER FACTOR ANALYSIS USING PHASOR DIAGRAMS

Power factor indicates the effective power transferred from source to load. Hence, achieving unity or close to unity power factor is an important control objective in any converter [14]. Assuming unity power factor is achieved, Figure 2.3 shows the phasor diagram where the input grid voltage V_g is in phase with grid current I_g. Voltage across the series inductor V_L is orthogonal to input current I_g. V_{ac} is the net ac voltage of the CBR which is equal to the sum of the ac voltages of all the CBR cells.

$$V_{ac} = \sum_{i=1}^{N} V_i \tag{2.5}$$

V_{ac} lags input current I_g by certain angle defined as θ as shown in Figure 2.3. During the time period indicated by θ, input current and input ac voltage are opposite in polarity. However, in all the Diode H-bridge modules (DHB), the current and voltage cannot be opposite in polarity due to the unidirectional property of diodes. Hence, during this period, 0 V ac voltage is generated across the CBR as shown in Figure 2.4.

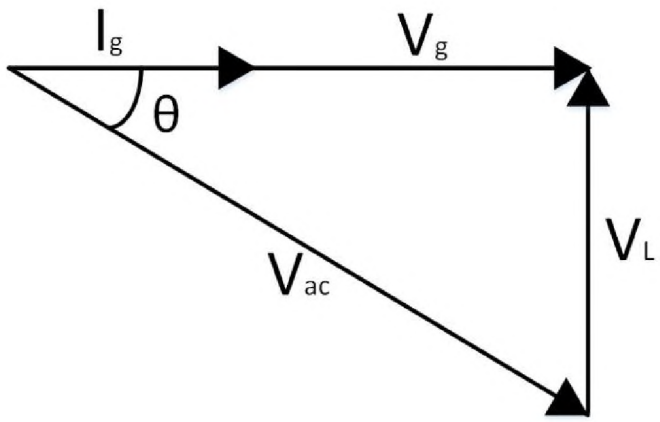


Figure 2.3. Phasor relationship under unity power factor

As a result, serious current distortion appears during the period of θ as shown in Figure 2.4. Thus, unity power factor can never be achieved if all of the cells are unidirectional DHB cells.

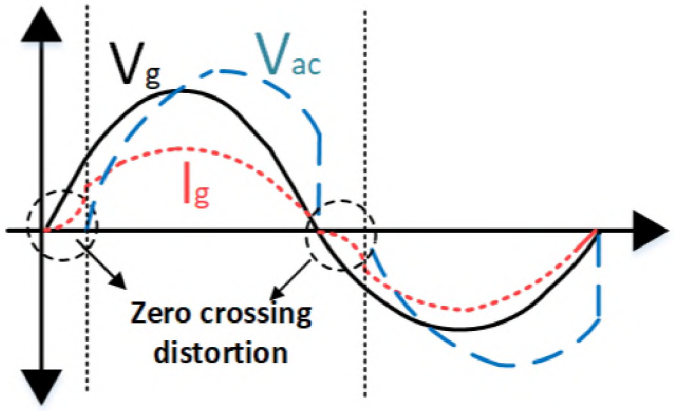


Figure 2.4. Zero crossing input current distortion

There are two possible solutions to eliminate zero crossing distortion. First idea is to make the input current I_g in phase with the net ac voltage V_{ac}. This can be achieved by introducing a lagging angle ϕ and thus lagging power factor. The resultant voltage wave forms are as shown in Figure 2.5

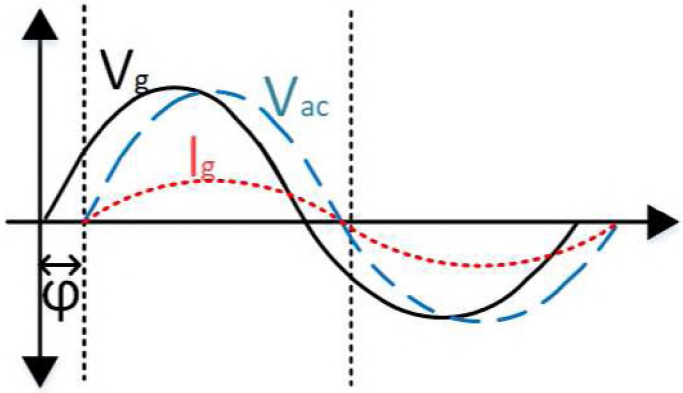


Figure 2.5. AC waveforms when ϕ is introduced

The better solution proposed in this work is the introduction of Fully controlled H-bridge (FHB) modules. FHB modules are bidirectional and can supply the sufficient reactive power to the inductor so that unity power factor is achieved at the grid. Reactive power compensation is one of the major advantages of the proposed topology. The first l modules are assumed to be DHB modules and the next m to be FHB modules. The net ac voltage across the DHB and FHB modules are V_{DHB} and V_{FHB} respectively satisfying,

$$V_{DHB} = \sum_{i=1}^{l} V_i \tag{2.6}$$

$$V_{FHB} = \sum_{i=l+1}^{N} V_i \tag{2.7}$$

$$V_{ac} = V_{DHB} + V_{FHB} \tag{2.8}$$

The number of FHB modules can be increased if the series inductor consumes higher amount of reactive power. Usually, the voltage drop across the inductor V_L is low compared to the to the supply voltage V_g or total ac voltage V_{ac}. Therefore, one or fewer FHB modules could be sufficient in most of the practical applications.

Figure 2.6 shows the phasor diagram of the proposed converter where V_g and V_{DHB} are in phase with the grid current I_g. As discussed before, V_{FHB} should contain the reactive component to supply sufficient reactive power to the series inductor. Hence, V_{FHB} lags grid current I_g by certain angle defined as α.

The active component voltage of each module can be expressed as,

$$V_{ai} = \begin{cases} V_i & i = 1, 2, 3, ..., l \\ V_i \cos\alpha & i = l+1, l+2, ..., N. \end{cases} \tag{2.9}$$

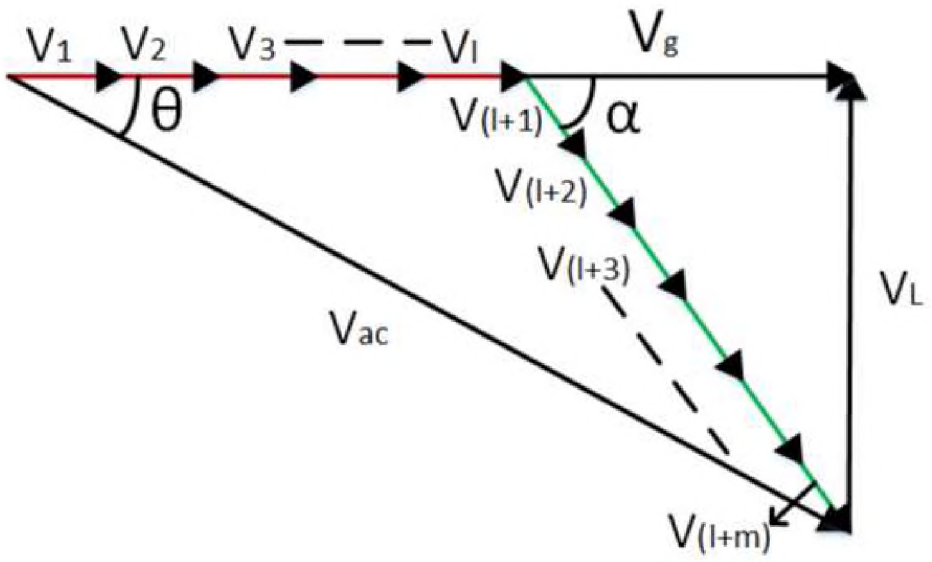


Figure 2.6. Phasor diagram of proposed CBR converter

Also, the sum of active components of ac voltages in all the N-modules is the grid voltage V_g, as shown below,

$$V_g = \sum_{i=1}^{N} V_{ai} \tag{2.10}$$

Under steady state conditions, dc link voltages are equal to the reference value and all the converters have same current flowing through them. Hence, the active component voltage of each module can be expressed as,

$$V_a = V_{ai} = \frac{V_g}{l+m} = \frac{V_g}{N}, \qquad i = 1, 2, 3, ..., N. \tag{2.11}$$

2.4. DETERMINATION OF NUMBER OF DHB AND FHB MODULES

The number of DHB modules (l) and FHB modules (m) are carefully determined satisfying the following principles of operation [20].

- Unity power factor rectification and sinusoidal input current.

- Balanced output dc voltages of each module. Imbalanced voltage may cause capacitor over voltage.
- Minimized number of FHB modules (m) to minimize the number of controlled switches, to reduce circuit complexity and to lower the implementation cost.

The maximum ac voltage of each module that can be obtained through modulation is

$$\begin{cases} V_{max} = \frac{4}{\sqrt{2}\pi} V_{dc} \\ V_{ai} \leq V_{max} \qquad i = 1, 2, 3, ..., N. \end{cases} \tag{2.12}$$

As shown in the phasor diagram of Figure 2.7, the total ac voltage across m FHB modules $\frac{m}{N} V_g$ forms a phasor triangle with voltage drop across the inductor V_L and the active component of V_{FHB} (mV_a) satisfying the following equation,

$$(mV_a)^2 + (V_L)^2 = V_{FHB}^2 \tag{2.13}$$

Substituting equations 2.6, 2.7, 2.12 in equation 2.13 gives,

$$(mV_a)^2 + (V_L)^2 \leq (mV_{max})^2 \tag{2.14}$$

Define the step up ratio as,

$$V_{dc} = kV_g \tag{2.15}$$

where V_{dc} is the dc voltage across all the modules under steady state conditions. Neglecting power losses and considering input-output power balance yields

$$V_g I_g = N \frac{V_{dc}^2}{R} \tag{2.16}$$

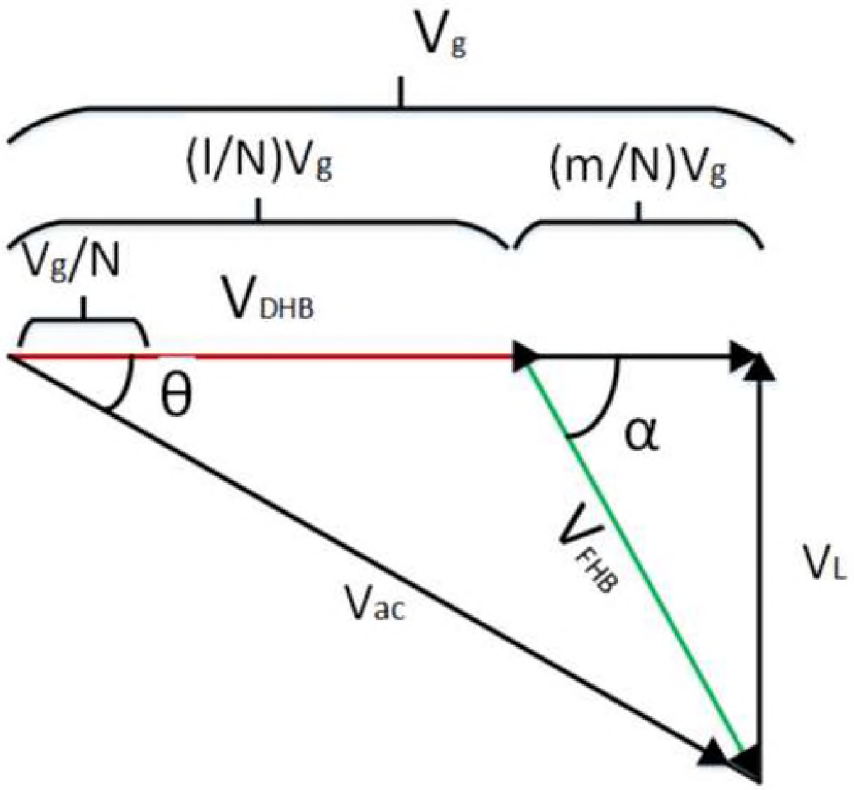


Figure 2.7. Alternative phasor representation of proposed CBR converter

Substituting equations 2.12, 2.15, 2.16 into 2.13 and plugging in $V_L = \omega L I_g$ gives the final expression for m under balanced load conditions as

$$m > \frac{\omega k N}{k^2 \sqrt{\frac{8}{\pi^2}} - 1} \frac{LI}{V_g} \tag{2.17}$$

After choosing the minimum value of m from the equation 2.17, the number of DHB modules can be easily chosen as $l = N - m$. It can be observed from 2.17 that the value of m increases when the load increases. Heavier load implies higher reactive power consumed by the series inductor and hence more fully controlled cells are necessary to compensate the reactive power.

For unbalanced dc loads, the core idea of determining the minimum value for m is the same. The active component of voltage across each cell is directly proportional to the load conductance and hence equation 2.11 is modified as,

$$V_{ai} = k_i V_g \tag{2.18}$$

where k_i is defined as the load ratio given by,

$$k_i = \frac{\frac{1}{R_i}}{\sum_{i=1}^{N} \frac{1}{R_i}} \tag{2.19}$$

Following the similar procedure as in the balanced load case, the value of m for unbalanced load conditions is determined by

$$m > \frac{\sqrt{2}\pi}{4} \sqrt{\frac{\omega^2 L^2 \left(\sum_{i=1}^{N} \frac{1}{R_i}\right)^2}{V_g^2} + \frac{N^4}{K^2} \left(\sum_{i=1}^{m} n_i\right)^2} \tag{2.20}$$

Similar to the case of balanced loads, the minimum number of FHB modules is obtained from equation 2.20 and then the number of DHB modules can be easily obtained as $l = N - m$.

2.5. INDUCTOR SIZING

In this section, the minimum value of inductance is derived for unbalanced load conditions. Inductor sizing is usually determined based on the maximum allowed current ripple in a power converter [21]. The maximum active component voltage across each module is given by equation 2.12. In addition, if V_L is the voltage across the inductor,

$$\left(\sum_{i=1}^{m} V_{ai}\right)^2 + V_L^2 \leq (m V_{max})^2 \tag{2.21}$$

The constraint for series inductance is determined by assuming the extreme condition of $m = N$, i.e., all of the modules used are fully controlled H-bridge modules. Therefore, equation 2.21 is modified to

$$V_L^2 < (NV_{max})^2 - \left(\sum_{i=1}^{N} V_a i\right)^2 \tag{2.22}$$

Substituting equations 2.12 and 2.11 into equation 2.14 gives,

$$V_L^2 < \left(\frac{8}{\pi^2}k^2 - 1\right) V_g^2 \tag{2.23}$$

where k is the step up ratio. Substituting $V_l = \omega L I_g$ in Equation 2.23 yields the final constraint for inductance,

$$L < \sqrt{\frac{\left(\frac{8}{k\pi^2} - \frac{1}{k^3}\right) NV_g}{V_{dc}\omega^2 \sum_{i=1}^{N} \frac{1}{R_i}}} \tag{2.24}$$

2.6. COST AND EFFICIENCY ESTIMATION OF CONVENTIONAL CHB AND PROPOSED CBR CONVERTER

This section compares the power loss, efficiency and overall cost of conventional CHB converter and CBR converter. For most of the ac-dc rectifiers in AFE applications, power loss occur in semiconductor switches (conduction and switching losses), series inductor, transformer (core and copper loss) and in resistive loads. cascaded H-bridge technology anyway eliminates the need of transformer and hence CHB/ CBR doesn't have transformer losses.

The series inductor is common to both CHB and CBR topologies, and so the only difference is with the semiconductor switches. The losses in semiconductor switches constitute most of the power loss in many power electronic converters. Fast recovery diodes are used to replace IGBT switches in CBR converter.

2.6.1. Calculation of Losses. Power losses in 4500 W CHB and CBR converters are calculated assuming same hardware parameters for both the converters. The discussion below assumes the use of an IGBT, but similar conclusions apply for applications that instead use a MOSFET.

2.6.1.1. Calculation of losses in IGBT. As mentioned before, IGBT switches have conduction and switching losses. Switching losses are caused by transition of switching devices between the blocking stage and conduction stage which are usually referred to as turn-on and turn-off losses. The switching losses (turn on and turn-off) can be calculated as

$$\begin{aligned} P_{OFF} &= \frac{1}{2} V_{OFF} I_{OFF} t_f f_{sw} \\ P_{ON} &= \frac{1}{2} V_{ON} I_{ON} t_r f_{sw} \\ P_{SW} &= (P_{ON} + P_{OFF}) \end{aligned} \tag{2.25}$$

where:

t_r Rise time of IGBT.

t_f Fall time of IGBT.

f_{sw} Switching frequency

Turn on and turn off switching energies (E_{on} and E_{off}) are usually mentioned in IGBT data sheets. In such cases, the switching losses can be directly calculated as

$$P_{SW} = (E_{on} + E_{off}) f_{sw} \tag{2.26}$$

The conduction losses occur when the device is in full conduction. Conduction losses are directly proportional to the duty cycle and computed by averaging the loss in each conduction cycle,

$$P_{CON} = \frac{1}{T} \int_0^T [v_f(t) i_{on}(t) D(t) dt] \tag{2.27}$$

where v_f is the voltage drop across the switch, i_{on} is the current flowing during the conduction mode, T is the switching period and D is the duty cycle. For a MOSFET,

$$P_{CON} = i_{on}^2 R_{ds,on} \frac{V_o}{V_{in}} \tag{2.28}$$

2.6.1.2. Calculation of losses in a diode. Most of the diodes have fast turn on time and reverse blockage current is negligibly small. As turn on and turn off losses are neglected, diodes have conduction and reverse recovery losses. The reverse recovery loss in a diode can be expressed as,

$$P_{rr} = E_{rr} f_{sw} \tag{2.29}$$

Where, E_{rr} is the turn off loss in a diode whose value is sometimes mentioned in the datasheet. Reverse recovery losses can also be calculated based on reverse recovery charge of diode as shown below,

$$P_{rr} = Q_{rr} V_{in} f_{sw} \tag{2.30}$$

Conduction loss calculation in a diode P_{CONd} is similar to that of an IGBT switch. Hence, the net loss in a diode can be expressed as,

$$P_D = P_{CONd} + P_{rr} \tag{2.31}$$

Net loss in the converter can be calculated as,

$$P_{Tot} = P_Q + P_D \tag{2.32}$$

2.6.2. Converter Specifications. A 4500 W ac-dc cascaded H-bridge converter has been chosen for the cost and efficiency estimation. Same hardware parameters have been chosen for both CHB and CBR converters to make a fair comparison. The fully controlled IGBT switches and the fast recovery diodes are designed based on the converter specifications shown in Table 2.2.

Table 2.2. CBR converter specifications

Parameters	Range/ Magnitude
RMS Grid voltage (V_g)	500 V
Switching frequency (f_{sw})	10 kHz
Reference DC voltage (V_{dc})	300 V
No of modules (N)	5
DC link capacitor (C_{dc})	3.2 mF
Output Power (P_{Max})	4500 W

The ratings of the selected IGBT and fast recovery diode are as shown in Table 2.3 and Table 2.4 respectively.

Table 2.3. IGBT ratings

Parameters	Range/ Magnitude
Part number	FGA25N120ANTDTU-F109
Voltage- Collector emitter max breakdown (V_{CE})	1200 V
Collector current (I_{Cmax})	50 A
Rise time (t_r)	60 ns
Fall time (t_f)	100 ns
Max Power dissipation	325 W

2.6.3. Power Loss and Efficiency Comparison. The power loss in a 5 module CHB converter with four fully controlled IGBT switches in each module is compared with a 5 module CBR converter with two IGBT switches and two fast recovery diodes in each module as shown in in Figure 2.8.

Table 2.4. Diode ratings

Parameters	Range/ Magnitude
Part number	APT60D60BG
Forward voltage (V_F)	1.6 V
Max Reverse DC voltage (V_R)	600 V
Max Average forward current (I_F)	60 A
Reverse recovery time (t_{rr})	130 ns
Reverse recovery charge (Q_{rr})	220 nC

It is evident that fully controlled switches constitute most of the losses in a power converter. Thus replacing IGBT switches with fast recovery diodes in CBR resulted in almost 35% reduction of total losses. This change become more significant in the case of three phase systems. For example, a 5 module three phase CHB converter has 60 fully controlled IGBT switches. When CBR topology is used instead of conventional CHB, it has just 30 fully controlled switches and 30 fast recovery diodes, assuming all the modules are diode H-bridges. In addition, reducing the number of controlled switches reduces gate drive power consumption and system complexity. Power loss in each case P_{LossT} was calculated according to equations discussed in section 2.6.1.

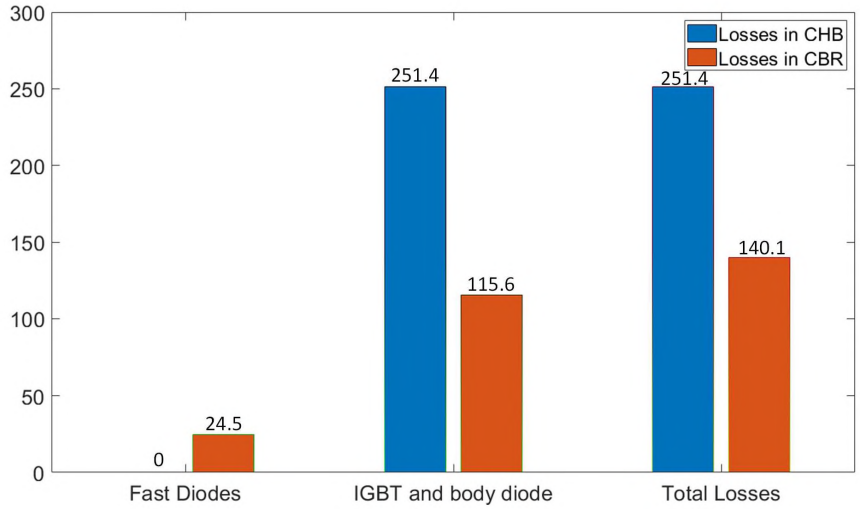


Figure 2.8. Power loss comparison of semiconductors in CHB and CBR

Efficiency for each load can be calculated by,

$$\eta(\%) = \frac{S_{TOT}}{S_{TOT} + P_{LossT}} \times 100 \tag{2.33}$$

Efficiency estimation of CHB and CBR converter under different load conditions (S_{TOT}) ranging from 1000 W to 6000 W is shown in Figure 2.9. It is evident that the CBR topology performs at the highest efficiency, reaching a peak of 97.2% at maximum load.

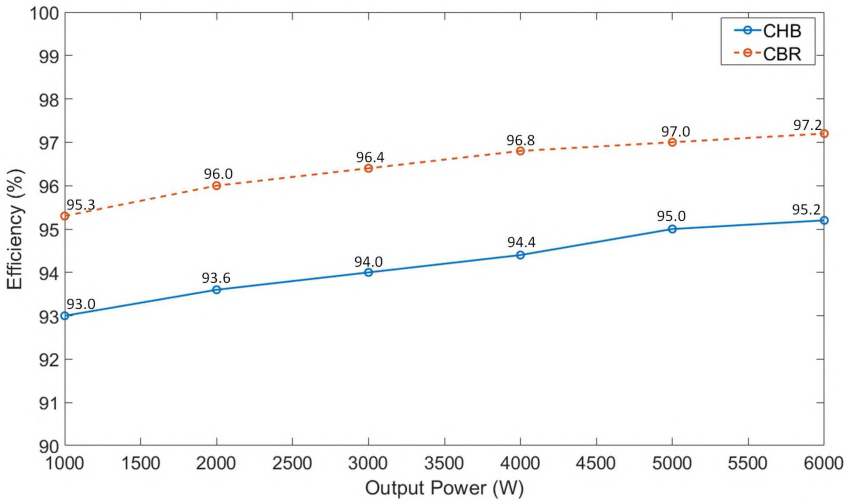


Figure 2.9. Efficiency for different load conditions

2.6.4. Cost Analysis. The cost of single phase AFE converters depends on the electrical power components used such as IGBT/ MOSFET, series inductor, diodes and dc link capacitors. The list of number of components used in a single phase N-module CHB and uncontrolled CBR topology is shown in Table 2.5.

Table 2.5. Number of components in an N-module single phase converter

Component	Cascaded H-bridge	Cascaded bridgeless rectifier
IGBT/ MOSFET	4N	2N
Fast Recovery diode	0	2N
Dc link capacitor	N	N
Inductor	1	1

The number of components seen in Table 2.5 gets tripled in the case of three phase converters and multiplies proportionally with the increase in number of stages. Hence, we can infer that the cost of a CBR is considerably lower than a CHB converter.

3. CONVERTER CONTROL UNDER BALANCED AND UNBALANCED LOAD CONDITIONS

This section describes the detailed control strategy for the proposed CBR converter. Figure 3.1 shows the control architecture used in this work. The core objectives of the proposed control system are to achieve grid synchronization, to perform dc voltage balancing for balanced and unbalanced loads and to eliminate zero crossing input current distortion.

The Second Order Generalized Integrated Phase Locked Loop system (SOGI-PLL) is used to synchronize internal control signals with the line phase ωt. Two control strategies are proposed. The first one is single phase dq based decoupled rectifier control, which regulates the average of dc link voltages. Phase angle ϕ is introduced to make grid current I_g in phase with total ac voltage across all the modules V_{ac} to prevent zero crossing distortion and to improve the power factor. The second method is an improved control where FHB modules are realised to achieve unity power factor. Dc voltage balancing under load and input voltage disturbances is also achieved.

Finally, simulation and experimental results are presented to validate the efficacy of the proposed control.

3.1. GRID SYNCHRONIZATION USING SOGI-PLL

The synchronization of control signals with the grid voltage is crucial in any rectifier/ inverter system. A typical three phase PLL system uses Clarke and Park transformations [22]. But the Clarke transformation cannot be used for single phase systems. The Orthogonal Signal Generator-based PLLs (OSG-PLL) are the most popular PLLs used for single phase systems [16]. In the OSG-PLL, a filter or other structure is used to create an artificial second phase orthogonal to the original phase. Among these OSG-PLLs, SOGI-PLL is the most popular technique because of its low computational burden, high robustness

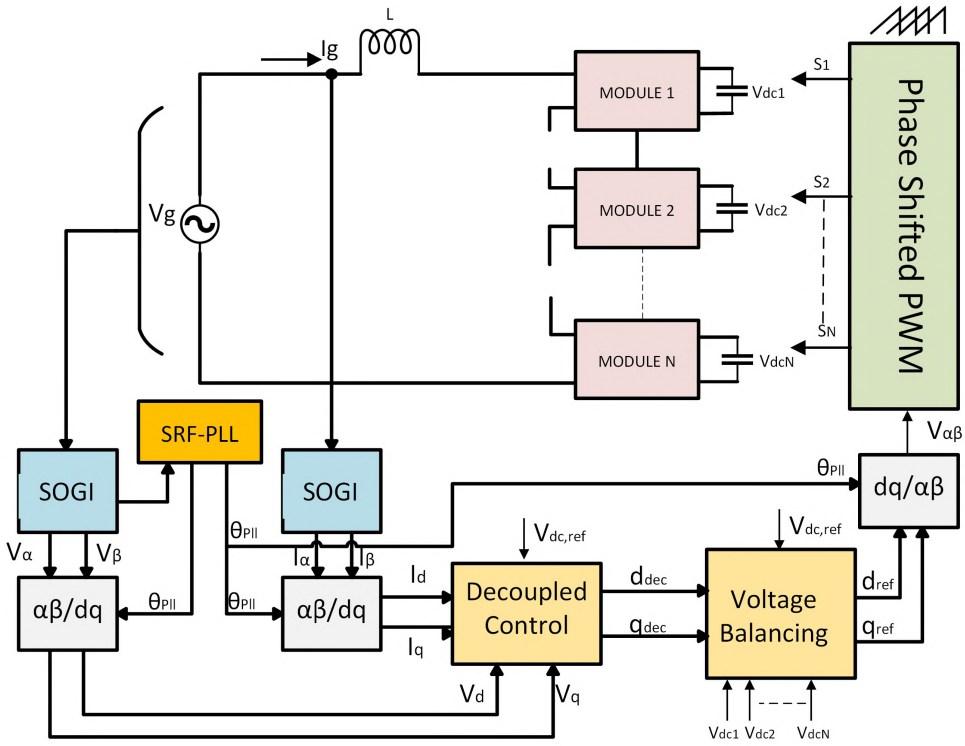


Figure 3.1. Control architecture for single phase N-module CBR

and high filtering capability. SOGI-PLL uses the second-order generalized integrator part as a substitute for Clarke transformation used in three phase systems [17]. SOGI-PLL can also be easily implemented in three phase systems to address imbalance and harmonics.

SOGI-PLL has two blocks as shown in Figure 3.2. The first one is a basic SOGI block which generates two othogonal signals V_α and V_β, which are the real and imaginary components of supplied grid voltage V_g. These orthogonal signals are sent to a Synchronous Reference Frame-based PLL (SRF-PLL) to implement the synchronization. The SRF-PLL block has a Park (stationary frame to rotating frame) transformation ($\alpha\beta/dq$). The estimated frequency ω_{PLL} is fed back to the SOGI block. SRF-PLL has a PI controller which finally generates θ_{PLL} such that the vectors $\sin(\theta_{PLL})$ and $\cos(\theta_{PLL})$ are synchronized with the grid voltage V_g.

The block diagram of SOGI-PLL is presented in Figure 3.2 where V_g is the grid voltage, ω_0 is the nominal grid frequency taken as $2\pi 60$ rad/s in this work, ω_{PLL} is the estimated frequency and θ_{PLL} is the estimated phase angle. The Park transformation is given by,

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos(\theta_{PLL}) & \sin(\theta_{PLL}) \\ -\sin(\theta_{PLL}) & \cos(\theta_{PLL}) \end{pmatrix} \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \tag{3.1}$$

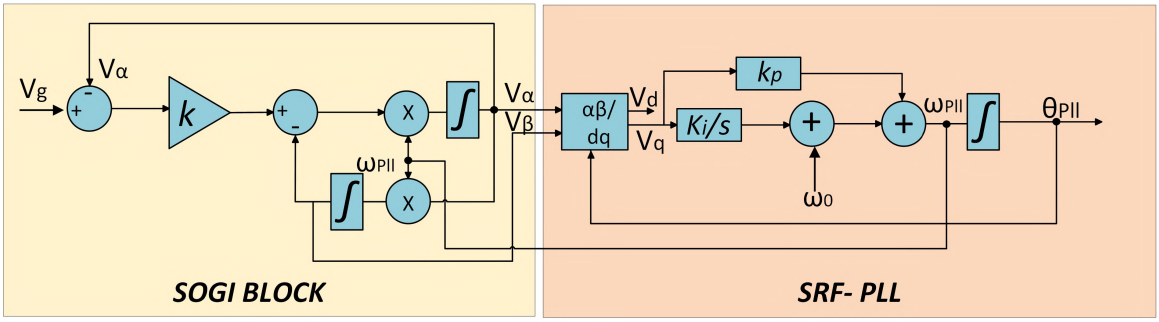


Figure 3.2. Block diagram of SOGI-PLL block

The characteristic transfer function of SOGI block in frequency domain (s-domain) is

$$\begin{cases} H_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\omega_{PLL}s}{s^2+k\omega_{PLL}+\omega^2} \\ H_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k\omega_{PLL}^2}{s^2+k\omega_{PLL}+\omega^2} \end{cases} \tag{3.2}$$

where s is the Laplace operator and k is the gain factor of SOGI block. The stability and dynamics are influenced only by SOGI gain k. Higher value of k results in wide bandwidth and fast transient response. On the other hand, it might also allow noise and voltage disturbances. Hence, k value is chosen to maintain the quality of voltage signal and speed of the response. The present work uses $k = 0.5$. The real and imaginary components of grid voltage V_α and V_β are obtained at the SOGI block.

Applying these quadrature signals to the $\alpha\beta/dq$ transformation matrix yields V_d and V_q as shown below

$$\begin{cases} V_d(t) = \cos(\theta - \theta_{PLL}) - \frac{e^{\frac{-k\omega t}{2}}}{\hat{k}}[\sin(\hat{k}\omega t)\sin\theta_{PLL} - \cos(\hat{k}\omega t - \phi)\cos\theta_{PLL}] \\ V_q(t) = \sin(\theta - \theta_{PLL}) - \frac{e^{\frac{-k\omega t}{2}}}{\hat{k}}[\sin(\hat{k}\omega t)\cos\theta_{PLL} + \cos(\hat{k}\omega t - \phi)\sin\theta_{PLL}] \end{cases} \tag{3.3}$$

where:

$$\hat{k} = \sqrt{1 - \left(\frac{k}{2}\right)^2} \tag{3.4}$$

$$\phi = \arctan\left(\frac{k}{2\sqrt{\hat{k}}}\right) \tag{3.5}$$

A small-signal model is derived in this section for SOGI-PLL based on a few assumptions and approximations. The second terms of Equation 3.3 decay to zero in steady state conditions. Hence, it is evident that V_d gives the estimated amplitude of voltage and V_q gives the phase error magnitude.

The estimated frequency and phase angle are assumed to be equal to their desired values (i.e $\omega_{PLL} \approx \omega$ and $\theta_{PLL} \approx \theta$). Hence, $\sin(\theta - \theta_{PLL}) \approx (\theta - \theta_{PLL})$ and $\cos(\theta - \theta_{PLL}) \approx 1$.

The transient terms in Equation 3.3 decay to zero with a time constant of $\frac{2}{k\omega}$. Hence, voltage component V_q can be estimated in Laplace domain as

$$V_q(s) \approx H_\tau(s)[\theta(s) - \theta_{PLL}(s)] \tag{3.6}$$

where $H_\tau(s) = \frac{1}{\tau_k s+1}$ and $\tau_k = \frac{2}{k\omega}$. Assuming $D(s)$ to be the perturbances arising from voltage harmonics, above equation can be modified as,

$$V_q(s) \approx H_\tau(s)[\theta(s) - \theta_{PLL}(s)] + D(s) \tag{3.7}$$

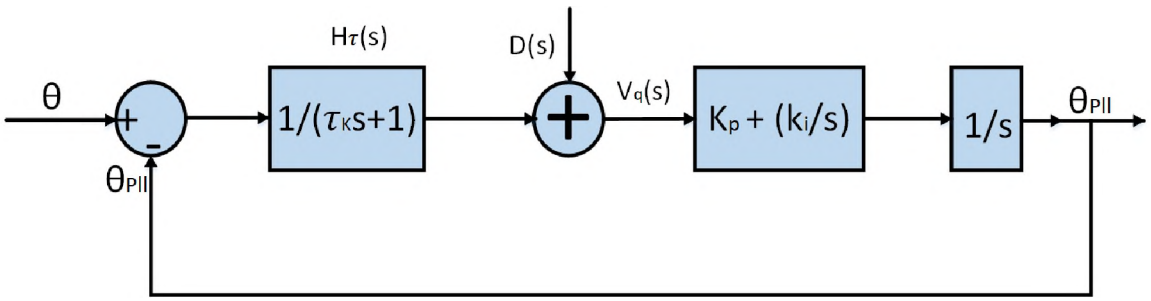


Figure 3.3. Small signal control structure of SOGI-PLL

The small-signal model is shown in Figure 3.3 based on the Equation 3.7.

3.2. SINGLE PHASE DQ DECOUPLED CONTROL SYSTEM

The proposed control system in this section has two objectives: to eliminate the zero crossing input current distortion and to balance the dc link voltage. The decoupled control uses single phase dq transformation as discussed in the subsequent sections.

3.2.1. Input Current Distortion. As discussed in Section 2.3, input current distortion causes a serious problem when the ac-dc converter is forced to operate under unity power factor. In this section, the core idea is to make the input current I_g in phase with the net ac voltage V_{ac} instead of grid voltage V_g.

The proposed control strategy introduces a new phase angle ϕ, which causes lagging power factor in the system. The net ac voltage V_{ac} is in phase with grid current I_g instead of grid voltage as shown in Figure 3.4. This phase angle ϕ adapts with the change in load as shown in Figure 3.5 where, the phase angle is changed from ϕ_1 to ϕ_2 when the load gets heavier.

From the phasor diagram in Figure 3.5, voltage across the inductor is given by,

$$V_L = \omega L I_g = V_g \sin\phi \tag{3.8}$$

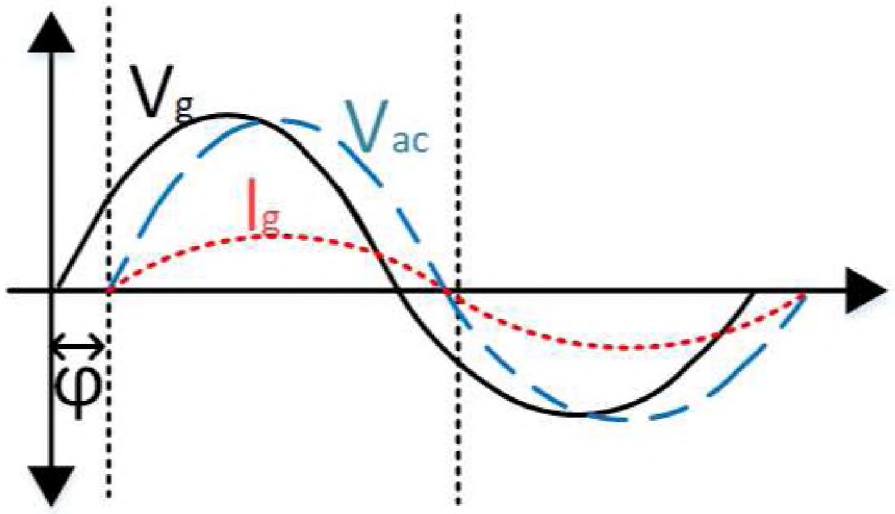


Figure 3.4. AC voltages and current under proposed control method

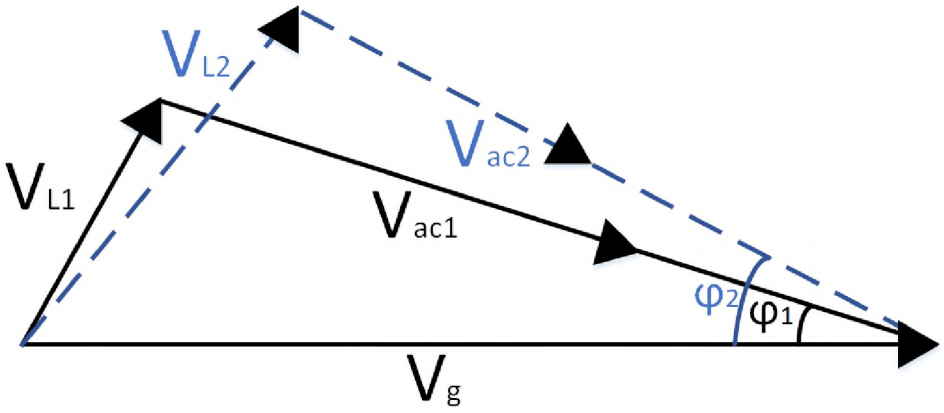


Figure 3.5. Phasor diagram when load is changed

The system input-output power balance yields

$$V_g I_g \cos\phi = \sum_{i=1}^{N} \frac{(V_{dci})^2}{R_i} \tag{3.9}$$

Assuming all the dc link voltages are well balanced in steady state and substituting equation 3.8 in 3.9 yields the following expression for the desired phase angle,

$$\phi = \frac{1}{2}\arctan\left(\frac{2\omega L V_{dc}^2}{V_g^2}\sum_{i=1}^{N}\left(\frac{1}{R_i}\right)\right) \tag{3.10}$$

3.2.2. Averaged Voltage Balancing Using DQ Decoupled Method. In this section, the average of all of the N-module dc link voltages is controlled using a single phase dq decoupled controller. The controller presented in Figure 3.6 controls the active and reactive power, and hence the power factor, to regulate the dc link voltages. The d and q component represent the active and reactive components respectively. The dq components of grid voltage and current are obtained using SOGI block as shown in Figure 3.6. During the steady state conditions, the phase locked loop aligns the voltage vector in the direction of d axis.

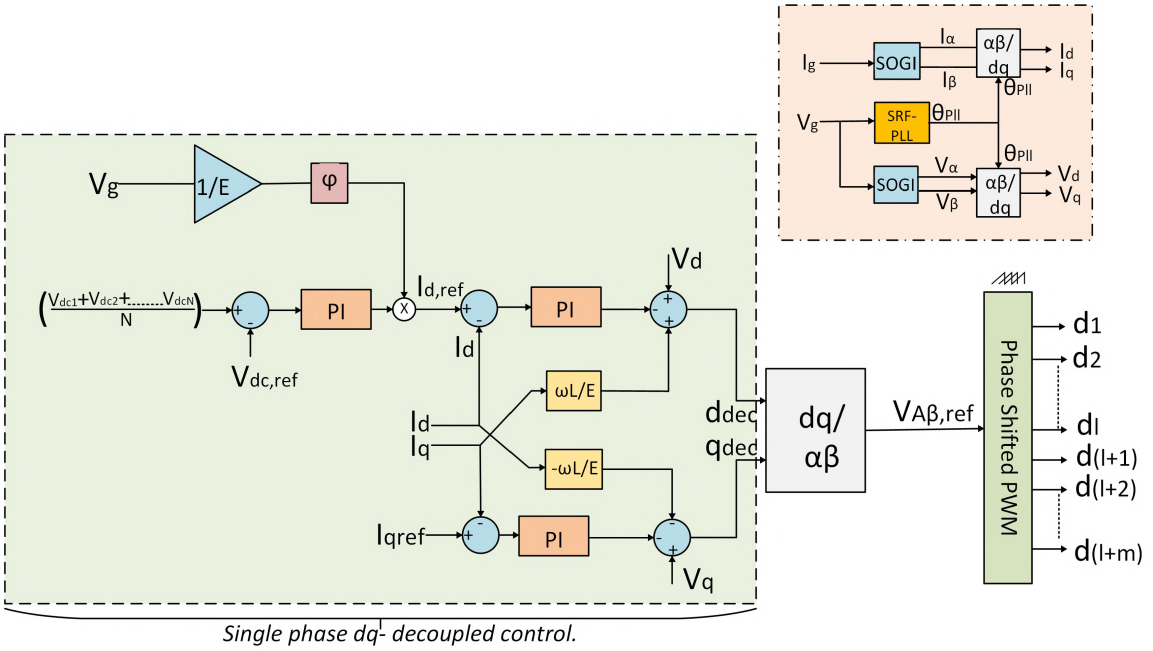


Figure 3.6. Block diagram of conventional decoupled control

The differential equations of the overall rectifier are given by the following equations,

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_L} - \frac{d_{pwm} i_g}{C} \tag{3.11}$$

$$\frac{i_g}{dt} = \frac{NV_{dc}}{L_s} d_{pwm} - \frac{V_g}{L_s} - \frac{R_s}{L_s} i_g \tag{3.12}$$

Where, N is the number of modules, i_g and v_g are the grid current and voltage respectively, L_s is the input series inductor with a series resistance R_s, V_{dc} is the dc link voltage, R_L is the equivalent output impedance and d_{pwm} is the rectifier PWM duty cycle.

The above set of equations, 3.11 and 3.12 can be applied to the voltage and current in $\alpha\beta$ reference frame. Hence, the equations can be rewritten as,

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_L} - \frac{\vec{d}_{pwm} \vec{i}_g}{2C} \tag{3.13}$$

$$\frac{\vec{i}_g}{dt} = \frac{NV_{dc}\vec{d}_{pwm}}{L_s} - \frac{\vec{V}_g}{L_s} - \frac{R_s \vec{i}_g}{L_s} \tag{3.14}$$

where:

$$\vec{i}_g = \begin{pmatrix} I_\alpha \\ I_\beta \end{pmatrix}, \ \vec{d}_{pwm} = \begin{pmatrix} d_\alpha \\ d_\beta \end{pmatrix}, \ \vec{V}_g = \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix}$$

The voltages and currents are controlled in synchronously rotating dq reference frame. The single phase dq transformation is applied to the equations 3.13 and 3.14.

$$\left(X\right)_{dq} = \left(T\right) \cdot \left(X\right)_{\alpha\beta}$$

where,

$$T = \begin{pmatrix} \cos\left(\theta_{PLL}\right) & \sin\left(\theta_{PLL}\right) \\ -\sin\left(\theta_{PLL}\right) & \cos\left(\theta_{PLL}\right) \end{pmatrix}$$

The corresponding equations of rectifier in dq reference frame are given by,

$$\frac{d}{dt}\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \frac{NV_{dc}}{L_s}\begin{pmatrix} d_d \\ d_q \end{pmatrix} - \frac{1}{L_s}\begin{pmatrix} V_d \\ v_q \end{pmatrix} - \begin{pmatrix} \frac{R_s}{L_s} & -\omega \\ \omega & \frac{R_s}{L_s} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix}$$

$$\frac{dV_{dc}}{dt} = -\frac{v_{dc}}{R_L C} - \frac{1}{2C}\begin{pmatrix} d_d \\ d_q \end{pmatrix}^T \begin{pmatrix} i_d \\ i_q \end{pmatrix}$$

As shown in Figure 3.6, the error between the mean of the N dc link voltages and the dc voltage reference $V_{dc,ref}$ is fed to a PI controller to generate d frame current reference $i_{d,ref}$. We similarly obtain $i_{q,ref}$. The actual i_d, i_q components are compared with their reference values and fed to another PI controller. We finally obtain the reference values d_{dec} and q_{dec} in synchronously rotating reference frame. The dq components are converted to $\alpha\beta$ stationary reference frame and compared with phase shifted triangular waves to generate switching pulses for all the N-modules.

Although the proposed control could eliminate the zero crossing input current distortion, unity power factor can never be achieved with this control strategy. Also, voltage balancing is inaccurate since the average of all the N cells is fed to the PI controller and individual dc link voltage balance is missing. Under unbalanced load conditions, this methodology cannot be used. Hence, we have developed an improved model in the next section involving the Fully controlled H-Bridge (FHB) modules and introduced voltage balancing technique for accurate balancing of dc link voltages under unbalanced load conditions.

3.3. IMPROVED CONTROL STRATEGY

In this section, we have modified the previous control strategy in order to achieve unity power factor and accurate dc link voltage balancing under unbalanced load conditions. The fully controlled H-bridge modules supply the necessary reactive power consumed by

the inductor, thus maintaining the unity power factor without the realisation of a lagging angle. A voltage balancing scheme is introduced where the error between the dc voltage reference $V_{dc,ref}$ and the dc link voltage V_{dci} is calculated and controlled for each cell using the PI controller. Figure 3.7 shows the overall block diagram of proposed control strategy.

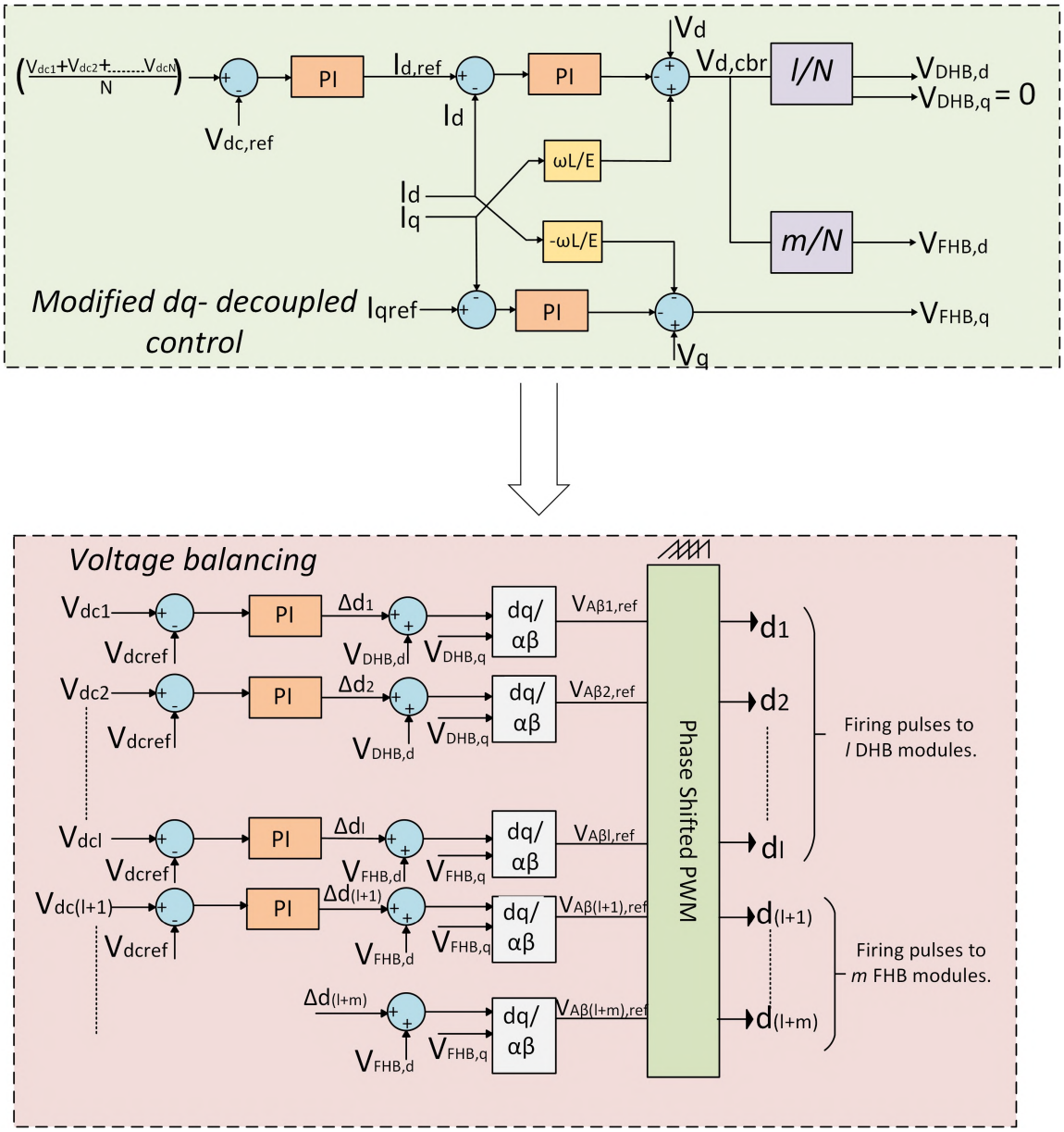


Figure 3.7. Block diagram of improved control system

To maintain unity power factor and to eliminate zero crossing current distortion, V_{DHB} should always be in phase with V_g and V_{FHB} lags V_g by an angle α as shown in the phasor diagram in Figure 3.8

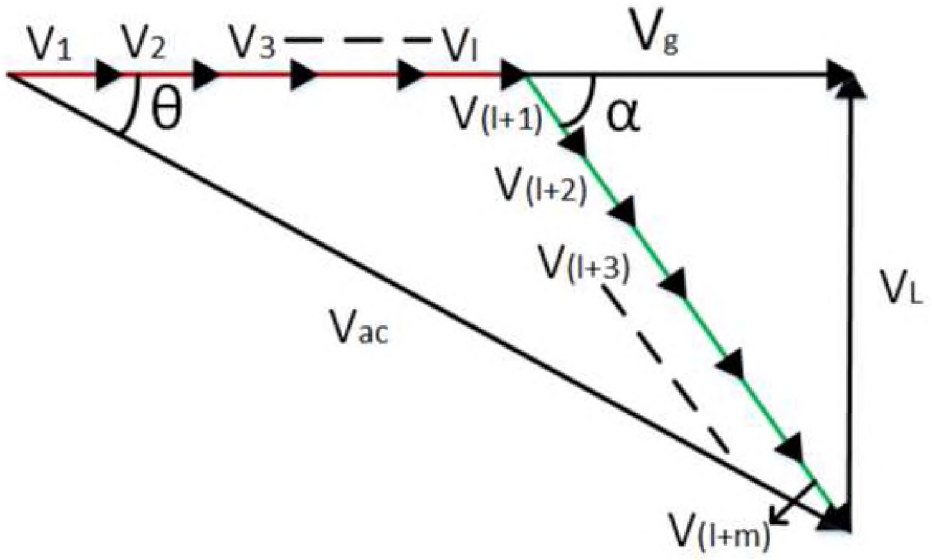


Figure 3.8. Phasor diagram of CBR under improved control

Similar to the previous control strategy, I_{dref} is calculated from the error between mean value of N-dc link voltages and the reference voltage $V_{dc,ref}$. $I_{q,ref}$ is set to be zero to maintain unity power factor. We obtain the active component $V_{d,cbr}$ and reactive component $V_{q,cbr}$ from the dq decoupling control. The active component is equally distributed among all the $(l+m) = N$ modules. Since V_{DHB} must be in phase with V_g, the reactive component of DHB modules is set to zero. Hence, the final ac voltage equations are

$$\begin{cases} V_{DHB,d} = \frac{l}{l+m} V_{d,cbr} \\ V_{FHB,d} = \frac{m}{l+m} V_{d,cbr} \end{cases} \tag{3.15}$$

$$\begin{cases} V_{DHB,q} = 0 \\ V_{FHB,d} = V_{q,cbr} \end{cases} \tag{3.16}$$

A voltage balance control method is proposed to resolve the imbalance in all the dc links of CBR converter. The voltage imbalance at each cell adjusts the modulations signals d_1, d_2, ...d_N individually to achieve different real power distributions. Error is calculated between each dc link voltage V_{dci} and the reference voltage $V_{dc,ref}$ to obtain δd_i for each cell. Then, these duty compensation signals δd_i are added to the $V_{DHB,d}$ for the first l DHB modules and with $V_{FHB,d}$ for the next m FHB modules. The real power is increased for the module with lower dc link voltage and decreased for the module with higher dc link voltage. In order to maintain the voltage regulation, duty compensation signal of the final H-bridge δd_N is calculated as,

$$\delta d_N = -\delta d - 1 - \delta d_2 - ..... - \delta d_{N-1} \tag{3.17}$$

Similarly, $V_{DHB,q} = 0$, $V_{FHB,q}$ form the reactive component q reference voltages for DHB and FHB modules respectively. Finally, we obtain the reference values of V_{DHB} and V_{FHB} in dq reference frame.The dq to $\alpha\beta$ reference frame transformation is employed and the $V_{\alpha\beta}$ signals are compared with phase shifted triangular waves to generate switching pulses for the N cells of CBR converter.

3.4. SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulation and experimental results for both control methodologies under different load and input voltage conditions are presented. The overall system is simulated in PLECS as shown in Figure 3.9 to verify the validity of proposed control strategy.

The present work uses a 5-module cascaded bridgeless rectifier for simulation and experimental studies. Low switching frequency of 2000 Hz is sufficient tor drive the IGBT switches in this model. Other system parameters are designed according to the steady state

Table 3.1. Parameters for simulation model

Parameters	Magnitude
Input grid voltage (V_g)	30 V
Grid current (I_g)	8 A
Switching frequency (f_{sw})	2000 Hz
Inductance (L)	5.0 mH
DC capacitance (C_{dci})	2.2 mF
Load Resistance (R_{dci})	100 Ω
Reference dc voltage ($V_{dc,ref}$)	20 V

modeling discussed in Section 2.2. The system parameters for the simulation model are listed in Table 3.1. The same parameters are considered for the experimental studies to make an easy comparison.

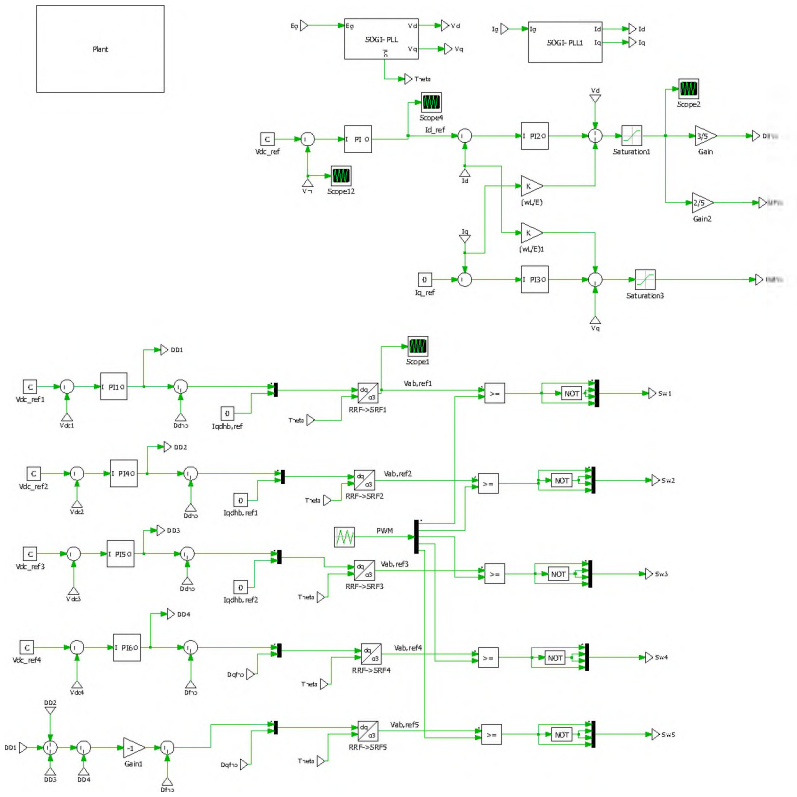
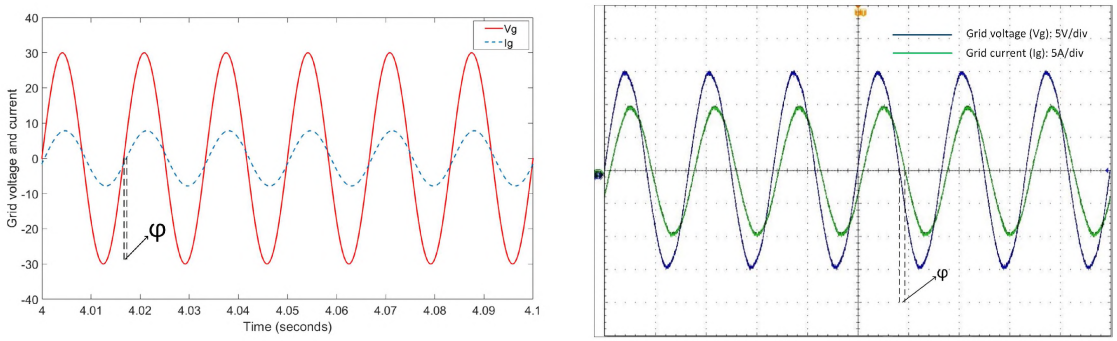


Figure 3.9. Schematic of simulation in PLECS

3.4.1. Results of Decoupled Control. In the case of decoupled control, all the modules are Diode H-Bridge (DHB) modules and the required power factor correction is provided by phase angle ϕ as discussed in Section 3.2. Reasonably high power factor can be achieved without any zero crossing input current distortion as shown in Figure 3.10.

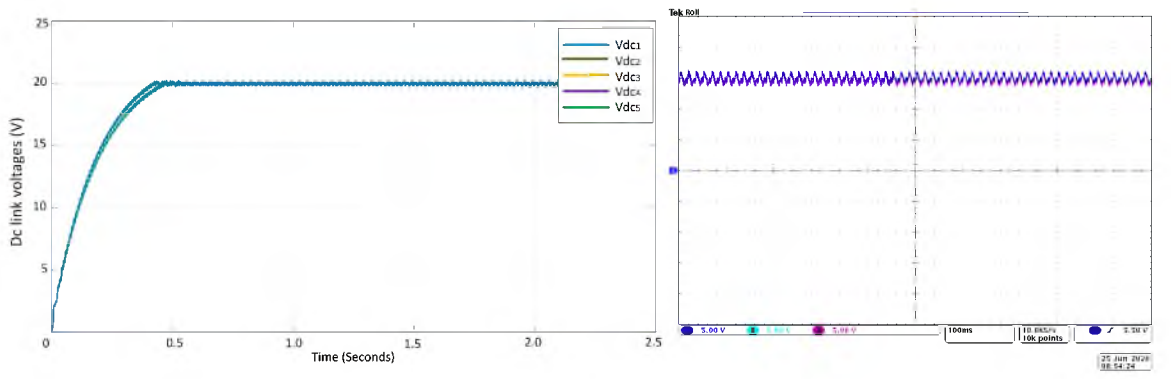


(a) Simulation (b) Experimental

Figure 3.10. Grid current and grid voltage under normal decoupled control

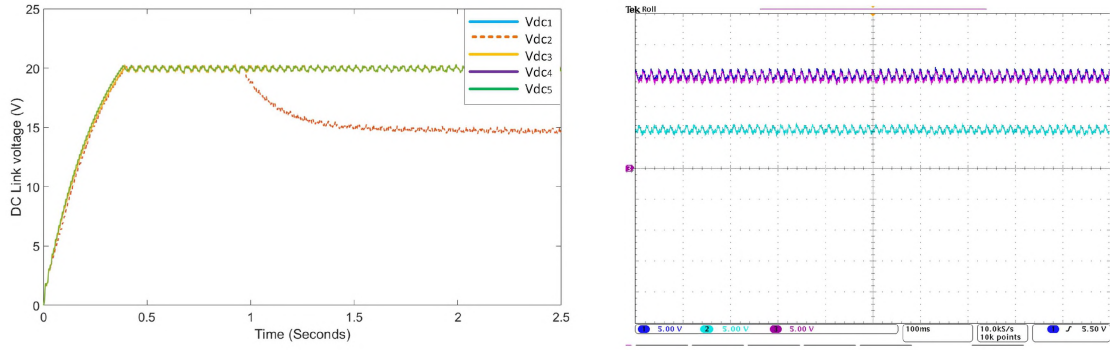
The dc voltages across all five modules are well balanced under balanced load conditions as shown in Figure 3.11. As mentioned in the section 3.2, the conventional decoupled control cannot be used for unbalanced load conditions. For instance, the load resistance of module-2 (R_2) is changed from 100 Ω to 50 Ω at t = 5 s while the other loads are left unchanged. The resultant output dc link voltages are shown in Figure 3.12.

3.4.2. Results of Improved Control. The fully controlled H-bridge modules are responsible to supply the reactive power needed by the inductor L, hence maintaining the unity power factor. The minimum value for m, i.e the number of FHB modules is calculated to be 1. Hence, we take two out of five to be FHB modules and the rest three to be DHB modules. The grid voltage is exactly in phase with the grid current thus achieving unity power factor as shown in Figure 3.13.



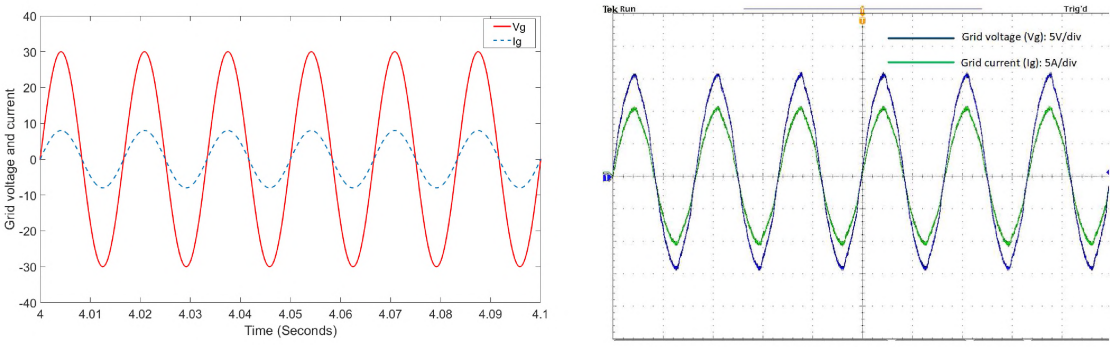
(a) Simulation (b) Experimental

Figure 3.11. Dc link voltages under balanced load conditions



(a) Simulation (b) Experimental

Figure 3.12. Dc link voltages when R_{L2} is changed from 100 Ω to 50 Ω at t = 5 s



(a) Simulation (b) Experimental

Figure 3.13. Grid voltage and current under improved control

The dc link voltages under balanced load conditions are shown in Figure 3.14. Similar to the decoupled control, module-2 load resistance is changed from 100 Ω to 50 Ω at $t = 5$ s and the resultant dc link voltages are well balanced as shown in Figure 3.17. The duty compensation signal for module-2, δd_2 adjusts itself to a new value in order to maintain the power balance in the second cell as shown in Figure 3.16.

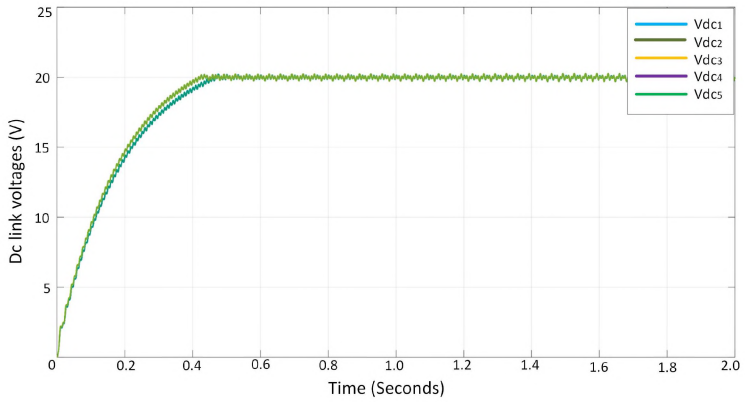
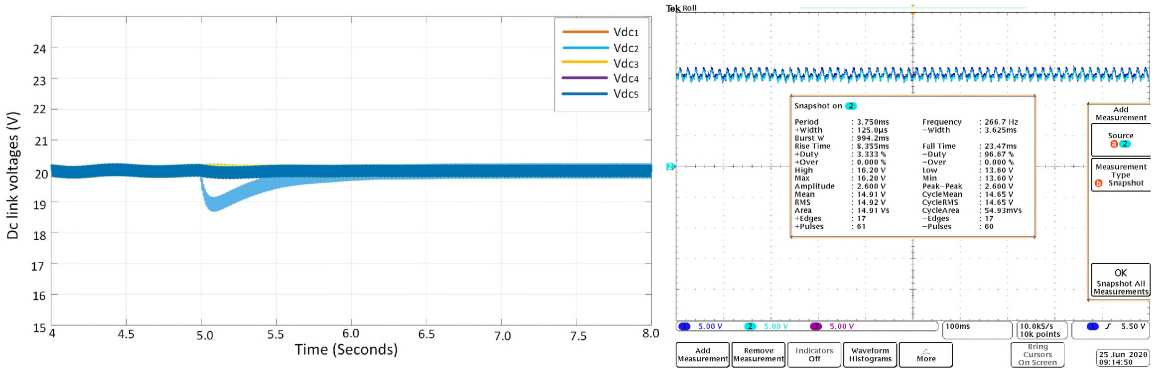


Figure 3.14. Dc link voltages under balanced load conditions for improved control



(a) Simulation (b) Experimental

Figure 3.15. Dc link voltages when R_{L2} is changed from 100 Ω to 50 Ω at $t = 5$ s under improved control

The input grid voltage is changed from 30 V to 45 V at $t = 5$ s as shown in Figure 3.17. The corresponding change of voltage in stationary reference frame $V_{\alpha\beta}$ is shown along with the all the five dc cell voltages in Figure 3.17.

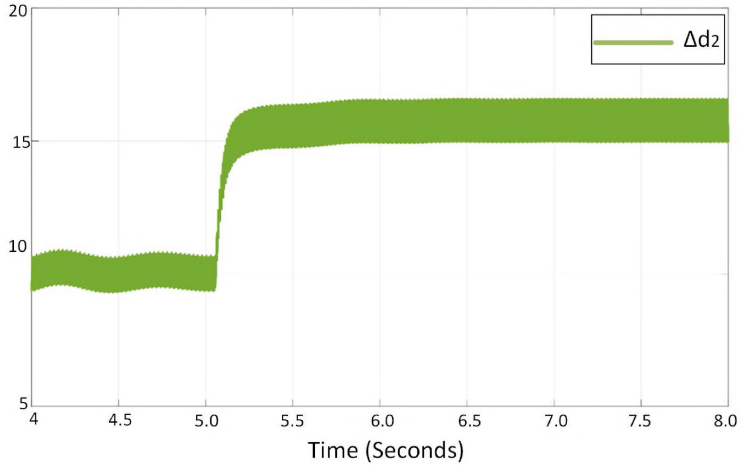
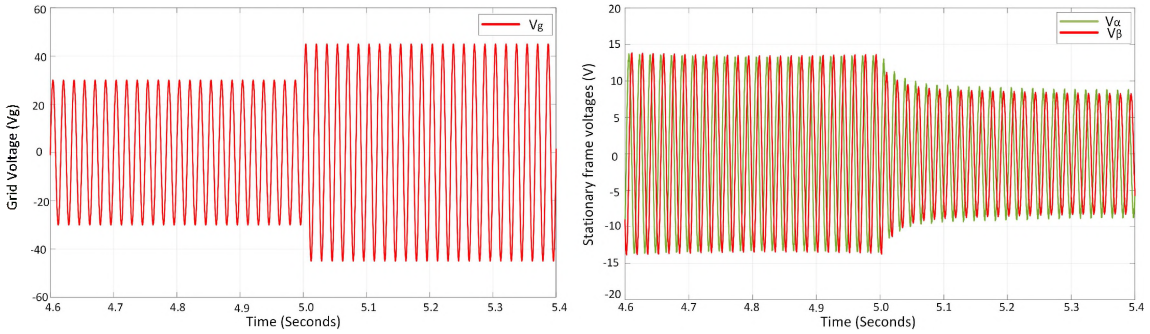
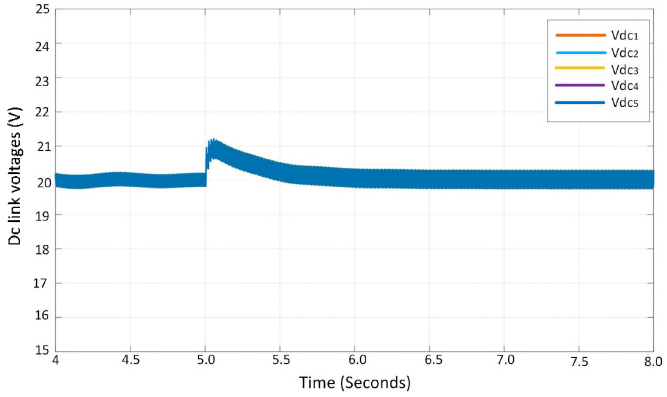


Figure 3.16. Change in δd_2 under unbalanced load conditions



(a) Grid Voltage

(b) $V_{\alpha\beta}$



(c) Dc link voltages

Figure 3.17. Voltages when V_g is changed from 30 V to 45 V at $t = 5$ s under improved control

Now, at t= 5 s, both input voltage and the load resistance of module-2 are changed from their default values. DC voltages are well balanced as shown in Figure 3.18.

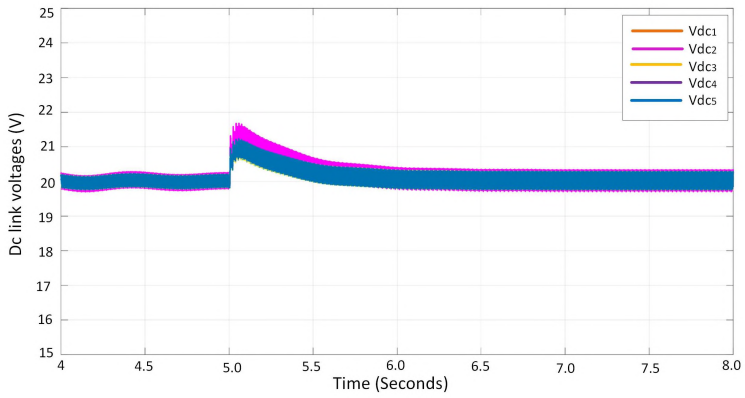


Figure 3.18. DC link voltages under unbalanced load and input voltage under improved control

Figure 3.19 shows the power factor comparison between the decoupled control and the improved control. Unity power factor is maintained in improved control with the change in load.

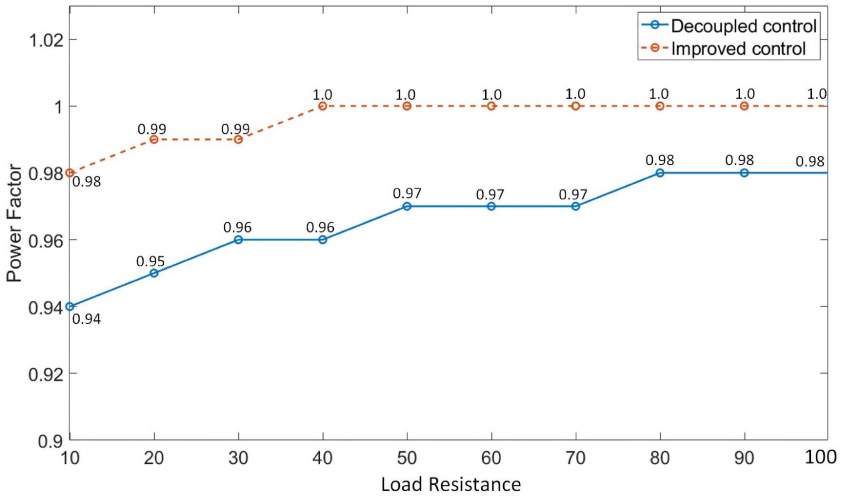


Figure 3.19. Power factor comparison between decoupled and improved control

4. HARDWARE IMPLEMENTATION

The experimental prototype of a 5-module cascaded ac-dc converter is shown in Figure 4.1. All five modules are stacked on one other. A 110 V, 12 A single phase auto transformer supplies ac voltage to the power converter. A 100 Ω resistor is connected across the switch to limit the input current overshoot. The overall system parameters used for the experimental studies are same as simulation parameters as shown in Table 3.1.

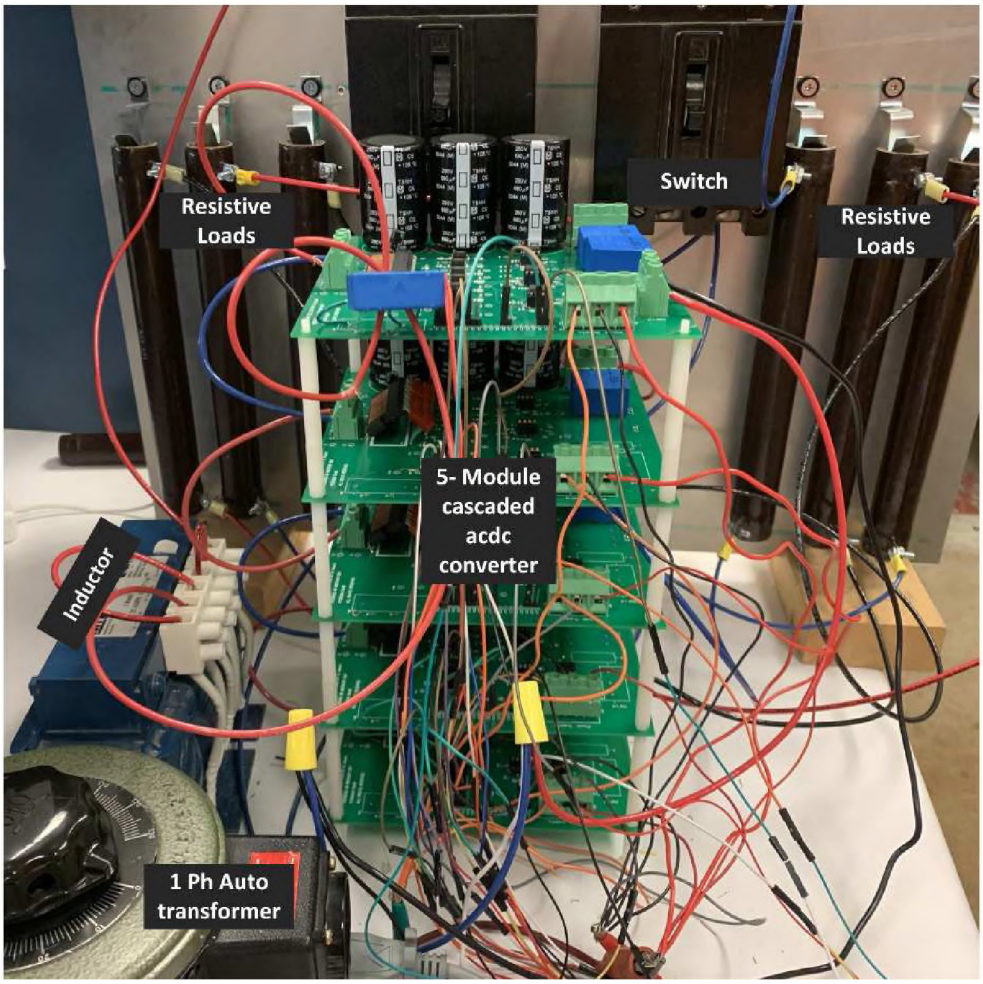


Figure 4.1. Experimental setup of 5-module CBR converter

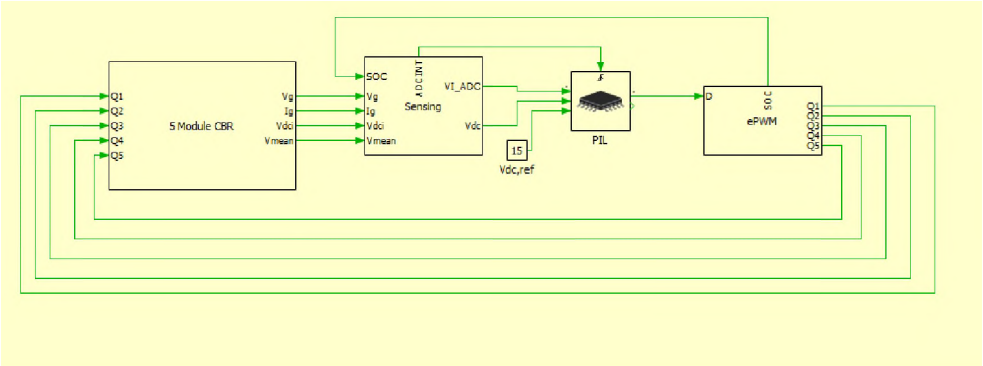


Figure 4.2. Processor in loop

4.1. PROCESSOR IN THE LOOP

The embedded firmware is written to F28377S TI Launchpad using Code Composer Studio (CCS) tool. The Processor In the Loop (PIL) technique is used to test the control algorithm on the real time embedded hardware. The major advantage of using this technique is the actual compiled code is executed on a real microcontroller while the power converter is simulated for safety. Figure 4.2 shows the implementation of PIL control for the proposed CBR converter in PLECS. First, the sensing block performs analog-to-digital conversion (ADC) of voltage and current signals generated by the simulation. PIL block runs the compiled code to generate a reference value for duty ratio. The ePWM block compares the reference value with the triangular wave signals to generate the switching pulses for all the five modules.

4.2. PWM SCHEME IMPLEMENTATION

As mentioned before, duty ratio is modified according to the reference voltage value in $\alpha\beta$ reference frame. Figure 4.3 shows the overall PWM scheme implementation for the 5-module cascaded converter. The compare values of each module, CMP1, CMP2,..., CMP5 corresponds to the reference duty ratio signal for each module. The low frequency

triangular waves are set to be in up-down count mode starting from zero to reach Max-count value and jumps back to zero. The triangular wave signals given to each module are phase shifted by certain angle Φ with respect to the previous module calculated as,

$$\phi = \frac{360}{N} \tag{4.1}$$

where, N is the number of modules.

Each FHB module has two pairs of complementary switches. The square wave pulses from EPWMA and EPWMB are given to the upper switch and lower switch respectively. Certain amount of delay is introduced during the rising and falling edge represented by Rising Edge Delay (RED) and Falling Edge Delay (FED) as shown in Figure 4.3 .

The upper switches of the intelligent power module (IPM) for the DHB modules are not given any PWM signals so that the anti-parallel diode co-packaged with each IGBT acts as a unidirectional switch.

4.3. VOLTAGE AND CURRENT SENSING

The controller needs grid voltage, dc link voltages and current measurement to employ the proposed control, obtained by feeding the values to the ADC pins of controller. The experimental system used LV25-P voltage sensors for the grid and dc link voltage measurement and LV55-P current sensor for the grid current measurement as shown in Figure 4.4. The characteristics of each sensor are calibrated individually to calculate the ratio between the actual voltage/ current and the voltage/ current at the sensor pins as shown in Table 4.1. The measured values at the out pins of each sensor are fed to the TL082-IP JFET Op-Amp such that the signals are amplified to 0 to 3.3 V range before feeding them to the ADC pins of the MCU.

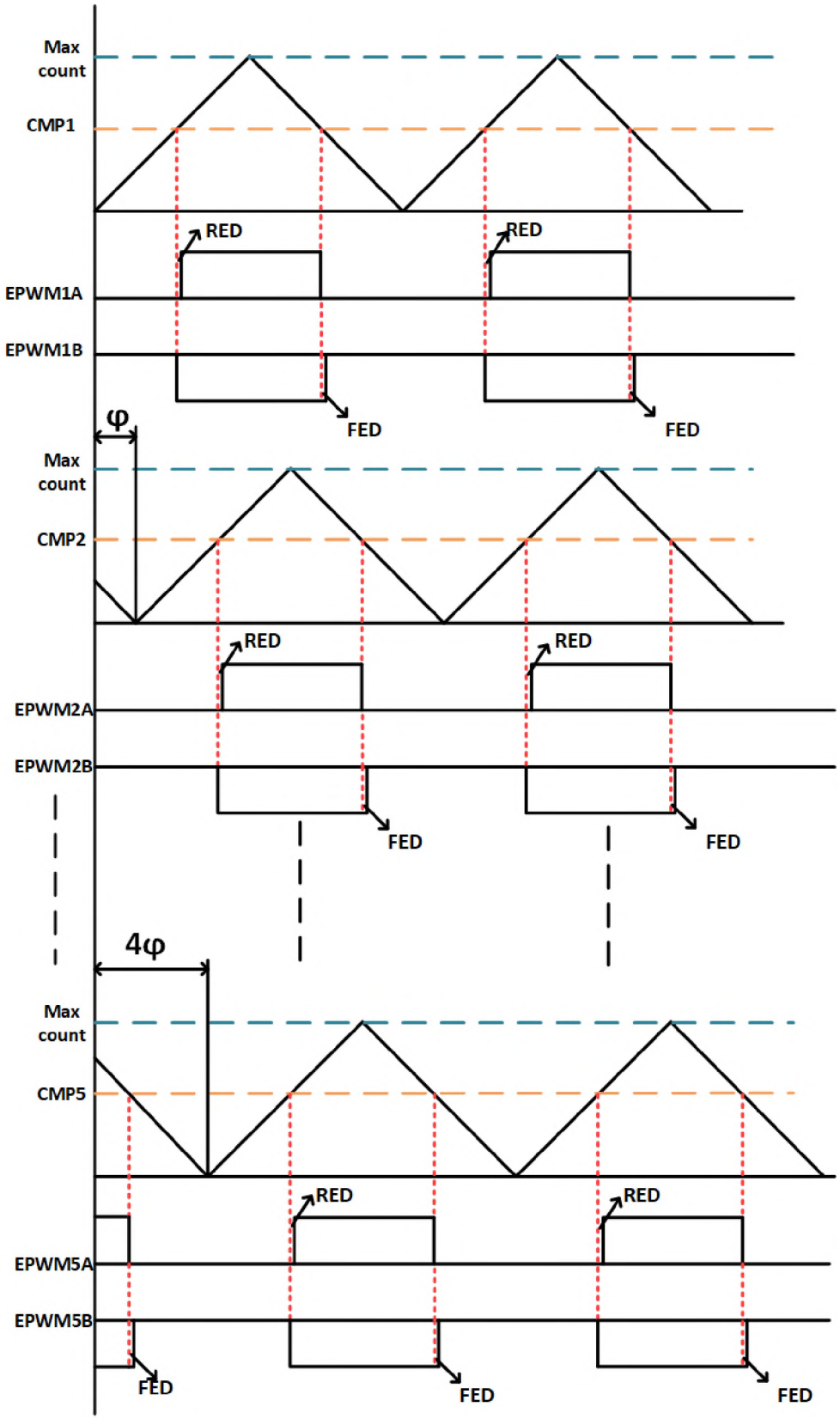


Figure 4.3. PWM implementation

Table 4.1. Calibration of sensors

Sensor	Actual to measured value ratio
grid voltage sensor	1:850
Grid current sensor	1:920
DC voltage sensor 1	1:835
DC voltage sensor 2	1:840
DC voltage sensor 3	1:835
DC voltage sensor 4	1:850
DC voltage sensor 5	1:850

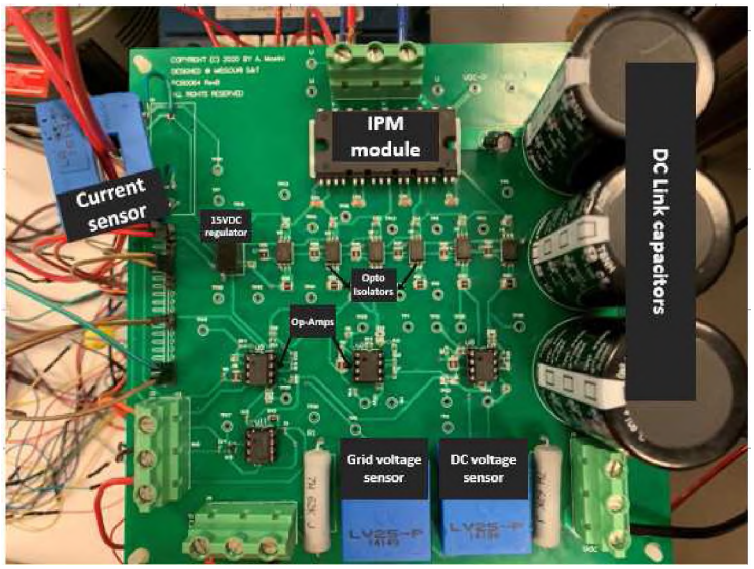


Figure 4.4. Each module in CBR converter

4.4. IPM MODULE

A 600 V, 30 A STGIPS30C60 IPM module has been used in each module shown in Figure 4.4. Each IPM has three pairs of complementary switches among which any two can be used for each module. To realise DHB modules, no switching pulses are given to the two upper IGBTs so that their co-packaged antiparallel diodes act as the uncontrolled unidirectional switches. The operation of IGBT switches in FHB modules is similar to that of conventional CHB converter. EPWM block generates the switching pulses to each

module based on the reference duty ratio signal from the MCU. Bootstrap capacitance of minimum 0.5 μF is necessary to maintain threshold bootstrap voltage of 15 V across each leg.

4.5. LOADS

The dc link for each module consists of a 100 Ω resistor and three 680 μF capacitors connected in parallel. Another 100 Ω resistor is connected to the load of module-2 through a switch. The switch is turned ON at a desired instant making the equivalent resistance 50 Ω. A Tektronix MSO4034B mixed signal oscilloscope is used to analyze the voltage and current signals of the converter.

5. CONCLUSIONS AND FUTURE WORK

5.1. SUMMARY

In this work, the modeling and control of a novel unidirectional Cascaded Bridgeless rectifier was investigated in detail. Much emphasis was given to the topological analysis, power factor correction, dc voltage balancing and hardware implementation. A five-module converter was used to validate the conclusions in simulations and experiments.

The main objective of this work was to implement a low cost cascaded H-bridge converter topology with accurate dc voltage balancing under unbalanced load conditions. Cascaded H-bridge technology is one of the most popular technologies used in medium and high voltage active frond end applications. The conventional CHB topology uses a significant number of fully controlled IGBT/ MOSFET switches, which increases the cost, hardware and control complexity. Also, switching losses constitute considerable amount of losses in cascaded converters. The idea of using fewer fully controlled IGBT/ MOSFET switches is considered in this work. The proposed cascaded bridgeless rectifier topology has up to half of its fully controlled switches replaced by unidirectional fast recovery diodes. The cost, power loss and efficiency were estimated and compared between the conventional CHB topology and the proposed CBR topology. The comparison studies justify the advantages of CBR topology over CHB topology in high power applications.

Frequency deviations can cause serious imbalances in a power system, so an effective grid voltage synchronization scheme is essential. SOGI-PLL is one of the most popular Phase Locked Loop (PLL) techniques for single phase applications. This work incorporates a SOGI-PLL for the grid voltage synchronization because of its low computational burden,

high robustness and filtering capability. SOGI block was used to obtain the values of grid current and voltage in synchronously rotating reference frame (dq). Small signal control structure was obtained based on few assumptions and approximations.

Dc voltage balancing is a common and significant challenge in any cascaded H-bridge topology since a single current is responsible for the voltage balancing in all the modules with different load conditions. Achieving unity or close to unity power factor is also a common objective in most of the power converters. However, serious input current distortion may occur when an unidirectional converter is forced to operate under unity power factor condition. Two control strategies were proposed in this work to achieve the dc voltage balancing and to eliminate the zero crossing distortion of input current.

The first one is based on single phase dq decoupled control method. All the modules are Diode H-Bridge modules in this scheme. The error between the reference voltage and the mean of all the dc link voltages generates the d frame current reference. The reference value in q frame is taken to be zero to achieve unity power factor. The error between these reference values and the actual current values in dq reference frame are fed to PI controller. Finally, decoupled terms are added to obtain reference values of voltage in dq reference frame. It was found that this scheme cannot be used for the voltage balancing under unbalanced load conditions. In this control, a lagging angle ϕ is introduced to make the net ac voltage across all the modules in phase with the grid current. The current distortion was found to be very small but it was inferred that unity power factor can never be achieved when all the modules are uncontrolled DHB modules. This led to modify the existing control to achieve better voltage balancing and unity power factor.

The second strategy assumes a small number of the modules to be Fully controlled H-Bridge modules (FHB) which are responsible to supply necessary reactive power to the inductor, thus achieving unity power factor. Single phase dq decoupled control is employed

similar to the previous case. However, this scheme includes individual voltage balancing for each cell. Active power is equally distributed among all the FHB and DHB modules. Reactive power is supplied only by the FHB modules.

The hardware of 15 V, 10 A 5-module cascaded bridgeless rectifier was implemented. A F28377S TI launchpad was used to run the embedded code and generate the duty signals for all switches in 5 modules. All the parameters are carefully designed to ensure a safe operation under laboratory conditions. Entire simulations were done in PLECS environment. Processor In Loop (PIL) technique was used to test the compiled code on a embedded microcontroller with a simulated power converter prior to full experimental validation. Experimental and simulation studies validate the efficacy of proposed control.

5.2. FUTURE WORK

Single phase partially controlled cascaded converter had been implemented in this work. Similar modeling and control can be extended to implement three phase cascaded bridgeless rectifier to better study the current distortion attenuation and dc voltage balancing in all the three phases. Three phase systems would also require accurate modeling of an LCL filter to mitigate input current harmonics, which is not discussed in this work. In this work, much emphasis was given to the unity power factor rectification alone. Hence, enhanced reactive power compensation by the cascaded converters could lead to further research in this field. Although the converter model is suitable for high power applications, the laboratory prototype was tested under low voltage and current conditions. High power scale model can be developed in the future to analyse the efficiency, stability and power quality of the converter.

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VITA

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