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DESIGN AND DEVELOPMENT OF POWER PROCESSING UNITS FOR  
APPLICATIONS IN ELECTRICALLY-PROPELLED SATELLITE SYSTEMS

by

KARTIKEYA JAYADURGA PRASAD VEERAMRAJU

A THESIS

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

2020

Approved by

Dr. Jonathan W. Kimball, Advisor

Dr. Mehdi Ferdowsi

Dr. Henry Pernicka

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## **PUBLICATION THESIS OPTION**

This thesis consists of the following one article which will be submitted for publication as follows:

Paper I: Pages 21 - 47, Dynamic Characterization and Closed-Loop Voltage Mode Control of Power Processing Units for Electrically Propelled Satellites. Under preparation for Transactions in Power Electronics Journal.



## ABSTRACT

Electrospray technology provides a way to ionize specialized liquids by applying high voltages across a sharp porous tip and a metallic mesh. This technology is widely used in the field of mass spectroscopy for generating ions for testing purposes. The dawn of nano-satellites posed new challenges in the miniaturization of many conventional satellite sub-systems. One significant challenge faced in such a process was the miniaturization of the propulsion system. Electrosprays have started to find their application in the field of Aerospace Engineering and now are formally known as Electrospray Thrusters. These thrusters provide high specific impulse and are attractive substitutes to conventional gas propelled thrusters as they can be scaled down in size and can also provide extended mission times. Some of the new challenges faced in such applications are the generation of high voltages from a low voltage onboard battery, grounding, spacecraft charging, clearance, and reliability issues for long term usage.

In this work, a complete design process is developed for the realization of such high voltages suitable for interfacing with an electrospray thruster. Simulation models for a new type of converter are assessed, and its feasibility is discussed. A hardware prototype is implemented, and the practical results are assessed.

An analysis of the converter is presented, and the semiconductor and passive components are selected. Magnetic components are designed based on the analysis. Parallels are drawn between the theoretical and prototype model of the concept converter.

Finally, the firmware of the converter is explained, and the communication protocol of the PPU is delineated. As the boards designed for the converter have to sustain high voltages and reliably operate in unfavorable environments, special PCB layout considerations must be used, which also forces a designer to look for various other materials for the PCB fabrication.

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## **SECTION**

### **1. INTRODUCTION**

Nanosatellites are gaining importance as the world started moving towards miniaturization. Many nanosatellites have already been developed and put in space by the leading aerospace organizations. It has also provided an economical way for student research organizations all over the world to learn new skills in the field of avionics, orbital mechanics, and structural design, which would otherwise be only available in the industry. They are especially useful due to their low mass and cheaper launch costs. Also, they are launched in clusters, making space flight way cheaper. They aid research by enabling the testing of new technologies on a smaller and cheaper scale before committing onto larger satellite systems.

#### **1.1. THE ELECTRICAL SUBSYSTEM**

Among all the subsystems implemented on a satellite, the power system is the most fundamental one, as all the other subsystems directly or indirectly depend on it. The major components of this subsystem include the onboard battery, Battery management System (BMS), Solar Panels, Maximum Power Point Trackers (MPPT), Electromechanical Drives, and Ionic Drives. All these systems must work correctly to achieve full mission capabilities. These systems are implemented using the concepts developed in the field of Power Electronics, which deals with the switching of semiconductor devices in a controlled fashion to obtain the necessary power processing effect. For achieving this, conventional electrical components such as transformers, inductors, capacitors, diodes, MOSFETS are used in par-

ticular topologies and are controlled by devices like microcontrollers or microprocessors. For this purpose, the power systems are implemented in closed-loop, and the controllers are optimized by trial and error methods or stability methods to meet the desired response time.

## 1.2. THE PROPULSION SUBSYSTEM

The other major subsystem that concerns the scope of this thesis is the propulsion subsystem. The propulsion system includes all the components that are responsible for affecting the orbital alignment and position of the satellite. The most important component among all these is the thruster. There are various kinds of thrusters available in rocketry, such as liquid fuel, gas-fuelled, and special thrusters. Special thrusters exploit unconventional scientific principles to achieve the thrust. These kinds of technologies have started to become relevant after the necessity for prolonged space flight and smaller form factors. Prolonged space flight can be associated to the specific impulse of the thruster, which relates the fuel consumed to the momentum gained. Hence, an ideal thruster is one that is has a high specific impulse, a smaller form factor, enables miniaturization, extended times of operation. Some of the types of thrusters are shown in Figures 1.1, 1.2, 1.3, and 1.4.



Figure 1.1. Hall Effect Thruster [1]

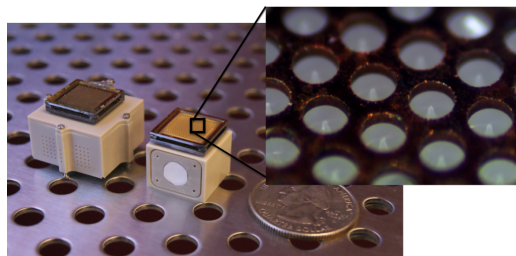


Figure 1.2. Electro Spray Thruster [2]



Figure 1.3. Coldgas Thruster Portrayed in the Movie: Gravity

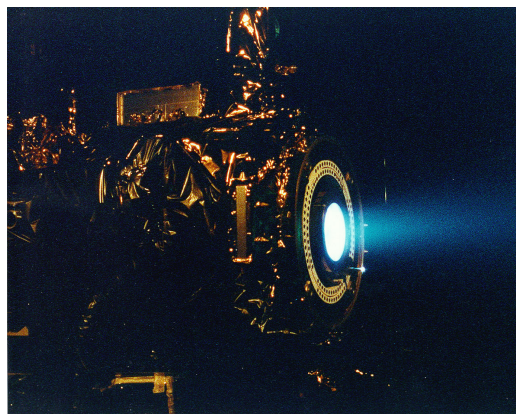


Figure 1.4. NASA's NSTAR Gridded Electrostatic Ion Thruster [3]

The ionic thrusters create thrust by emitting ions. Because of a frictionless environment in space, these micro thrusts can be generally enough to control the orientation of the satellite. Hence these types of thrusters can be used in very fine attitude adjustments. Also, if these thrusters are fired for a very long time, they can propel the payloads at high velocities.

The charge neutrality of spacecraft surfaces is maintained by the use of an additional neutralizing cathode. But these cathodes have heating elements, which can make the process of energy conversion inefficient.

Electrospray thrusters are capable of emitting both positive and negative ions, which removes the necessity of hot cathodes when used in clusters with alternating emission modes [5, 6].

Thrusters typically have four essential components, namely, the thruster, the propellant feed system, control valves, and the propellant storage tank. When additional capabilities are desired, thruster topologies can be mixed to get hybrid thrusters. One such implementation within the scope of this thesis is a multimode thruster [4], where a cold-gas and an electrospray thruster are mixed to get the desired thrust capabilities. A model of

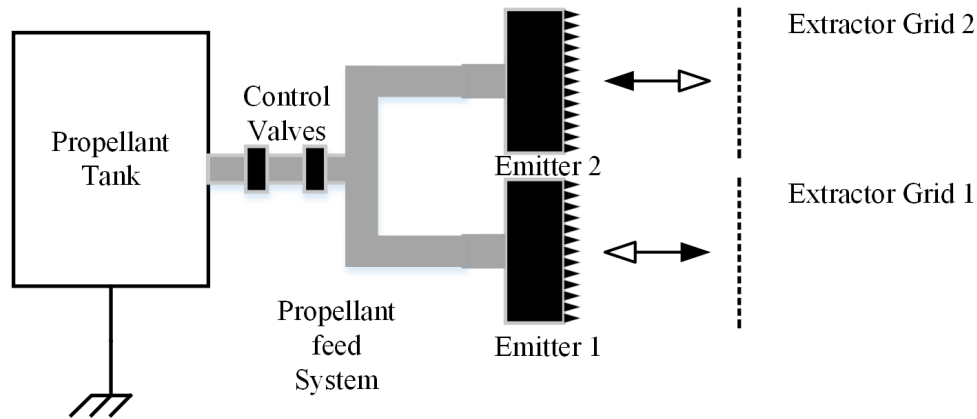


Figure 1.5. Proposed Multimode Monopropellant Thruster

the proposed thruster is shown in Figure 1.5. For the functioning of this thruster, the control valves are actuated, and the thrust is achieved by using chemical/cold gas mode. The chemical mode results in high thrust and hence is referred to as high-thrust mode.

By exciting the emitter and extractor grids with high voltages, thrust due to electrospray emission mode is achieved, which causes high specific impulse [4] and is suitable for long burns and fine attitude adjustments. But for using the thruster in electrospray emission mode, high voltages are to be generated from a low voltage battery. This thesis deals with the development of power electronic converters responsible for the generation of high voltages from a low voltage battery. Also, the converter developed thereby should adhere to the particular requirements of the electrospray thruster system, which will be explained throughout the length of this thesis.

### 1.3. TECHNICAL CHALLENGES

Some of the major problems faced in such miniaturization for nano-satellites are the necessity to scale down the conventional satellite systems such as structures, communication systems, science equipment, power, and propulsion systems. This thesis mainly deals with



the design and development of miniature propulsion systems and the Power Processor Units (PPU) used to drive them. The work also investigates on only two types of thrusters, namely the cold gas thruster and the electrospray thruster.

**1.3.1. Challenges Faced Due to the Propulsion System.** In this section, various issues about the propulsion system are discussed, with particular emphasis on electrospray, and cold gas thrusters. The specifications of the system are presented, and their practicality is discussed.

**1.3.1.1. Cold gas thrusters.** Cold gas thrusters are one of the most basic thrusters, simple in the principle of operation, and belong to a very mature technology. They produce thrust by ejecting gas by depressurizing a pressurized gas cylinder using control valves. The main issue with this form of a thruster in nano-satellite systems is the scaling and space constraints. Also, if the control valves fail, the mission will come to a grinding halt. The propellant tank occupies much of the space, and the volume should be taken into consideration right from the beginning of the structural design process.

**1.3.1.2. Electrospray thrusters.** Electrospray thrusters are useful as they scale up/down very well [5]. But they need high voltages to operate and become a challenge as the voltage of the onboard battery on the satellite is only used to power the flight computer, communication systems, and other equipment, which predominantly work on low voltages. Hence, a separate power processor unit (PPU) has to be constructed to boost the voltages to the required high voltage.

**1.3.2. Challenges Faced Due to Power Processor Units.** The power processor unit is a power electronic converter with a high gain. To make the converter lightweight, the magnetic components and switching networks should be as small and lightweight as possible. Also, as the PU generates high voltages across low clearances, the issues of arcing, tracking, and overall failure at high voltages become significant. Hence, methods should be developed to prevent the breakdown mechanisms from affecting the PPU.

## 2. LITERATURE REVIEW

This chapter describes the existing technological trends in the field of electrospray thrusters and power electronics. Excerpts and conclusions from some of the prominent works relevant to this thesis are explained. The review starts with the explanation of the multi-mode thruster and continues with the explanation and working principles of the electrospray thruster system and justifies the rationale behind the implementation of dual thrusters. An investigation into power electronic converters used previously to generate high voltages for electrosprays will be discussed next, and then the paper dealing with the generalized approach to designing high gain DC-DC converters will be presented.

### 2.1. RECENT TRENDS IN NANOSATELLITE PROPULSION TECHNOLOGY

A multi-mode thruster is a system that incorporates a chemical and an electrospray thruster and is explained in [4]. The paper offers a way to realize both chemical and electrospray emission modes on a single platform and discusses the mission capabilities and lifetimes of such missions. The mission capabilities in high-thrust and high specific impulse modes are compared and contrasted. An assessment is made by comparing the chemical and electric mode burns for achieving a similar objective and the prospects of using both emissions in the same maneuver is discussed. It is concluded that the use of more than one type of emission greatly improves the overall usage of the thruster and increases the flexibility in mission planning.

One of the other significant works in the context of electrospray thrusters is done in by using dual electrospray thrusters [5], where extensive work on the functioning, modeling, and hardware implementation of electrospray thrusters on nano-satellites is presented. It discusses various aspects of the thruster construction and realizability of electrospray's as micro-thrusters. Focus on spacecraft charging phenomenon induced by the operation

of electrospray thrusters and explanation of the physics behind spacecraft charging and various issues that it causes to other electrical systems and the thruster are done in [5, 6]. The charging phenomenon can be thought of as the charging of a fictitious capacitance between the spacecraft and its surrounding environment: a plasma whose density and characteristics vary with the orbital altitude [5, 6]. These works provide expressions to assess the capacitance in such an environment and can be useful while analyzing the spacecraft charging dynamics. Additionally, [5] provides a mathematical model of the electrospray thruster, which is extensively used to build a simulation model of the system on Simulink<sup>®</sup> and assess the changing dynamics of the system.

The aforementioned works also suggest the usage of an even number of clusters, which operate in complementary ionic emission modes, to alleviate the spacecraft charging issue. This fact has been carefully taken into consideration throughout the design process and also has been incorporated into the simulation models to test its validity and significance. Also, the PPU's should abide by some other specifications set by [5],[6], and [7] to maintain chemical neutrality of the propellant in the system, which should also be taken into account.

The problem of spacecraft charging was first studied when satellites were charging up to thousands of volts leading to a subsequent failure, leading to the SCATHA (Satellite Charging at High Altitudes) program by the US Air force to study this charging phenomenon. The results of these findings were published in [8], with an emphasis on space plasma induced charging, nature of the space plasma, differential charging, and discharging strategies. It is established that the emission of electron beams can discharge a negatively charged satellite to a certain extent and may lead to additional problems such as differential charging. Low energy ion beams can discharge a negatively charged satellite by a returning ion theory explained in the same work. Finally, a plasma beam emission consisting of electrons and low energy ions was theorized to be an effective way of charge removal from a negatively charged spacecraft. The aspect of spacecraft charging due to external and

internal factors of the spacecraft in the context of an electrospray thruster can be studied by a Retarding Potential Analyser (RPA) [5, 9]. The capacitance of small spacecraft moving in a plasma environment is studied in [10].

## **2.2. HIGH VOLTAGE DC-DC BOOSTING POWER ELECTRONIC TOPOLOGIES**

So far, the literature describing the ionic thruster technology and allied topics were presented. These topics provide essential guidelines for the realization of a practical PPU. However, the PPU's construction is heavily based on power electronic principles, and some of the significant works relevant to this thesis work will be discussed in the following paragraphs. The class of power electronic converters that deal with the high voltages needed for electrospray thruster operation are called High Gain DC-DC Converters. These employ a range of traditional power electronic topologies cascaded with diode-capacitor voltage multiplier networks to generate the high voltages.

Some of the prominent papers in the context of high gain DC-DC converters are two phase interleaved boost converters interleaved to Cockcroft-Walton Voltage Multipliers [11, 13, 14, 15]. In these available papers, [15] proposes a PPU topology customized for a multi-mode mono-propellant electrospray thruster. It proposes a coupled inductor type thruster, which provides high gain ratios. But this converter suffers from two major issues when it comes to interfacing a multi-mode thruster. Firstly, it provides a floating ground which causes a short circuit due to the propellant tank being grounded to the absolute chassis ground. It also provides a single voltage that cannot be used for interfacing with a dual thruster arrangement. Reference [11], on the other hand, provides a range of high gain dc-dc multiplier topologies along with the one presented in [15] and presents a generalized approach for designing a converter. Construction of a high gain dc-dc converter for PV applications and closed-loop control strategies for the converter are discussed in [13]. A high voltage, high wattage lightweight converter for electro-aerodynamic propulsion applications

is described in [14], which discusses the design of lightweight converters and also provides a lot of practical considerations for achieving the desired functionality while also making the converter lightweight.

As the PPU is operated in high altitudes, and produces high voltages, disruptive mechanisms such as Corona and Partial discharges come into play [17, 18, 19, 20, 21, 22, 23]. These mechanisms can lead to complete failure of the insulation systems on PCB of the PPU and may lead to fault conditions. Therefore, a survey on materials qualified for these aerospace environments and operation conditions is necessary. High voltage PCB layout and material selection guidelines are provided in [18, 23].

### **2.3. CONCLUSIONS AND PROBLEM STATEMENT FORMULATION**

The papers discussed in this chapter give important guidelines to realize a safe and reliable PPU that is compatible with the electrospray thruster. The required features in such a PPU are:

- Ability to provide high voltage transfer ratios to be able to startup the thruster
- Ability to provide a low frequency alternating high voltage supply to the thruster to maintain chemical neutrality in the thruster propellant
- Ability to minimize the spacecraft charging problem by supplying voltages to a cluster of thrusters that work in complementary emission modes
- Groundability of the thruster to the satellite chassis
- Compactness to fit well within the space and volume constraints
- Flight computer integration and self regulation capabilities
- Closed-loop tracking for constant output voltage under varying battery voltages
- Predictable lifetime for mission sizing

All the above pointers lead to the final problem statement for this thesis work:

***Realizing a compact, safe, and reliable power processing unit that generates high bipolar voltages from a low voltage onboard battery supply that is safe to ground, provides a voltage alternating feature to maintain chemical neutrality of the propellant and alleviates the spacecraft charging issue while parallelly maintaining a constant output voltage under changing battery voltage conditions by closed loop voltage tracking.***

### 3. TOPOLOGICAL SURVEY

This Section describes the critical challenges faced in the realization of the PPU based on the hardware aspects and constraints set in Section 2.3. Therefore, the Section discusses the hardware aspects first and then proceeds with a topological analysis and inspection of some of the traditional high gain DC-DC power converters. Some of the merits and demerits of each topology are delineated, and the final topology for this thesis work is established.

#### 3.1. ELECTRICAL MODEL OF THE MULTI-MODE THRUSTER SYSTEM

The electrical model of the multimode thruster is again shown in Figure 3.1 for reference. It shows the entire model of the multimode dual thruster configuration with the PPU interfacing with it. The propellant tank stores the propellant needed for chemical

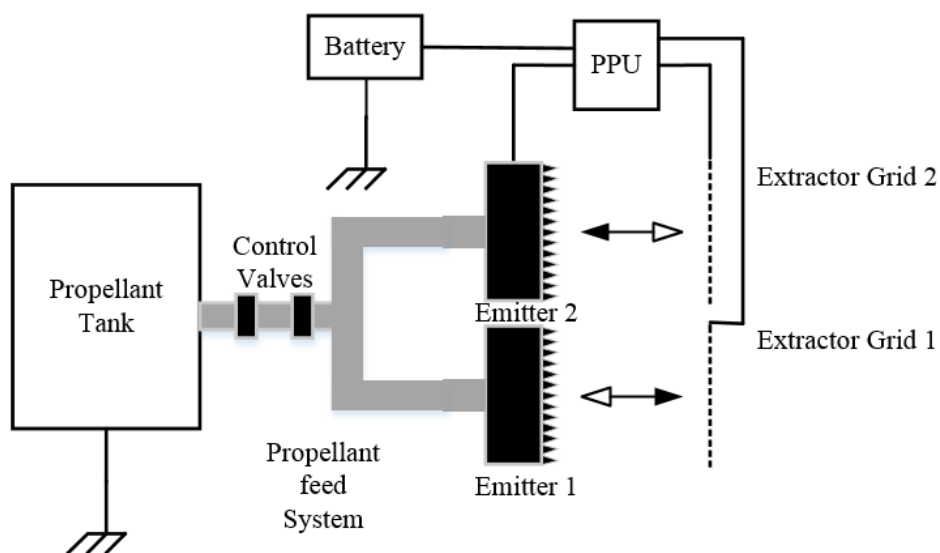


Figure 3.1. Hall Effect Thruster

mode while the tubes connected to the emitters hold the ionic propellant for electrospray mode. Depending on the requirements of the mission, either the chemical or electrospray modes are activated.

The chemical mode works by controlled depressurization of the propellant tank with the help of the control valves. The electric mode works by activating the PPU and emitting the ions from the ionic propellant stored in the emitter tubes.

The propellant tank, connected to the chassis of the satellite, implies not only a mechanical connection but also an electrical one, due to a continuous metallic path from the emitters of the thruster to the propellant tank.

The propellant feed tubes are also metallic, and hence there is a continuous electrical circuit from the emitters of the thruster to the propellant tank. Hence, one can assume that the emitters are electrically 'grounded' to the satellite's chassis.

### **3.2. THE THRUSTER GROUNDING ISSUE**

The electrical model of the thruster gives a critical understanding of the way the PPU should generate the output voltages. The PPU could short out when connecting to the emitter, which could happen when the PPU generates a high voltage with respect to a floating ground. This floating ground interacts with the chassis ground (to which the battery gets connected) and causes fault currents to flow through the PPU, damaging the switching MOSFETs in the PPU.

Therefore it becomes essential to generate high voltages with respect to the satellite chassis ground and not some arbitrary floating ground, which is the main reason for the grounding issue to get specified as one of the vital consideration parameters in Section 2.3.



### 3.3. TOPOLOGICAL ANALYSIS

One of the essential classes of converters in Switched-Capacitor Converters (SCC's) is the Cockcroft Walton Voltage Multiplier (CWVM) shown in Figure 3.2. These provide a convenient way to boost bipolar square wave voltages to very high voltages with the help of simple capacitors and diodes. The other significant advantage of these converters is the voltage stress on each component in the multiplier. The multiplier provides an individual cell-by-cell voltage stress instead of cumulative voltage stress, which makes the generation of high voltages possible with relatively low voltage rated components as described in [11] and [15]. Various possible ways of feeding voltages to a CWVM stage is discussed in [11].

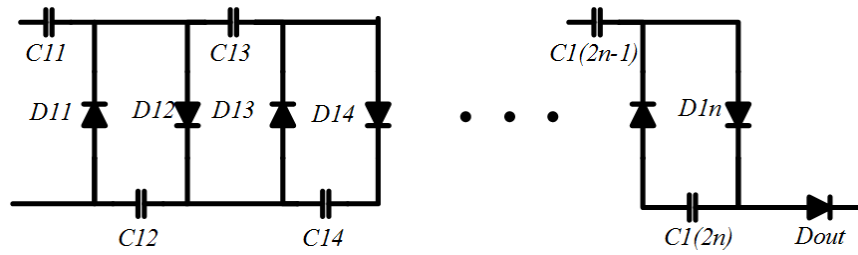


Figure 3.2. A Positive Voltage Cockcroft Walton Multiplier

#### 3.3.1. Connection Configurations to Cockcroft Walton Voltage Multiplier Stage.

The way one can feed the high voltage to the Cockcroft Walton voltage multiplier can change depending on the topology in which it is connected and the required target voltage. Some of the common types of connection typologies described in [11], and [15] and their feasibility and relevance of use are discussed in the subsequent sections.

**3.3.1.1. Simple two-phase interleaved boost converter.** In this topology, two simple boost converters, each comprising of MOSFET and an inductor are used. The converter shown in Figure 3.3 is different from a traditional boost converter in the sense that the forward diode and the filter capacitors are missing. The converters are connected in anti-phase rather than being connected to a node point, as one would expect in a traditional

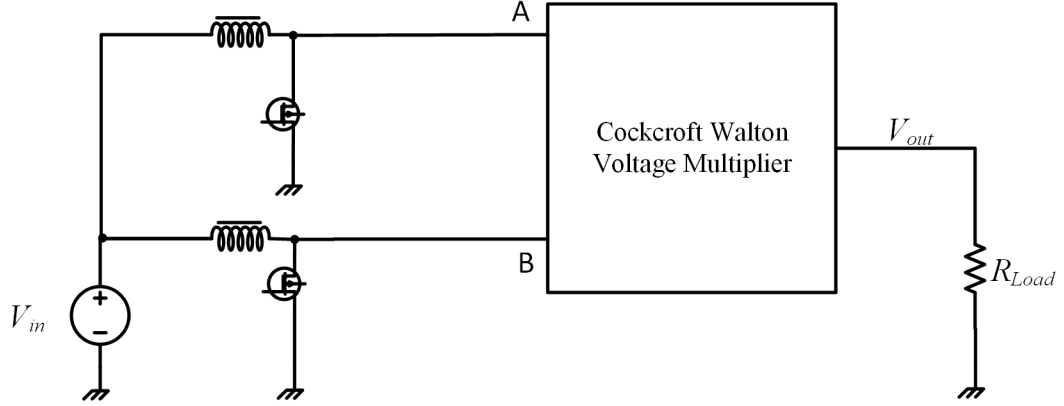


Figure 3.3. A Simple Boost Converter Based Input Feed

interleaved boost converter. This anti-phase connection results in a Modified Square Wave (MSW) feed, crucial to the working of the CWVM, which will be explained in the subsequent chapters.

If the converter is assumed to be working in Continuous Conduction Mode (CCM), the output of the converter is given to be

$$V_{out} = \pm \frac{V_{in}}{1 - d} \quad (3.1)$$

where,  $d$  is the duty cycle of the converter, the  $\pm$  symbol is added to account for the polarity of the MSW wave. It should also be noted that the converters are to be given anti-phase PWM signals, as shown in Figure 3.4 to maintain inductor current continuity, which is a basic necessity for any converter described in this chapter. Without this anti-phase PWM scheme, the switches will suffer from inductor over-voltage spikes, that completely damage the high speed switching MOSFETS.

This converter is fit for boosting to high voltages and is extensively used in PV systems for grid integrated inverter feed as described in [13]. However, the major drawback of this type of converter is the necessity of a higher number of voltage multiplier stages needed to get the target voltage. The duty cycle could also be used to increase the output

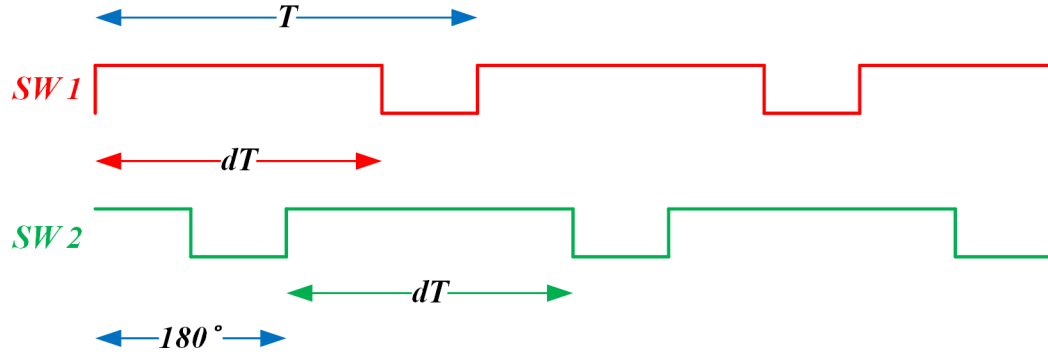


Figure 3.4. Preferred PWM Scheme for All the MSW Feed Converters

voltage, but the boost converters are known to have a non-ideal voltage transfer, which drops at high duty values due to the parasitic resistance in the inductors. Also, the converter only generates a pure DC signal with respect to the output voltage point and point B in the converter shown in Figure 3.3. However, point B is a floating voltage point and cannot be connected directly to the emitters as they would short out the converter via the propellant feed system of the converter shown in Figure 3.1. Even if the load was connected to the ground, the converter generates a voltage with a ripple riding over it, making the thrust emission unsteady.

**3.3.1.2. Coupled inductor based boost converter fed CWVM.** Coupled inductor based high gain DC-DC converters have significant advantages over a simple interleaved boost converter as it has significantly lower voltage stress on the switches. The converter also has a higher gain value for a relatively lower duty value when compared to a simple boost converter, making the coupled inductor based converter the right choice for standalone electrospray thruster systems, which have a single thruster and have no hybrid functionalities. They bode well on the space constraint perspective too. However, even this type of topology will fail in the case of a hybrid electrospray thruster as the point B, shown in Figure 3.5 is floating at a higher voltage than the chassis and will cause a dead-short circuit between

the source and the inductors, leading to a failure. From an implementation perspective, the construction of coupled inductors is a little more involved and will also lead to more design considerations during the PCB layout as both the inductors are coupled.

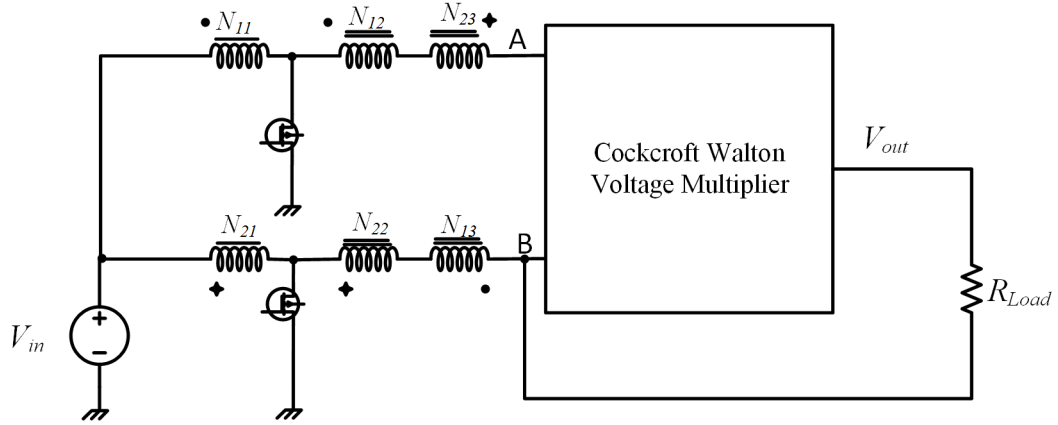


Figure 3.5. Coupled Inductor Based Boost Converter

**3.3.1.3. Transformer coupled CWVM.** The schematic of the transformer-coupled topology is shown in Figure 3.6. Points A and B are entirely isolated from the primary side's TPI stage, which makes the point B free to be coupled anywhere the designer chooses. It also performs well in the volume front as the transformer can be used to set a voltage transfer ratio which relieves stress on the primary side switches while also reducing the number of CWVM cells needed to achieve the target voltage. This makes the converter reach higher voltages at a relatively lower duty cycle value when compared to a boost or a coupled-inductor based boost converter. Hence this converter can be considered as modular and highly scalable. The converter can be used for both grounded (hybrid/standalone) or ungrounded (standalone) thruster applications due to the isolating nature of the converter.

**3.3.1.4. Concluding notes on the converter's base topology.** Based on the converter topologies described so far, it has been established that the transformer coupled high gain DC-DC converter is highly versatile and flexible for electrospray thruster design. It provides an excellent way to connect to the electrical ground/chassis of the electrical system and also provides a modular feature to get high gains at low duties, which was almost impos-

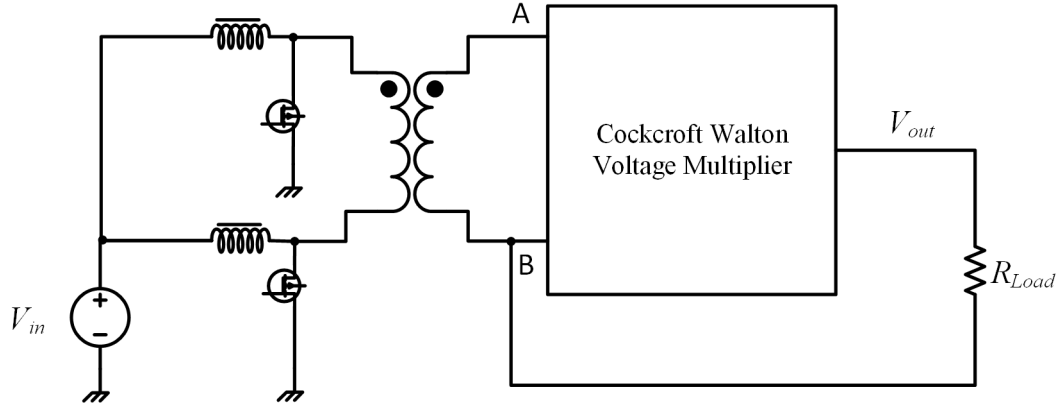


Figure 3.6. Transformer Fed CWVM

sible in a simple boost converter based TPI topology. The design problem is recognized as a trade-off between the switch stress, transformer's turns ratio, number of Cockcroft Walton Voltage Multiplier Stages and the target voltage range.

### 3.4. MEETING THE VOLTAGE DEMANDS OF THE THRUSTER

Sections 2.1, and 2.3 establish that the PPU should be able to supply bipolar voltages to the thruster to ensure the maintenance of chemical neutrality in the propellant. The voltage should alternate at a low frequency, to make the thruster emit positive and negative ions alternatively in each excitation. This as a challenging task as the switching element should be able to withstand the high voltages generated by the CWVM. In the following sections, two possible high voltage switching connections are explained.

**3.4.1. Using a Full-Bridge Inverter.** Using a standard H-Bridge is an obvious choice when alternation in voltage polarity for a load is required. However, controlling a high side switch, at times, can be an issue due to the additional isolated gate drive requirements. H-Bridge works best for a standalone type thruster where the emitter can be left floating, as shown in Figure 3.7.

However, a H-bridge is unsuitable for a case where the emitter is tied to the ground (via the propellant feed system), as shown in Figure 3.8. This fixed point causes short circuits when the H-bridge switches the switch S1 ON, causing the entire supply voltage to short circuit to the grounded emitter.

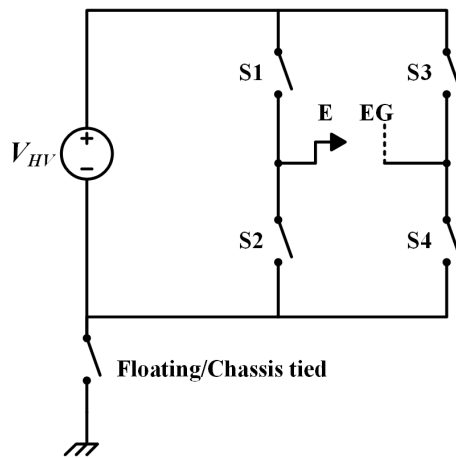


Figure 3.7. A H-Bridge Inverter Supplying High Voltage to a Standalone Thruster

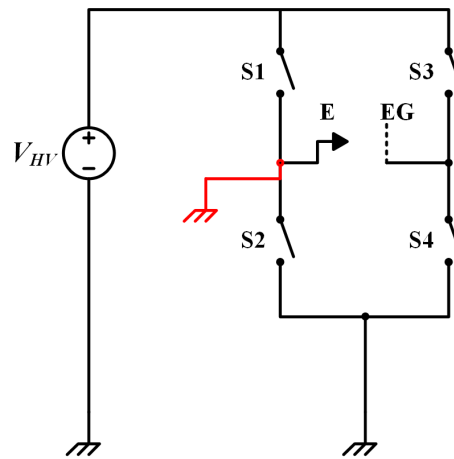


Figure 3.8. A H-Bridge Inverter Supplying High Voltage to a Hybrid Thruster

**3.4.2. Using a Half-Bridge Inverter.** A half-bridge inverter is a better option compared to a H-Bridge as the load's return path is not interacting with any high voltage rail. A schematic of the proposed concept is shown in Figure 3.9. In this case, a Single Pole Double Throw (SPDT) switch is used to switch between a positive high voltage and a negative high voltage rail alternatively. The EG is connected to the high voltage lead and E to the chassis. This scheme, however, demands a preexisting negative rail. Figure 3.2 shows a positive high voltage multiplier. However, a Half-Bridge Inverter needs a dedicated positive and negative high voltage source. Therefore, the negative high voltage multiplier can be realized by reversing the direction of the diodes in the Cockcroft Walton Voltage Multiplier, as shown in Figure 3.10. Thus, this scheme of connection requires two independent sources of high voltage, and each can be selected based on the ion emission mode required.

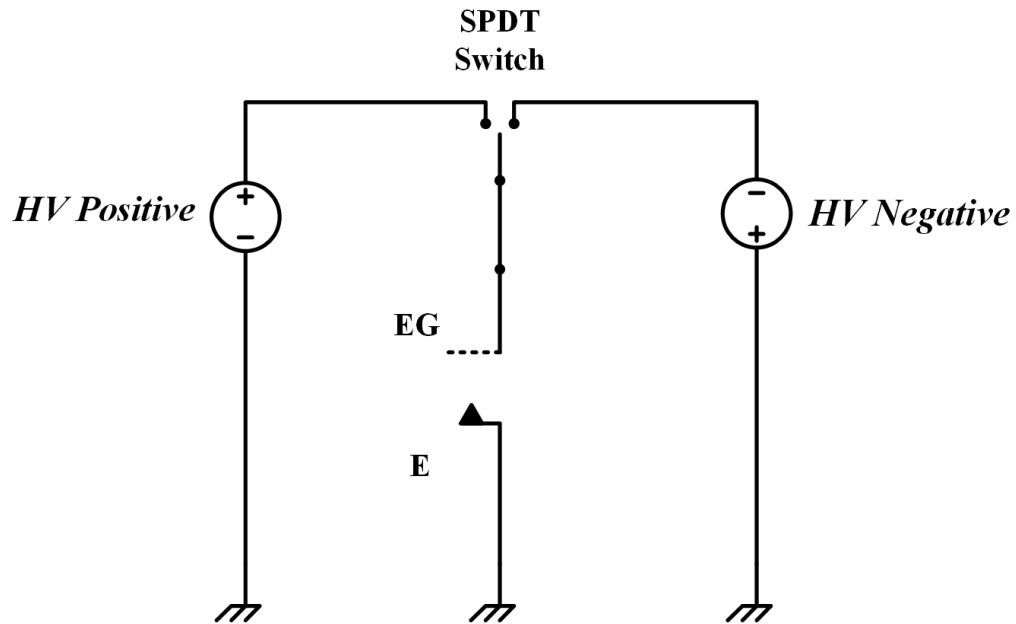


Figure 3.9. Half Bridge Inverter Fed Hybrid Thruster

Therefore, the half-bridge inverter scheme is a compelling solution to meet the alternating voltage features of the electrospray thruster.

In order to accommodate multiple thrusters, the number of SPDT switches over the high voltage rails can be increased, and this can lead to a multi-thruster operation. This dual CWVM feed can be fed with MSW's from the transformer-coupled topology explained in Subsubsection 3.3.1.3.

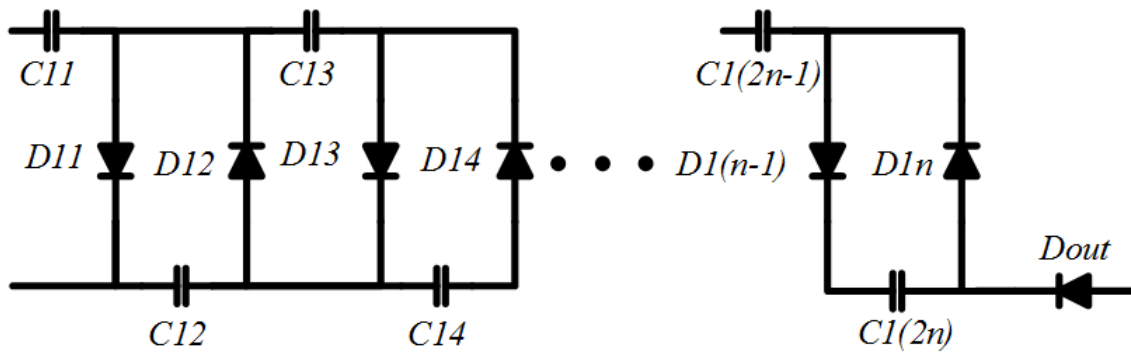


Figure 3.10. A Negative Cockcroft Walton Voltage Multiplier

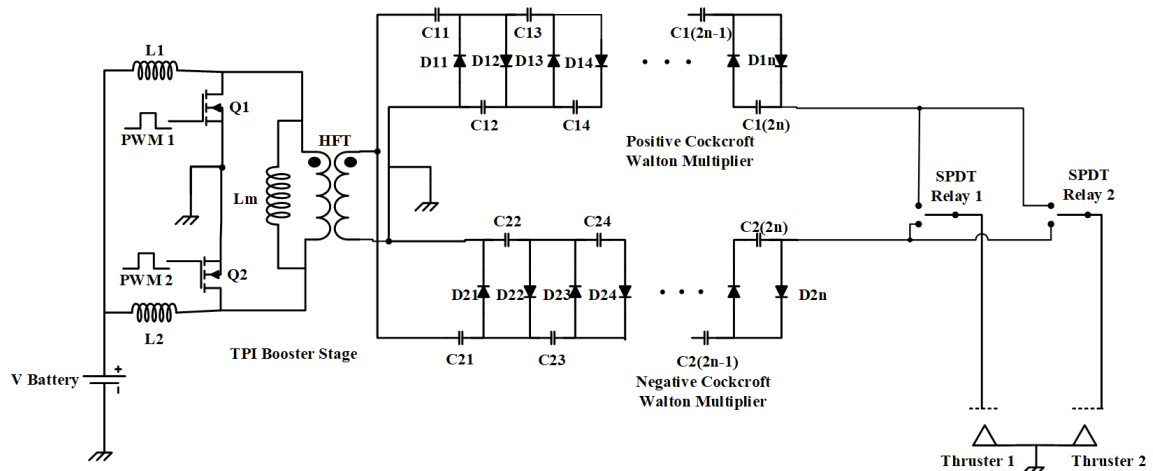


Figure 3.11. PPU Topology for a Dual-Hybrid Electro Spray Thruster

### 3.5. ELECTRICAL SCHEMATIC OF THE PROPOSED CIRCUIT

Based on the discussions in the previous sections, a transformer fed dual output, alternating high voltage half-bridge topology is established to be capable of meeting almost all the constraints put forth by the electro spray satellite propulsion system. It majorly takes care of the grounding and voltage alternating features that ensure safe grounding of the hybrid thruster and also helps maintain chemical neutrality in the propellant. A schematic of the converter topology proposed in this thesis is shown in Figure 3.11.

The proposed converter consists of two Cockcroft Walton voltage multipliers, which are fed by the high-frequency transformer. The transformer's secondary is tied to the satellite chassis. Hence the second terminal of the secondary is the one that applies both the positive and negative polarities on the CWVM stages.



## **PAPER**

### **I. CLOSED-LOOP VOLTAGE MODE CONTROL OF POWER PROCESSING UNITS FOR ELECTRICALLY PROPELLED SATELLITES**

#### **ABSTRACT**

In this paper, a transformer coupled high gain DC-DC converter is proposed for applications in electrospray thruster systems. The proposed converter consists of a two-phase interleaved boost converter, a step-up transformer, and a Diode-Capacitor multiplier. The proposed converter enhances the reliability of the thruster by alternating the voltage across the extractor grids, which ensures the neutrality of the propellant. The paper addresses the grounding issue of the multi-mode thruster, which is pivotal to the successful operation of the propulsion system. A hardware prototype is presented and the theoretical and practical converter gains are analyzed and compared. The converter proposed in this paper is found to be highly modular and scalable in nature, enabling enhanced mission capabilities.

#### **1. INTRODUCTION**

Electrospray thrusters are promising for the emerging field of nano-satellites, such as CubeSats. The phenomenon of an electrospray occurs when a high voltage is applied to a conductive liquid in a nozzle, ionizing a droplet. Based on the direction of the electric field, either positively or negatively charged droplets are expelled out of the emitter with high velocities, which results in micro to nano Newtons of thrust but with high specific impulse. Due to an almost frictionless environment in space, this thrust generated is adequate to propel the satellite. Electrospray thrusters find their use in places where very

fine adjustments in attitude and position are required. In micro and nano-satellite systems, space and mass are highly constrained. In these cases, electrospray thrusters have excellent potential due to their highly scalable nature.

This paper addresses the design of a power processing unit (PPU) for a multi-mode electrospray thruster [1]. Previous approaches [2] have been found to be acceptable for laboratory testing, but unsuitable for spacecraft deployment. Although an electrospray

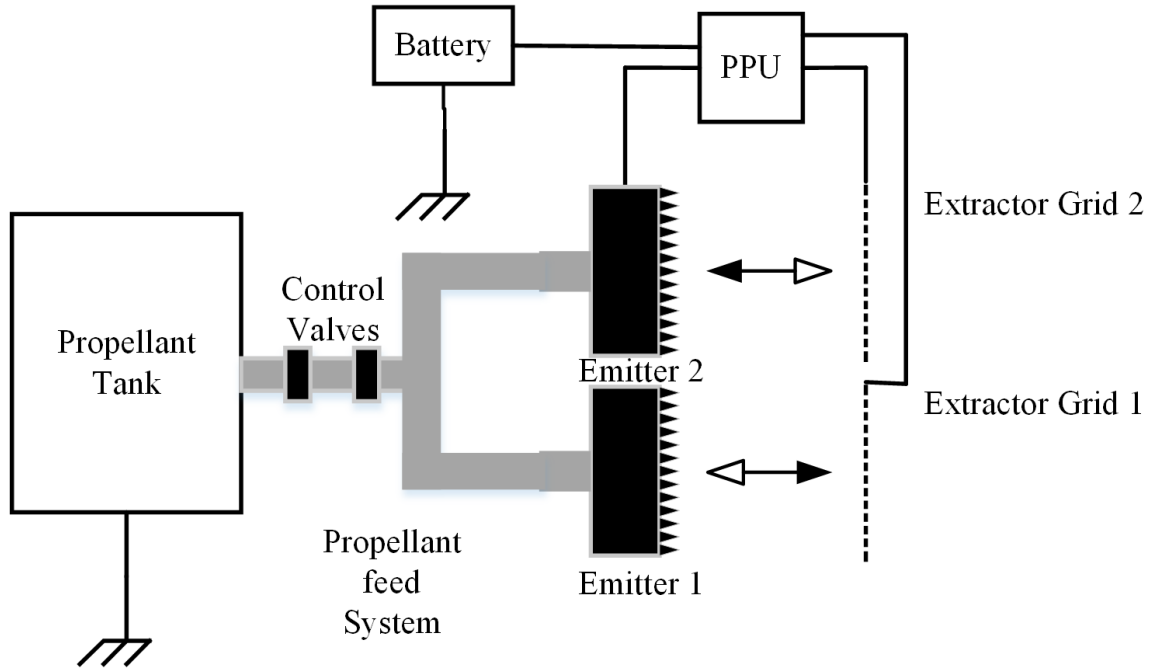


Figure 1. Configuration of the Thruster

thruster is technically a two-terminal device, only one terminal is electrically available. Particularly in the case of a multi-mode system [1], the emitter is mechanically and electrically attached to the chassis with the propellant feed tubes and the propellant storage tank, which are conductive as shown in Figure 1. If the terminal of the PPU connected to the emitter section is floating at a different voltage level other than zero (considering the chassis to be the reference potential), a short circuit would exist, leading to damage to the system.

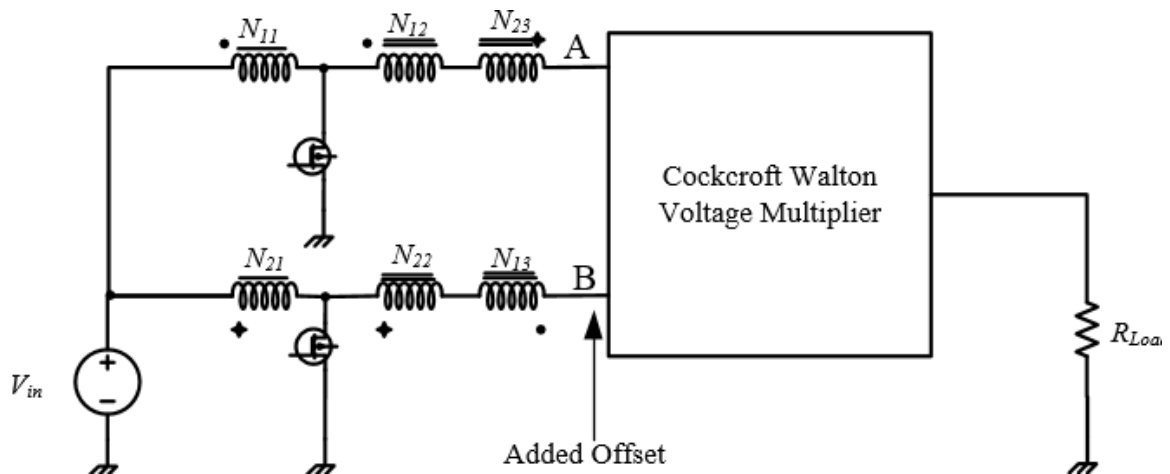


Figure 2. Floating Return Issue in Inductor Coupled PPU Configuration [2]

Two emitters and two extractor grids are shown in Figure 1 as recommended in [3, 4]. This configuration ensures the health of the emitter tips while also alleviating the spacecraft charging issues. To ensure the health of emitter tips and to maintain the neutrality of the propellant, voltage applied to the extractor grids should be alternated [3].

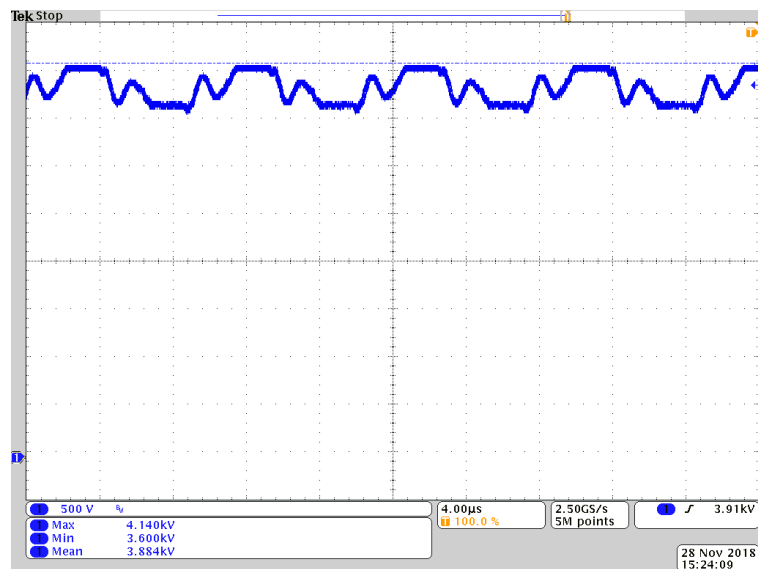


Figure 3. Voltage Ripple Caused Due to the Operation of the Coupled Inductor Topology with the Load Terminal Returning to the System Ground

Some of the previous implementations in the field of electrospray propulsion are listed in [2, 4, 5, 6, 7, 8]. The implementations involved a standalone thruster approach where a single or a cluster of electrically isolated thrusters with dedicated and isolated propellant tanks were propelled with a PPU.

An isolated propellant tank is used in the PPU topologies proposed in [5], [7]. However, this wouldn't be practical in the case of a hybrid thruster where the cold gas mode is regulated by control valves that are driven by chassis referenced electronics of the flight computer. Due to the propellant liquid being conductive, this approach would lead to failure of electronics due to ground mismatch. In order to solve the unequal ground issue, all the electronics and mechanical elements tied to the extractor are referenced to the chassis potential as shown in Figure 1. This would also mean that the propellant storage tank and the propellant feed system would be referenced to ground and would simplify structural integration. Hence the actual voltage is applied to the extractors while the emitters are referenced to the chassis ground, making it possible to operate in both the modes without any grounding issues.

The converter proposed in [2] and illustrated in Figure 2 assumes that the voltage need not be alternating. It also provides voltage supply to power only a single thruster, which would exacerbate the spacecraft charging issues described in [9, 10]. The converter also has a floating return path, different from chassis potential, and would create the unsafe grounding situation.

This issue is caused by the coupled inductor based Two-Phase Interleaved (TPI) boost converter. The output is intended to be taken differentially with respect to point B as in Figure 2. However, point B is alternating with respect to circuit common as Q2 switches, so the output is also alternating with respect to ground. Figure 3 shows the voltage ripple issue in such a configuration. Hence, the propellant feed tank, feed system, and other associated components would need to be electrically insulated from the satellite chassis and the load would have to be connected to output and point B to get a ripple free voltage as

presented in [5]. This is an impractical approach that poses many structural design issues for a nano-satellite. In this paper, a better approach has been pursued: **a change of topology of the converter such that the return path is at the same level as that of the chassis.**

Section 2 introduces the topology of an improved PPU, that takes care of the considerations for a groundable propellant feed system and describes the modes of the converter. Section 3 presents the analysis of the converter for parameters such as overall gain, the critical inductance of the TPI stage inductors, and overall efficiency. Section 4 explains the factors affecting the dynamics of the converter. Section 5 discusses the hardware implementation and design aspects. Section 6 discusses the results and the paper is concluded by Section 7.

## 2. TRANSFORMER COUPLED SWITCHED CAPACITOR CONVERTER

The proposed converter topology is shown in Figure 4. This is a derivative of one of the many topologies presented in [11]. Two switches, Q1 and Q2, and inductors, L1 and L2, form the TPI stage. The TPI stage then feeds a Modified Square Wave (MSW) to the High Frequency Transformer (HFT), which does two important tasks. Firstly, it boosts the MSW's amplitude so that the TPI's duty value is within safe limits. Secondly, the HFT separates the primary and secondary sides, which provides protection to low voltage switching electronics and also provides a way to ground the transformer's secondary to the chassis, which was not previously available in the case of a coupled inductor based topology implemented in [2].

The HFT supplies the boosted MSW to the two Cockcroft-Walton Voltage Multiplier (CWVM) stages which generate the positive and negative high voltage levels which in turn are supplied to a single-pole double-throw (SPDT) switch. SPDTs sufficient to switch the single terminal of each extractor between positive and negative potentials.

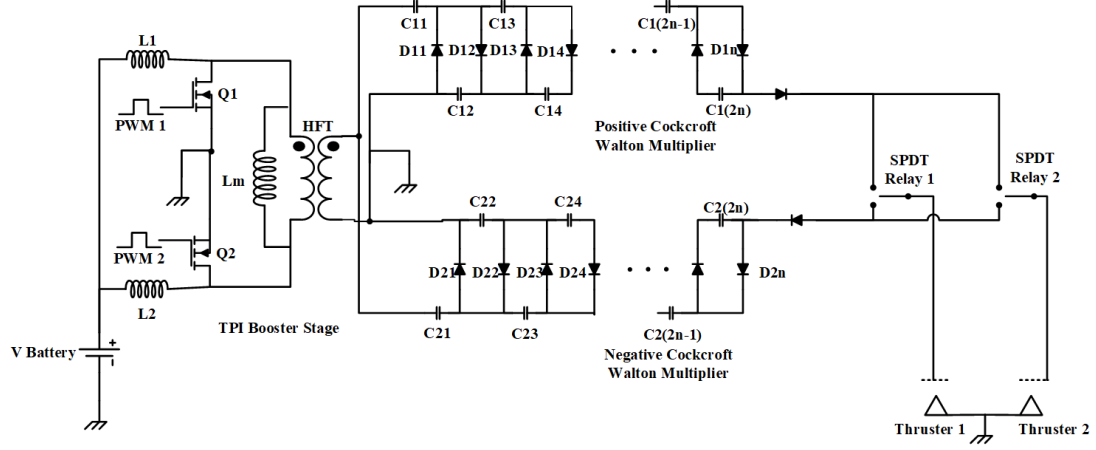


Figure 4. Proposed HFT Coupled Switched Capacitor Converter

## 2.1. CONVERTER MODES

Figure 5 shows one complete switching cycle of the converter and the four modes the converter goes through. Prior to Mode 1, the circuit is in Mode 4 with Q1 off, Q2 on,  $I_{L1}$  at its minimum, and  $I_{L2}$  rising. The various modes of the TPI and HFT stages are shown in Figures. 6,7,8,9.

**2.1.1. Mode 1.** Both the TPI stage switches are switched on while the currents in  $I_{L1}$  and  $I_{L2}$  in the TPI stage inductors rise as shown in Figure 5, and Figure 6. It is assumed that the switch Q2 is previously switched on and  $I_{L2}$  was previously rising from its minimum value  $I_{Min}$ . At the end of this interval, the inductor current  $I_{L2}$  reaches its peak. The HFT's magnetizing inductance current  $I_{Lm}$  starts decreasing due to the freewheeling action with the Q1 and Q2. The secondary current in the HFT starts to flow out of the dot and into the CWVM sections. The positive CWVM can be represented by Figure 10 and the negative CWVM can be represented by Figure 11 during this phase.

**2.1.2. Mode 2.** In this mode, Switch Q1 is on while Switch Q2 is off, causing the current  $I_{L2}$  in inductor L2 to flow through the HFT's primary, while finally reaching to its minimum value as shown in Figure 5 as shown in Figure 7. The current  $I_{L1}$  continues to rise in this mode. The current in the magnetizing inductance of the inductor starts rising

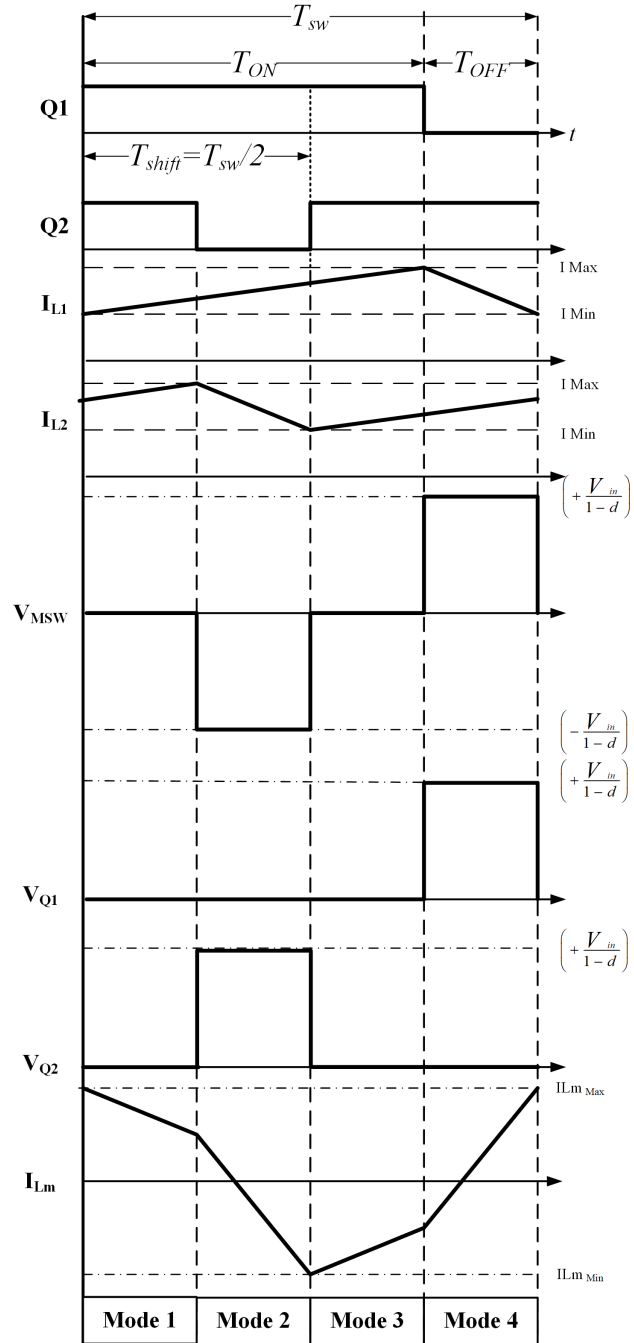


Figure 5. Converter Modes and Switching Scheme

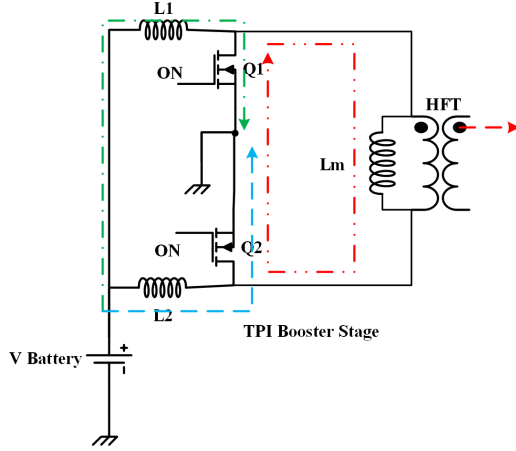


Figure 6. TPI Mode 1

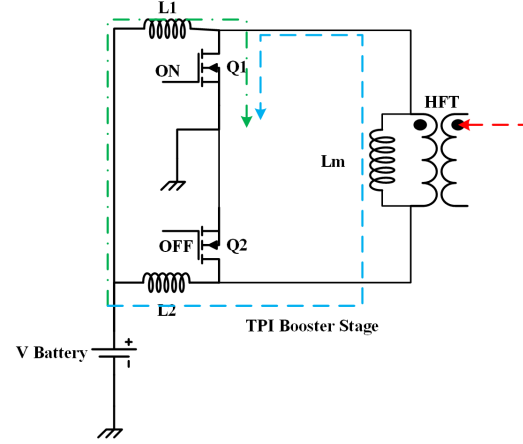


Figure 7. TPI Mode 2

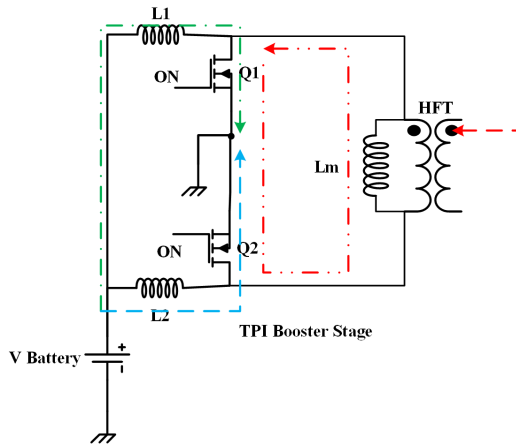


Figure 8. TPI Mode 3

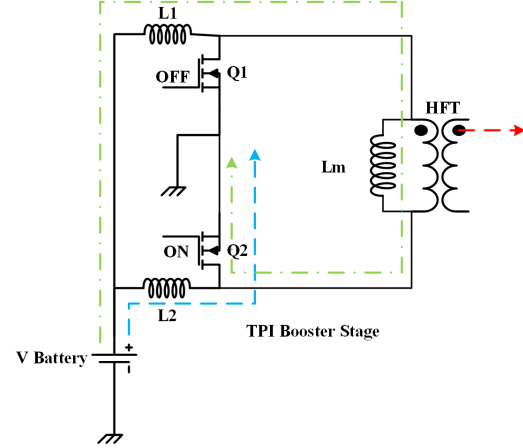


Figure 9. TPI Mode 4

and reaches the negative peak by the end of the mode. A negative voltage is impressed on the primary, that gets stepped up by the HFT. In this stage, the positive CWVM takes the form shown in Figure 11 and the negative CWVM takes the form as shown in Figure 10.

**2.1.3. Mode 3.** This mode is similar to mode 1, where Q1 and Q2 are switched on. The inductor current  $I_{L1}$  continues to rise and reaches the maximum value  $I_{Max}$  by the end of the mode. The inductor current  $I_{L2}$  starts to increase from its minimum value. The HFT current  $I_{Lm}$  starts to decrease as it freewheels with the switches Q1 and Q2 as shown in Figure 8. The Positive CWVM continues to take the form of the circuit model represented in Figure 11 and the negative CWVM take the form of Figure 10.



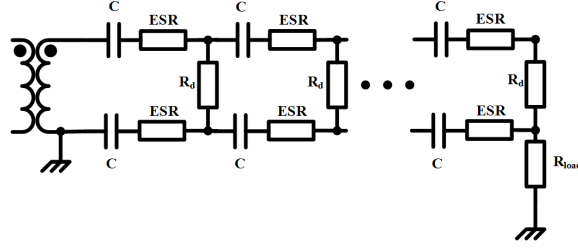


Figure 10. Multiplier Mode 1

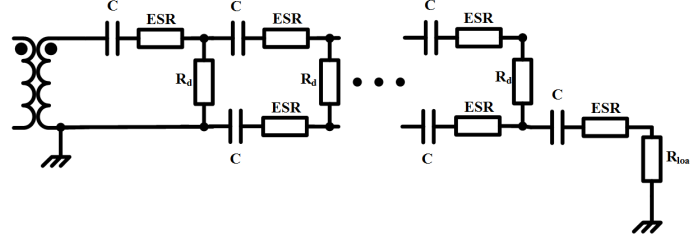


Figure 11. Multiplier Mode 2

**2.1.4. Mode 4.** In this mode, the switch Q1 is turned off and switch Q2 is kept turned on. This causes the Inductor L1's current,  $I_{L1}$  to start flowing through the HFT's primary. This also causes the HFT's magnetising inductances' current  $I_{Lm}$  to rise, until it reaches a maximum at the end of the period. The current  $I_{L2}$  starts rising through the period, until it reaches a maximum value  $I_{Max}$ . A positive voltage is impressed on the primary, that gets stepped up by the HFT. The positive CWVM take the form of of Figure 10 and the negative CWVM takes the form as shown in Figure 11.

## 2.2. DUTY RESTRICTION

At no point during the operation of the converter can the duty of switches Q1 or Q2 fall below 50% as one of the inductors L1 or L2 will be going through a charging phase at any given point in time as shown in Figure 5. Thus, the minimum possible duty of this converter topology is 50% and reducing the duty value below 50% can cause a catastrophic

failure in the converter due to overvoltage spikes caused due to the electrical inertia of the inductor. The two PWM channels should be maintained at a  $180^\circ$  phase difference to enable smooth inductor current cycling as shown in Figure 5.

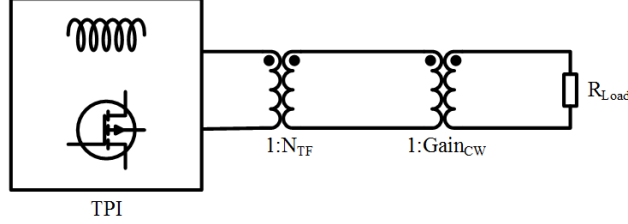


Figure 12. Load Referencing Model

### 3. ANALYSIS OF THE PROPOSED CONVERTER TOPOLOGY

The steady state gain of the converter is presented in this section along with other important performance parameters. This converter can be envisioned as a simple boost converter with a constant high voltage multiplication block. therefore, the gain of the expression can be given by [12]

$$V_{out} = \frac{2nN_{TF}}{(1-d) \left( 1 + \frac{1}{fR_{load}C} \left( \frac{2n^3}{3} + \frac{n^2}{2} - \frac{n}{6} \right) \right)} V_{in} \quad (1)$$

where  $N_{TF}$  is the HFT's turns ratio and  $n$  is the number of CWVM stages. One of the other major considerations in this topology is the design of magnetic components L1, L2, and HFT, which are critical to the operation of converter.

#### 3.1. INDUCTOR SIZING

TPI stage is assumed to be operating in Continuous Conduction Mode (CCM). For this, the minimum current through any inductor should be greater than zero. Therefore, critical inductance for a minimum duty of  $d_{min}$  at a frequency  $f$  is given by,

$$L_{crit} \geq \frac{d_{min}(1-d_{min})^2 R'_{load}}{2f} \quad (2)$$

where  $R'_{load}$  is the thruster, modeled as a resistor referenced to the TPI side as shown in Figure 12. This approach approximates the CWVM to be working as a simple transformer. Now,  $R'_{load}$  can then be expressed for a *Gain* of  $V_{in}$  in (1) as,

$$R'_{load} = \left( \frac{1}{Gain} \right)^2 \times R_{load} \quad (3)$$

### 3.2. SWITCH SIZING

The maximum voltage stress on Q1 or Q2 is given by Equation 4. However, the MOSFET should be selected such that it withstands the voltage stress at switching edges caused due to the leakage inductance spike in the HFT stage. This restriction can be relaxed if a clamp circuit is used between the TPI and the HFT stages.

$$V_{stress} = \frac{V_{in}}{1 - d} \quad (4)$$

### 3.3. CWVM CAPACITOR SIZING

The CWVM capacitors must withstand a voltage equal to the peak to peak value of the MSW wave input from the HFT stage. Therefore, for a set maximum duty of  $d_{max}$  the capacitor rating is given by,

$$V_{cap} = \frac{2V_{in} N_{TF}}{1 - d_{max}} \quad (5)$$

Equation 5 is valid for all the capacitors except  $C_{11}$ , and  $C_{22}$  as shown in in Figure 4, whose voltage rating is half of the voltage rating.

The capacitors should conform to the size constraints, while also having the required voltage ratings. Generally, Multi Layered Ceramic Capacitors (MLCC) are suited for the mentioned voltage and space constraints. However, MLCC's suffer from capacitance loss with dc voltage bias and may have to be paralleled to get the required capacitance.

### 3.4. LIMITATIONS ON VOLTAGE RANGE

The converter can be redesigned for any desired output voltage range, provided the voltage impressed on a CWVM's capacitor is below its voltage rating. Thus, the HFT turns ratio can only be increased till the MSW's peak-peak voltage is below the voltage rating of a selected multiplier capacitor. Higher voltage ranges can be achieved by adding more CWVM stages on top of each other as the voltage rating of a single cell is dependent only on the constraints imposed by the cell and is independent of other cells.

## 4. FACTORS AFFECTING DYNAMICS

The major factors affecting the dynamics of the converter are the TPI boost stages' inductors, the HFT's parasitic winding resistance, the magnetization inductance, the capacitance, ESR and the diode resistance of CWVM stages and the load resistance. The PLECS<sup>®</sup> environment was used in finding the major factors affecting the converter dynamics. It was found upon giving a step input to the converter's duty input and investigating the output voltage dynamics that the magnetization inductance and the winding resistance of the transformer and the CWVM capacitors.

As the CWVM stage has six stages, and twelve capacitors, leading to a total of fifteen state variables after including the states of the TPI stage inductors and the magnetization inductance of the HFT, the process of modeling the dynamics of the converter, extremely hard. For this purpose, the cause of the dynamic responses are inspected and a closed loop converter is implemented by a trial and error method on the hardware converter. A step change in the duty input is applied to the converter and the dynamics of the converter are inspected. For a step change in input from 55% to 65%, the output voltage varies on the hardware converter as shown in Figure 13. The first trace is the HFT secondary voltage and

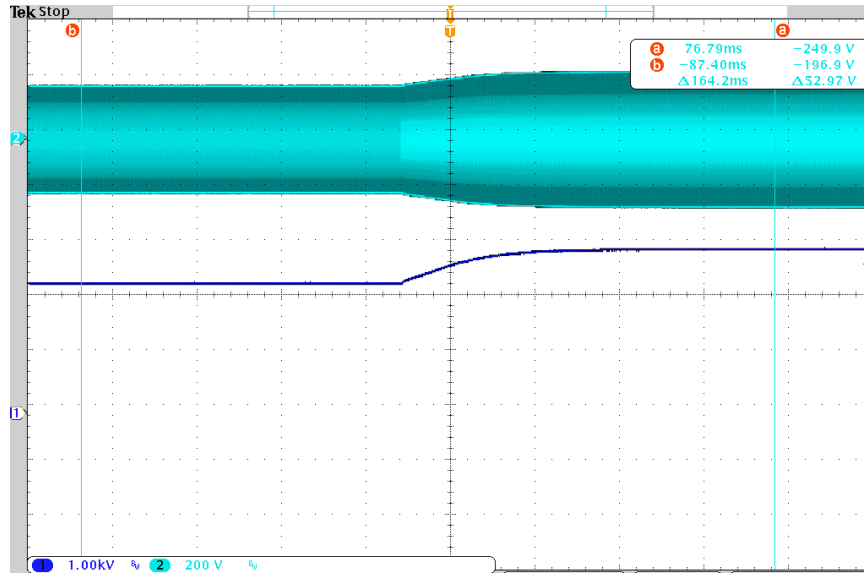


Figure 13. Secondary Voltage Rise and Output Voltage Rise for a Step Change in Duty from 55% to 65%

the second trace is the output voltage. Upon running the same converter in the PLECS® environment, the voltage was found to change in similar fashion to the hardware converter. The results of the simulation are shown in Figure 14.

## 5. HARDWARE IMPLEMENTATION AND DESIGN

A hardware prototype of the converter is shown in Figure 22. The PPU has two boards stacked on top of each other. The lower board has the digital controller and the first two stages of the topology (i.e the TPI stage and the HFT stage). The upper board has the high voltage CWVM multipliers, the high voltage SPDT relay's, the high voltage acquisition units and the SPDT relay firing networks. The selected components for the topology are shown in Table 1 for reference. The MLCC capacitors are rated for 630 V which limits the maximum dc voltage applied on them to about 600 V which in turn limits the maximum allowable output voltage of the CWVM to 3.6kV. MLCC capacitors offer

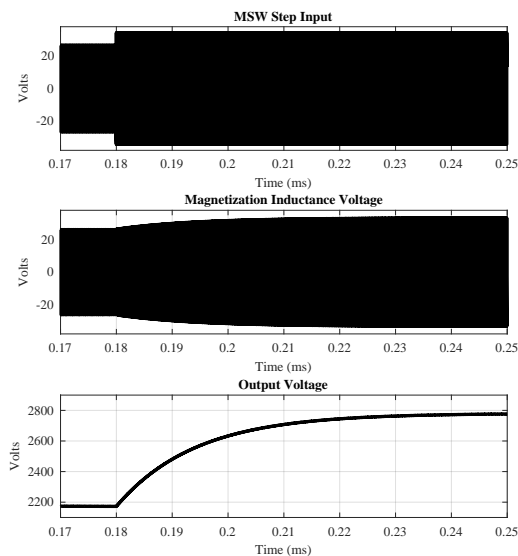


Figure 14. Simulation Model Results for a Step Change in Duty from 55% to 65%

superior space savings when compared to their film capacitor counterparts but suffer from capacitance degradation when dc voltages are applied. They also come with an inherent ESR and tend to be more lossier.

## 5.1. MAGNETICS

Two 400  $\mu\text{H}$  inductors were designed using the methods in [13] and constructed on PQ 32/30 cores as shown in Figure 15. Similarly, a HFT with a turns ratio of 10:70 was constructed on an ETD39 core, as shown in Figure 16.

## 5.2. FEEDBACK NOISE AND LINEARITY

The feedback signal from the half tap point of the CWVM stage is taken and divided by a 100  $\text{M}\Omega$  and a 100  $\text{k}\Omega$  high precision resistors. Upon sensing the voltage of the feedback signal from the high precision potential divider, it is observed that the MSW feed signal's

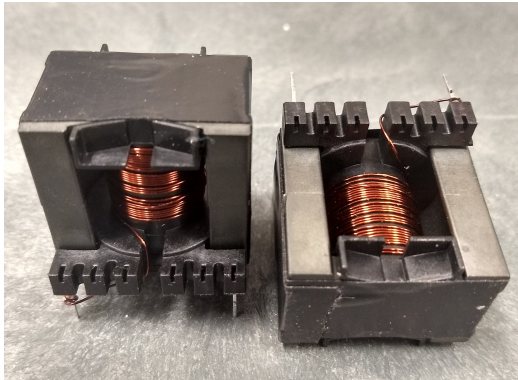


Figure 15. TPI Stage Inductors

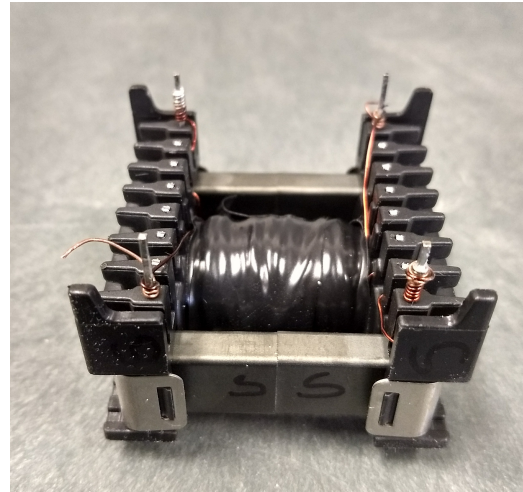


Figure 16. High Frequency Step-Up Transformer

noise creeps into the output of the of the CWVM and appears in the feedback voltage as shown in Figure 17 and 18. The signal cannot be used by an ADC as it is a varying signal caused due to the MSW feed, and as the signal is expected to be a dc signal.

The signal however, has a non zero average, which indicates the actual voltage information necessary for the measurement of the voltage by the ADC. Hence it becomes necessary to filter out the 100 kHz MSW signal by adding a 470 nF capacitor in parallel to the sense resistor in the precision voltage divider. The output voltage after adding the filter capacitor is shown in Figure 19.

The filtered feedback voltage was acquired for various output voltage values as shown in Figure 20 and was found to be linear. A first order curve fit was applied to the data in Figure 20 to get a mapping equation to be implemented on the flight computer, making it possible to implement safe shutdown procedures and have a way to log voltage data during flight.

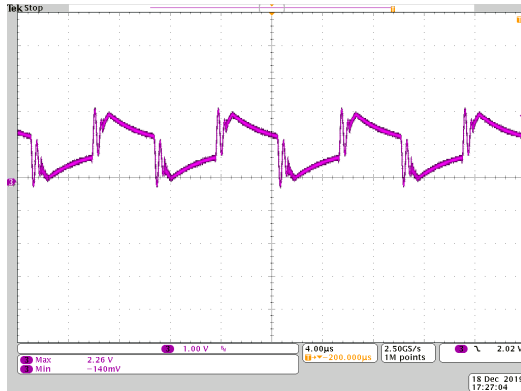


Figure 17. MSW Noise in Feedback Signal at 12 V and 55% Duty at 100 kHz Operation

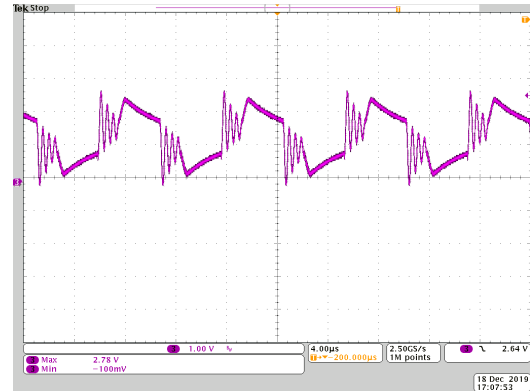


Figure 18. MSW Noise in Feedback Signal at 12 V and 65% Duty at 100 kHz Operation

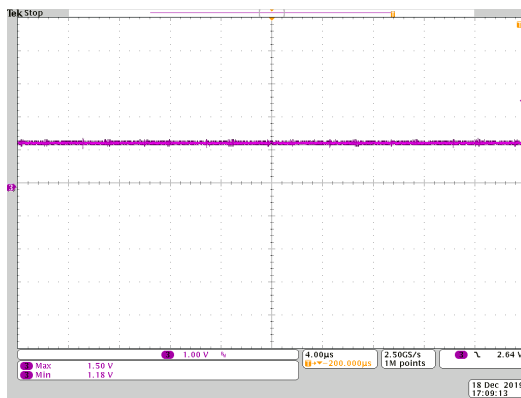


Figure 19. Filtered MSW

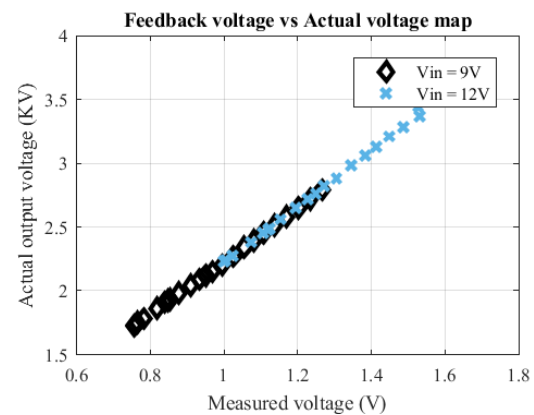


Figure 20. Feedback Linearity

### 5.3. CONTROL AND DATA COMMUNICATION INTERFACE

For the purpose of control, a dsPIC33 MCU was used to generate the necessary PWM signals, which were fed to a MIC4424 low side MOSFET gate driver to achieve the necessary drive voltages. The dsPIC was controlled using a Raspberry Pi, working as an I<sup>2</sup>C master and the dsPIC was configured as an I<sup>2</sup>C slave. This enabled direct online manipulation of converter properties and also laid down the necessary framework for flight computer integration. Some of the functions implemented over the I<sup>2</sup>C interface were



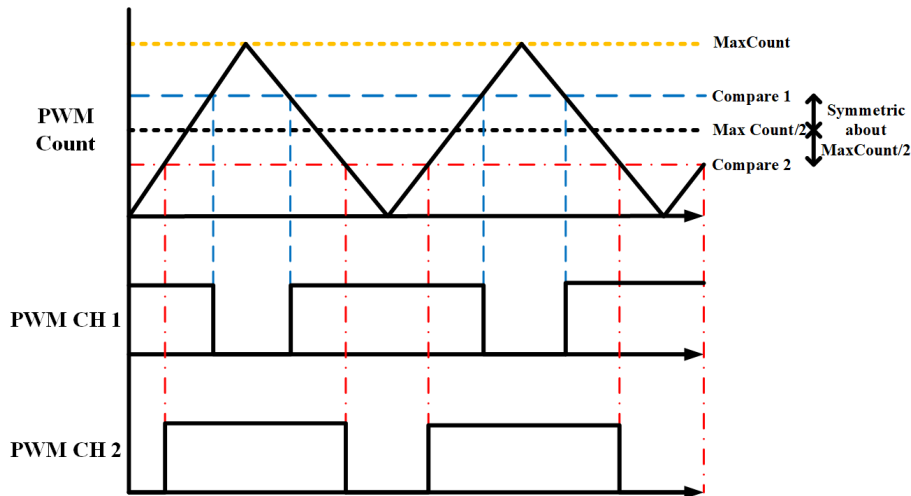


Figure 21. Implementation of the PWM Scheme in the dsPIC33F MCU

toggle, online duty override, online PWM frequency override, ADC value echo, online adjustment of control parameters and set points. The PIC MCU core was run at a 40 MHz clock and the PWM was run at 100 kHz primarily.

#### 5.4. PWM SCHEME IMPLEMENTATION

A hardware level PWM implementation method is shown in Figure 21. One PWM module can be used to generate the required PWM waveforms. The 50% duty restriction can be set by using two compare values on the same timer base, but by mirroring them symmetrically about the 50% MAXCOUNT value. The first PWM value signal was obtained from the PWM's channel 2 high pin and the second signal was obtained from the PWM's channel 1 low pin. It should be ensured that the PWM module is configured in complementary switching mode.

The 50% duty restriction can be enforced by a software duty lock that restricts the compare values to stay within range. Therefore, compare 1, shown in Figure 21 is always restricted above the 50% MAXCOUNT breakpoint while the compare 2 register's value is always restricted to stay below the 50% MAXCOUNT breakpoint.

## 5.5. VOLTAGE INSTRUMENTATION

A Tektronix<sup>®</sup> MSO-4054 B mixed signal oscilloscope was used for measuring various signals in the PPU. For measuring the high voltages from the CWVM stages and the MSW waveforms from the TPI and the HFT's secondary, THDP0100 high voltage differential probes and P5205 differential probes were used wherever appropriate.

The voltage is sampled by implementing an onboard potential divider as discussed in Section 5.2. The voltage is tapped from the half-tap (third stage) point on the positive CWVM so as to reduce the voltage stress across the pads of the resistive divider and prevent the probability of arcing. This difference in sampling points carries as a transportation delay in the sensed output and the controlled output due to the dynamics of the CWVM stages between the third stage and the sixth stage. As the negative and positive CWVM's are assumed to have same values and dynamics, controlling the positive CWVM will control the negative CWVM in the same sense.

## 5.6. LOADS

Two 620 k $\Omega$  resistors were connected in series to form a 1.2 M $\Omega$  effective resistance. Two of these resistor banks were used to load the positive and negative CWVM stages. The resistance values can deviate from their nominal depending upon the heat that they generate due to the high-voltage operation. It is advisable to have a coolant fan in the vicinity of these resistors to maintain the resistance value.

## 5.7. HIGH VOLTAGE SWITCHES

Two Kilovac K81C235 SPDT through hole type relays were used to switch the output terminal voltage at low frequencies. The relays were also controlled by a timer running in the dsPIC MCU. The switches were rated to withstand 10 kV DC and had a two million mechanical cycle limitation.

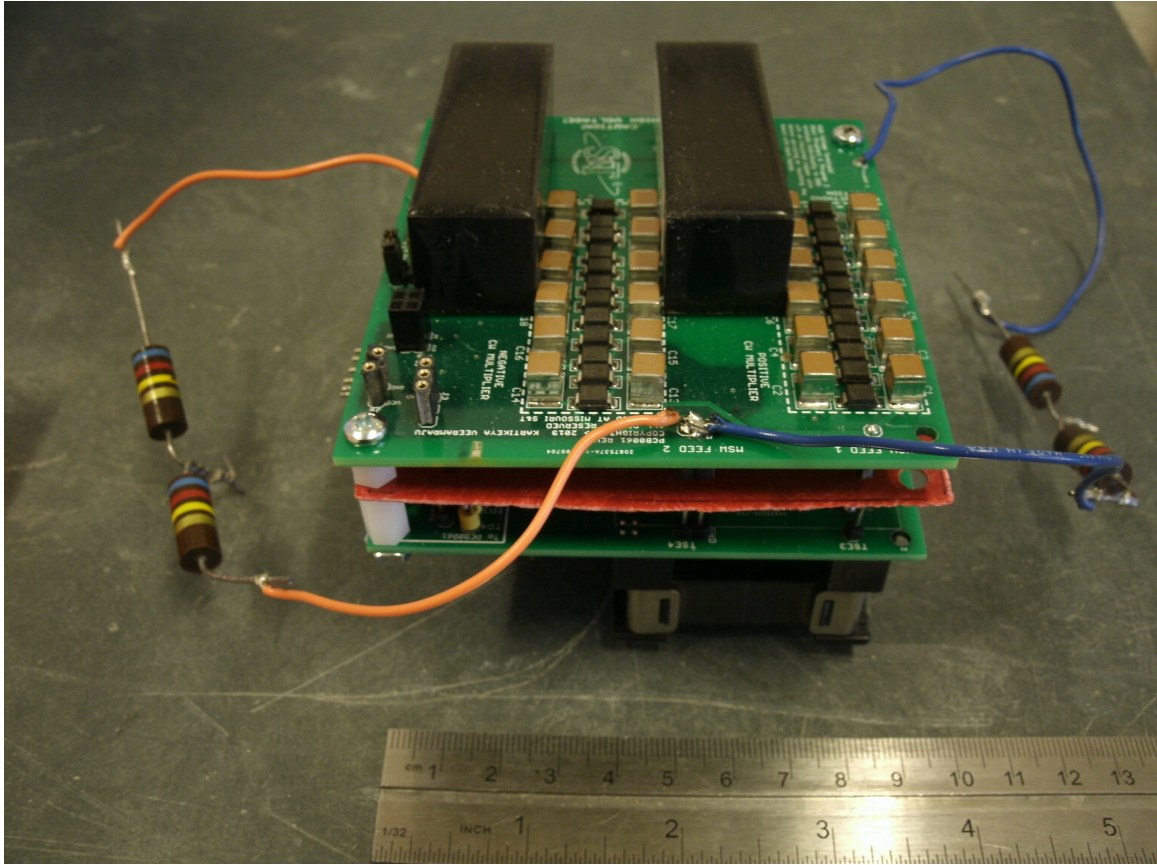


Figure 22. Prototype of the PPU Showing the Stacked PCB's

## 5.8. TEST CASES AND PROCEDURES

The converter is tested at various input voltages and duties and parameters such as voltage transfer, input power, output power, and efficiency are extracted from the readings.

To acquire the aforementioned parameters, the converter is run at different duty values and the corresponding input voltage, output voltage, input currents are measured and tabulated. The output power is calculated based on the output voltage and the load resistance values, which are carefully maintained constant by running each operating point for 5 s and noting the values at the end of the period. It is previously ensured that this 5 s time period is well above the settling time of the initial startup transient or intermediate online transient of the converter.

Table 1. Component Listing

Part No.	Ratings	Purpose
FQD18N20V2TM	200 V 15 A	TPI Stage MOSFETS
CKG-Series	1 $\mu$ F $\pm$ 20% 630 V	CWVM MLC Capacitor
GB01SLT12-214	1.2 kV 2.5 A	CWVM SiC Shottky Diode
K81C235	10 kV 5 A	SPDT High Voltage Switching Relay

The I<sup>2</sup>C interface is very useful when changes in duty are needed when the converter is online and also helps to monitor the PPU's parameters with considerable ease.

## 5.9. CLOSED LOOP CONTROLLER AND ARCHITECTURE

The PPU was run in closed loop control using a digital PI controller. The filtered analog feedback signal is sampled by ADC of the MCU at 62 Hz. The PI controller was implemented on a fixed point processor. The architecture of the fixed point DSP controller is shown in Figure 23. The controller constants and set point of the voltages are also set using the data communication interface over I<sup>2</sup>C and are writing to the internal RAM buffer, which serves as a shared data space between the MCU and the flight computer. The DSP running on fixed point computation computes the duty when the controller is activated and directly feeds the control duty value to the shadow buffers in the PWM peripheral, which take effect in the subsequent PWM timing cycle. The PWM module also provides the SOC trigger to the ADC block via a set prescaler. In order to make the data compatible with the fixed point processor used to implement the PI controller, Q point representation is used in the controller's firmware to accommodate fractional values and the actuation values are rescaled to duty values by appropriate bit shifts to ensure the values do not overflow. The 50% restriction is still enforced to ensure proper operation of the converter.

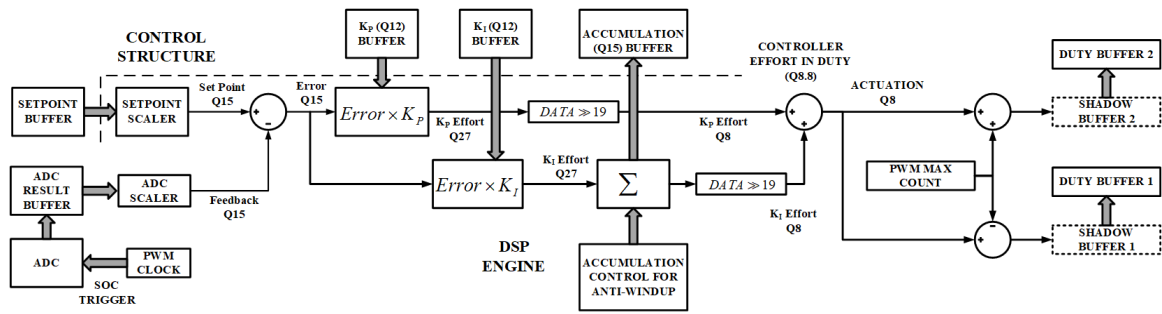


Figure 23. Fixed Point Controller Implemented on a dsPIC33F MCU

## 6. RESULTS AND DISCUSSION

### 6.1. OPEN LOOP CONTROL

The converter was run in open-loop mode at 100 kHz and the the voltage transfer at different input voltages was observed. The results of the voltage transfer test are shown in Figure 24. The dashed lines represent the output values computed using the mathematical gain expression. Theoretical gain and practical values match considerably, verifying the gain expression of the converter.

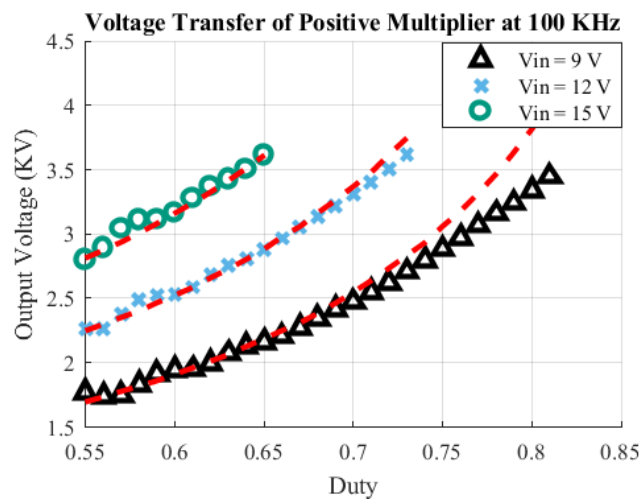


Figure 24. Voltage Transfer Curves for Various Input Voltages

The converter was run at 55% duty at 100 kHz with an input of 9 V to test the CCM operation of the TPI stage inductors as shown in Figure 25. The top two traces belong to gating signals of TPI MOSFETS (Scale: 5 V/div), the third trace belongs to the inductor one's current (Scale: 200 mA/div) while the fourth trace belongs to inductor two's current (Scale: 200 mA/div). The conditions ensured that the inductors were subjected to least possible frequency, duty and input voltage. This test proved the load referencing technique presented in Section 3 to be a reliable way of calculating the  $L_{crit}$  of the TPI stage inductors. Figure 26 shows the dsPIC's PWM waveforms and the resulting MSW feed in the TPI and HFT stages. The top two traces correspond to PWM switching signals generated by the dsPIC MCU, the third trace belongs to the TPI stage MSW, while the fourth trace is the HFT secondary side MSW. A ringing phenomenon was observed to be taking place at the edges of the MSW pulses in the primary and the secondary side of the HFT stage. This behaviour could be attributed to the ringing between the magnetizing inductance of the HFT's primary and the TPI side MOSFET's drain-source capacitance. The ringing could be removed by adding dissipative snubbers across each MOSFET's drain-source terminals.

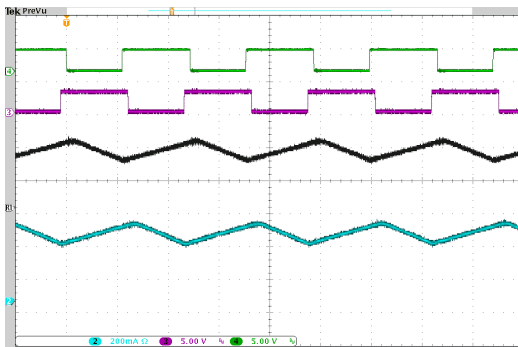


Figure 25. Inductor Current Waveforms at 55% Duty and 100 kHz

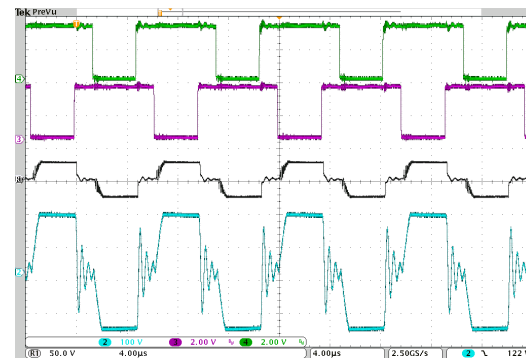


Figure 26. MSW Output of TPI and Secondary at 65% Duty at 9 V Input

The relay firing networks were run at 0.4 Hz, in complementary switching mode. Two relays were run in complementary mode as shown in Figure 27 at 5.16 kV P-P.

## 6.2. CLOSED LOOP CONTROL

The PPU was run in closed loop control and the voltages on the CWVM stage's full tap point, the half tap point and the feedback are shown in one scale for comparison in Figure 28.

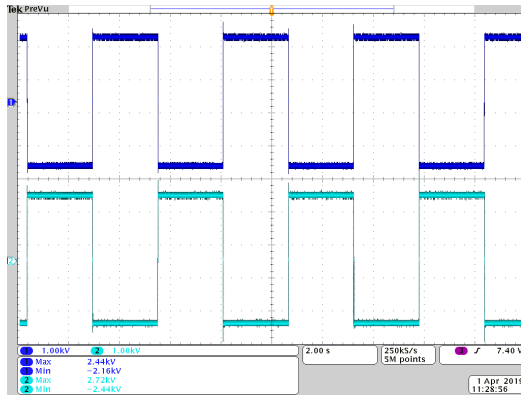


Figure 27. Filtered MSW

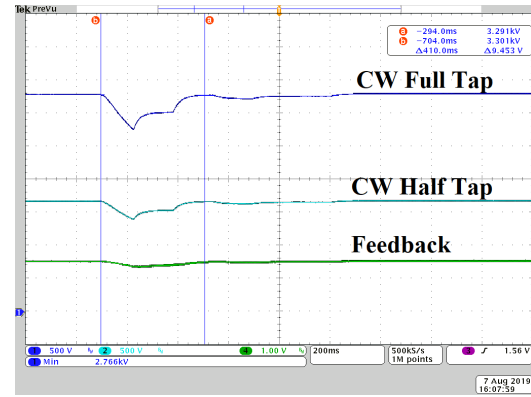


Figure 28. Full-Tap, Half-Tap and Feedback Signals for a Test Transition

**6.2.1. Closed Loop Control and Relay Switching.** In the first test, the controller was run in closed loop mode at a set point of 3.2 kV and the switching edges were inspected as shown in Figure 29. The relay switching causes a sudden rise in the CWVM's output voltage when the relay is switching over. The controller however is found to reject this short pulse due to the analog and the digital filters implemented in the feedback.

## 6.3. INPUT VOLTAGE DISTURBANCES

In the next test, the input voltage was changed and the converter was allowed to self regulate the output voltage. A transition from 12 V to 15 V when the set point was set at a value of 3.2 kV was tested. The performance of the controller under the specified conditions is shown in Figure 30. The voltage settled down in 102 ms and the peak voltage was observed to be 3.5 kV. Another test was conducted for a transition from 15 V to 12 V at the same set point. The performance of the controller is shown in Figure 31. The first

trace is the relay 1 output voltage, the second trace is relay 2 output while the third trace is the ac coupled input used for triggering the disturbance event. The voltage settled down to the set point in 130 ms and the valley voltage was 2.8 kV.

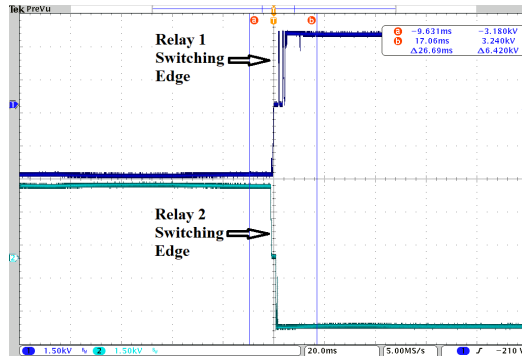


Figure 29. Closed-Loop Control and Regulation at Switching Edges

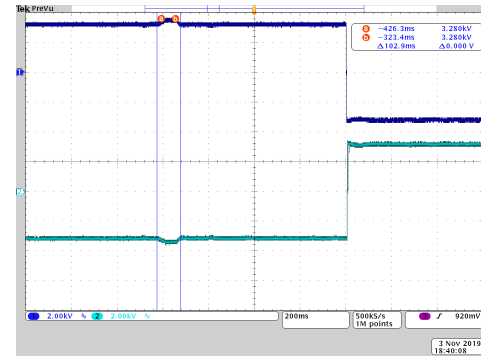


Figure 30. Voltage Regulation at a Supply Transition of 12 V to 15 V

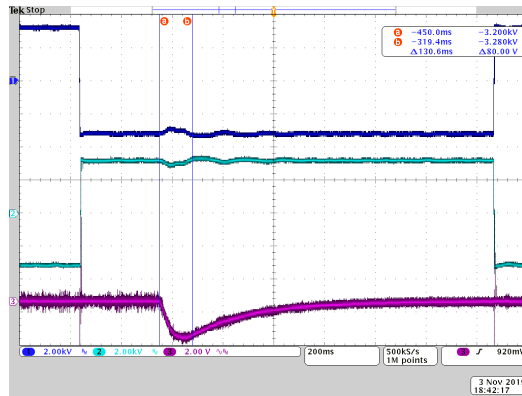


Figure 31. Voltage Regulation at a Supply Transition of 15 V to 12 V

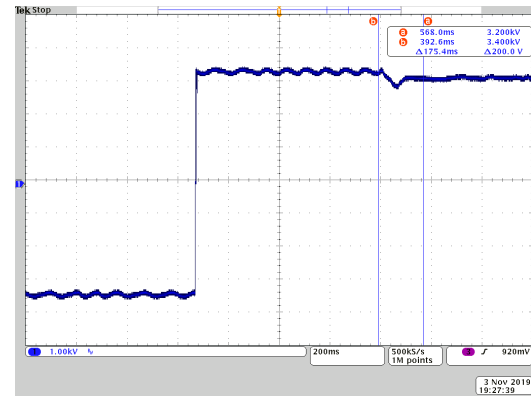


Figure 32. Response to Set Point Change from 3.4 kV to 3.2 kV

#### 6.4. REFERENCE TRACKING

The reference is changed over the I<sup>2</sup>C and can be considered as a step input to the converter. Figure 32 shows a set point change from 3.4 kV to 3.2 kV at a constant input voltage of 15 V. The PPU is observed to track the new reference accurately. Therefore the PPU can be set to any voltage within its trackable range and be made to regulate the voltage at a constant value under varying input voltages.



## 6.5. EFFICIENCY

The converter's efficiency plots are shown in Figure 33 for increasing duty and output power values. These values can be compared to 85.57%, 80.4%, 36%, and 88.5% reported by [2], [5], [7] and [14] respectively. The low efficiency in the converter could be attributed to MOSFET switching losses, drain-source capacitance charging losses, diode forward losses, magnetic component losses and diode reverse capacitance charging losses as characterized in [15].

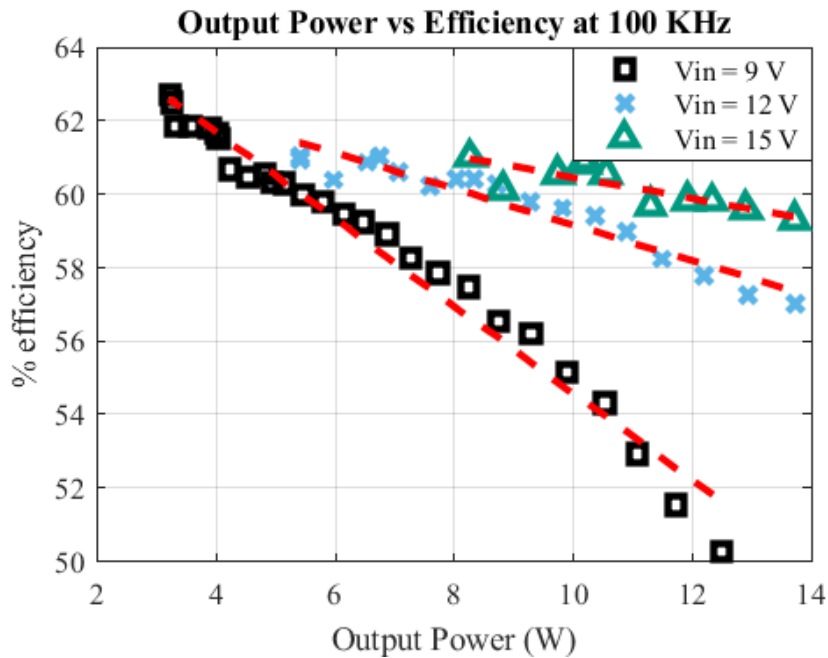


Figure 33. Output Power Versus Efficiency Plots of the Converter at Various Input Voltages

## 7. CONCLUSIONS

The converter presented in this paper is an improvement to the previous work done in the field of electrospray propulsion technology. The improved converter supports dual thruster operation, which is necessary to prevent spacecraft charging. Also, the converter can provide an alternating voltage to each thruster thereby ensuring the maintenance of

charge neutrality in the ionic propellant. The topology implemented in this paper is found to provide a ripple free voltage to the chassis-tied thruster, which was not previously achievable in a coupled inductor topology used in a chassis tied load configuration.

A hardware prototype of the converter was implemented and tested for various input voltages and duty values and the output voltage was quantified and analysed. The voltage transfer was found to be in agreement with the mathematical gain expression of the converter. The SPDT relays were tested at desired voltages in complementary modes and were found to be stably switching the output voltage at low frequencies. The proposed topology was found to be modular and could be redesigned for any desired voltage range.

The converter was finally run in a closed-loop mode by a digital PI controller implemented on the embedded system to enable the voltage tracking by feedback. Additionally, sources of noise in the feedback network are explained and a way to filter out such noise is realized. The resulting controller was then inspected at the relay switching edges and for varying input voltages for a preset tracking voltage on the high voltage outputs.

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## SECTION

### 4. SIMULATION STUDIES ON SPACECRAFT CHARGING PHENOMENON

Electrospray thrusters are used in satellite propulsion due to their high specific impulse and modularity. However, the operation of such a thruster would cause an unwanted buildup of charge on the body of the satellite, which would endanger the functioning of onboard electronics. Hence it is essential to quantify and study the rate of charge buildup in such a scenario. Simulation studies are performed on such a system using Matlab, and the charge buildup is assessed.

In this Section, a dual thruster operation is studied. This type of thruster configuration ensures a slower charge buildup when compared to a single thruster. This happens as both the thrusters are made to emit complementary ions, which neutralize after exiting the spacecraft, causing no net effective charge seen by the surrounding plasma. However, no two thrusters have matched emission characteristics due to manufacturing differences, which leads to a net non zero current being ejected out of the spacecraft, leading to a charge buildup. In order to curtail this, the roles of the thrusters are swapped periodically in order to compensate for the charge buildup, based on the assumption that a thruster emits equal current in both positive and negative emission modes.

#### 4.1. THRUSTER EMISSION MODELS

In order to characterize a thruster, one needs to know the mathematical expressions that approximately describe the operation of the emission modes. The operation of the electrospray thruster and the approximating empirical mathematical equations are delineated

in [5]. The mathematical expressions relate the applied voltage to the output thrust current exiting the spacecraft in the form of ions. The overall simulation model of the thruster is shown in Figure 4.1.

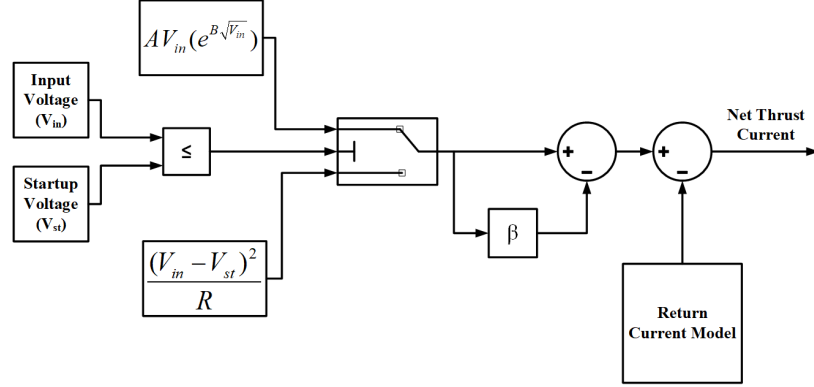


Figure 4.1. Single Thruster Model

**4.1.1. Emitter Current Model [5].** The emission model relates the voltage applied to the thruster to the current ejected out of the emitter tips. It has two emission models depending on the applied voltage, as shown in Equation 4.1.

$$I_e(V_{th}) = \begin{cases} AV_{th}e^{B\sqrt{V_{th}}}, & v < V_{str}. \\ \frac{(V_{th}-V_{str})^2}{R}, & v > V_{str}. \end{cases} \quad (4.1)$$

where,  $A$ ,  $B$  and  $R$  are curve fitting constants unique to a particular thruster.  $V_{th}$  is the applied voltage, and  $V_{str}$  is the startup voltage. The startup voltage is the voltage applied to the thruster that causes significant ionic emissions from the electrospray.

**4.1.2. Intercepted Current Model [5].** The intercepted current is defined by the scalar multiplier  $\beta$  that signifies the emitted current returning to the extractor grid without ejecting through it. Thus the intercepted current can be given by,

$$I_{int} = \beta I_e \quad (4.2)$$

**4.1.3. Return Current Model [5].** Return currents are caused due to the ions returning to the body of the satellite. These return currents cannot be included as a part of the thruster model as they depend on the spacecraft potential. The return currents can be computed as a function of the voltage of the satellite by a Retarding Potential Analyzer (RPA) explained in [5, 9].

RPA is a device that is used to assess the stopping potential required to repel all the ions emitted out of the electrospray. If the electrospray emits negative charges, the RPA should start applying a positive potential to repel all the emitted charges. When the RPA's potential is equal to the potential of the thruster, no ions are emitted out, which is interpreted as a capacitor that charges up as current gets ejected out of the electrospray. As the potential of the capacitor goes up, the current starts reducing, and an equal and opposite magnitude charge starts accumulating on the spacecraft's surface due to the opposite polarity ions remaining on the emitter. Due to the negative charge accumulating on the body of the satellite, all the ejected ions get attracted to the chassis and stay back. This process continues until the chassis potential reaches the applied potential, after which all the emitted current returns back to the chassis, and no effective ions are ejected out, leading to zero thrusts. The RPA data for a thruster is shown in Figure 4.2. The RPA data can be loaded as a lookup table, and a curve fit can be used to interpret the charge buildup. The voltage of the satellite is normalized with respect to the thruster voltage. This normalized voltage is then mapped to the corresponding normalized satellite potential and subtracted from unity to get the normalized return current. The charging model for a single thruster burn is shown in Figure 4.3. Based on the models and equations described in [5], a Simulink® model was developed for describing the emitter current for a single thruster. However, a single thruster can be made to work in both positive and negative emission modes owing to the phenomenon of electrospray. Hence a negative emission model can be achieved by just adding a negative unity gain block in the  $I\_Emitter$  signal.

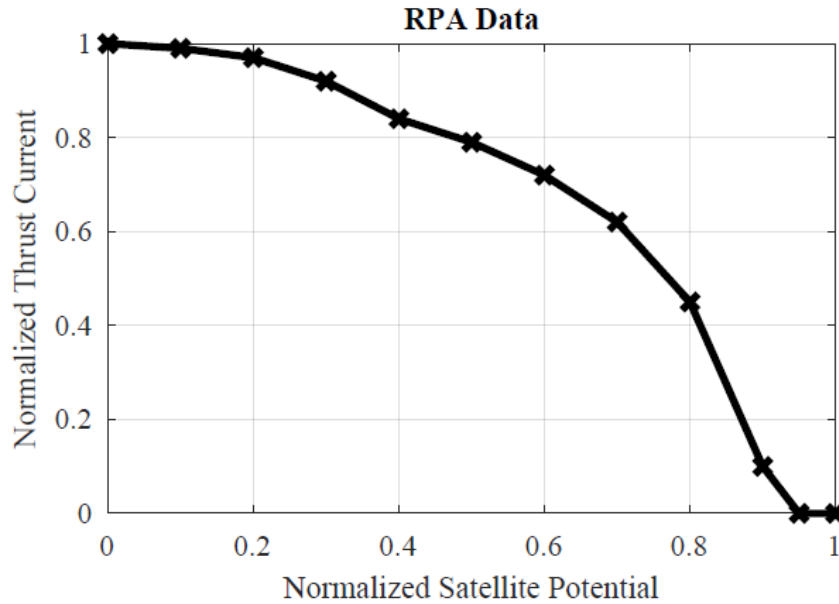


Figure 4.2. RPA Data for a Test Thruster [5]

Hence, the overall model for the thruster in both positive and negative ion emission modes is shown in Figure 4.4. In order to incorporate the second thruster, another copy of the thruster model depicted in Figure 4.4 has to be made. This will allow the usage of two different sets of thruster parameters for the two thrusters, which might crop up due to manufacturing differences. The final emission model for the two thrusters combinedly is shown in Figure 4.5. One can observe that the two models have a *enable* signal, which controls the emission mode of the thruster. Hence, it is complemented for the second thruster. The inputs to each thruster block are the return currents  $I_{Ret\_1\_1}$ ,  $I_{Ret\_1\_2}$  and the input voltage supplied by the PPU. The outputs of each block are the thrust and the output currents, which are clearly explained in [5].

**4.1.4. Spacecraft Charging Model.** Spacecraft charging occurs due to the residual charge left in space due to the unequal ion emission of the thrusters. Figure 4.3 shows the mechanism of the charge buildup on the spacecraft. In this study, the space plasma's effect on charging is not considered and is assumed to serve as an absolute 'ground' [5].

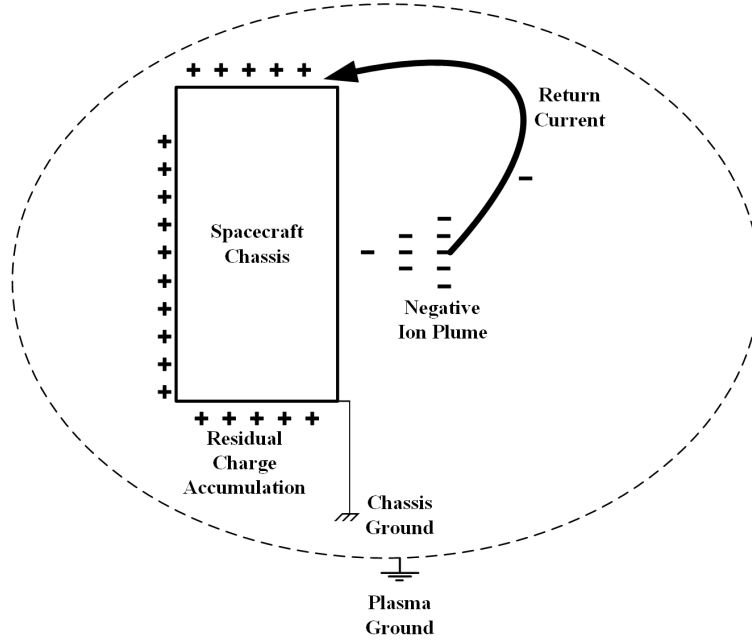


Figure 4.3. Charge Buildup Mechanism in a Single Thruster

Charging of a spacecraft can be explained by the charging of a parasitic capacitance between the spacecraft's body and the surrounding plasma. The value of such a capacitance is quantified in [6] and [10]. The capacitance of the spacecraft with respect to plasma is given by,

$$C_{sc} \approx 4\pi\epsilon_0 R_{sc} \left( \frac{R_{sc}}{\lambda} + 1 \right) \quad (4.3)$$

Where  $\lambda$  is the Debye length, a quantity that varies with the density of the plasma and the orbital altitude,  $R_{sc}$  the radius of the satellite in centimeters, and  $\epsilon_0$  the permittivity of free space, the value of the capacitance in this article is assumed to be 130 pF. The capacitor charges due to the effective thrust current exiting the spacecraft can be seen in Figure 4.6 that all the thrust currents (positive and negative) are summed before being fed to the charging model. This summation allows the residual charge to flow through the capacitance, causing the charge buildup. The end result of the computation is the voltage built up on the satellite  $V_{Sat}$ .



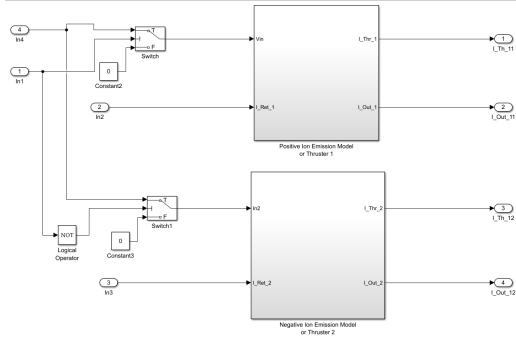


Figure 4.4. Single Thruster Model

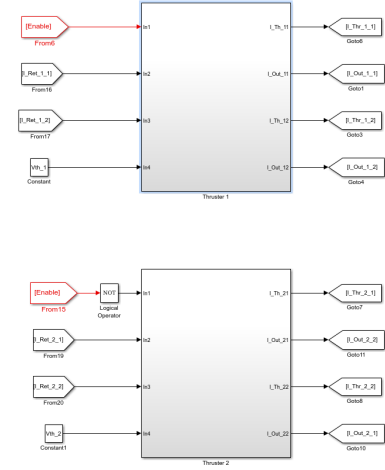


Figure 4.5. Dual Thruster Model

**4.1.5. Charge Control Strategy and EOL Calculation Model.** In order to constrain the voltage of the satellite within a certain window, the voltage has to be sensed, and a feedback loop has to be implemented. A hysteresis controller has been implemented to this end, and toggles the voltage of both the thrusters via high voltage relays connected to each of them. Since relays are subject to mechanical stress, the end of life of the relay can be assumed to the end of the mission. Hence it is essential to know the remaining lifetime of the PPU. A counter is used to sense the mode change and account for the switching action of the relay. This count is then subtracted from the preloaded switching lifetime of the relay to give the remaining number of switches before the end of life of the Power Processor Unit. This model assumes that the satellite voltage to the hysteresis controller is made available by either an estimator or an absolute sensor. Descriptions about such estimation/sensing mechanisms are out of the scope of this study.

A manual switch is added before the relay to ease the simulation process and has no real significance. For the hysteresis controller to work correctly, the satellite potential has to hit the negative threshold voltage first. If the voltage, for whatever reason, drifts

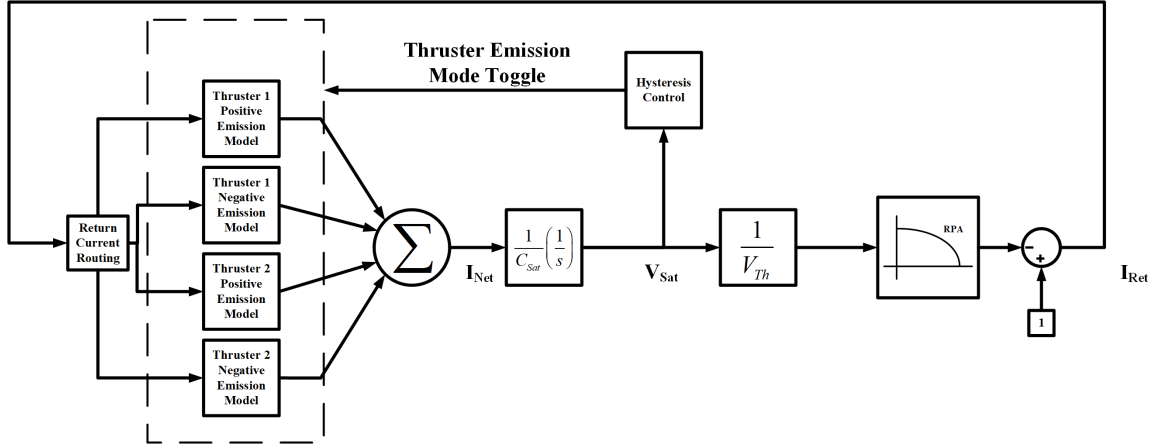


Figure 4.6. Spacecraft Charging and Return Current Model

to the positive side, the controller will not be able to control the toggling functionality as the positive threshold was not made active. The manual switch is to be used to invert the polarity of the voltage to hit the negative threshold first.

## 4.2. RESULTS AND DISCUSSION

**4.2.1. Test Parameters and Conditions.** In the following test, the relay switching frequency is computed with respect to the applied voltage when the satellite potential is constrained within a particular voltage window. This type of study is necessary to predict the mission time of the PPU and its utility. Hence the relay is assumed to be the weakest link in the system and all the reliability studies have been done with respect to it.

Some of the parameters under consideration for this configuration are the thruster constants, satellite capacitance, and voltage window of the satellite. The parameters of the thruster are taken from [5] and are again listed in Table 4.1 for convenience.

The thruster parameters are slightly different from one another, owing to the inevitable manufacturing differences. The number of switchovers is now counted using the simulation model for a charging window of 200 V and 500 V, and the frequency of switching is plotted against the applied voltage. The resulting graph is shown in Figure 4.7. The graph

Table 4.1. Thruster Parameter Set 1 from [5]

Parameter	Thruster 1	Thruster 2
A	1.075e-24	1.075e-24
B	1.173	1.173
R	430e+6	430e+6
Beta	0.01	0.014
Vstr (V)	915	910

helps to account for the response delay time of the thruster. If the delay time is known, and a particular charging window is selected, the operating voltage can be determined. This approach, however, limits the amount of producible thrust but safeguards the system from a possible malfunction.

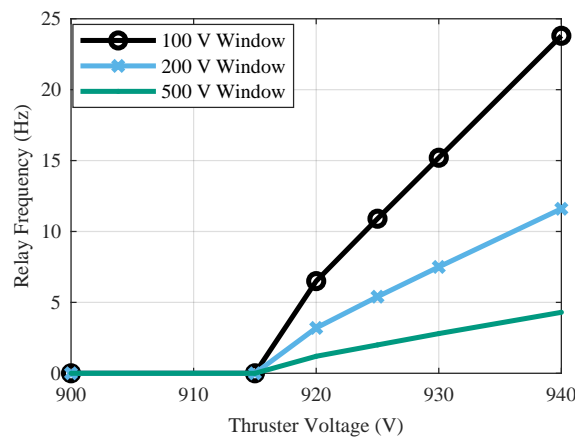


Figure 4.7. Relay Switching Frequency Variations with Applied Voltage

**4.2.2. Spacecraft Charging Dynamics.** This section deals with the charging of the satellite and how that affects the thruster switchover. The charging window is selected, and the thruster is fired for a period of one s, and various thrust current and spacecraft voltages are plotted for a particular window constraint.

**4.2.2.1. Test parameter set.** Figure 4.8 and 4.9 show the performance of the system when the thrusters are fired at 920 V and the parameters listed in Table 4.1 are enforced on the simulation model.

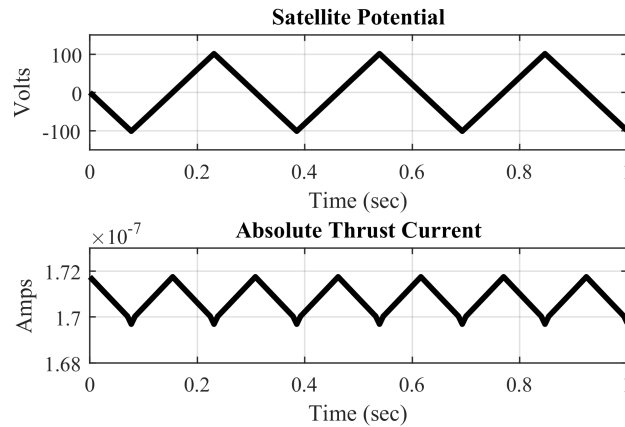


Figure 4.8. Charging Characteristics Induced by Thrusters Fired with Parameter Set in Table 4.1 for a Charging Window of 100 V

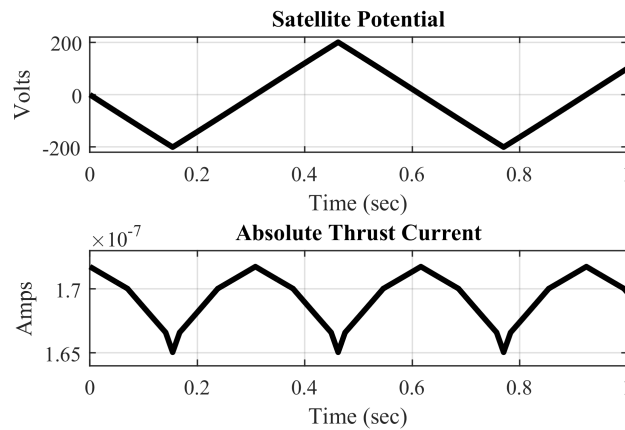


Figure 4.9. Charging Characteristics Induced by Thrusters Fired with Parameter Set in Table 4.1 for a Charging Window of 200 V

The number of transitions increases as the window is made more and more narrow, emphasizing the necessity to keep the thruster parameters as close as possible. Even a small change in the parameters causes a marked change in the charge/discharge dynamics of the spacecraft. If the relay is switched more often, the mechanical cycle limitation of the relay will be expended faster than the case where the relay is switched at a lower frequency. Therefore the thruster parameter matching effects the relay lifetime for a particular window constrain on the spacecraft's chassis.

### 4.3. CONCLUSIONS

A simulation model is developed for the dual electrospray thrusters, and the spacecraft charge buildup is assessed for such a system when fired at a particular voltage. The lifetime of the PPU is assessed, assuming the relay to be the weakest link. Also, the thruster parameters are to be pre-tested practically, and the curve fitting constants, namely:  $A$ ,  $B$ ,  $R$ ,  $\beta$ , and  $V_{str}$  are to be found out before incorporating into the model.

Finally, the spacecraft charging dynamics are assessed when the thruster is fired at a particular voltage, and the transitions in thruster parameters are plotted. This data is run for a set of thruster parameters, and the importance of parameter matching is recognized.

## **5. EMBEDDED FIRMWARE DESIGN AND BOARD LAYOUT CONSIDERATIONS**

In this Section, the firmware of the converter will be discussed, and particular emphasis on various peripheral configurations, interrupt structure, and controller design will be provided. A dsPIC33FJ128MC802 microcontroller will be used and referred to throughout the discussion of this chapter, and the firmware is explained with respect to the dsPIC's architecture and peripherals. The firmware was developed using the MPLAB X IDE, and a PICKIT 3 programmer was used to deploy the firmware onto the target hardware.

The chapter proceeds to discuss some of the unique design considerations to be adhered to while laying out a high voltage PCB and discusses the reasons behind the considerations. The discussion also includes the type of materials to be used to prevent various issues occurring in a high voltage PCB.

### **5.1. THE DSPIC33F MCU**

The dsPIC33F is a family of economical 16-bit fixed-point microcontrollers with essential DSP features for time-sensitive hardware applications. The processor features a 40 MIPS 16-bit DSP core with single-cycle MAC/MPY and MUL plus hardware divide features, which are essential for fast processing. The dsPIC33FJ128MC802 specifically has two 16-bit Motor Control Pulse Width Modulation (MCPWM) modules that support both complementary and similar outputs. The MCU also has five 10/12-Bit Analog to Digital (ADC) modules capable of 1.1 Msps. It also features essential communication interfaces such as UART, Two-Wire (I<sup>2</sup>C), SPI, and CAN interfaces. The MCU can be set to various interrupt priority levels based on the necessity and criticality of computations.

## 5.2. ARCHITECTURE OVERVIEW AND FIRMWARE STRUCTURE

The overall firmware structure of the PPU with an I<sup>2</sup>C interface is shown in Figure 5.1. The PPU manager is a program responsible for controlling the RAM buffer's data pointer index and controls the operation of all the peripherals of the MCU after they are initialized. The control structure is another part of the firmware that holds the data of the PI control parameters such as the KP, Ki constants, the filtered ADC value, error accumulation, setpoints, proportional effort, integral effort, and overall control efforts. These data points are used in the structure for on the fly access and are written to the RAM buffer locations when no other interrupt is active.

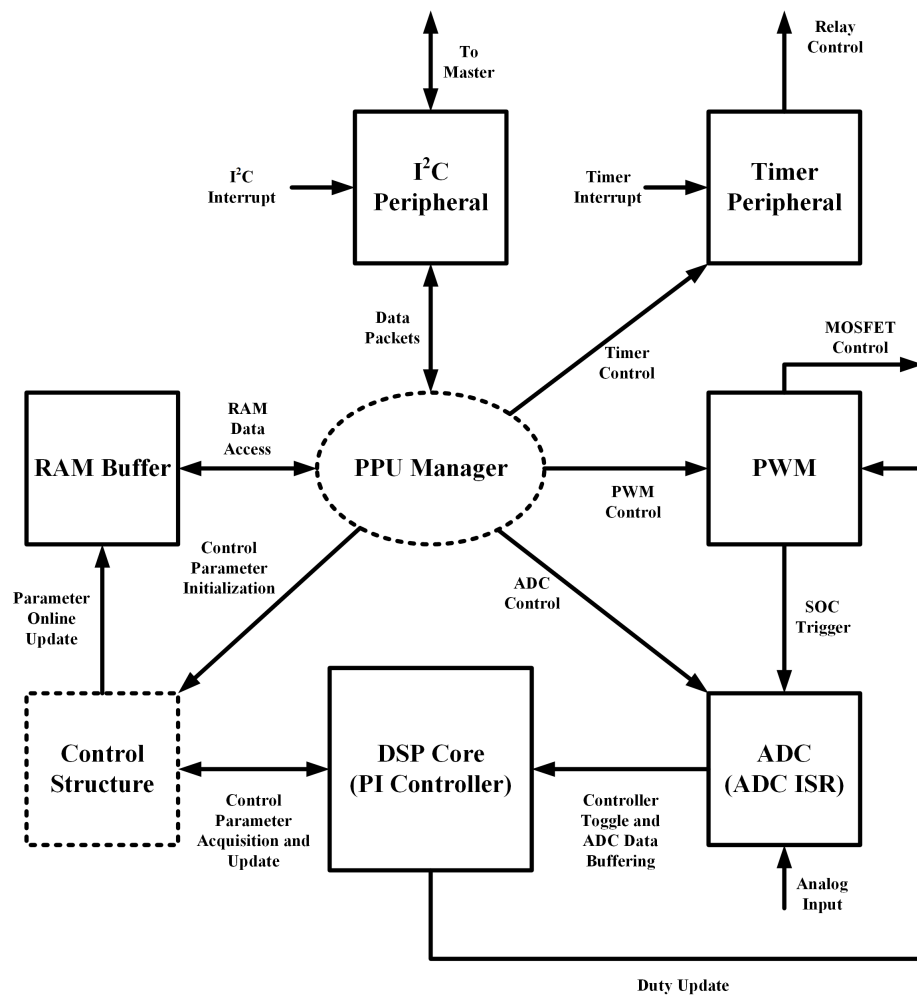


Figure 5.1. Firmware Structure

There are three interrupts running on the MCU, namely, the I<sup>2</sup>C Interrupt, the ADC interrupt, and the timer interrupt. The timer interrupt has the least priority as it is used to switch the relay signals at a very low frequency by toggling GPIO pins at the interrupt event. Whereas the ADC and the I<sup>2</sup>C interrupts run at 100 kHz. The ADC interrupt, in this case, assumes the highest priority, and the I<sup>2</sup>C interrupt assumes the next highest priority.

### 5.3. COMMUNICATION INTERFACE AND SLAVE DATA BUFFER

The Power Processing Unit uses an I<sup>2</sup>C Interface to enable communication between the flight computer and the PPU. In the context of the application, a Raspberry Pi was used as a master device controlling the dsPIC33F MCU onboard the PPU, which acts as the slave device.

The flight computer is responsible for sending various configuration words to the PPU to configure the MCU and make it function in desired modes. For the purpose of communication, the dsPIC is configured as an I<sup>2</sup>C slave, and the Raspberry Pi is configured as an I<sup>2</sup>C master.

A data buffer is declared in the dsPIC MCU to serve as a shared data space between the Raspberry Pi and the MCU. The structure of the RAM data buffer is shown in Figure 5.2

**5.3.1. General PPU Status and Configuration Locations.** Most of the locations of the RAM Data Buffer are used in pairs as the I<sup>2</sup>C interface is predominantly 8-bit. Hence 16-bit words are broken to 8-bit words and handled by the PPU Manager to control the read and write operations appropriately.

**5.3.1.1. RAW command.** The command the flight computer sends (needs to be translated by the slave device). This command serves as the command identifier for the PPU Manager to sequence the RAM pointer locations to extract the necessary data.

**5.3.1.2. Data write.** A general-purpose single-byte write field. Any single-byte reads are read off from this location.



General PPU Status and Configuration Locations	Controller Data Locations
Raw Command	Set Lo
Data Write	Set Hi
PPU Response	KP_Q12_Lo
ADC 1 Lo	KP_Q12_Hi
ADC 1 Hi	KI_Q12_Lo
ADC 2 Lo	KI_Q12_Hi
ADC 2 Hi	AD_Value_Lo
DSET Lo	AD_Value_Hi
DSET Hi	V Sense Q Lo
Duty Lo	V Sense Q Hi
Duty Hi	V Set Q Lo
Freq Lo	V Set Q Hi
Freq Hi	Error Q Lo
	Error Q Hi
	P Effort Q Lo
	P Effort Q Hi
	I Effort Q Lo
	I Effort Q Hi
	C Effort Q Lo
	C Effort Q Hi
	Accumulator Lo
	Accumulator Hi

Figure 5.2. Structure of the RAM Buffer Used for Communication Interfacing

**5.3.1.3. PPU response.** A reflection of the translated command or PING returned by the CPU post-register-processing; This location is also used to read the PPU Status Byte that signifies the status of various critical parameters.

**5.3.1.4. ADCx Lo and ADCx Hi.** Lo and Hi bytes of the ADC conversion results. These locations are directly modified right after reading the data of the ADC Result Buffers of channel x.

**5.3.1.5. DSET Lo and DSET Hi.** Used to override the current duty value of the PPU. Forces the closed-loop mode to open-loop when the closed-loop is active while the command invokes the PPU Manager. The flight computer restricts manual entry range from 51% to 90% to prevent damage to the PPU. The incoming data is directly loaded into the duty buffers of the PWM peripheral. The incoming duty values are preprocessed to load values by the flight computer before transmitting over I<sup>2</sup>C.

**5.3.1.6. Duty Lo and Duty Hi.** These locations update the current duty value of the PWM signal.

**5.3.1.7. Freq Lo and Freq Hi.** These locations correspond to PWM switching frequency settings. It is mostly used during initialization.

**5.3.2. Controller Data Locations.** The controller data locations are used to monitor the proper functioning of the closed-loop controller and modifying the parameters of the controller. When the controller is active, the byte locations pertaining to the controller get updated when the ISR is not running.

**5.3.2.1. Set Lo and Set Hi.** These locations correspond to set points. When written to these locations, the PPU manager automatically enforces the new set point on the controller, and the controller is made to track this reference. If the PPU is running in open-loop mode, writing to these memory locations has no effect and only takes effect when the controller is kicked into the loop.

**5.3.2.2. KP q Lo and KP q Hi.** These are the locations for setting the K<sub>p</sub> value of the PI controller. The flight computer expects these values to be in Q4.12 format.

**5.3.2.3. KI q Lo and KI q Hi.** These are the locations for setting the K<sub>i</sub> value of the PI controller. The flight computer expects these values to be in Q4.12 format.

**5.3.2.4. AD Value Lo and AD Value Hi .** The AD Value is the value acquired after running the raw ADC value through a filter in the MCU. This value is used in the controller whenever it is invoked in the Interrupt Service Routine (ISR).

**5.3.2.5. V Sense q Lo and V Sense q Hi.** These bytes store the filtered ADC value after the ADC Prescaler scales it. More details on ADC prescaling will be discussed in the details of the fixed-point implementation.

**5.3.2.6. V Set q Lo and V Set q Hi.** These bytes store the Setpoint values after the ADC scaler value scales them. More details on ADC prescaling will be discussed in the details of the fixed-point implementation.

**5.3.2.7. Error q Lo and Error q Hi.** These bytes store the Error computed by the dsPIC, after subtracting the Set Point q from the V Sense q.

**5.3.2.8. P Effort q Lo and P Effort q Hi.** The byte locations store the Hi and the Lo bytes of the proportional effort part computed by the PI controller.

**5.3.2.9. I Effort q Lo and I Effort q Hi.** The byte locations store the Hi and Lo bytes of the integrator effort computed by the PI controller.

**5.3.2.10. C Effort q Lo and C Effort q Hi.** The byte locations store the Hi and Lo bytes of the net effort computed by the PI controller after adding P effort and I effort.

**5.3.2.11. Accumulator Lo and Accumulator Hi.** The byte locations update the value stored in the accumulator of the integrator error.

## **5.4. PULSE WIDTH MODULATOR PERIPHERAL SETTINGS**

In this section, the settings of the Pulse Width Modulation Peripheral of the dsPIC MCU will be presented. The PWM module primarily needs the PWM timer load value and initialization duty. The values are extracted from the RAM buffer locations corresponding to duty and frequency running.

The PWM uses complementary output mode to meet the specifications of the TPI stage's PWM waveforms. The PWM modules are configured in up/down count mode, and two compare values are used symmetrically about half the MAX COUNT value of the

PWM counter, as shown in Figure 5.3. When the PWM module is run on complementary switching mode, the two PWM signals are obtained, one from the high pin and the other corresponding to the complement of the high pin for the Compare 2 value.

When the controller is active, the duty value is modified by the controller. The PWM peripheral is configured to update the duty only during a new interval and not during the current running interval. This method is known as shadowing, and the duty value gets updated when a new timing cycle in the PWM timer is initiated. Hence, when the controller writes the duty value to the duty cycle register, the value gets written to a shadow register, which updates the main register in the subsequent cycle. This feature can be invoked by writing a zero to the Immediate Update Enable (IUE) bit in the PWM control register.

The PWM module is also responsible for generating the Start of Conversion (SOC) trigger for the ADC. The signal can be generated in fractional multiples of the period. The SC trigger for the ADC can come from multiple sources, but in the context of this application is linked to the PWM module. The frequency of triggering can be controlled by Special Event output Prescale bits (SEVOPS) in the PWM control registers.

The duty load value for the  $PxTPER$  register for the PWM timer in Up/Down count mode is given by [16],

$$PxTPER = \frac{F_{cy}}{F_{PWM} \times PxTMRPrescaler \times 2} - 1 \quad (5.1)$$

where  $F_{CY}$  is the cycle frequency,  $F_{PWM}$  is the target PWM frequency, and  $PxTMRPrescaler$  is the prescaling factor for the PWM timer. The equation is implemented in the Raspberry Pi to calculate the timer load value and transmitted over I<sup>2</sup>C so that the frequency can be changed on the fly.

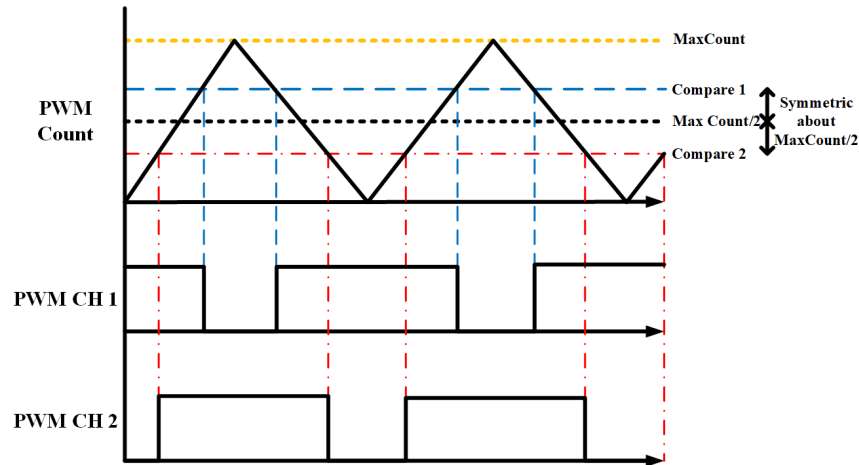


Figure 5.3. PWM Scheme for the TPI Stage

## 5.5. ANALOG TO DIGITAL CONVERTER PERIPHERAL SETTINGS

Analog to Digital converter is used to acquire the analog output voltage that is stepped down from the actual converter output via a set of resistors and a filter capacitor. The ADC needs a SOC trigger that can be directed from many sources such as self trigger, timer induced SOC, PWM induced SOC, externally induced SOC to name a few. In the context of the application, the SOC trigger is generated by the PWM module whenever it underflows, and the timer value is reset to start counting up.

The sense network's output scales the voltage in kilo-volt range to a maximum of 3.3 V for the ADC sensing. The prescaling factor for the sensor network was found to be 2239. This value was obtained after the MSW polluted signal in the output voltage was filtered with the help of the capacitor and applying a first-order curve fit to the range of high voltage inputs and subsequently sensing the low voltage outputs.

The ADC is also responsible to generate initiate the controller during the interrupt event so as to load the correcting duty to the PWM duty buffers when the controller is activated. If the controller is inactive, the ADC acts as a voltage monitor and updates the ADC value to the ADC lo and ADC Hi locations to enable voltage sensing in open-loop mode of operation.

## 5.6. FIXED POINT CONTROLLER IMPLEMENTATION

The fixed point controller's structure is shown again in Figure 5.4 for ease of reference. The controller acquires the ADC value and scales it to a Q15 number so that it is suitable for computation. The controller also takes the setpoint from the RAM buffer locations allocated for the set point. The values are scaled to a base voltage VBASE of 4 kV, which is chosen in such a way that the converter's output voltage is always less than the VBASE value.

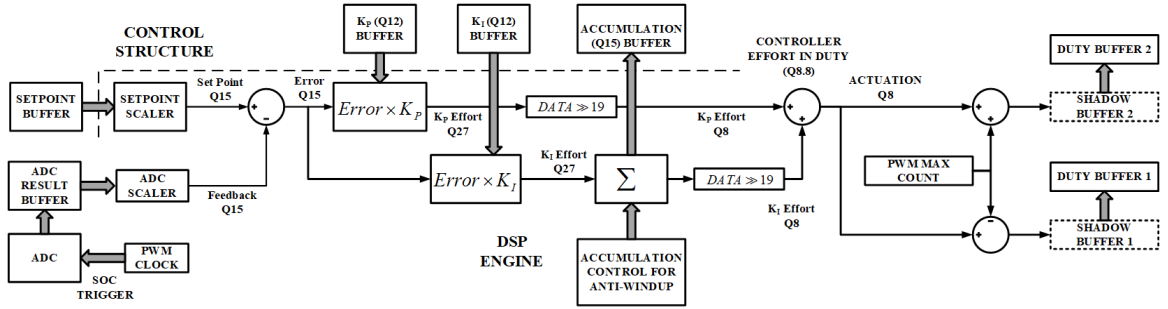


Figure 5.4. Fixed Point Controller

**5.6.1. ADC Scaling.** The setpoint is scaled in such a way that sense voltage, converted to a digital word, is normalized to the VBASE value specified in the earlier section. The first step involved in achieving the normalized voltage is to convert the sensed digital ADC value to a voltage from 0 V to 3.3 V. For a 12-bit ADC, the value is given by,

$$V_{sense} = \frac{ADValue \times 3.3}{2^{12}} \quad (5.2)$$

The value is then converted to the actual sensed voltage in KV by multiplying with the scaling factor of the voltage sense network, which was predetermined to be 2239 using the first-order curve fit technique. Hence the actual voltage converted to a Q15 number is given by,

$$V_{out_{Q15}} = \left( ADC\ Val \times \frac{3.3}{2^{12}} \right) \times \left( \frac{2239 \times 2^{15}}{4000} \right) \quad (5.3)$$

Equation 5.3 can be computed once during the initialization or can be defined as a constant and used anytime the scaler is to be multiplied with the sensed ADC value.

**5.6.2. Set Point Scaling.** The setpoint can be scaled by taking the value of the actual voltage and dividing it by the VBASE value and converting it to a Q15 number. It can be given by,

$$SetPt_{Q15} = \left( Set\ Point \times \frac{2^{15}}{4000} \right) \quad (5.4)$$

**5.6.3. Error Computation.** The error signal is computed by the difference of the sensed voltage and the setpoint voltage, which are in Q15 and referred to the same VBASE. Thus the quantities are subtracted using the assembly level subtraction instruction is the DSP core.

**5.6.4. Proportional Effort Computation.** The proportional effort is computed by multiplying the acquired error to a Kp constant, which in this case is defined to be a number in 4.12 format. The multiplication is again an inbuilt assembly-level DSP instruction. As a Q15 error is being multiplied by a Q12 number, the resulting multiplication is a Q27 number.

**5.6.5. Integration Effort.** The integration effort is computed by first accumulating the error using a running sum and then multiplying the error with the Ki value. Similar to the case of the proportional effort, the resulting integration effort is also a Q27 number.

The issue of the integrator anti-windup is solved by applying constraints on the accumulation of the error so that the maximum and minimum duty bounds are never violated.

**5.6.6. Computation of Net Effort.** The net error is computed by taking the summation of the proportional and integration efforts. However, before actually adding these two quantities, they should be shifted right by 19 bits to make them scale to the level of the PWM timer range. If this is not done, the duty values will overflow, and the operation of the converter will be indeterministic.

The PWM control signal is then generated by adding and subtracting the control effort to the PWM timer count value, as shown in Figure 5.3.

## **5.7. HIGH VOLTAGE PCB LAYOUT CONSIDERATIONS FOR AEROSPACE ENVIRONMENTS**

The PPU generates high voltages to interface with the Electrospray Thruster. The high voltages pose a significant challenge in designing the PCB's for the PPU. High voltages on small PCBs cause issues such as arcing, tracking, and partial discharges that cause failure in the insulation of the PCB material and insulation strength degradation between high voltage traces [18, 19, 22]. The boards being manufactured for satellite missions are mostly subjected to unfavorable aerospace environments, which are rich in plasma and radiation, which leads to the outgassing of insulators and plastics. Outgassing is of significant concern and causes drastic degradation of insulation strength and lifetime. For the reasons mentioned earlier, it is thus imperative on the part of a PCB designer to make the board aerospace grade by making it tolerant of outgassing and tracking issues.

The environment in a lower Earth orbit is classified as a low-pressure environment [5, 17, 18, 19, 20, 21, 22]. The environment is responsible for the initiation of the disruptive mechanisms that eat away into the insulator due to high voltages being impressed between the traces and the board's core and prepreg materials. Some of the discharge mechanisms relevant to insulation breakdown are described in the next section.

**5.7.1. Terminology of Breakdown Mechanisms.** The definitions of various breakdown mechanisms, according to [23] are quoted below.



- **Corona:** "Luminous usually localized discharge with a low current flow due to a deionization release of energy. Typically a "point" breakdown with a negative electrode and a "film" breakdown with a positive electrode" (Battel, 2012, p.27)
- **Discharge:** "Any conducting mechanism between two electrodes separated by a dielectric." (Battel, 2012, p.27)
- **Flashover:** "A discharge around or over the surface of a liquid or solid dielectric." (Battel, 2012, p.27)
- **Partial Discharge:** "Localized discharge due to transient gaseous ionization within an insulating system typically due to gaps or voids in combination with a dielectric transition." (Battel, 2012, p.28)
- **Tracking:** "Development of conducting channels primarily on a dielectric surface where the surface is damaged by the process." (Battel, 2012, p.28)
- **Treeing:** "A cumulative failure where hollow channels branch slowing through a dielectric material resulting in permanent failure." (Battel, 2012, p.28)

## 5.8. FACTORS AFFECTING CORONA AND PARTIAL DISCHARGES

High voltages across closely spaced components can initially cause partial discharges and Corona, which can deteriorate into treeing and tracking, thereby leading to a cumulative failure of critical parts of the PCB [18, 19, 22].

Additionally, Corona starting voltage is found to be a function of pressure surrounding the traces being subjected to high voltages [17, 20, 21], implying that the Corona Starting Voltage presents a similar behavior to that of Paschen's Law. Therefore as the altitude of the environment increases, the Corona Starting Voltage decreases and reaches a minimum and then increases as the pressure continues to decrease. Therefore, even if the board exhibits reasonably good performance in withstanding the high voltage stress on the ground and

when subjected to the atmospheric pressure, the board could still suffer from Corona and partial discharges at high altitudes for the same conditions of operation. Figure 5.5 shows Cockcroft Walton Voltage Multiplier's capacitor pads that suffered from treeing.

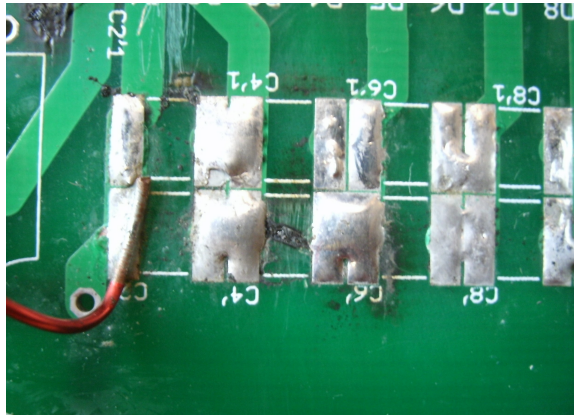


Figure 5.5. Capacitor Pads Belonging to a Cockcroft Walton Multiplier Stage that Suffered from a Partial Discharge and Subsequent Treeing

The selection of PCB materials also affects the dielectric properties of the insulation and the corona withstand capability of the PCB. The Corona properties can quickly destroy the insulation properties of organic compounds if the materials cannot withstand the fields.

The geometry and construction of the board traces and clearances plays a crucial role in the dielectric withstand capability of the board. Sharp edges cause a magnification of electric field at the edge and can initiate a partial discharge/ corona discharge even if the voltage is not at the Corona startup voltage.

## 5.9. BOARD LAYOUT CONSIDERATIONS TO PREVENT BREAKDOWN

**5.9.1. Material Selection.** The core and prepreg material selected for the board design should have less porosity and outgassing properties as they increase Corona and Partial Discharges. Selecting a high Comparative Tracking Index ( $CTI \geq 3$ ) solder mask with multiple overcoats can be another way to increase the voltage withstand capability

between traces and pads [18]. Adding a conformal coating over the surface of the high voltage pads can prevent surface tracking. However, the conformal coating should be aerospace grade.

**5.9.2. Board Layout Considerations.** The board should be laid out with careful considerations for trace clearances, pad geometry, and trace edges. IPC 2221 Standards provide a general guideline for safe clearances between PCB traces for an FR4 material to prevent tracking.

IPC 2221 standard categorizes trace placement on a board in seven categories namely,

1. B1 - Internal Conductors
2. B2 - External Uncoated Conductors sea level to 3050 m
3. B3 - External Uncoated Conductors over 3050 m
4. B4 - External Conductors, with permanent polymer coating
5. A5 - External Conductors with conformal coating over assembly (any elevation)
6. A6 - External Component lead/termination, uncoated, sea level to 3050 m
7. A7 - External Component lead termination, with conformal coating (any elevation)

Among the listed categories, IPC2221 reports category B1 to exhibit the lowest clearance of  $0.0025 \text{ mm V}^{-1}$  between two traces. This would imply high voltage traces being sandwiched between the board layers (second layer or the third layer). Sharp corners are to be avoided on high voltage traces to avoid field concentration and subsequent breakdown of insulation due to localized tracking. The solder pads corresponding to high voltage components should have rounded corners to prevent breakdown.

In order to further decrease the arc probability, the PCB core material is milled between pads subjected to high voltages. This is done in order to increase the tracking distance between the surface mount pads.

Based on the techniques mentioned above, the high voltage PCB's with the Positive and Negative CWVM stages was constructed as shown in Figure 5.6 and the fabricated PCB is shown in Appendix B.

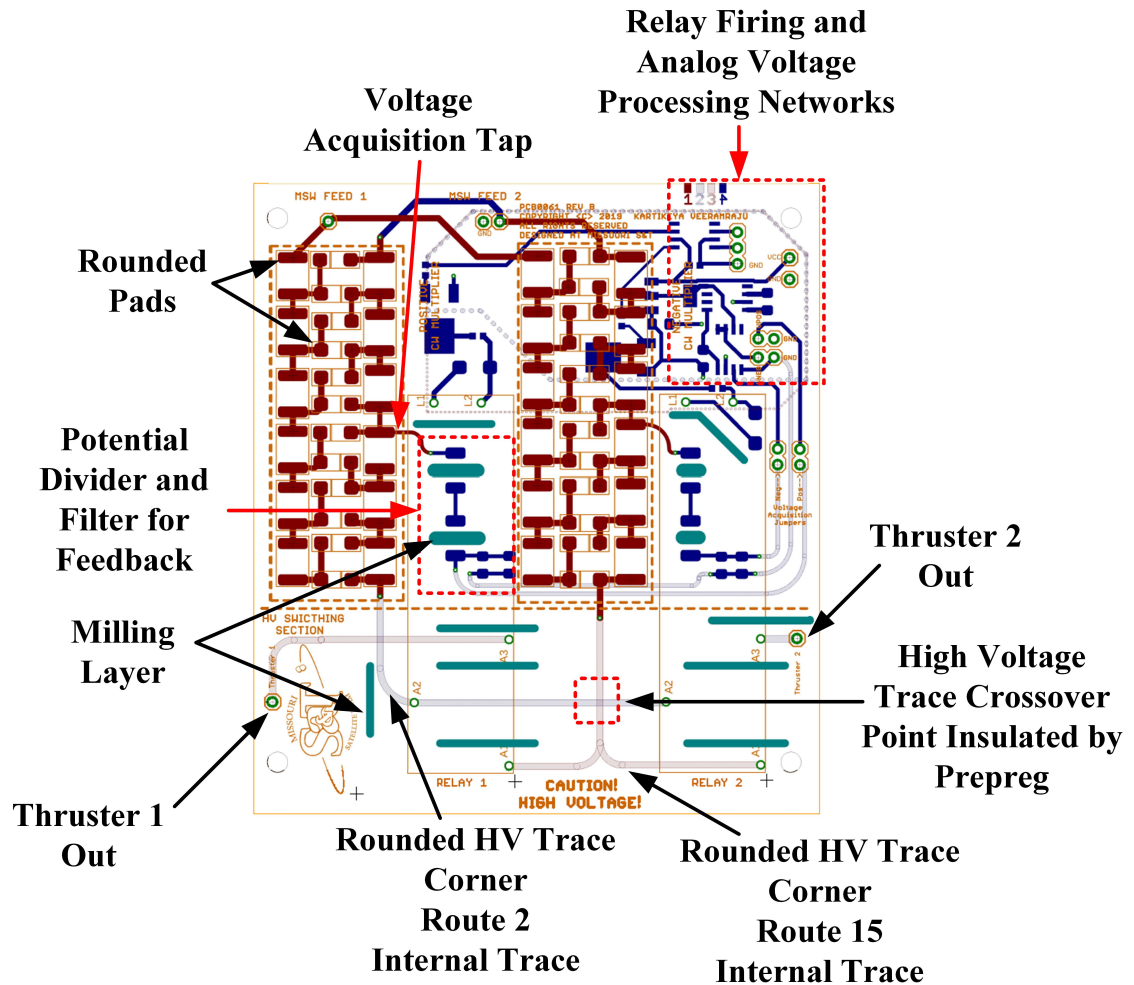


Figure 5.6. High Voltage PCB Layout

## 6. CONCLUSIONS AND FUTURE WORK

### 6.1. SUMMARY

In this work, the design and development of a multi-mode mono-propellant electrospray thruster system are investigated, with particular emphasis on topological analysis, match to industry standards, and hardware implementation.

The designed PPU was required to be compatible with the multi-mode thruster system in various aspects, primarily in aspects of bipolar high voltage generation, groundability, induced spacecraft charge alleviation, and self-regulation of voltage by closed-loop operation under degrading battery voltage.

The significant challenges in the development of such a PPU were found to be the ability to boost voltage to kilo-volt ranges in minimal form factors while regulating the voltage within an acceptable output window. Another major challenge was to alternate the generated high voltage output periodically at low frequencies to allow propellant charge neutrality and curb charge buildup. The high voltage generated by the PPU had to be sensed and fed back to the embedded system to allow voltage tracking by voltage mode control, which presented a challenge in stepping down and filtering the signal being fed back.

A three stage cascaded booster with Two Phase Interleaved Boost Converter, a High Frequency Transformer and Cockcroft-Walton Voltage Multiplier was designed and run at the target voltage spec of  $\pm 3.4$  kV, while switching at low frequencies. The converter was analysed for its output voltage and component sizing aspects and compared to its practical performance. The converter was observed to be within the theoretical steady state specs, described by the mathematical steady state relations.

The closed-loop voltage control of the converter was achieved by using potential dividers with high step-down ratios and filter capacitors. The stepped down voltage was fed back to the embedded system, on which a digital PI controller was implemented and controller's structure in fixed-point implementation was explained. The embedded firmware was built around a dsPIC33F MCU and special focus to a communication interface developed around an I<sup>2</sup>C protocol was explained. The communication interface enabled safe control of the converter and integration with a flight computer.

The Aspect of spacecraft charging was discussed with particular emphasis on charging induced due to the operation of electrospray thrusters. It was observed that the spacecraft's chassis charges up with respect to the surrounding space plasma and reaches high voltages. This voltage build up may lead to disruption of onboard electronics and also cause net zero thrust in thruster system. In order to curb this unwanted phenomenon, a dual thruster system was proposed and literature and a framework was built to assess the spacecraft charging due to this

Finally the high voltages generated by the PPU had to be withstood by the PPU's PCB and various types of breakdown mechanisms in a PCB material were explained to this end and the factors affecting this breakdown in context to an aerospace environment were described. The Lower Earth Orbit was characterized to be a low pressure, ion and radiation rich environment which could induce Corona and Partial Discharges in a High Voltage PCB, which ultimately led to treeing of PCB Core thereby completely damaging it. Proper selection of PCB materials, special attention to trace layout and usage of conformal coats was found to be a way to curb the ill effects of high voltage impression on PCB's in aerospace environments. The high voltage arcing probability between high voltage points and traces on the high voltage PCB was further decreased by milling slots on the surface of the PCB, which increased the creepage path for an arc to form.

## 6.2. FUTURE WORK

Although the converter provides the target voltage at the input voltage range, the conversion efficiency was experimentally found to be around 65%. The low efficiency is attributed to losses in magnetics, mainly due to skin and proximity effects in the transformer. Switching losses in the TPI MOSFETs, CWVM charging losses, and ESR losses could also add up to further lowering of the efficiency. An exact breakdown of these losses could lead to the improvement of the overall converter efficiency, which could be a possible direction to venture in the future. The overall size of the PPU is further reduced by employing planar magnetics, in order to reduce the height and increase the overall power density of the converter, which might also be another paradigm to venture in.

The converter was not run on the target thruster to assess its performance. In the future work, the PPU must be run on the actual multi-mode thruster in order to validate the results of the spacecraft charging and compatibility of the overall PPU with other subsystems on the satellite.

Furthermore, it is realized that the high voltage could be achieved with numerous topologies belonging to the class of high gain dc-dc converters, that generally lead to a more compact, more efficient and highly reliable PPU's could lead to further research in this field.

## **APPENDIX A.**

### **EMBEDDED FIRMWARE**



## 1. PWM PERIPHERAL

### 1.1. PWM INITIALIZATION

```

/*****
DESC: Initializes the PWM module with a set frequency in up/down count
      mode
INPUT: Target PWM_Frequency, calling_function_identifier
RETURNS: Nothing
CAUTION: Make sure that the frequency is within reasonable limits of the
          MOSFET being used.
* Make sure that this function is being called everytime the PWM
  frequency changes, in order to
* re calculate the time step of the controller and also change the
  frequency
*****/

void PWM_init(uint32_t PWM_freq,uint8_t called_from)
{
    control_vars_t *struct_p;
    struct_p = Export_struct_vars();    //import the controller
        structure pointer
    //unsigned int *remainder;
    if(called_from == MAIN)
    {
        temp = (FCY/PWM_freq);//__builtin_divmodud(FCY,PWM_freq,
            remainder);//(FCY/PWM_freq);
        temp = temp>>1;
        temp = temp-1;
    }
    else if(called_from == PPU_MGR)
    {

```

```

    temp = PWM_freq; //directly give the load value as the incoming
        data from master is actually the load value
    temp_PWM1 = (FCY)/((uint16_t)(temp+1));
    temp_PWM1 = temp_PWM1>>1; //now temp1 has the actual pwm
        frequency
}

P1TCONbits.PTEN = 0; //disable timer
P1TCONbits.PTOPS = 0b0000; //pwm time base postscale bits set o 1:1
    postscale
P1TCONbits.PTCKPS = 0b00; //1:1 prescaler
P1TCONbits.PTMOD = 0b10; //up/down mode
P1TPER = (uint16_t)temp;

PWM1CON1 = 0x0000;
PWM1CON1bits.PMOD1 = 0; //PWM 1 on complementary output mode
PWM1CON1bits.PMOD2 = 0; //PWM 2 on complementary output mode
PWM1CON1bits.PEN1H = 1; //enable PWM1H1as pwm output
PWM1CON1bits.PEN1L = 1; //enable PWM1L1 as pwm output
PWM1CON1bits.PEN2H = 1; //enable PWM1H2 as pwm output
PWM1CON1bits.PEN2L = 1; //enable PWM1L2 as pwm output

P1OVDCON = 0x0F0F;
PWM1CON2 = 0x0000;
PWM1CON2bits.UDIS = 0; //updates enabled
PWM1CON2bits.IUE = 1; //shadow updates
P1SECMpbits.SEVTDIR = 0; //special event counting up
P1SECMpbits.SEVTCMP = 1; //special event compare value
PWM1CON2bits.SEVOPS = 0b1111; //ADC conversion once every 16 cycles
if(called_from == MAIN)
{
    interrupt_frequency = (PWM_freq/PWM1CON2bits.SEVOPS);
    struct_p->dt_q = 32768/interrupt_frequency; //convert the
        interrupt frequency to a Q15 number

```

```

    }
    else if(called_from == PPU_MGR)
    {
        interrupt_frequency = (temp_PWM1/PWM1CON2bits.SEVOPS);
        struct_p->dt_q = 32768/interrupt_frequency; //convert the
            interrupt frequency to a Q15 number
    }
    //IFS3bits.PWM1IF = 0;      //Clear MCPWM flag
    //IPC14bits.PWM1IP = 0b111; //Set to highest priority
    //IEC3bits.PWM1IE = 1;      //Enable Interrupt request
}

```

---

## 2. ADC PERIPHERAL

### 2.1. ADC INITIALIZATION

```

/*****
DESC:      Initializes ADC in specified mode
INPUT: Mode Selection
RETURNS: Nothing
CAUTION: Make sure mode is specified while calling the function
*****/

void adc_init(uint8_t mode2)
{
    control_vars_t *struct_p;
    //import the controller structure pointer
    struct_p = Export_struct_vars();
    filter_out = 0; //initialize filter value to zero
    AD1CON1 = 0; // Clear control registers
    AD1CON2 = 0;
    AD1CON3 = 0;
    AD1CHS0 = 0x0000; // Channel select AN0

```

```

//TRISBbits.TRISB0 = 1; //set AN2 pin as input
TRISBbits.TRISB1 = 1; //set AN3 pin as input
AD1CON1bits.ADON = 0; //ADC1 disabled
if(mode2 == BIT10)
{
    AD1CON1bits.AD12B = 0; //10 Bit ADC
    adc_mode(mode2);
    struct_p->ADC_Max = 1024; //for controller computations
}
else if(mode2 == BIT12)
{
    AD1CON1bits.AD12B = 1; //12 Bit ADC
    adc_mode(mode2);
    struct_p->ADC_Max = 4096; //for controller computations
}
AD1PCFGL = 0xFFFF;
AD1PCFGLbits.PCFG3 = 0; //enable an3 as an analog input
//AD1PCFGLbits.PCFG2 = 0; //enable an2 as an analog
AD1CON2bits.VCFG = 0b000; //VrefH = AVDD AND VrefL = AVSS
//Always starts filling the buffer from the start address
AD1CON2bits.BUFG = 0;
AD1CON2bits.CSCNA = 0; //Do not scan inputs
AD1CON3bits.ADCS = 9; //Clocking (to be verified)
AD1CON3bits.SAMC = 15; //Auto sample time bits set to 1.TAD
                        //(to be checked))
AD1CSSL = 0; // Select AN0 for input scan
AD1CHS0bits.CH0SA = 3; //Channel 0 positive input is AN3
//AD1CHS0bits.CH0SA = 2; //Channel 0 positive input is AN2; comment
    for M3
AD1CON2bits.CHPS = 0b00; //Using Channel 0 for ADC
AD1CON1bits.SSRC = 0b011; //Use MCPWM as SOC trigger source
AD1CON2bits.SMPI = 0b0000;
//generates an interrupt after every sample and

```

```

    //conversion operation (every 16 clock cycles
    //in this instance)
    AD1CON1bits.ASAM = 1; //auto sampling enabled
    AD1CON1bits.FORM = 0b00; //Unsigned integer formatting
    //AD1CON1bits.SAMP = 0;

    PWM_timer_count = get_PWM_timer_count();
}

```

---

## 2.2. ADC INTERRUPT

```

/*****
DESC:  ADC interrupt service routine fired by the PWM timer overflow
INPUT: Nothing
RETURNS: Nothing
CAUTION: Make sure the interrupt mask and priority bits are set
         appropriately
*****/

void __attribute__((__interrupt__, no_auto_psv)) _ADC1Interrupt(void)
{
    control_vars_t *struct_p;
    struct_p = Export_struct_vars(); //import the controller
        structure pointer
    while (!AD1CON1bits.DONE); //wait for conversion
    temp1 = ADC1BUF0;
    //adc_filter();
    temp2 = temp1*get_PWM_timer_count(); //to enforce the 50% duty
        restriction
    temp2 = temp2>>mode;
    RAMBuffer[ADC1_LO] = temp1;
    RAMBuffer[ADC1_HI] = (temp1>>8);
    //update RAM_Buffer every cycle
    adc_temp = get_ADCVals(CH2);

```

```

RAMBuffer[ADC2_LO] = filter_out;
RAMBuffer[ADC2_HI] =(filter_out>>8);
if(struct_p->controller_status == INACTIVE && PWM1CON2bits.UDIS ==
    0) //update duty only when updates are enabled and controller is
    inactive (openloop mode)
{
    temp1 = get_PWM_timer_count() - (uint16_t)temp2;
    PWM_modify_duty(CH1, (uint16_t)temp1);

    temp1 = get_PWM_timer_count() + (uint16_t)temp2;
    PWM_modify_duty(CH2, (uint16_t)temp1);
}
else if(struct_p->controller_status == ACTIVE && PWM1CON2bits.UDIS
    == 0) //call the controller if the controller is turned active (
    closed loop mode)
{
    i = i+1;
    if(i >= 100)    //interrupt frequency = PWM_FREQ/(16*i)
    {
        compensator();
        i = 0;
        comp_duty = struct_p->Controller_effort_q;
        temp1 = get_PWM_timer_count() - comp_duty;
        PWM_modify_duty(CH1, (uint16_t)temp1);
        temp1 = get_PWM_timer_count() + comp_duty;
        PWM_modify_duty(CH2, (uint16_t)temp1);
    }
}
IFS0bits.AD1IF = 0; // clear ADC interrupt flag
}

```

---

### 3. CONTROLLER

#### 3.1. CONTROLLER DATA STRUCTURE

```
//control variables structure
//this is a shared resource, which can be accessed by other files by
    pointers

typedef struct
{
    uint16_t dt_q;           //the time step of the sampler. It is the
                             reciprocal of interrupt frequency. See pwm.c to know how its
                             calculated
    uint16_t ki_q_ram;
    uint16_t kp_q_ram;
    int16_t error_q;         //error to the PI controller in Q15
    uint16_t I_effort_q;     //total integral effort in Q15
    uint16_t P_effort_q;     //total proportional effort in Q15
    uint16_t Controller_effort_q; //total controller effort in Q15
    uint16_t Set_pt_q;       //current set point in Q15
    uint16_t ADC_Max;        // assigned by the adc_init function. See
                             adc.c for details
    uint16_t ad_val;         //the actual ad_value given out by the
                             filter. See adc.c for the filter function
    uint8_t controller_status;
    uint16_t v_sensed_q;
    uint16_t duty_load;
    uint16_t error_accum;
    uint16_t error_accum_max;
    uint16_t error_accum_min;

} control_vars_t;
```

---

### 3.2. DIGITAL PI CONTROLLER

```

/*****
DESC:  Initializes the DSP engines core functions
INPUT: nothing
RETURNS: nothing
MODIFIES: CORCON register
CAUTION: Know what you are doing! These setting are extremely important.
         Reverify before making any changes.
*****/

void controller_init(void)
{
    CORCONbits.US = 0; //DSP engine multiplications are signed
    CORCONbits.IF = 1; //DSP engine in integer mode (Q15 mode)
    CORCONbits.ACCSAT = 0; //supersaturation mode disabled (1.31
        saturation). Guard bits active
    CORCONbits.RND = 1; //convergent rounding
    //clear aReg
    aReg = __builtin_clr();
    control_struct.error_accum = 0;
}

/*****
DESC:  PI controller Implementation
INPUT: nothing
RETURNS: nothing
MODIFIES: control structure
*****/

void compensator(void)
{
    PORTBbits.RB4 = 1;

    kp = (RAMBuffer[KP_Q12_LO] | (RAMBuffer[KP_Q12_HI]<<8));
    ki = (RAMBuffer[KI_Q12_LO] | (RAMBuffer[KI_Q12_HI]<<8));

```



```

//__builtin_nop();

//compute the sensed voltage

//control_struct.v_sensed_q = __builtin_muluu(control_struct.ad_val
    ,ADC_SCALER_q);

//control_struct.v_sensed_q = control_struct.ad_val*ADC_SCALER_q; //
    sensed volts in Q15

control_struct.v_sensed_q = adc_filter()*ADC_SCALER_q;

//load the sensed volts to bReg
bReg = __builtin_lac(control_struct.v_sensed_q,0);

//load the set point to aReg
aReg = __builtin_lac(control_struct.Set_pt_q,0);

//subtract aReg from bReg and thereby compute the error
aReg = __builtin_subab(aReg,bReg); //aReg has the result

//load the result of subtraction into the error variable
control_struct.error_q = __builtin_ACCH(aReg);

    //Task: Process the proportional effort; multiply kp_q with the
        error and store in P_effort_q

    // subtask: clear the aReg
aReg = __builtin_clr();

//subtask: use the builtin mpy function to multiply error_q
    variable with kp_q coefficient
aReg = __builtin_mpy(control_struct.error_q,kp, 0, 0, 0, 0, 0,
    0); //result is a Q30 number
aReg = __builtin_sftac(aReg,15); //right shift by 19 bits for
    8.8
aReg = __builtin_sftac(aReg, 4);

//subtask: round the product using Q15 support function and load
    it back into the P_effort_q variable
control_struct.P_effort_q = __builtin_sacd(aReg,0);

//Task: Process the integrator effort;

//subtask: clear the bReg
bReg = __builtin_clr();

```

```

aReg = __builtin_clr();
//load bReg with I_effort
control_struct.error_accum += control_struct.error_q;    //keep
    accumulating the error
bReg = __builtin_mpy(control_struct.error_accum,ki,0,0,0,0,0,0);
bReg = __builtin_sftac(bReg,15); //right shift by 19 bits for
    8.8
bReg = __builtin_sftac(bReg, 4);
control_struct.I_effort_q = __builtin_sacd(bReg,0);

//anti windup clamping
if(control_struct.I_effort_q >= dut_75)
{
    //constrain error accumulation to the maximum value, that
        would correspond to the
    //maximum value of the duty value. This prevents accumulation
        overflow.
    control_struct.error_accum = control_struct.error_accum_max;
    //control_struct.error_accum = E_ACCUM_MAX;
    //constrain the duty to the max duty value (75% in this case)
    control_struct.I_effort_q = dut_75;
}
else if(control_struct.I_effort_q <= dut_52)
{
    //constrain error accumulation to the minimum value, that
        would correspond to the
    //minimum value of the duty value. This prevents accumulation
        underflow.
    control_struct.error_accum = control_struct.error_accum_min;
    //control_struct.error_accum = E_ACCUM_MIN;
    //constrain the duty to the min duty value (52% in this case
        )
    control_struct.I_effort_q = dut_52;
}

```

```
}  
//Task: Add the two efforts  
aReg = __builtin_addab(aReg,bReg);  
control_struct.Controller_effort_q = control_struct.I_effort_q +  
    control_struct.P_effort_q;  
//saturation block starts  
if(control_struct.Controller_effort_q > dut_75)  
{  
    control_struct.Controller_effort_q = dut_75;  
}  
if(control_struct.Controller_effort_q < dut_52)  
{  
    control_struct.Controller_effort_q = dut_52;  
}  
//saturation block ends  
//}  
  
PORTBbits.RB4 = 0;  
  
}
```

---

## **APPENDIX B.**

### **PCB LAYOUT**

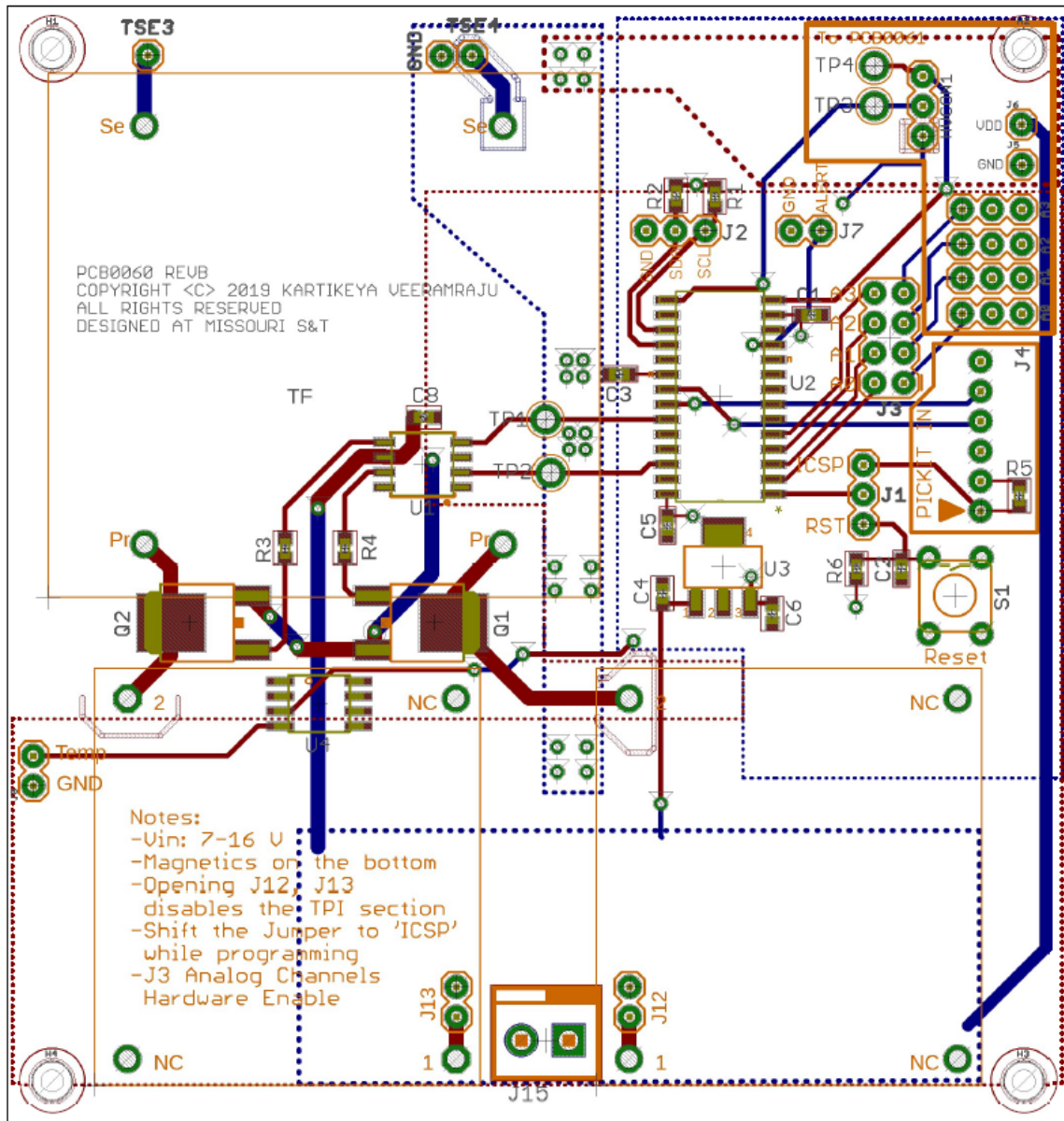


Figure 1. Embedded Controller, TPI, and HFT Stages; PCB Level 1

Figure 2. PCB Fabricated for High Voltage Stages; Front Side

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## VITA

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