2014

Design and implementation of two non-isolated high gain DC-DC converters

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Department:

DESIGN AND IMPLEMENTATION OF TWO NON-ISOLATED HIGH GAIN DC-DC CONVERTERS

by

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A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2014

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ABSTRACT

In most solar energy systems, the output voltage of a photovoltaic panel is usually between 20 to 40 Vdc. In order to interface the panels to a 400 Vdc bus, a high voltage gain dc-dc converter is required.

This thesis starts with analyzing and simulating several topologies that have been already introduced for this application. The voltage gain and efficiency are investigated analytically. A hardware prototype of one of the existing topologies, the interleaved boost converter with voltage multiplier cell, has been developed. Finally, a new topology with a higher voltage transfer ratio is proposed and its experimental results are compared with former topologies. Simulations are used to verify the design and predict the performance of each topology.

ACKNOWLEDGMENTS

I would like to express my sincere and grateful thanks to my advisor, Dr. Mehdi Ferdowsi, for his generous guidance and support throughout my research. His critical and passionate research attitude always inspires me. I have achieved a lot with his help not only in the course of this study but also on how to be a successful researcher. I would also like to thank my committee member, Dr. Jonathan W. Kimball and Dr. Mariesa L. Crow for their valuable suggestions in my research.

Thanks also goes to my colleagues and fellow friends in electrical machines and drives laboratory at Missouri S&T, such as Lucas Müller, Darren Paschedag, Jacob Mueller, Venkata Anand, Stephen Moerer, and Bhanu Prashant Reddy. I benefit a lot from many stimulating discussions with them.

Special thanks goes to my family, my father, my mother as well as my sister, who endowed me and helped me constantly and countlessly. Your indispensable support is always with me and I am really grateful. All in all, I would like to thank everyone who has made it possible for me to have such a valuable opportunity in my graduate research.

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1. INTRODUCTION

1.1. REVIEW ON HIGH-GAIN DC-DC CONVERTERS

High performance and high-gain DC-DC Converters are widely employed in many industry applications. For example, some renewable energy resources, such as, solar would require high gain DC-DC converters to lift the output voltage of the photovoltaic panels from 20~40V to 400V. Those applications have two typical characteristics including high efficiency and high gain.

Theoretically, a simple boost converter with an extreme high duty ratio close to 1 is able to achieve this high gain. However, practically, simple boost converter performance is far from satisfaction. There are several limitations:

1) Voltage stress on the switch is equal to the output voltage which is typically 400V. This high voltage stress on the switch could increase the switch loss significantly and there is not many choices of MOSFETs in the market that can handle this high voltage and still have a good efficiency.

2) The inductance of the inductor would be very large to minimize its current ripple.

3) The output diode reverse recovery loss is large.

4) The efficiency of the basic boost converter is poor.

Due to these limitations, many different topologies based on basic boost converter have been introduced in recent years. These topologies have relatively high efficiency with high voltage transfer ratio. In general, these topologies can be classified into different category based on their principal voltage lift cell. Mainstreams are interleaved boost converter with different voltage lift cell[1-11] and converters with switched

capacitors [12-16]. Those boost converters usually have one or more inductors or coupled inductors as a part of voltage lift cells. Switched capacitor converters, on the contrary, usually only have switches and capacitors to lift the voltage. The control scheme is complicated for switched capacitor converters and the cost of them are also higher because they require capacitors that have small equivalent series resistance, such as film capacitors. Figure 1.1 is a parallel diode clamped coupled inductor boost converter proposed in [1].

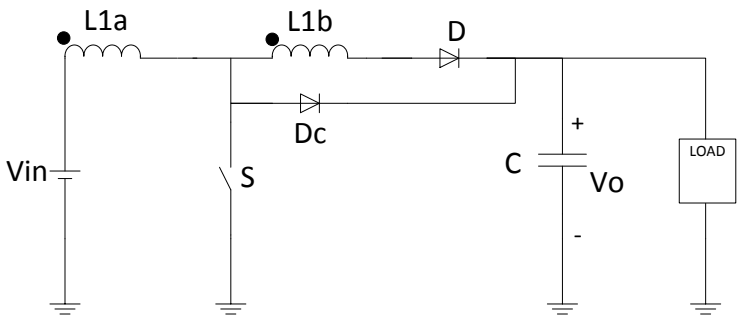

Figure 1.1 Parallel diode clamped coupled inductor boost converter

In this topology, the author uses a center tapped coupled inductor. The coupled inductor has two windings. The primary winding serves as the similar function as the filter inductor. The second winding operates as a voltage source in series to the power branch. The voltage gain can be extended by a proper turns ratio design of the coupled inductor. Dc is the clamped diode to pass the energy stored in the leakage inductor to the output side. Assuming the converter is operating in continuous conduction mode (CCM), the steady state output voltage to input voltage ratio for an ideal converter is

$$\frac{V_0}{V_{in}} = \frac{1+ND}{1-D} \tag{1.1}$$

Where V_o and V_{in} are the output and input voltages respectively, N is the secondary inductor turn to primary inductor turn ratio and D is the duty cycle. In this clamped circuit, the switch voltage stress is clamped to the output voltage and is not suitable for high voltage step-up application though its voltage transfer ratio is high.

Another topology is shown in Figure 1.2 [2]. This topology introduced a three-winding-coupled inductor interleaved with another three-winding inductor. This topology has a voltage transfer ratio which is

$$\frac{V_o}{V_{in}} = \frac{N}{1-D} \tag{1.2}$$

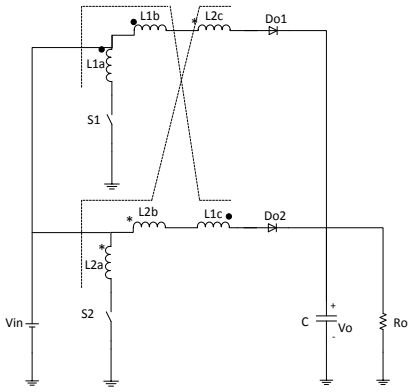

Figure 1.2 Boost converter with winding-coupled inductor

Where, N is the secondary inductor turn to primary inductor turn ratio.

This topology interleaves two boost converters to get a smooth input current and the voltage stress across the switches is $\frac{V_o}{N}$. By adjusting the inductor turns ratio, the switch voltage would be relatively small. However, the three-winding-coupled inductor design would be challenging. And the switch voltage stress is not ideally small in high output voltage applications since the turns ratio is usually under 3.

Another approach to design high-gain DC-DC converters is to add voltage lift cells to a basic boost converter to achieve high output voltage. As described in Figure 1.3, a basic Luo converter cell is introduced in [3]. When adding more elementary cells in series, it can have a higher output voltage transfer ratio. A two-cells in series circuit is shown in Figure 1.4.

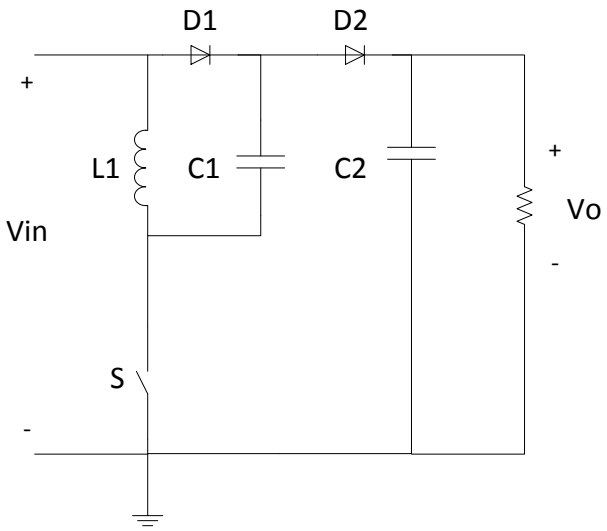

Figure 1.3 Elementary Luo converter

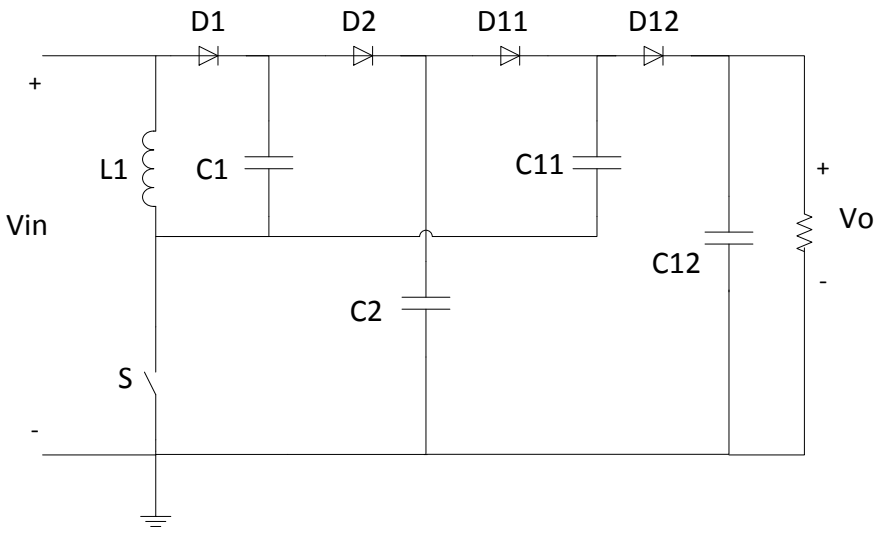

Figure 1.4 Elementary additional circuit

By charging the capacitors in parallel and discharging them in series, this converter can lift the output voltage to a significant high level. The voltage transfer ratio of this two-cell converter is

$$\frac{V_o}{V_{in}} = \frac{3-D}{1-D} \tag{1.3}$$

Also, by adding more elementary cells, the transfer ratio further increases. This kind of converter is using a lot of capacitors and diodes, which makes it more complicate and less efficient. As for the experimental results provided in the paper, it only has 80% overall efficiency. Also, since capacitors flow the main current to the output, it requires capacitors that have a small ESR. Usually, these capacitors are expensive.

Despite these disadvantages, this converter open up a gate for researchers that by adding different cells to converters, one can easily get a high voltage transfer ratio.

Another similar topology that uses voltage lift cells is depicted in Figure 1.5 [4]. This converter also has a basic voltage lift cell as shown in Figure 1.6. This topology is simple. However, the voltage transfer ratio shown in (1.4) is not high enough. Adding cells to increase the gain is not an efficient way.

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{1.4}$$

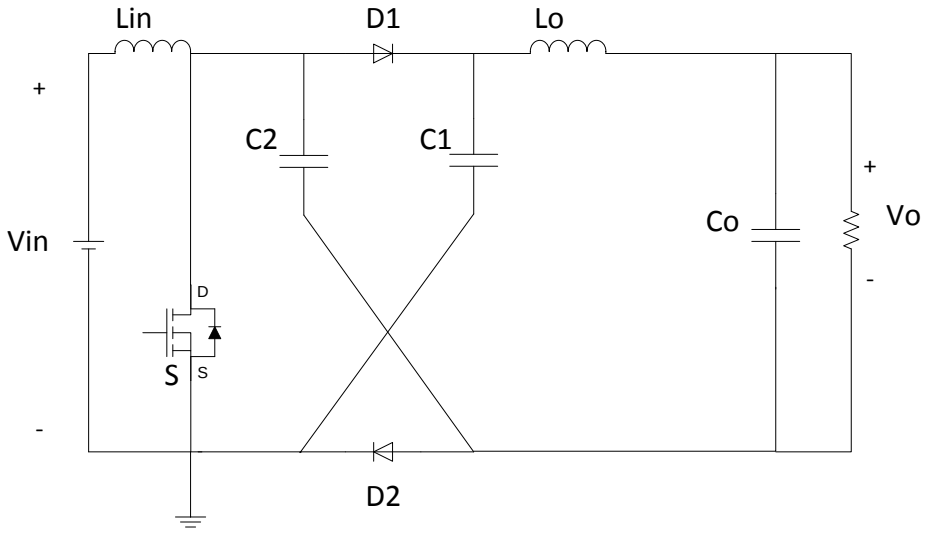

Figure 1.5 Hybrid step up converter with switching structure

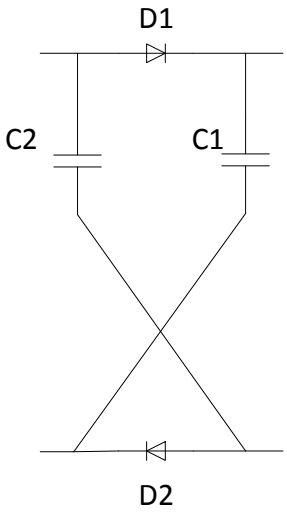

Figure 1.6 Basic step up structure

Among those boost converters with voltage lift cells, one topology drawn most attention, the schematic is as Figure 1.7 [5]. This topology introduces the voltage multiplier that are usually employed in AC voltage lift applications. Small L_r is used for zero current switch (ZCS) of the diodes. The voltage transfer ratio is

$$\frac{V_o}{V_{in}} = \frac{1+M}{1-D} \tag{1.5}$$

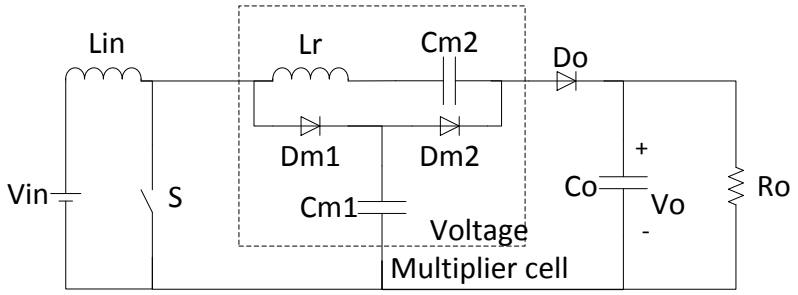

Figure 1.7 Boost converter with voltage multiplier cell

M refers to the number of voltage multiplier cell. The voltage multiplier cell is simple and efficient. The overall efficiency is high according to [5]. However, the voltage gain is not good enough for high output voltage applications. Adding more cells to increase the gain is not an efficient and simple way because this would increase the circuit complexity and cost. Another way to increase the voltage gain is to couple input inductor and clamp inductor L_r, which is reported in [6].

Figure 1.8 shows another modified edition of boost converter with voltage multiplier. This topology interleaved two basic boost with one voltage multiplier cell. The reason to interleave two boost is to achieve a continuous and smooth input current from the source. This topology has a voltage gain as

$$\frac{V_o}{V_{in}} = \frac{2N+1}{1-D} \tag{1.6}$$

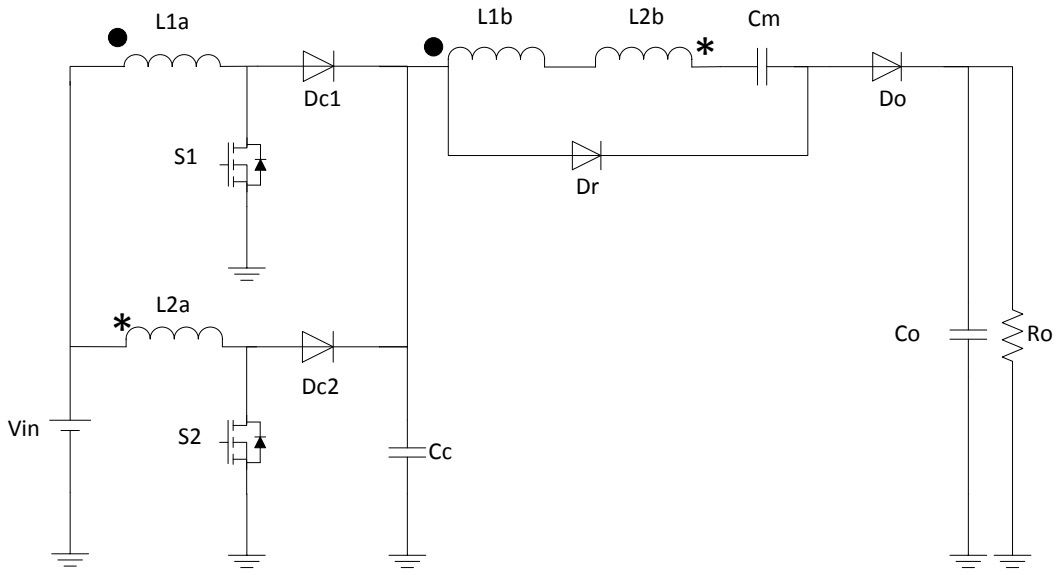

Figure 1.8 Interleaved boost converter with voltage multiplier cell

Where, N is the turns of the secondary winding to the primary winding turns ratio. By adjusting the turns ratio, the voltage gain could increase significantly. The voltage stress on the switches is also clamped by the voltage multiplier cell to $\frac{V_{in}}{1-D}$, which is relatively smaller than other topologies. This is a good topology with high potential.

In all, employing voltage lift cells into basic converters and interleaving them is a promising research stream and shows a good potential with a great high voltage gain.

1.2. RESEARCH OBJECTS AND THESIS ORGANIZATION

After reviewing many high step-up voltage converter topologies, one realizes there are many topologies developed in many different ways in high voltage applications. The main concern is to design a high gain converter with high efficiency. Many converters would meet the high voltage gain requirement but without good efficiency. Other topologies may meet the high efficiency but with a relatively inadequate voltage gain. Or in order to get a high gain, they require adding more voltage lift cells to the converter which will increase the cost and deteriorate the efficiency.

Under this circumstance, the motivation is to design a new topology that has a high voltage transfer ratio and good efficiency at a low cost. This task is challenging. To design a new topology, one needs to fully understand how different types of converters work theoretically. Further, one needs to simulate several converters for reference, check components behavior and calculate the theoretical estimated efficiency to determine a general direction to explore more options, e.g., using a three-winding coupled inductor or a normal two-winding coupled inductor, using an interleaved boost converters or just one stage, and adding voltage lift cells or using other types boost converters.

After the converter to be built is chosen, a necessary procedure is to build a converter to test its performance and improve its efficiency and voltage gain. By doing so, some useful experience has been acknowledged and it's helpful to design and build one's own converter in a good way.

In Section 2, existing promising topologies are simulated, one particular, the interleaved boost converter is built. Inspired by this interleaved boost converter topology, a new topology is proposed and built. This topology has a higher voltage gain with the same components as the interleaved boost converter and will be fully explained in Sections 3. The test results of both topologies are compared in Sections 4.

2. SIMULATION AND HARDWARE TEST OF EXISTING CONVERTERS

2.1. BRIEF ANALYSIS OF EXISTING CONVERTERS

Among those high-gain DC-DC converters, the boost converter with voltage multiplier cell, as depicted in Figure 1.7, draws much attention. First, the voltage transfer gain is high, as shown in(1.5). Second, the structure is simple. It combines a basic boost converter with a voltage multiplier cell. Third, the experiment efficiency is reported to be 92% [5]. All these characteristics are the essential requirements for a high-gain DC-DC Converter. However, there are still some possibilities to improve this converter. For instance, the number of voltage multiplier cells affects the voltage gain. The more cells used, the more voltage gain is achieved. However, adding more cells would cause other side effects, like cost increase and efficiency decrease. Also, the inductance of the resonant inductor L_r has a great effect on the output voltage which is not mentioned in the original paper, which will be discussed later in Section 2.2.1.

So, the first step is to modify this converter to a converter which has a higher voltage gain while at a low cost and high efficiency at the same time. My first thought is to use a coupled inductor to replace input inductor L_{in} and resonant inductor L_r. This modification has been made through simulation and the results would be discussed in Section 2.2.2. From the result, it would increase the voltage gain while the input current ripple is significantly increases. This is not a good solution since the input current should be as smooth as possible. To fix this problem, having two stages of input current interleaved with each other with proper phase lag would be a good way to decrease the input current ripple.

This method has been proposed in [6]. A simplified version of interleaved boost converter with voltage multiplier cell is shown in Figure 1.8. It has a higher voltage gain compared with the one stage boost converter with voltage multiplier cell and also has a good efficiency [6]. Simulation and hardware building of this converter will be discussed later in this chapter to fully understand its operation.

2.2. SIMULATIONS OF EXISTING PROMISING CONVERTERS

In this section, simulations results of two converters is discussed, the boost converter with voltage multiplier cell and the interleaved boost converter with voltage multiplier cell.

2.2.1. Simulation of Boost Converter with Voltage Multiplier Cell. The boost converter with a voltage multiplier cell is simulated and the outputs match with the result in [5]. The simulation schematic and parameters are as Figure 2.1 shows.

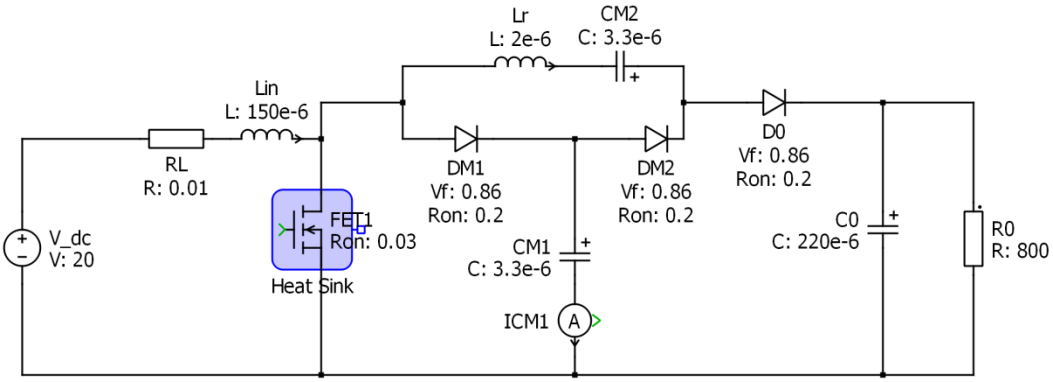

Figure 2.1 The boost converter with voltage multiplier cell simulation circuit

The parameters are chosen from [5]. For input voltage equals 20V, and output is 400V, the simulation result of the output voltage is as shown in Figure 2.2. Also, the

input current ripple is small at output power of around 200W, as Figure 2.3 shows. The ripple is around 1.2A, while, the RMS value is 10.39A. Therefore the ripple is 11.54%.

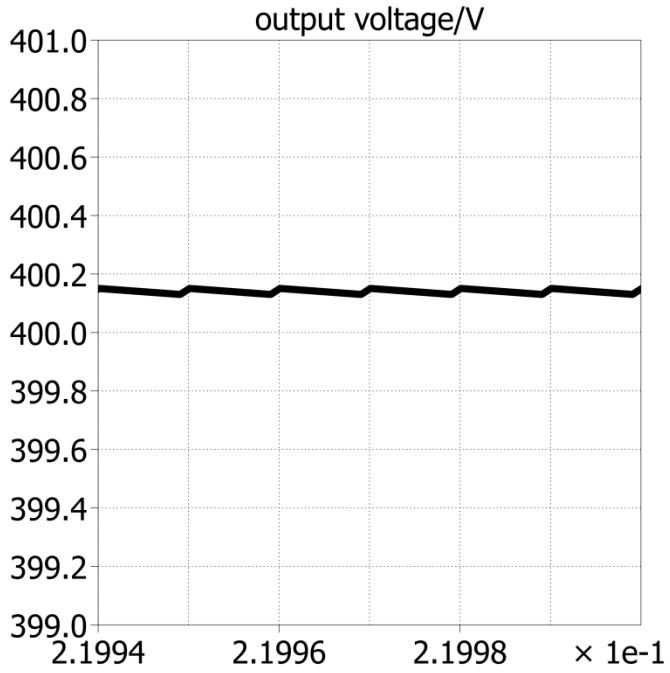

Figure 2.2 Output voltage of boost converter with voltage multiplier cell

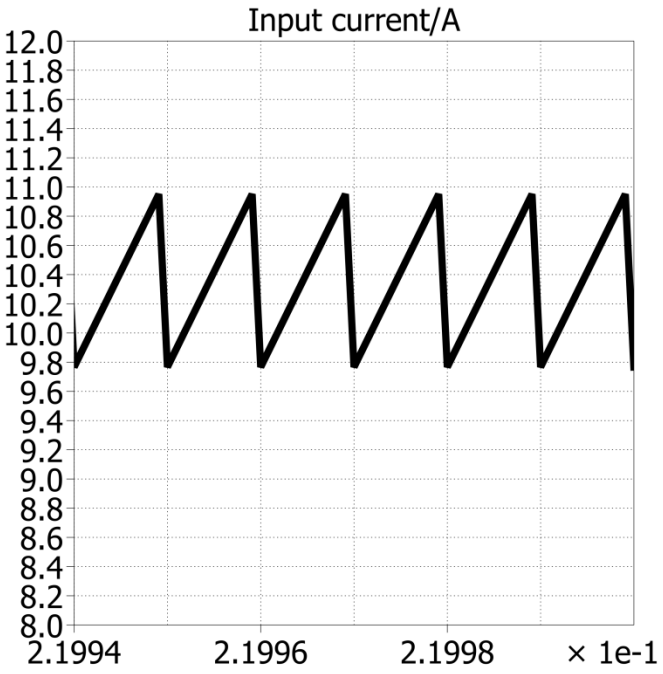

Figure 2.3 Input current of boost converter with voltage multiplier cell

The simulation results are in steady state. The output voltage can maintain 400 V while the duty ratio is around 0.907. There are some concerns about this converter. Normally, the duty ratio should be lower considering the switch rise and fall time and the reverse recovery effect of diodes. Also, as Figure 2.4 shows, the switch stress on the MOSFETs is around 210V, which is relatively higher than normal. This is because the switch voltage is clamped by capacitor CM1. The ideal switch voltage stress is $\frac{V_{in}}{1-D}$, for a boost based converter. A lower switch voltage usually means a lower switching loss and conduction loss.

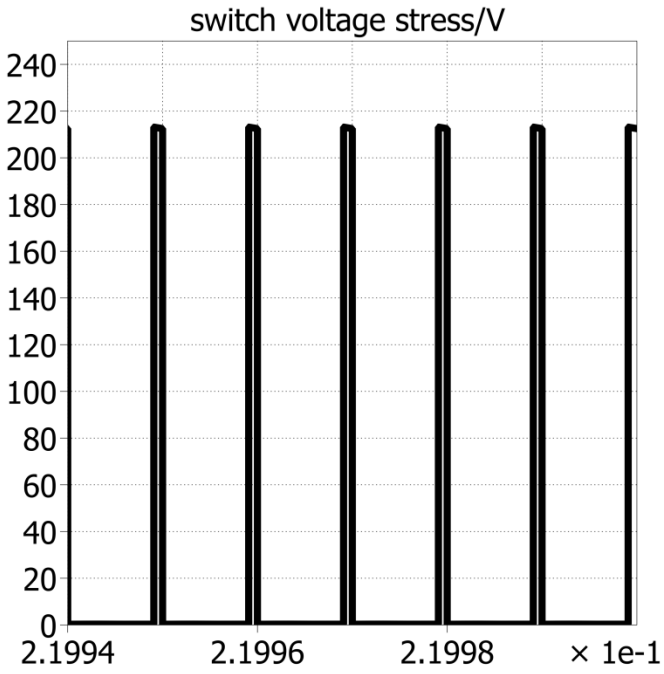

Figure 2.4 Switch voltage stress of boost converter with voltage multiplier cell

Another disadvantage is the inductance value of L_r would affect the output voltage much, which is not mentioned in the original paper. This effect is simulated by setting three different values of Lr, $2\mu H, 1\mu H, 3\mu H$, and the output voltage is shown as Figure 2.5 through Figure 2.7. As these figures show, slightely different L_r values significantly affect the output voltage. A $1\mu H$ difference inductance would change the output voltage by 9V. $1\mu H$ inductance is relatively large since the Lr value is small. Also, this small inductor should handle almost 200V maximum voltage stress, as Figure 2.8 depicts. For these disadvantages, this topology may not have a good potential on high-gain DC-DC conversion applications. The next step is to simulate the interleaved boost converter with voltage multiplier to examine its performance.

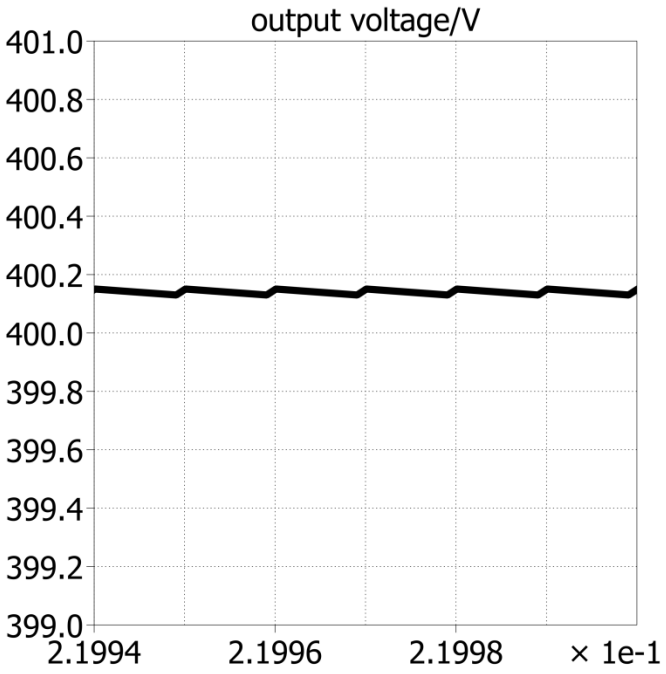

Figure 2.5 Output voltage @Lr=2μH

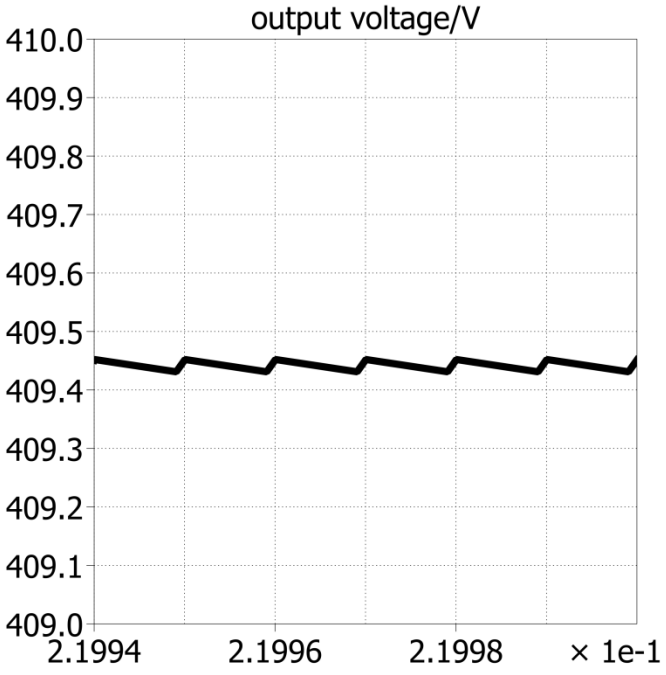

Figure 2.6 Output voltage @Lr=1μH

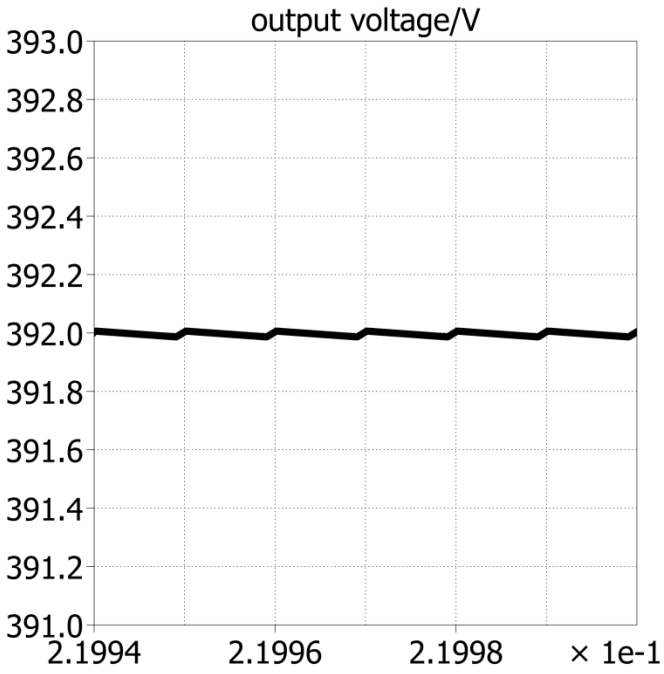

Figure 2.7 Output voltage @Lr=3μH

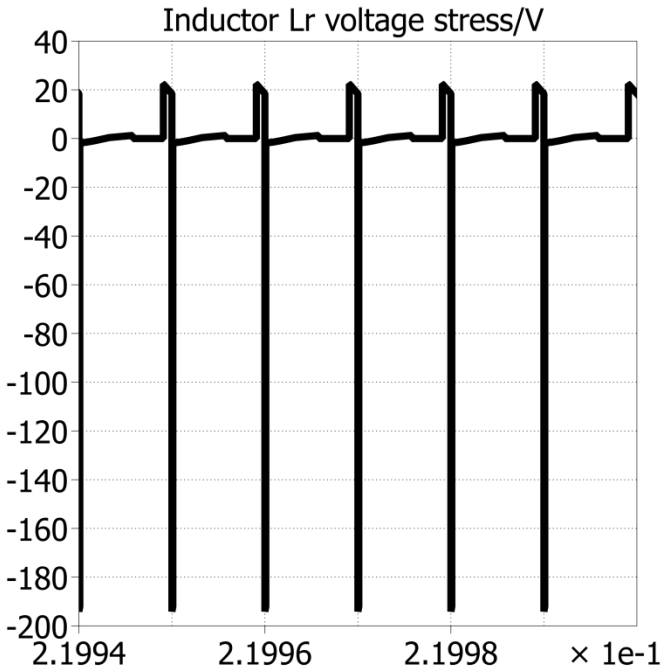

Figure 2.8 Inductor Lr voltage stress

2.2.2. Simulation of Interleaved Boost Converter with Voltage Multiplier Cell. The schematic of the circuit is as Figure 2.9 shows [6]. For the input voltage of 20V, the output voltage is 400V when the output power is 200W. The simulation result for the output voltage is as Figure 2.10 shows.

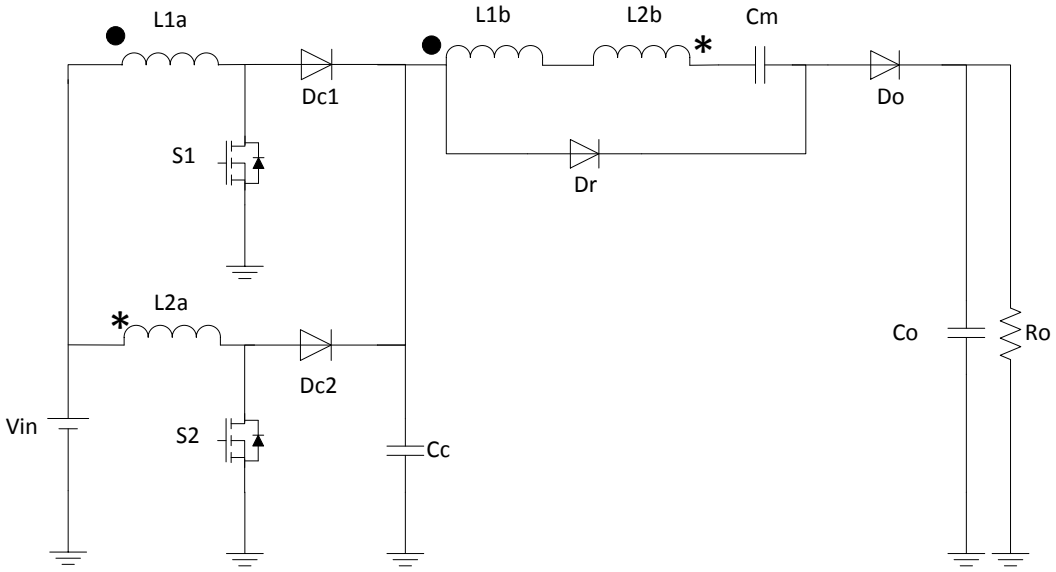

Figure 2.9 Schematic of the interleaved boost converter

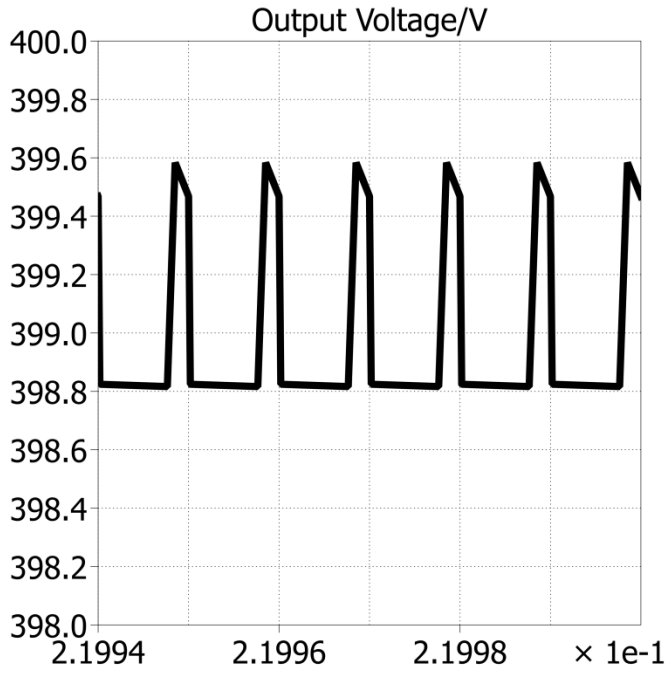

Figure 2.10 Output voltage of the interleaved boost converter

The simulation results are in steady state. The duty ratio is around 0.854 when N=1. N is the secondary turns to the primary turns ratio. The voltage transfer ratio is as equation (1.6). This converter has a higher voltage transfer ratio compared with boost converter with voltage multiplier cell. The switch voltage stress is depicted in Figure 2.11. As we can see, the switch voltage stress is clamped by capacitor Cc to 137V, which matches $\frac{V_{in}}{1-D} = \frac{20}{1-0.854} = 137V$.

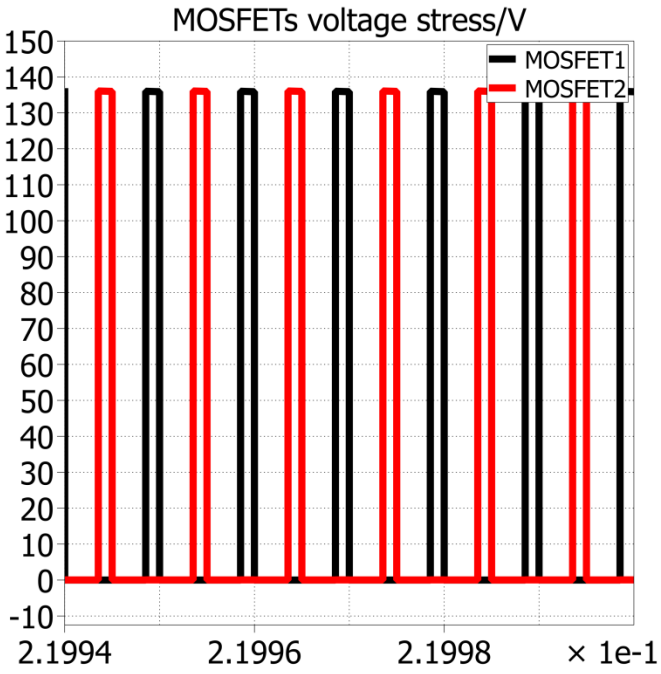

Figure 2.11 Switch voltage stress on both MOSFETs

The input current ripple is also small, as Figure 2.12 shows. The average current is 10.30A, while the current ripple is 1.4A, which is 13.59% of the average current. The efficiency is another concern. It is reported that, the efficiency is around 91% at 200W [6]. Since this topology employs many diodes and capacitors, it is necessary to check the voltage and current through these components in simulation first and find out whether the diodes and capacitors would significantly deteriorate the overall efficiency.

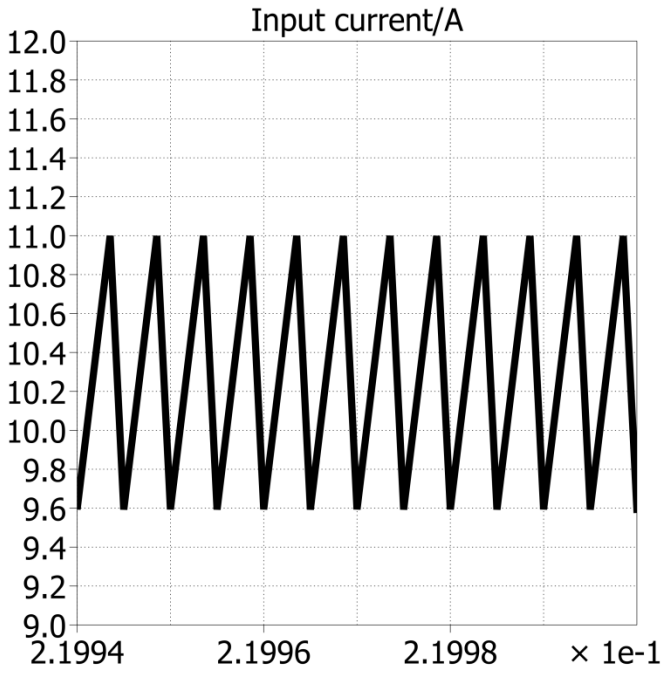

Figure 2.12 Input current of interleaved boost with voltage multiplier

Figure 2.13 shows the four diodes current at the 200 W output power. The diodes only conduct for a short time, nearly 10% of the cycle. The RMS currents are around 1.5 A, which is small. So the conduction of diodes would not harm the efficiency significantly. And neither do the capacitors, as depicted in Figure 2.14.

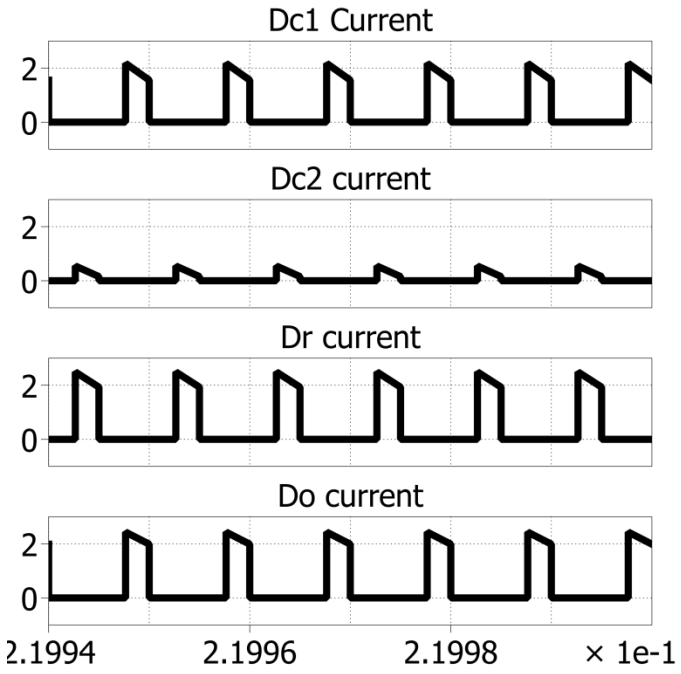

Figure 2.13 Four diodes current

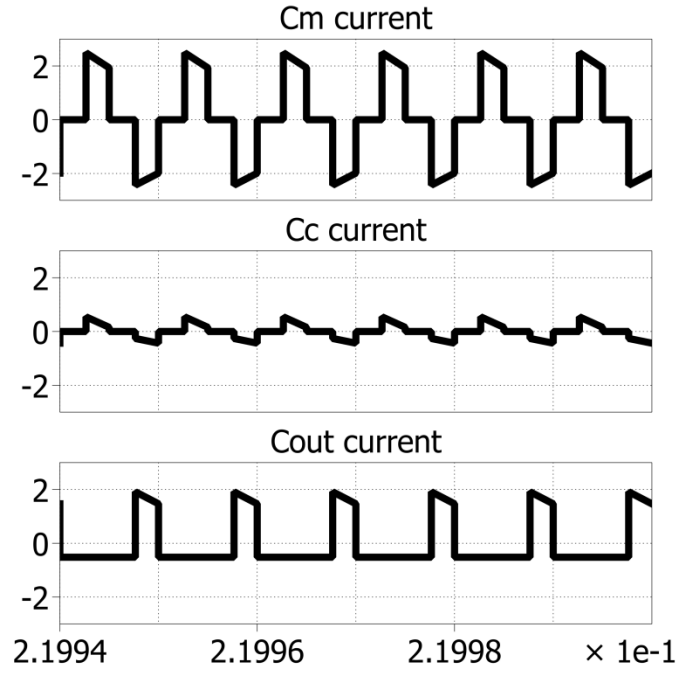

Figure 2.14 Cm and Cc currents

The last concern is the coupled inductors. There are two coupled inductors used in this topology. In practice, the turn's ratios for both inductors may be slightly different with each other. Also N may not be exactly integer. So, the turn's ratio is changed a bit in the simulation, for example, N_1 and N_2 to 0.9 and 1.1 respectively. N_1, N_2 are the first inductor turns ratio and the second respectively. The circuit can still work and the output voltage waveform in steady state is still plain but with a slight increase, as depicted in Figure 2.15.

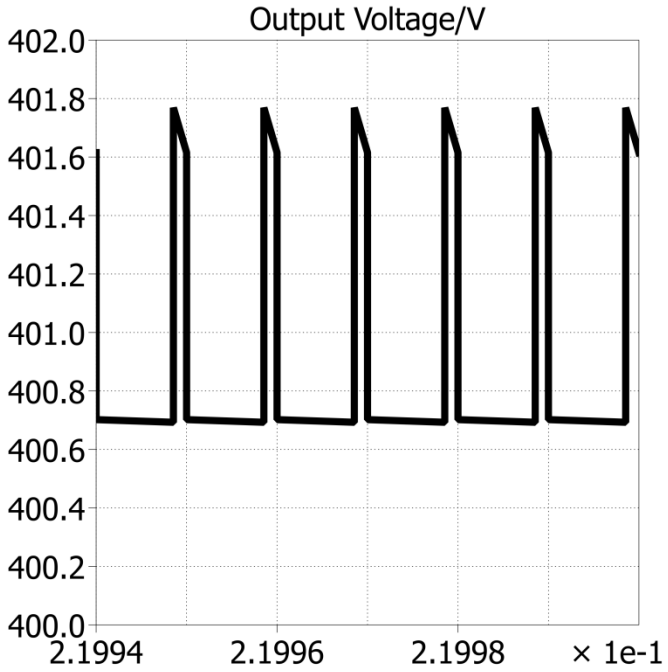

Figure 2.15 Output voltage with different turns ratios

The results are good so far. The voltage transfer ratio is high, and can be easily increased by increasing the secondary turn s number to the primary turns number ratio.

The switch voltage stress is acceptable. So this topology is with good potential to further explore. Coupled inductor and voltage multiplier are two attractions. And this topology is capable of lifting 20V to 400V with good a performance. The next step is to build this topology and test it and compare its performance with the new topology which will be introduced in the following chapter.

2.3. HARDWARE DEVELOPMENT OF THE INTERLEAVED BOOST CONVERTER WITH VOLTAGE MULTIPLIER

In this section, hardware development and test results of the interleaved boost converter with voltage multiplier is presented. Performance improvement is also discussed.

2.3.1. Coupled Inductor Design. Coupled inductor's structure is similar to a transformer. Primary and secondary windings are very close to each other. The difference is the magnetic cores. For coupled inductors, there are two different cores, gapped cores and powder cores. Gapped cores create an air gap between the two half cores and stored energy in the gap. Powder cores introduced a distributed air gap into the core structure. Design concerns and procedure are analyzed in this section.

2.3.1.1 Skin effect. It is best to use only one layer of each winding to reduce the leakage inductance and parasitic capacitance [17]. Another issue is the skin effect. When using some large wires, skin effect would increase the resistance significantly, especially when at high frequency [17]. To reduce the skin effect, proper wire size should be carefully chosen. According to Table 2.1 [17], skin effect, depicted as $\frac{R_{ac}}{R_{dc}}$, varies depending on different AWG wire sizes and operation frequency. For optimal design, $\frac{R_{ac}}{R_{dc}}$

should be as small as possible. When operating at 50 kHz, AWG24 wire should be employed. If operating at 100 kHz, the largest wire would be AWG28.

Table 2.1 AWG ac/dc Resistance Ratio at Common Converter Frequencies

AWG ac/dc Resistance Ratio at Common Converter Frequencies						
	25kHz		50kHz		100kHz	
AWG	ε cm	$\frac{R_{ac}}{R_{dc}}$	ε cm	$\frac{R_{ac}}{R_{dc}}$	ε cm	$\frac{R_{ac}}{R_{dc}}$
18	0.041868	0.032	0.029606	1.211	0.020934	1.530
20	0.041868	1.001	0.029606	1.077	0.020934	1.303
22	0.041868	1.000	0.029606	1.006	0.020934	1.137
24	0.041868	1.000	0.029606	1.000	0.020934	1.033
26	0.041868	1.000	0.029606	1.000	0.020934	1.001
28	0.041868	1.000	0.029606	1.000	0.020934	1.000

AWG28 is relatively thin and therefore the DC resistance is relatively large. Using AWG28 would reduce the skin effect but with a higher DC resistance. To minimize the conduction resistance, Litz wire is introduced. Litz wire is generally defined, as a wire constructed of individually, film insulated wires, braided together in a uniform pattern of twists and length of lay [17]. This kind of wire would minimize the skin effect and conduction resistance at the same time. The maximum and minimum number of strand for standard Litz wire is shown in Table 2.2.

Table 2.2 Standard Litz wire

Standard Litz Wire				
AWG	Minimum Strands	Approximate AWG	Maximum Strands	Approximate AWG
30	3	25	20	17.0
32	3	27	20	19.0
34	3	29	20	21.0
36	3	31	60	18.5

Unfortunately, there is no available AWG24 wire or Litz wire in the lab. For optimal design, 3 strands of AWG30 Litz wire should be employed to minimize both the conduction loss and skin effect. For convenience, a standard AWG22 wire is used for both primary and secondary windings. And for its best performance, the operation frequency should be 50 kHz.

2.3.1.2 Design procedure. In [6], the primary side inductance is $100\mu H$. So, as to be identical, the inductance value should also be $100\,\mu H$. Based on the design procedure given in [17], the first step is to calculate the energy-handling capability. The peak current is obtained based on simulation.

$$Energy = \frac{L \times I_{pk}^2}{2} = \frac{100 \times 10^{-6} \times 11.29^2}{2} = 6.373 \times 10^{-3} [w - s] \tag{2.1}$$

Then calculate the electrical conditions, K_e.

$$K_e = 0.145 P_o B_m^2 \times 10^{-4} = 0.145 \times 111 \times 0.25^2 \times 10^{-4} = 1.006 \times 10^{-4} \tag{2.2}$$

Then calculate the core geometry, K_g.

$$K_g = \frac{Energy^2}{K_e \alpha} = \frac{(6.373 \times 10^{-3})^2}{1.006 \times 10^{-4} \times 1.0} = 0.403 \tag{2.3}$$

According to [17], one must choose a core that has a larger K_g. The best one is ETD49 ferrite core, which has a K_g of 0.5917.

In [6], the authors have used 20 turns for both primary and secondary sides of the coupled inductor with $100\mu H$ inductance. The best way is to design an inductor that has the same number of turns and inductance for comparison with the results of the original paper. There is one magnetic core, gapped ETD49 with an A_L value of $250nH/T^2$, can meet this requirement.

Approximately, inductance L can be calculated as (2.4)

$$L \cong n^2 \times A_L \tag{2.4}$$

Where n is the turns number and A_L is inductance per square turn.

So, using 20 turns for primary and secondary winding would have an inductance of $100\mu H$. Since both primary and secondary side would have the same turns number, the DC resistance would be same. The diameter of ETD49 bobbin is 18.9mm.

$$L_W = \pi \times D \times N = 1.2m \tag{2.5}$$

$$R_{dc} = \rho \times L_W = 33.31 \times 1.2 \times 10^{-3} = 0.04\Omega \tag{2.6}$$

Copper loss, P_{cu},

$$P_{cu} = R_{dc} \times I_{1,RMS}^2 \tag{2.7}$$

The input current RMS value is determined:

$$V_{in,RMS} \times I_{in,RMS} \times \eta = P_{out} \tag{2.8}$$

For P_{out}=200W, the $I_{in,RMS}$ is 11.11A. Since there are two interleaved coupled inductor and their currents are synchronized, the RMS current for each inductor is approximately a bit more than half of the input current. So, take $I_{1,RMS}$=$I_{2,RMS}$=6.0A.

Thus,

$$P_{cu,pri} = P_{cu,1} + P_{cu,2} = 2 \times 6.0^2 \times 0.04 = 2.88W \tag{2.9}$$

For secondary winding, $I_{2nd,RMS}$=1.0A,

$$P_{cu,2nd} = 2 \times 1.0^2 \times 0.04 = 0.08W \tag{2.10}$$

So, total copper loss is,

$$P_{cu,tot} = 2.88 + 0.08 = 2.96W \tag{2.11}$$

For core loss,

$$P_{fe} = (\frac{mW}{g}) \times W_{tfe} \times 10^{-3} \tag{2.12}$$

Where,

$$\frac{mW}{g} = k \times f^m \times B_{ac}^n \tag{2.13}$$

$$B_{ac} = \frac{0.4\pi \times N \times \left(\frac{\Delta I}{2}\right) \times 10^{-4}}{L_g} \tag{2.14}$$

L_g is the gap length, which is 0.10cm. $W_{tfe}$is the core weight, which is 124g for ETD49 and k, m, n are the core loss coefficients for P Ferrites material at switching frequency of 100KHz, which are 4.855×10^{-5}, 1.63 and 2.62 respectively, for worst condition [17]. ΔI is the primary current ripple, which is 6.35A in simulation.

So, take these numbers into the equations listed above, the core loss is,

$$P_{fe} = \left(\frac{mW}{g}\right) \times W_{tfe} \times 10^{-3} = 31.33 \times 124 \times 10^{-3} = 3.88W \tag{2.15}$$

The total loss would be

$$P_{tot} = P_{fe} + P_{cu} = 10.72W \tag{2.16}$$

Calculate the fringing flux factor F.

$$F = 1 + \frac{l_g}{\sqrt{A_c}} \ln(\frac{2G}{l_g}) = 1 + \frac{0.1}{\sqrt{2.110}} \times \ln(\frac{2 \times 3.540}{0.10}) = 1.29 \tag{2.17}$$

Calculate the peak flux density:

$$B_{pk} = \frac{0.4\pi \times N \times F \times I_{pk} \times 10^{-4}}{l_g + \frac{MPL}{\mu_m}} = \frac{0.4\pi \times 20 \times 1.29 \times 12.06 \times 10^{-4}}{0.1 + \frac{11.40}{2500}} = 0.194[Tesla] \tag{2.18}$$

For ferrite core, the peak flux density should not be larger than 0.5 Tesla to avoid inductor saturation.

2.3.2. Theoretical losses analysis. Other losses including MOSFETs switching and conduction losses, diodes conduction losses also contribute overall power dissipation.

2.3.2.1 MOSFETs loss. MOSFETs loss has two parts: conduction loss and switching loss.

Switching loss:

Switching loss is a combination of turn-on losses, turn-off losses, and MOSFET body diode switching losses. Turn-on loss includes switch on energy of MOSFET itself and caused by the reverse recovery of the body diode [18].

$$P_{SW\_ON} = (V_{ds} \times I_{Don} \times t_{on} + Q_{rr} \times V_{ds}) \times f_{sw} \tag{2.19}$$

Where V_{ds} is the drain-source voltage, I_{Don} is the turn-on current, Q_{rr} is the reverse recovery charge capacitor.

T_{on}, which is turn-on time, is actually a median of fall times, due to the non-linearity of the gate –drain capacitance, two-point estimation is introduced to simplify the non-linearity turn-on time, so t_{on} can be defined as below:

$$t_{on} = \frac{t_{on\_1} + t_{on\_2}}{2} \tag{2.20}$$

$$t_{on\_1} = (V_{ds} - R_{dson} \times I_{Don}) \times \frac{C_{rss\_1}}{I_{Gon}} \tag{2.21}$$

$$t_{on\_2} = (V_{ds} - R_{dson} \times I_{Don}) \times \frac{C_{rss\_2}}{I_{Gon}} \tag{2.22}$$

$$I_{Gon} = \frac{V_{Dr} - V_{Gth}}{R_G} \tag{2.23}$$

C_{rss_1} is the reverse transfer capacitance at V_{DS}=0V, and C_{rss_2} is at V_{DS} is at the worst condition determined by the application. V_{Dr} is the gate driver output voltage and V_{Gth} is MOSFET gate the threshold voltage, R_G is gate resistance.

Turn on energy of the body diode mostly consists of the reverse recovery energy:

$$P_{D\_ON} \approx (\frac{1}{4} Q_{rr} \times V_{ds}) \times f_{sw} \tag{2.24}$$

Turn off loss is a similar process. The turn off loss of body diode can be neglected.

Turn off loss of MOSFET is:

$$P_{SW\_off} = V_{ds} \times I_{Doff} \times t_{off} \times f_{sw} \tag{2.25}$$

$$t_{off} = \frac{t_{off\_1} + t_{off\_2}}{2} \tag{2.26}$$

$$t_{on\_1} = (V_{ds} - R_{dson} \times I_{Don}) \times \frac{C_{rss\_1}}{I_{Goff}} \tag{2.27}$$

$$t_{on\_2} = (V_{ds} - R_{dson} \times I_{Don}) \times \frac{C_{rss\_2}}{I_{Goff}} \tag{2.28}$$

$$I_{Goff} = \frac{-V_{Gth}}{R_G} \tag{2.29}$$

Conduction loss of MOSFETs can be calculated:

$$P_{SW\_C} = R_{dson} \times I_{D_{rms}}^2 \tag{2.30}$$

Conduction loss of body diode can be calculated:

$$P_{D\_C} = R_D \times I_{F_{rms}}^2 + V_{DF} \times I_{Favg} \tag{2.31}$$

2.3.2.2 Diode and capacitor loss. Diode conduction loss is as (2.31).

Capacitor loss can be expressed as (2.32)

$$P_{Cap\_C} = ESR \times I_{C_{rms}}^2 \tag{2.32}$$

Where, ESR is the equivalent series resistance of capacitor.

Pluging numbers into (2.19), (2.24), (2.25), (2.30), (2.31) and (2.32), the theoretical total loss is as

$P_{switching}$=0.218W, P_{SW_C}=0.227W, P_D=$0.40 \times 2 + 0.64 + 0.64 = 2.08W$,

P_c=$0.393 + 0.75 + 0.377 = 1.52W$,

MOSFETs loss	Diode loss	Capacitor loss	Inductor loss	Total
0.89W	2.08W	1.52	10.72W	15.21W

2.3.3. Circuit Performance Improvements. In this section, the factors that affect the circuit performance have been analyzed and approaches to solve and improve them are introduced.

2.3.3.1 Ringing voltage of MOSFETS. The switch voltage has a slight ringing during the turn off status. The peak voltage is near 150V, which is the maximum drain-source voltage of the MOSFET. This high spike voltage would damage the MOSFET. This ringing problem is caused by the parasitic capacitance and inductance connected at the switch node, where diode Dc and the inductor are connected. When the switches turn off, the suddenly interrupted current of the leakage inductance will flow into parasitic capacitor of MOSFETS and leads to a sharp voltage rise. Additionally, the conducted emissions would cause problems for any nearby Integrated Circuits, like gate drivers [19]. Without solving this problem and at this circumstance, this ringing voltage would require other MOSFETS that have a relatively higher drain-source voltage but with a higher static drain-source-on resistance, which in this case, will increase the conduction loss and harm the efficiency.

To solve this problem, either adding a snubber circuit or optimizing the gate resistance would be helpful. A snubber circuit, especially for those only conducts during the switch transient period, will eliminate ringing voltage during switch turn off status while consume only the energy stored in parasitic capacitors and inductors. This circuit will not only reduce the ringing voltage significantly but also help improve the efficiency [20]. There are a lot of snubber circuits and can be divided into two main groups, the passive and active snubbers. Passive subbers, as the word passive indicates, are composed of tiny inductors, capacitors and diodes. They do not require extra sensors and

switches to control the circuit to conduct at certain precise time, which makes them simple and small[21-25]. Active snubber circuits, on the other hand, are composed of switches, inductors, capacitors and diodes. They use switches to control the circuit conducting during the switch turn off period[26-30]. Among them, a particular one, which only conducts during transient period, seems promising[31]. The snubber circuit proposed in [31] works well in simulation. However, in hardware prototype, it's not good.

Optimizing the gate resistance could be another way. This resistance includes the driver output resistance, external gate resistance and built-in internal gate resistance of MOSFETs. The only one that can be changed is the external gate resistance. Adding an external resistance would slow down turn on/off time of switches because the time required to charge/discharge the input capacitor of MOSFET(C_{ISS}) would increase. A smaller gate resistance would result an overshoot in the switch voltage but with a higher switching time while higher resistance will underdamp the oscillation but increase switching time and driver power dissipation.

A proper external gate resistance, balance the switching time and overshoot voltage, should be applied to the gate circuit [32]. As depicted in Figure 2.16, the gate driver, gate resistor, series inductor, MOSFET input capacitor form a loop.

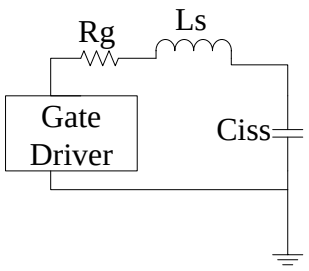

Figure 2.16 Gate driver with MOSFET connection loop circuit

The oscillatory spikes observed in most gate driver circuit are caused by the gate driver output voltage steep edges. These spikes can usually be damped or improved much by the external gate resistor and the internal resistor built in the drivers. By adjusting the external gate resistor, the spikes can be damped. R_g can be calculated for optimum performance by :

$$R_{gate,OPT} = 2 \times \sqrt{\frac{L_s}{C_{iss}}} - \left(R_{driver} - R_{G,I} \right) \tag{2.33}$$

where, Ls is the inductance in series with the gate driver and MOSFET gate; C_{iss} is the input capacitance of MOSFET, R_{driver} is the output resistance of gate driver and $R_{G,I}$ is the input gate resistance of MOSFET [32].

The only unknown parameter is L_s. It comes from the wire that connects driver and MOSFET, and the built in inductance of gate driver and MOSFET. The wire inductance is measured under 50kHz, which is the current switching frequency, with an approximate value of 0.47μH. Plugging this value into (2.33),

$$R_{gate,OPT} = 8.8\Omega \tag{2.34}$$

Inductance should be a bit larger than 0.47μH,by including the built-in inductance of gate driver and MOSFET. So, in practice, the gate resistance is 10 Ω. Different values

of gate resistances have been applied to the circuit on breadboard and compared with each other, as Figure 2.17 and Figure 2.18 depict. The waveforms of drain-source voltage are as below, other components and parameters of the circuit are identical. The ringing spikes have been dumped by applying 10 Ω gate resistance. It also improves the efficiency by 0.4%.

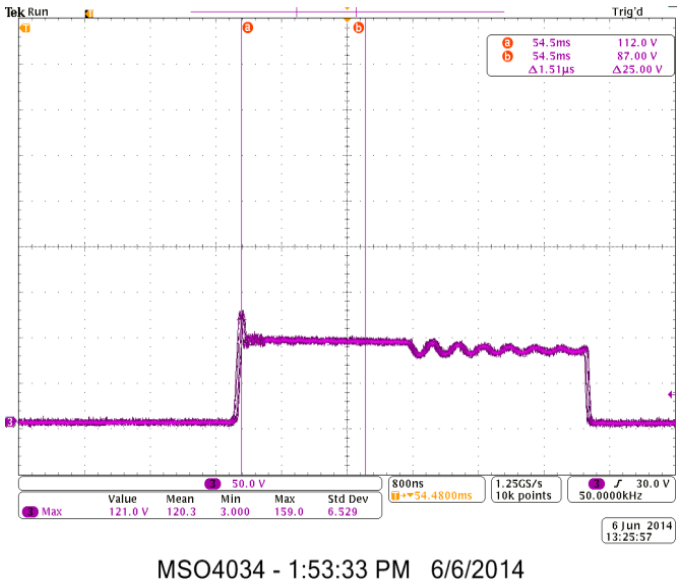

Figure 2.17 MOSFET drain-source voltage with R_g=10Ω

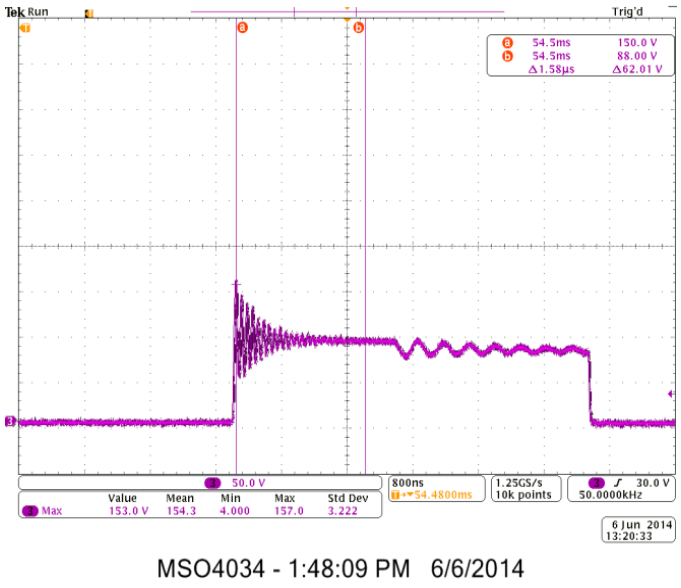

Figure 2.18 MOSFET drain-source voltage with R_g=2.7Ω

2.3.3.2 Efficiency improvements. The overall efficiency can be further improved by replacing components, such as diodes with more efficient ones. Also, the winding of coupled inductor can be further optimized. For example, put two wires in parallel with each other for the primary side. This method would decrease the DC resistance and skin effect and also help improve the conduction loss of primary side in fact of it conducts much more current than secondary.

Another way may help is to increase the turns ratio N. By increasing N, the secondary current would reduce and voltage transfer ratio would increase. Also, with a larger N, the duty cycle would decrease which could lead to a smaller conduction loss and a lower voltage stress on MOSFETs. Figure 2.19 and Figure 2.20 show the simulation results of MOSFETs voltage stress difference.

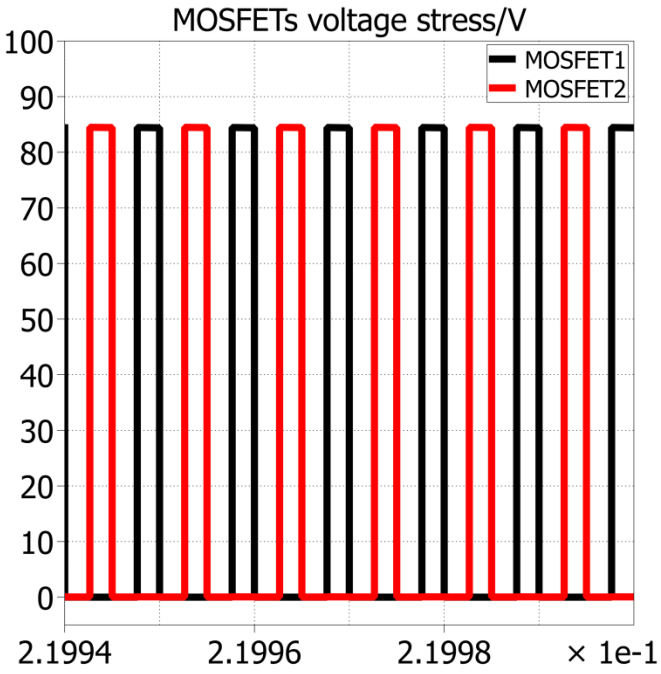

Figure 2.19 Simulation results of MOSFETs voltage stress with N=2

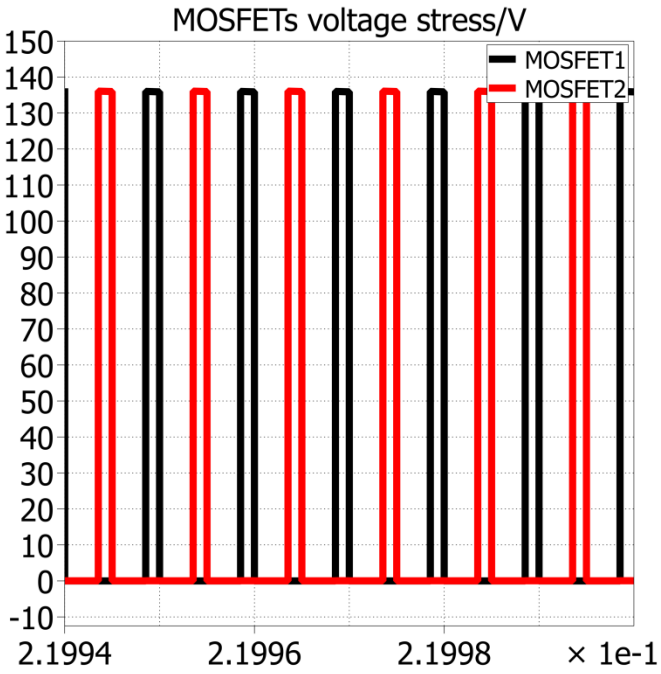

Figure 2.20 Simulation results of MOSFETs voltage stress with N=1

3. DESIGN OF NEW TOPOLOGY

3.1. SCHEMATIC

The new topology depicted in Figure 3.1 is inspired by [5]. It basically combines a voltage multiplier cell with an interleaved boost converter. The proposed topology somewhat resembles the topology that was discussed in chapter 2. However, its voltage transfer ratio is higher.

As shown in Figure 3.1, L_{1p} and L_{1s} are the primary and secondary windings of the first coupled inductor, respectively. Similarly, L_{2p} and L_{2s} are the primary and secondary windings of the second coupled inductor. S_1 and S_2 are the power MOSFETs. D_1 serves as a classic boost converter output diode, and D_2, which is in dotted line, is the clamping diode. The role of D_2 will be explored later. C_1 functions like an output capacitor of the two interleaved boost converters and also compose the voltage multiplier cell along with D_3, C_2, and the coupled inductor secondary windings. C_{out} is the output capacitor, and R_o is the load resistor. N is the primary turns' number to the secondary turns' number (n_2/n_1) for both coupled inductors.

The magnetizing inductance of the coupled inductors serve as the boost inductor with turns number of n_1, the secondary windings with turns number of n_2 are connected in series with capacitor C_2 to achieve high voltage gain. Coupling references of coupled inductors are pointed as "•" and "*" as given in Figure 3.1.

Each coupled inductor can be modeled as a combination of a magnetizing inductor, representing the actual inductance of the coupled inductor, and an ideal transformer with corresponding turns ratio and a leakage inductance in series with the

magnetizing inductor. To simplify the analysis, the leakage inductance is temporarily neglected. The equivalent circuit is shown in Figure 3.2

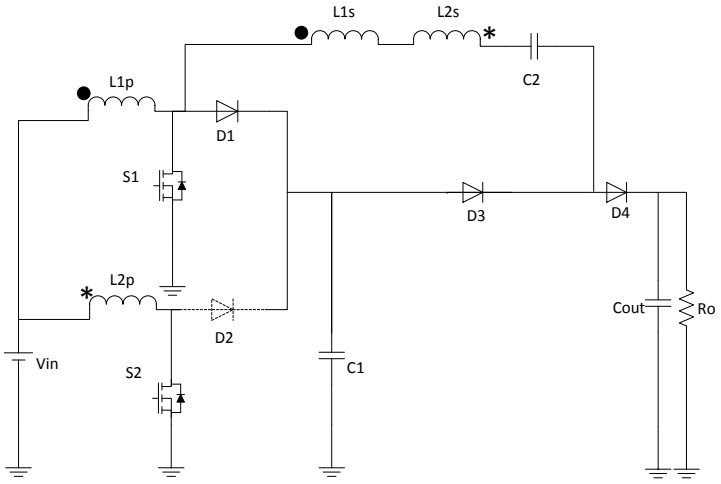

Figure 3.1 Proposed topology

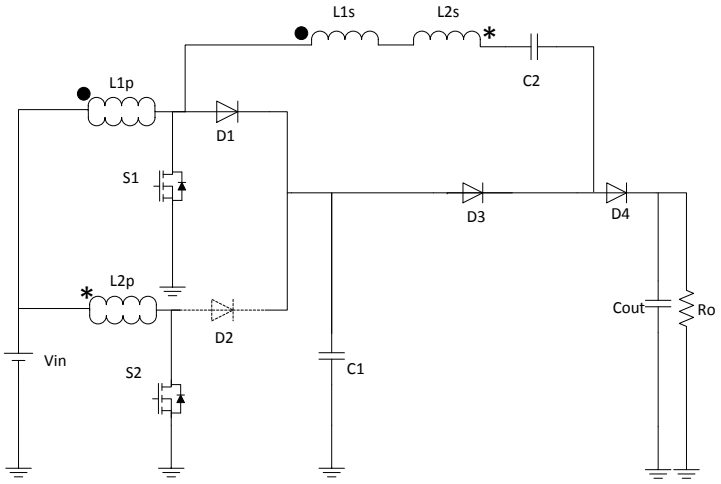

Figure 3.2 Proposed topology with magnetizing inductance

3.2. THEORETICAL ANALYSIS

3.2.1. Operation Modes. Assuming the converter works in continuous conduction mode (CCM), then there are 3 different operation modes in one switching period as depicted in Figure 3.3. At any given time, one of the switches should be on. Usually, the command to S_2 is similar to that of S_1, but with a 180^o of phase shift. Both switches conduct with the same duty cycle D. T is the cycle time. The equivalent circuit of each mode is explored. The bold lines indicate which part is conducting during a certain mode.

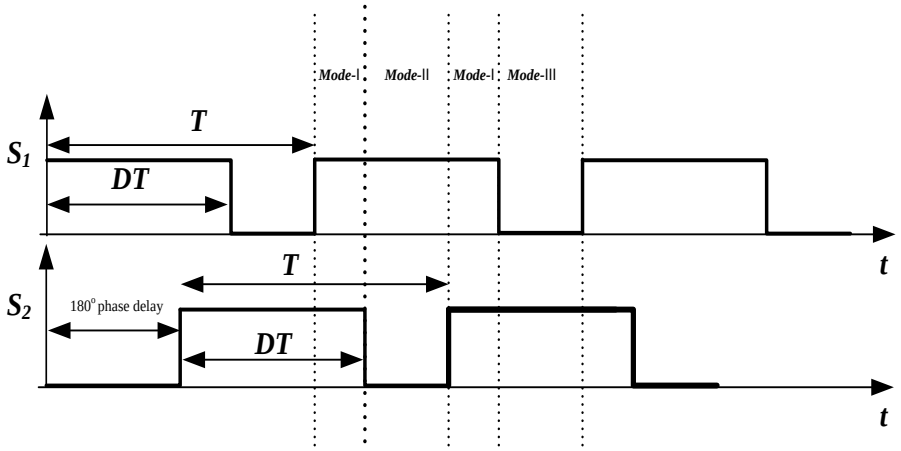

Figure 3.3 Switch pattern

Mode I: In this mode, both switches are conducting. Therefore, L1 and L2 are charged through the DC source (see Figure 3.4). The voltage drop on both inductors is the input voltage. Each inductor current rises linearly. The voltage multiplier cell does not conduct yet. The load is powered through the output.

$$V_{L1p} = V_{L2p} = V_{in} \tag{3.1}$$

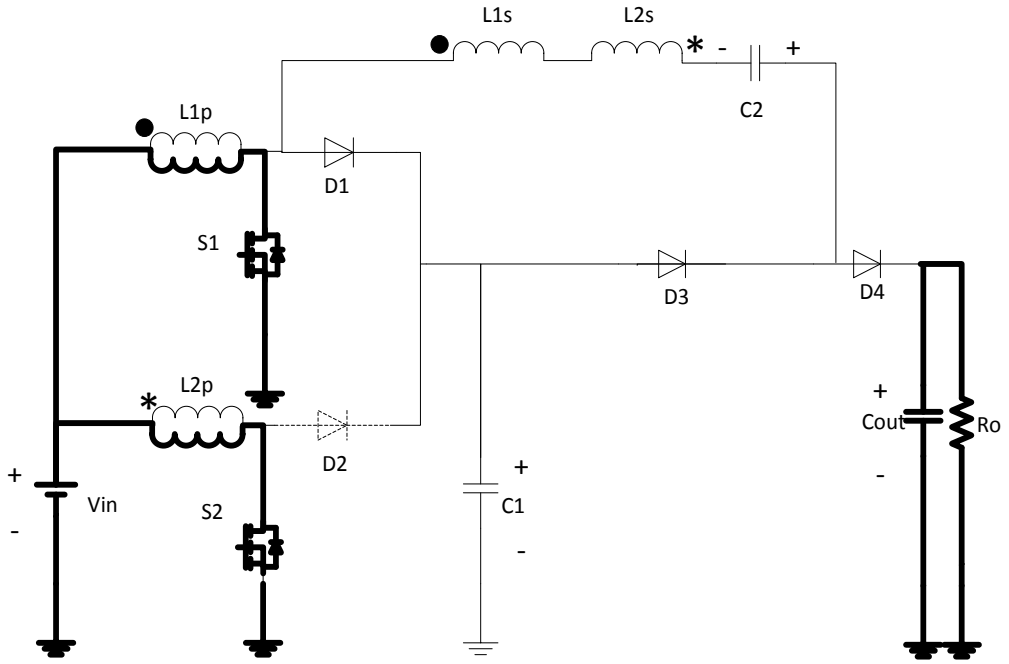

Figure 3.4 Operation mode I of proposed converter

Mode II: In this mode, S_2 opens while S_1 stay closed (see Figure 3.5). The energy stored in magnetizing inductance L_2 is transferred to the secondary side and turns diode D_3 on. Therefore, C_1 discharges and C_2 charges. D_1 and D_2 are backward biased, and so is the output diode. The voltage on L_{1p} is the input voltage. Thus, the voltage on L_{2p} can be derived.

$$V_{L1p} = V_{in} \tag{3.2}$$

$$V_{L2p} = V_{in} + \frac{V_{C1}}{N} - \frac{V_{C2}}{N} \tag{3.3}$$

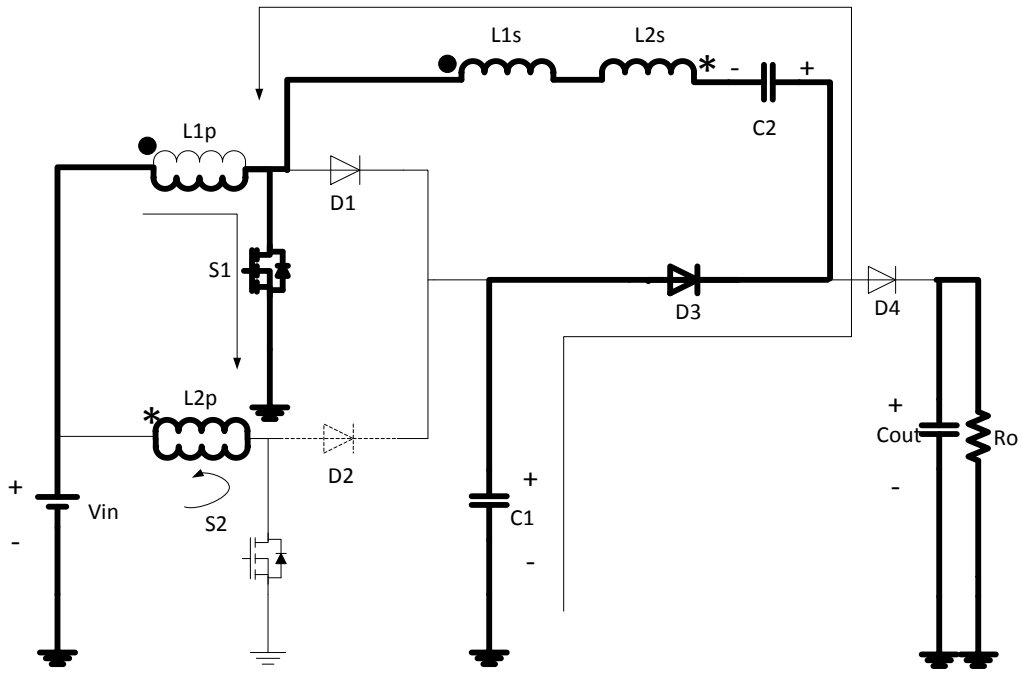

Figure 3.5 Operation mode Ⅱ of proposed converter

Mode III: In this mode, S_1 is off while S_2 starts to conduct (see Figure 3.6). Capacitor C_1 is charged through L_1 and the input source. Meanwhile, the output capacitor is also charged through L_{1p}, the secondary windings, C_2 and D_4. L_{2p} is also charged through the source. Also, C_2 discharges. The voltages on two primary side inductors can be derived.

$$V_{L1p} = V_{in} - V_{C1} \tag{3.4}$$

$$V_{L2p} = V_{in} \tag{3.5}$$

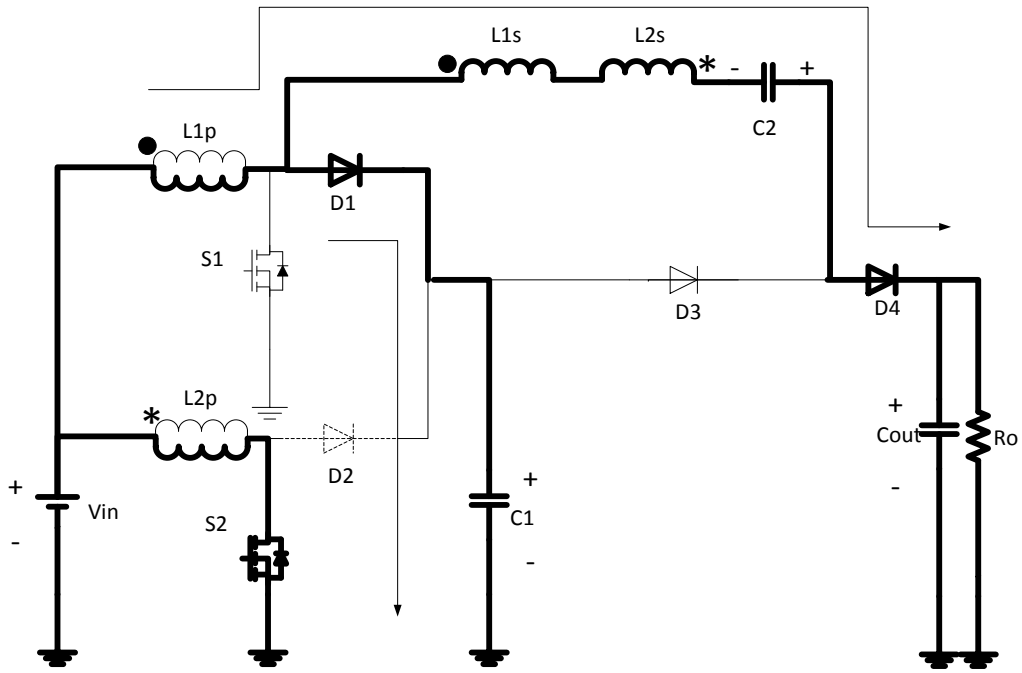

Figure 3.6 Operation mode III of proposed converter

3.2.2. Voltage Transfer Ratio. During an entire switching cycle, the average voltage on the inductors is zero [33].

$$< V_{L1p} >= 0 \tag{3.6}$$

$$< V_{L2p} >= 0 \tag{3.7}$$

From operation modes analysis, the voltages on the inductor primary side in different modes are all given. The equations and derivations are below:

$$< V_{L1p} >= DT \times V_{in} + (1-D)T(V_{in} - V_{C1}) = 0 \tag{3.8}$$

$$< V_{L2p} >= DT \times V_{in} + (1-D)T(V_{in} - \frac{V_{C1}}{N} - \frac{V_{C2}}{N}) = 0 \tag{3.9}$$

Therefore,

$$V_{C1} = \frac{V_{in}}{1-D} \tag{3.10}$$

$$V_{C2} = \frac{(N+1)V_{in}}{1-D} \tag{3.11}$$

For the output voltage, in mode Ⅲ, capacitor C_1, the secondary windings, C_2, D_4 and output capacitor C_{out} form a loop. By applying KVL to this loop, the output voltage can be obtained.

$$-V_{C1} + N(V_{in} - V_{C1}) - NV_{in} - V_{C2} + V_{out} = 0 \tag{3.12}$$

$$V_{out} = (1+N)V_{C1} + V_{C2} = \frac{2N+2}{1-D}V_{in} \tag{3.13}$$

For solar power system application, typically the minimum output voltage of a solar panel is around 20V, and the DC converter output voltage is 400V. The simulation parameters are listed in Table 3.1. Components including MOSFETs, diodes and capacitors are assumed to be ideal, without conduction and switching losses.

Table 3.1 Converter simulation parameters

Components	Parameters
Input voltage	20V
Turn's ratio	N=2
Duty ratio	0.70
Output voltage	400V
Output power	200W
Switching frequency	50KHz
Coupled inductor inductance	$100\mu H$
C_1,C_2	$47\ \mu F$
C_{out}	$470\ \mu F$

The output voltage and source current can be verified through simulation, as given in Figure 3.7:

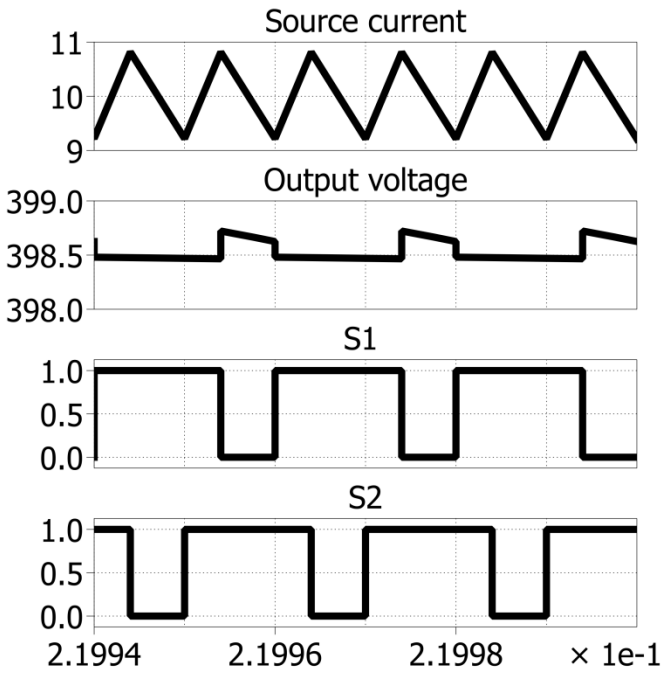

Figure 3.7 Proposed converter output voltage

3.2.3. Voltage Stress on Components. Voltage stress is another issue that draws attention. Generally, the voltage stress on every component should be as low as possible, especially for the MOSFETs. In this high voltage gain converter, every component voltage stress is theoretically analyzed.

MOSFETs voltage:

The Voltage stress on MOSFETs is big concern. Usually, the smaller voltage stress would lead to a smaller switching loss and conduction loss for MOSFETs. In this

topology, the voltage stress on both MOSFETs $\frac{V_{in}}{1-D}$ is$\frac{V_{in}}{1-D} = 67V$. The simulation result is shown in Figure 3.8.

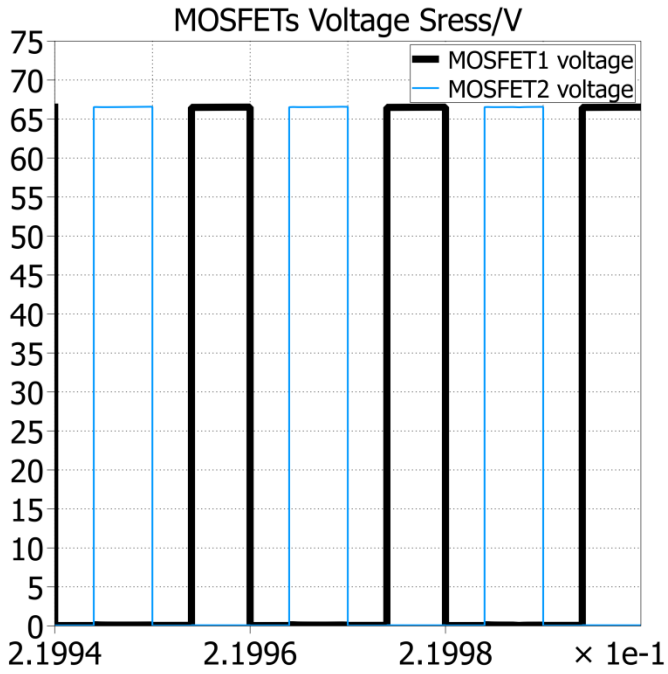

Figure 3.8 MOSFETs voltage stress of proposed converter

Diodes voltages:

In mode I, D_1 and D_2 act like an output diode of a classical boost converter. Their voltage stress is the output voltage of the classical boost converter, as shown in Figure 3.9, given as:

$$V_{D_1 \& D_2} = V_{C1} = -\frac{V_{in}}{1-D} \tag{3.14}$$

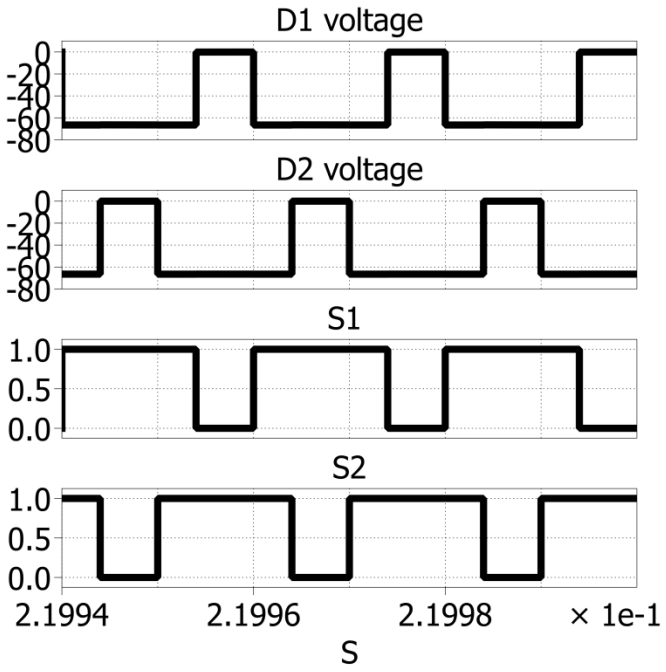

Figure 3.9 D1&D2 voltage

For voltage multiplier diode D_3, in mode II,

$$V_{D3} = V_{C1} - V_{out} = -\frac{2N+1}{1-D} V_{in} \tag{3.15}$$

In mode I,

$$V_{D3} = V_{C1} - V_{C2} = -\frac{2}{1-D} V_{in} \tag{3.16}$$

For output diode D_4 , in mode Ⅲ,

$$V_{D4} = V_{C1} - V_{out} = -\frac{2N+1}{1-D} V_{in} \tag{3.17}$$

In mode I,

$$V_{D4} = V_{Cout} - V_{C2} = -\frac{N+1}{1-D} V_{in} \tag{3.18}$$

These voltages can be verified by simulation results, as shown in Figure 3.10:

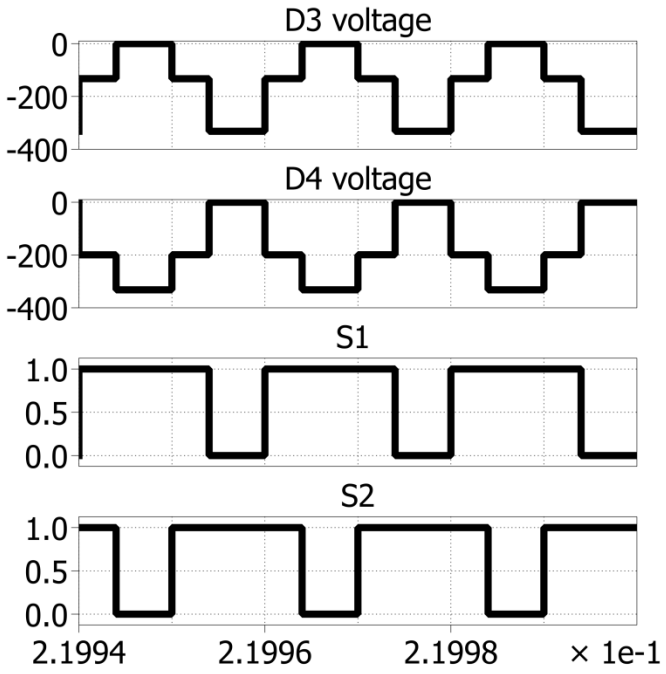

Figure 3.10 Diodes D_3 and D_4 voltage stress

Capacitor voltages:

For output capacitor, the voltage is the output voltage. For the clamping capacitor, which is acting like a classical boost converter output capacitor, the voltage stress has been derived before, and the waveform is as Figure 3.11 shows.

$$V_{C1} = \frac{V_{in}}{1-D} \tag{3.19}$$

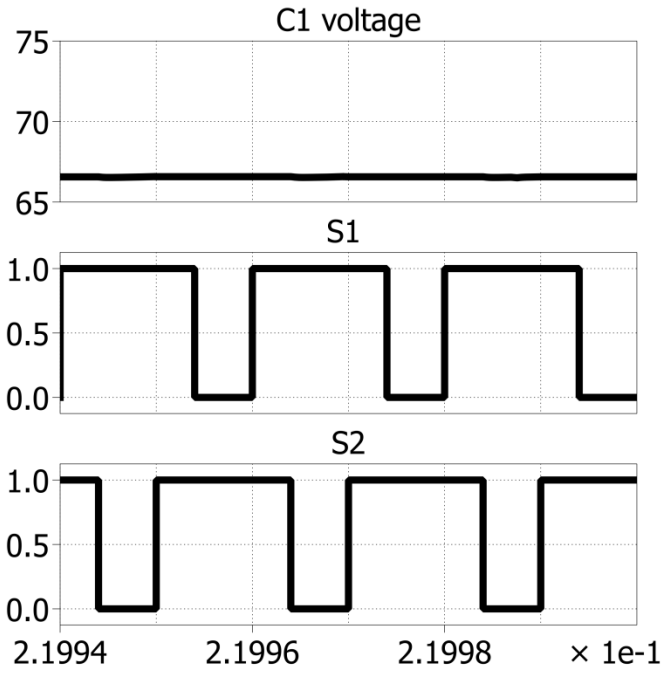

Figure 3.11 C1 voltage

For voltage multiplier capacitor C_2, the simulation waveform is shown in Figure 3.12, the theoretical voltage is,

$$V_{C2} = \frac{N+1}{1-D} V_{in} \tag{3.20}$$

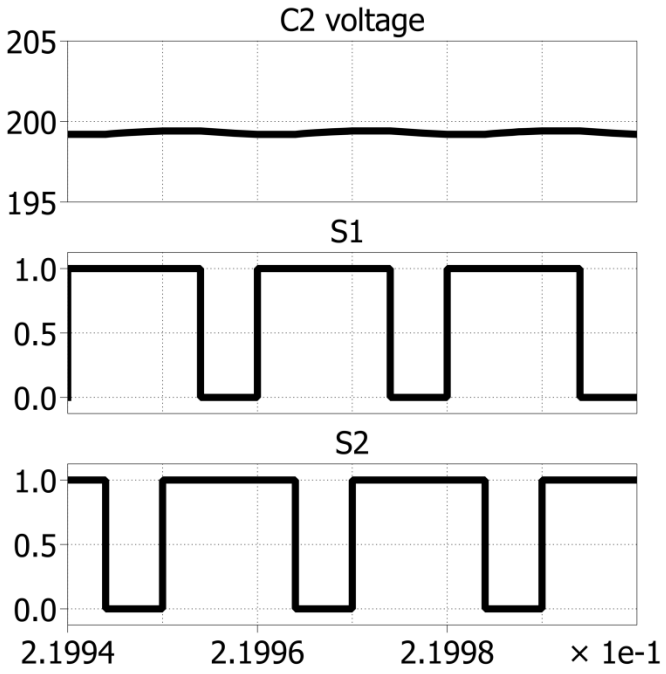

Figure 3.12 C2 voltage

3.2.4. Coupled Inductor Design. The coupled inductor design process is almost the same as what has been presented in section 2.3.1. Besides turns ratio N equals exactly 1, a different inductor with N=2, has been made to measure how it effects the efficiency. Also, considering primary current is nearly 11A, two wires in parallel consist the primary winding to reduce the conduction loss.

3.2.5. Analysis with the Leakage Inductance. As mentioned earlier, all the analysis before is based on ideal conditions. This procedure would simplify the entire converter behavior. However, in practice, none of components are ideal and some of these non-ideal components would entirely change the converter operation condition. For example, the leakage inductance of the coupled inductor has a significant influence on converter operation modes and voltage stress on switches and other components. Also, the built-in series resistance of MOSFETs, diodes and capacitors would also deteriorate the efficiency and increase voltage drop on these components.

Fortunately, not all these non-ideal parameters have negative impacts. Leakage inductance may increase the converter complexity, but will also help achieve MOSFETs zero current switching. When MOSFETs are turned off, the energy stored in leakage inductance charges C1 and C2. Since the leakage inductance is relatively small and capacitor C1 and C2 are large enough, all the energy would transfer from the leakage inductance to the capacitors and there is no current flowing in coupled inductors and diodes D1 and D2. Thus, the zero current switching condition is obtained. Therefore, the turn on switching loss of MOSFETs and reverse recovery energy loss on diodes have been minimized. The equivalent circuit is as Figure 3.13 shows.

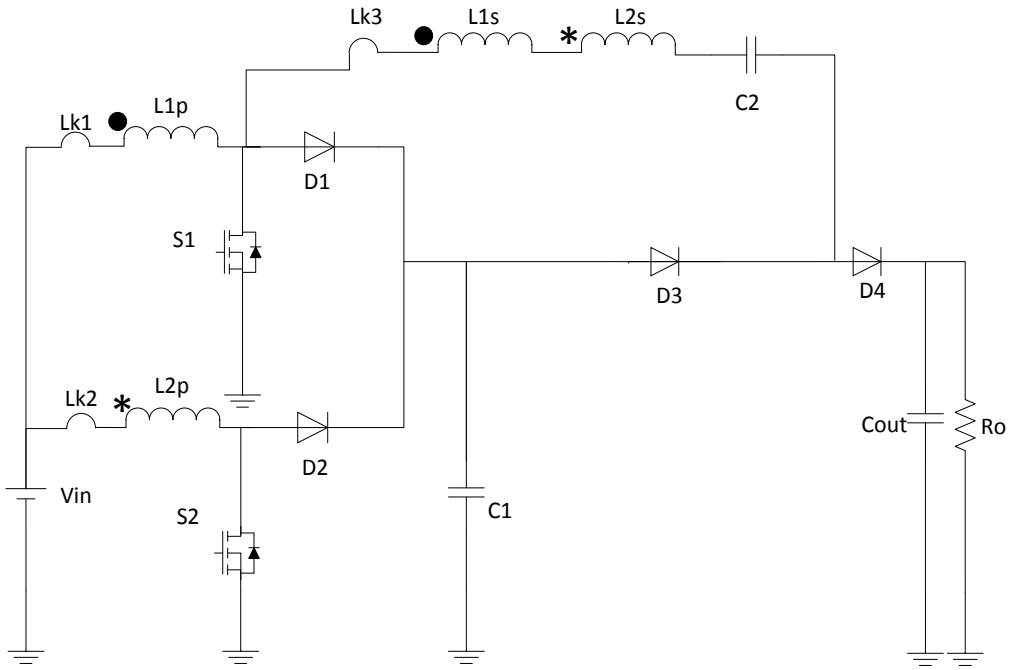

Figure 3.13 Equivalent circuit with leakage inductance

When taking leakage inductance into picture, diode D_2 is added to allow the energy stored in leakage inductance flow into C_1. Another big difference is the operation modes. By adding leakage inductance into account, more transients will happen during the modes introduced earlier. The transient modes are analyzed and they are marked in switch pattern, as Figure 3.14 shows.

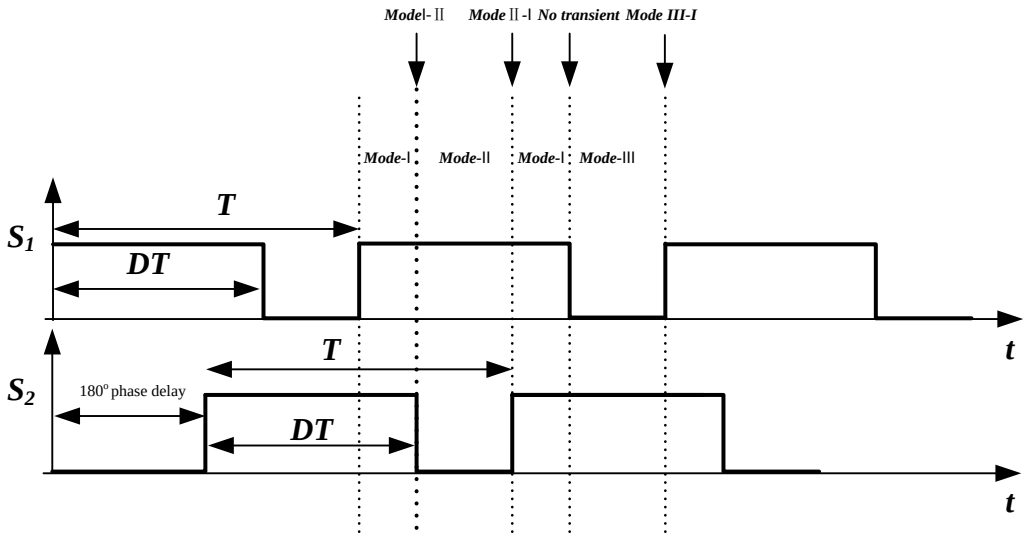

Figure 3.14 Switch pattern with leakage inductance

Mode I-II: During this transient mode(see Figure 3.15), switch S_2 is turned off. Diode D_2 is forced to turned on and capacitor C_1 is charged through source. Meanwhile, D_3 is forward biased and capacitor C_2 is charged by the source. Secondary windings are forced to conduct through S_1. The energy stored in leakage inductance keeps D_2 conducting till all the energy is transferred to C_2.

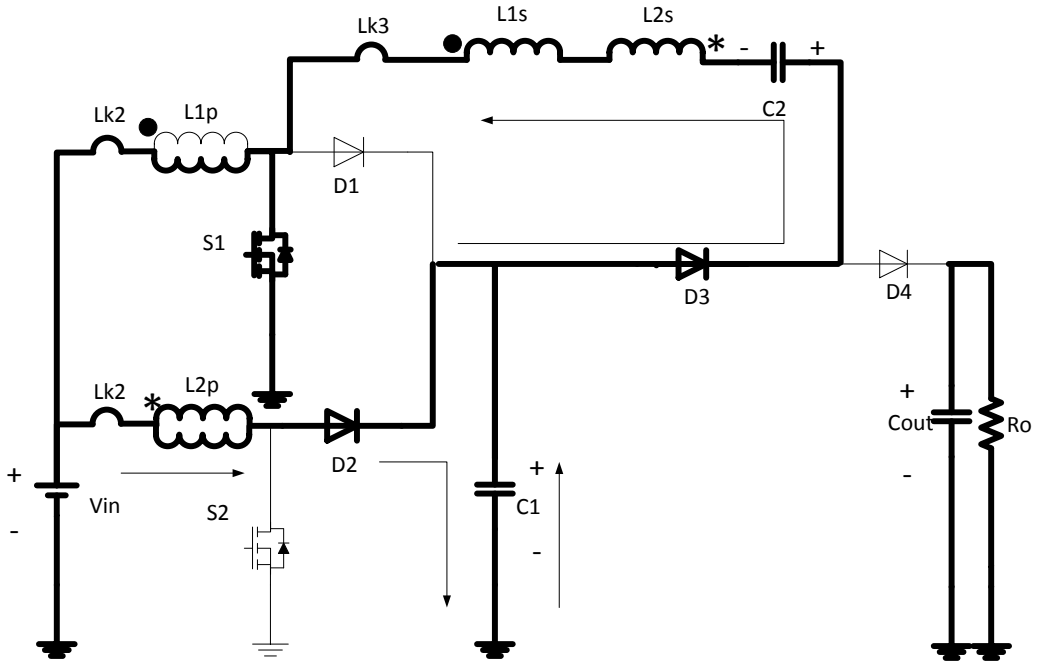

Figure 3.15 Transient mode I-II

Mode II-I: During this mode(see Figure 3.16), switch S_2 is turned on. Source begins to charge L_2. D_2 is reverse biased. C_1 continues to charge C_2 until C_2 is fully charged. The energy stored in leakage inductance on secondary windings of the coupled inductors reaches zero which leads to the end of this mode.

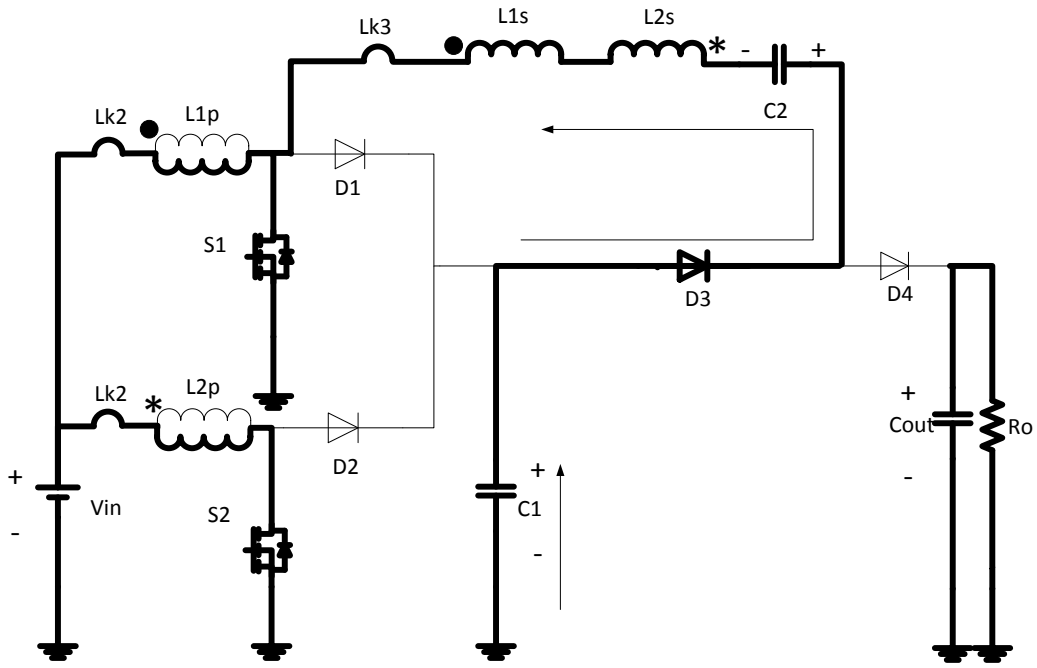

Figure 3.16 Transient mode II-I

Mode III-I: In this mode(see Figure 3.17), capacitor C_1 has been fully charged by the source through D_1 and thus D_1 is reversed biased. C_{out} is still being charged until S_1 turns on and Mode II starts.

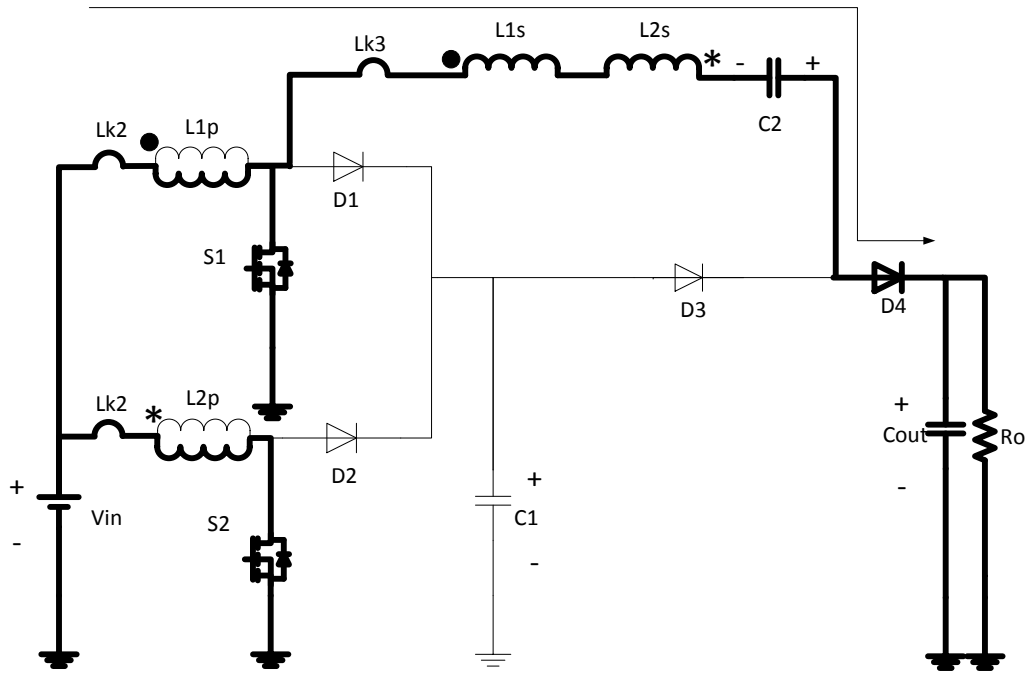

Figure 3.17 Transient mode III-I

4. HARDWARE TEST RESULTS AND ANALYSIS

In order to verify converter performance other than simulations, the circuit is built on the breadboard. The circuit is tested under open-loop condition. The input side is an Agilent Tech N5766A DC power supply instead of a set of solar panel, which gives constant input voltage and current. The load is composed of pure resistors. Components and Parameters are listed as Table 4.1 and Table 4.2.

Table 4.1 Test condition and components list

Components	Parameters
V_{in}(input voltage)	20V
V_{out}(output voltage)	400V
F_s(switching frequency)	50kHz
Duty cycle	0.71 for proposed converter 0.78 for interleaved boost converter
Output Power range	100W-270W
N(turns ratio,n_2/n_1)	20/40

Table 4.2 Components list

L_M(magnetizing inductance)	98µH
C_{out}(output capacitor)	B43504A5477M(450V,470µF)
R_{Cout}(ESR of C_o)	0.29Ω
S_1 and S_2	IRFP4568
D_4(output diode)	VS-ETL1506-M3
D_3	VS-ETL1506-M3
C_2	EEU-EE2E470S
R_{C2}(ESR of C_2)	0.12 Ω
D_1 and D_2	FES16DT-E3/45GI-ND
C_1	EEU-EE2E470S
R_1(ESR of C_1)	0.12 Ω

4.1. INPUT AND OUTPUT WAVEFORMS

4.1.1. Input Voltage and Current. Input voltages and currents are measured by an MSO4034 oscilloscope with current and voltage probe. The scale is as in waveform. All the measurements are done on breadboard with 200 Watts of output power. The input voltage is around 20 V and the input current is around 11 A. The high frequency spikes come from the series small inductance in the long connection wires. Both topologies are facing this problem since all the waveforms are obtained on breadboard. Employing PCB design would decrease these spikes. The input voltages and currents of both converters is shown in Figure 4.1 through Figure 4.4.

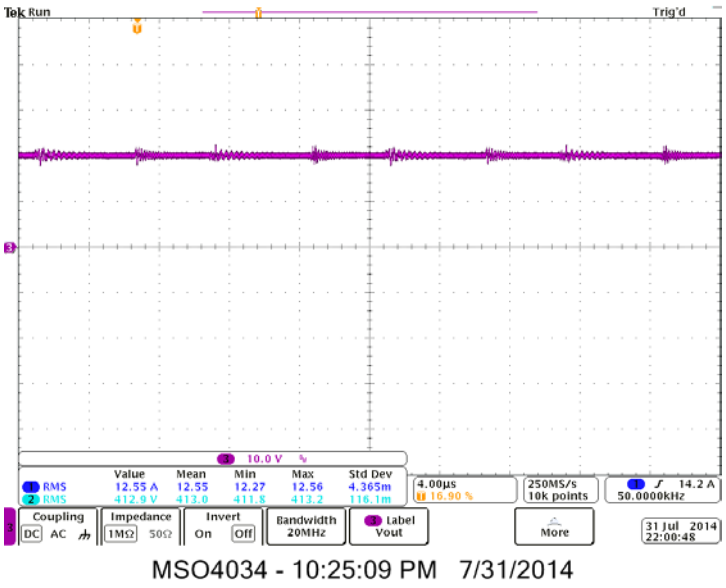

Figure 4.1 Input voltage of interleaved boost convert in [6] (10V/div)

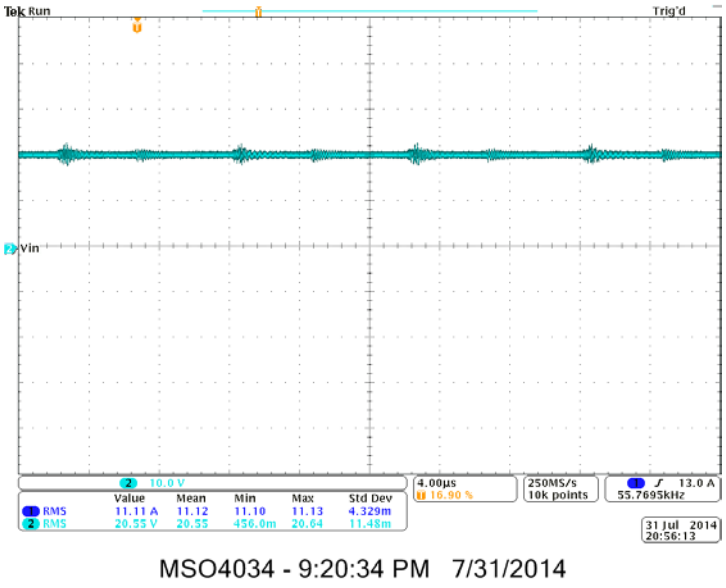

Figure 4.2 Input voltage of proposed converter (10V/div)

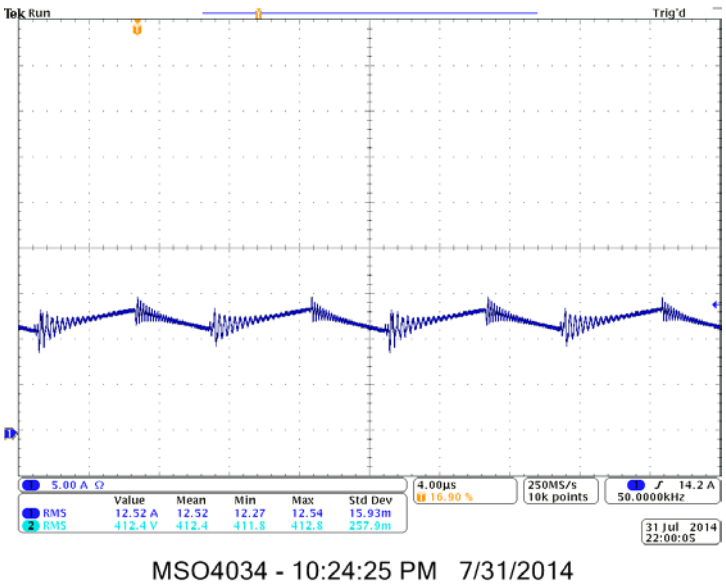

Figure 4.3 Input current of interleaved boost convert in [6] (5A/div)

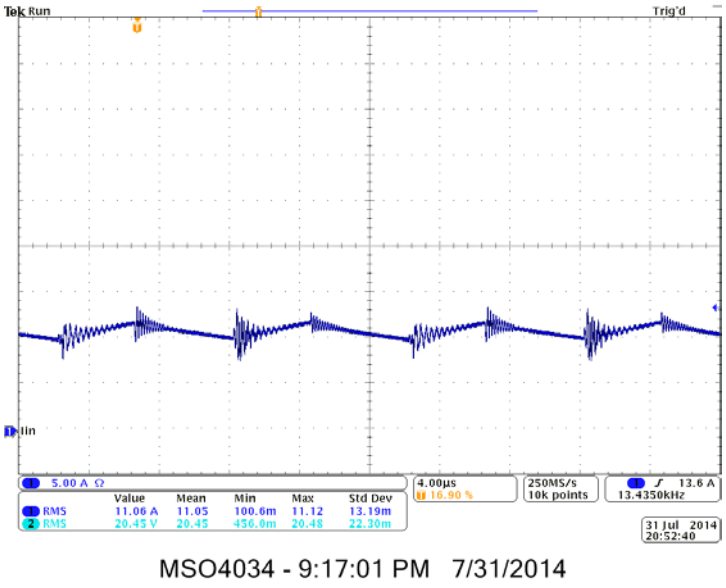

Figure 4.4 Input current of proposed converter (5A/div)

4.1.2. Output Voltage and Current. Both converters' output voltages and currents are flat and constant as depicted from Figure 4.5 through Figure 4.8. There is not much difference between these voltages and currents. This means regarding of the output voltage and current, both converters' performance are in the same level and there is no significant distinguish between them.

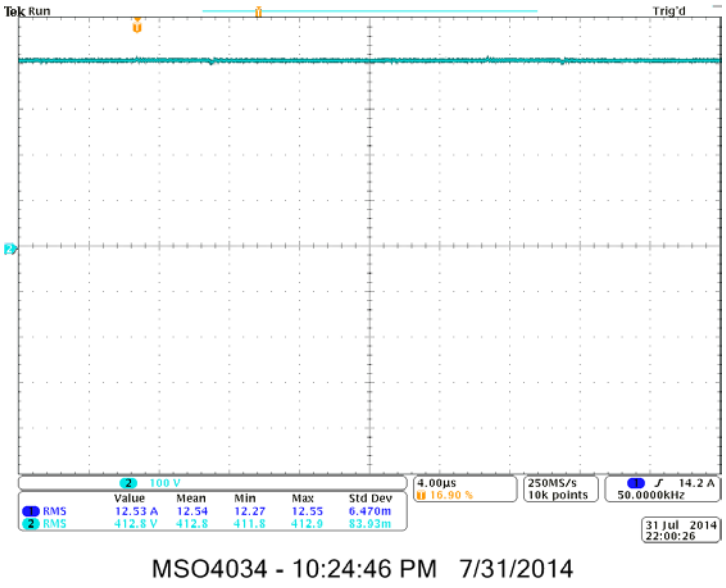

Figure 4.5 Output voltage of interleaved boost convert in [6] (100V/div)

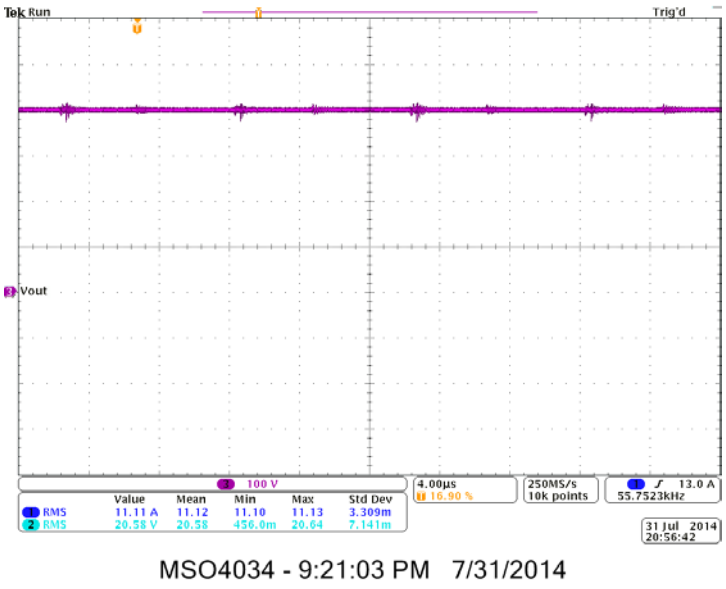

Figure 4.6 Output voltage of proposed converter (100V/div)

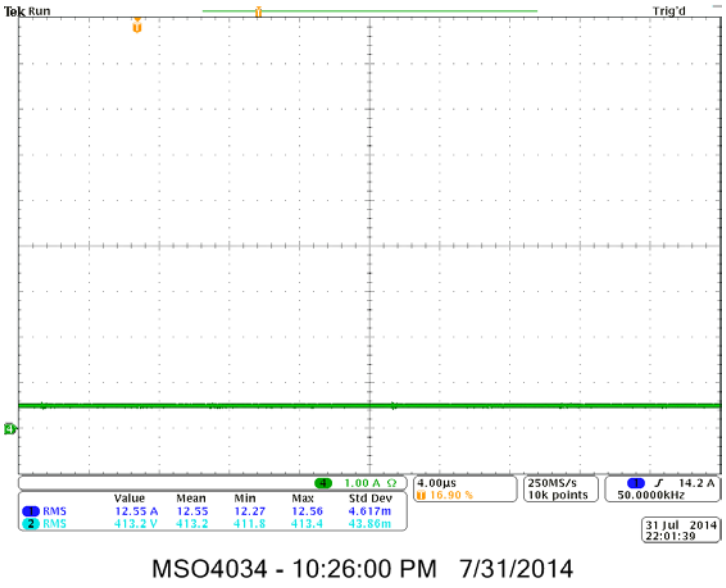

Figure 4.7 Output current of interleaved boost convert with in [6] (1A/div)

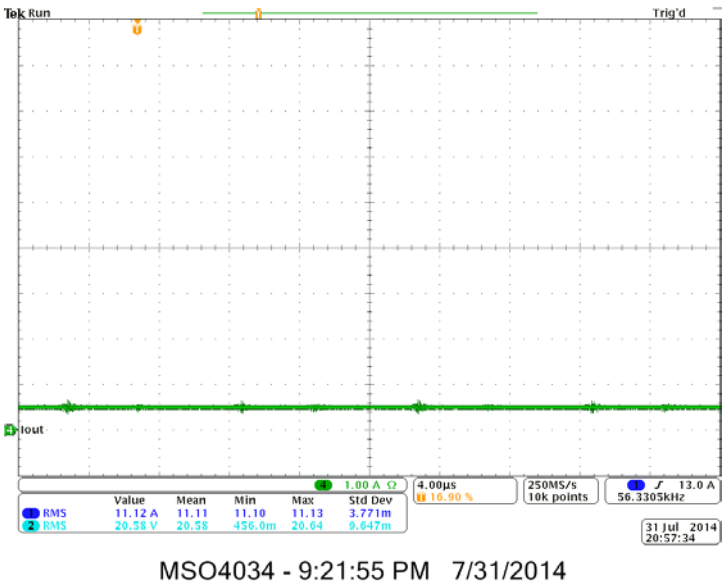

Figure 4.8 Output current of proposed converter (1A/div)

4.2. VOLTAGE STRESS ON COMPONENTS

4.2.1. Voltage Stress Across MOSFETs. The MOSFETs drain-source voltage is another concern. Normally, the smaller voltage stress could help reduce switching loss and conduction loss. In practice, MOSFETs with low voltage limit usually have a low drain-source resistance which would decrease the conduction loss. Since proposed converter has a larger voltage transfer ratio, the duty cycle would be smaller than topology in [6] which leads to a smaller voltage stress ($\frac{V_{in}}{1-D}$) across the MOSFETs as shows from Figure 4.9 through Figure 4.12 in 50V/div.

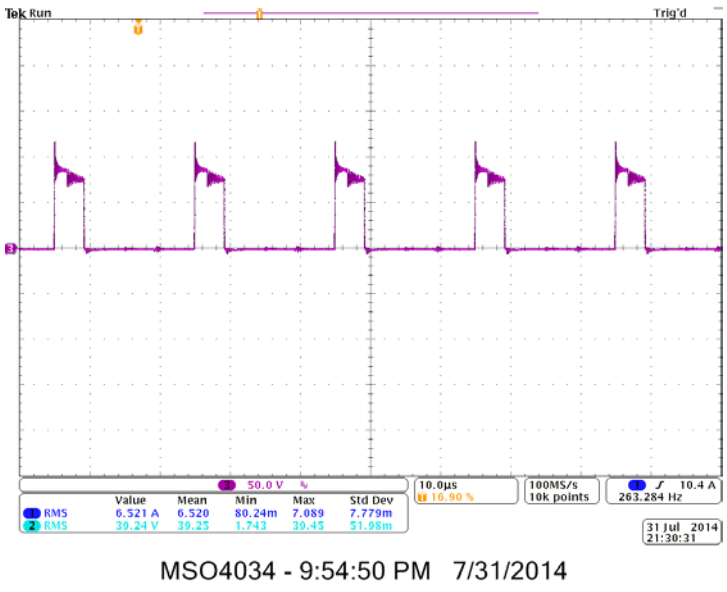

Figure 4.9 Drain-source voltage stress on S_1 of interleaved boost converter in [6]

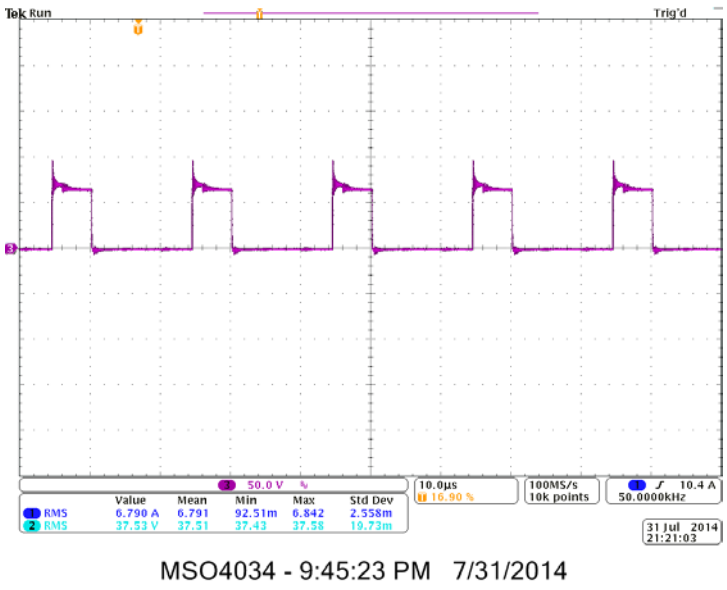

Figure 4.10 Drain-source voltage stress on S_1 of proposed converter

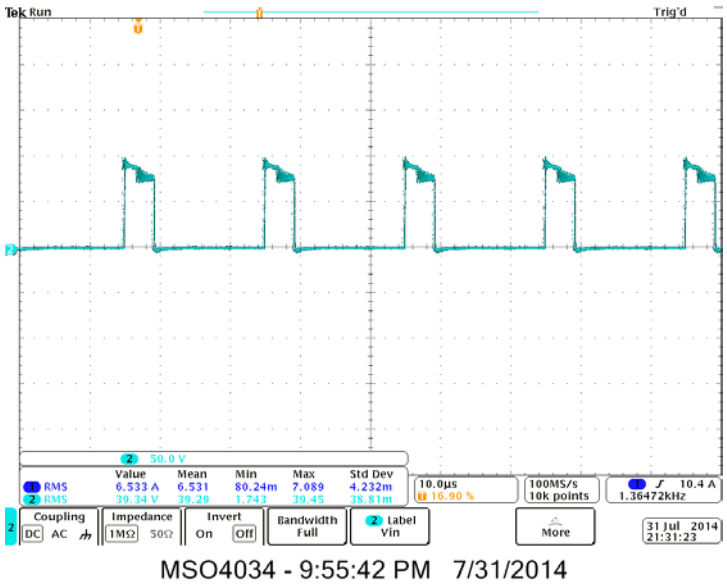

Figure 4.11 Drain-source voltage stress on S_2 of interleaved boost convert in [6]

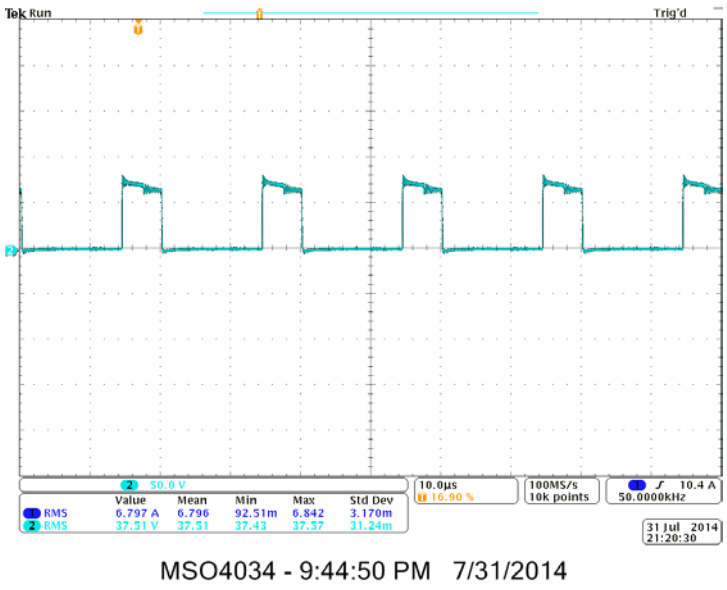

Figure 4.12 Drain-source voltage stress on S_2 of proposed converter

4.2.2. Voltage Stress on Diodes. The voltage stress on diodes has some high frequency resonations, as depicted from Figure 4.13 through Figure 4.18. This phenomenon is caused by the parasitic capacitor built in with diodes. Fortunately, this does not have an impact on efficiency because there is no current through diodes when diodes are reverse biased.

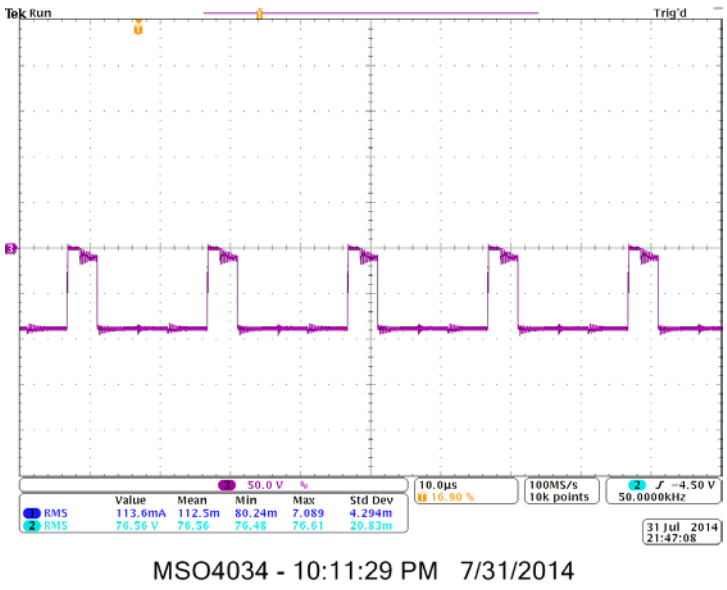

Figure 4.13 D_{C1} voltage stress of interleaved boost convert in [6]

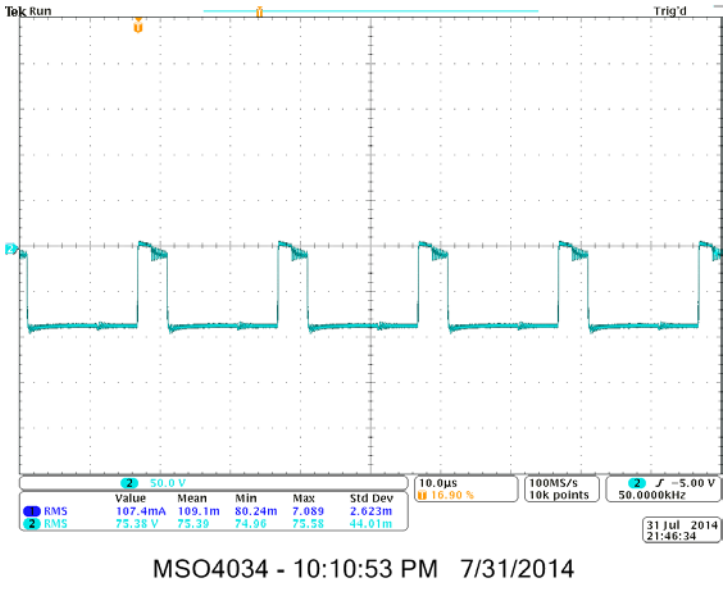

Figure 4.14 D_{C2} voltage stress of interleaved boost convert in [6]

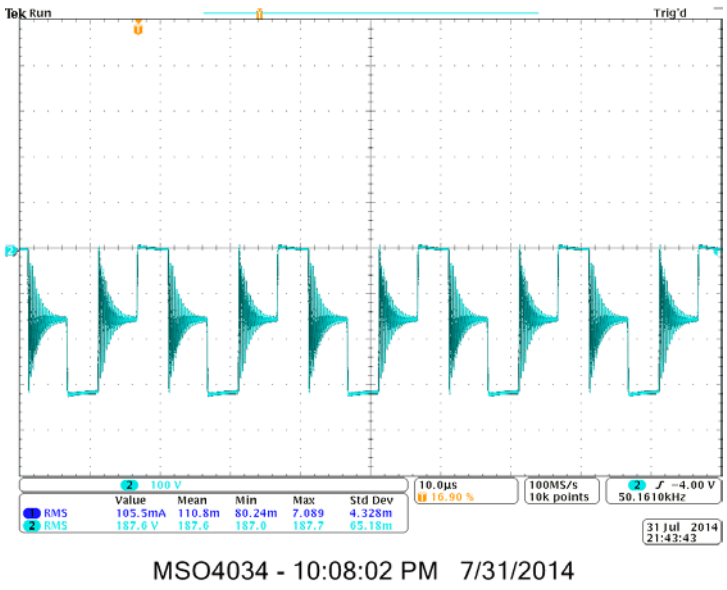

Figure 4.15 D_o voltage stress of interleaved boost convert in [6]

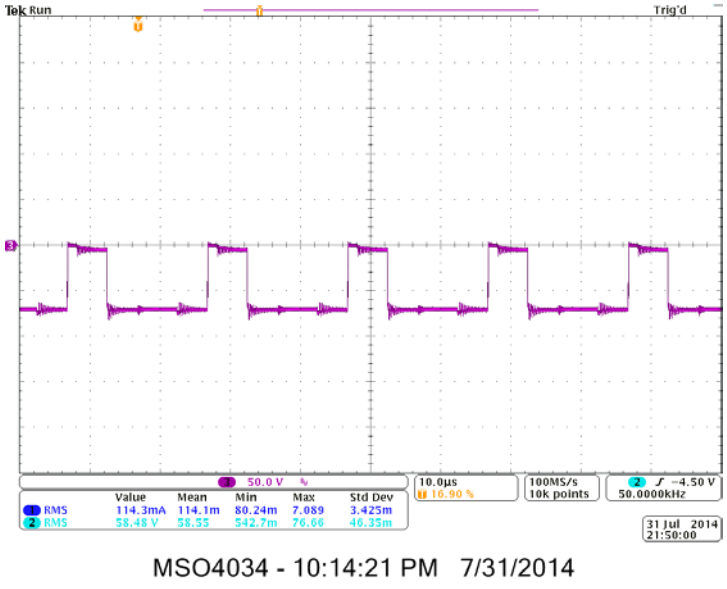

Figure 4.16 D_1 voltage stress of proposed converter

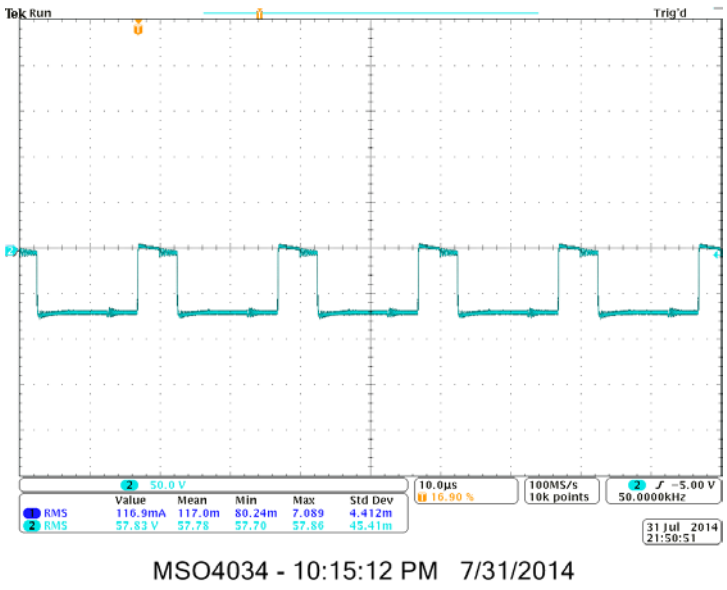

Figure 4.17 D_2 voltage stress of proposed converter

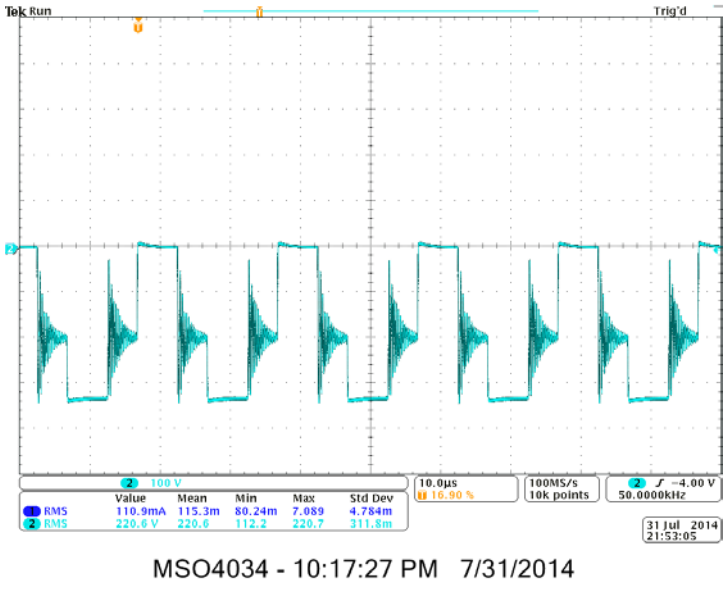

Figure 4.18 D_4 voltage stress of proposed converter

4.3. EFFICIENCY ANALYSIS

The input voltage and output voltage and current are measured by Fluke 8845A digit precision multimeter. The input current is around 12A, which is beyond the maximum current range of the multimeter, so the input current is based on the number given by power supply. These values are all RMS values. The efficiency of both Topologies are compared under the same conditions. The efficiency is defined as below:

$$\eta = \frac{output\ power}{input\ power} = \frac{V_{out,RMS} \times I_{out,RMS}}{V_{in,RMS} \times I_{in,RMS}} \times 100\% \tag{4.1}$$

Efficiency is measured under different output power with same input and output voltage. Comparison has been done between these two topologies, as listed in Table 4.3. the proposed converter has about 1% higher efficiency than the interleaved boost converter proposed in [6]. When the output power increases from 110 W to 270 W, both converters' efficiency decrease as Figure 4.19 shows.

Table 4.3 Efficiency test of both topologies

Interleaved boost converter in [6]							
Vout(V)	Iout(A)	Vin(V)	Iin(A)	Rout(Ω)	Pout(W)	Pin(W)	Efficiency
400.8	0.26464	19.881	5.83	1500	106.0677	115.9062	0.915117
400.7	0.3988	20.29	8.64	1000	159.7992	175.3056	0.911546
399.008	0.49165	20.492	10.66	800	196.1723	218.4447	0.898041
400.5	0.6763	21.11	14.37	600	270.8582	303.3507	0.892888
Proposed converter							
Vout(V)	Iout(A)	Vin(V)	Iin(A)	Rout(Ω)	Pout(W)	Pin(W)	efficiency
402.65	0.2648	20.12	5.76	1500	106.6217	115.8912	0.920016
403.8	0.3994	20.546	8.58	1000	161.2777	176.2847	0.914871
398.038	0.49202	20.5245	10.5	800	195.8427	215.5073	0.908752
401	0.6767	21.16	14.25	600	271.3567	301.53	0.899933

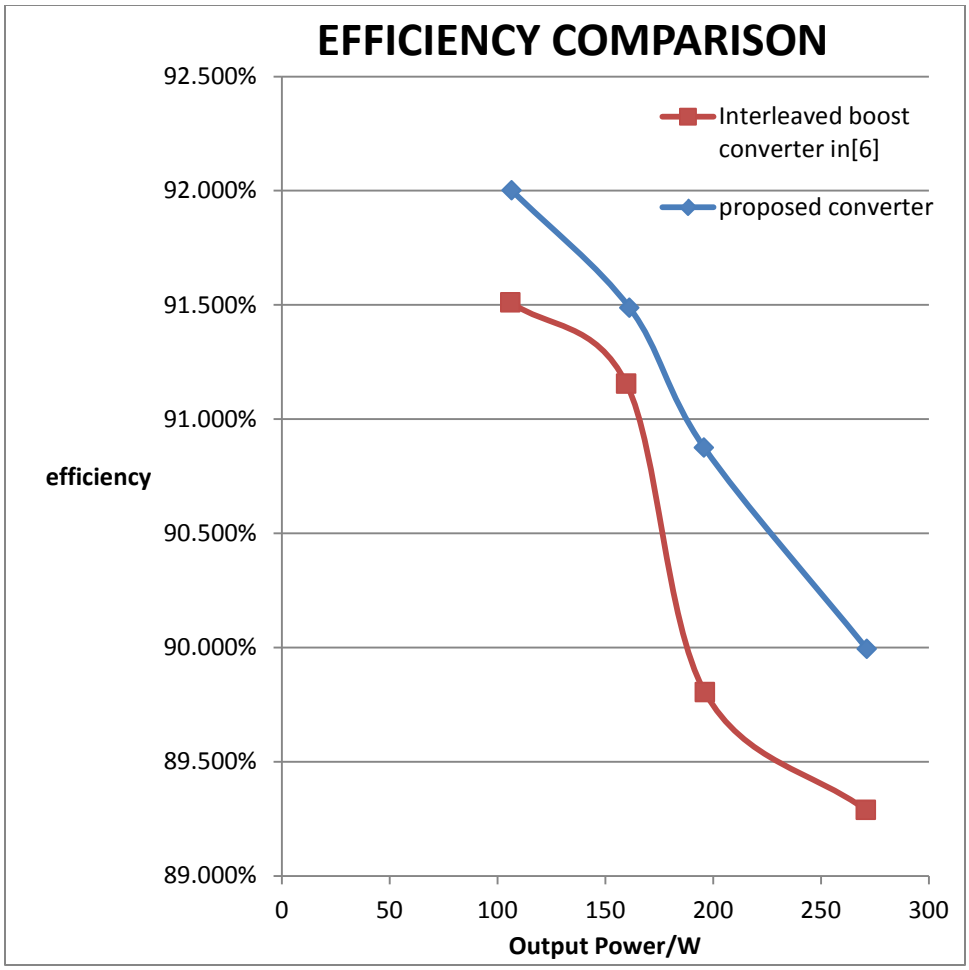

Figure 4.19 Topologies efficiency comparison

5. CONCLUSIONS

This dissertation has introduced numbers of high gain DC-DC converters with different design considerations. One particular has been analyzed to inspire a new topology. The new topology proposed is based on the interleaved converter with voltage multiplier cell with some modifications. For both converters, theoretical and experimental analyses have been performed to compare their performance. Several key improvements has been seen in newly proposed converter, including a higher voltage gain, better efficiency and a lower voltage stress on MOSFETs, compared with the former one.

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