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DESIGN AND IMPLEMENTATION OF LOW COMPLEXITY WAKE-UP RECEIVER FOR UNDERWATER ACOUSTIC SENSOR NETWORKS

by

MING YUE

A THESIS

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Approved by

Dr. Yahong Rosa Zheng, Advisor Dr. David J. Pommerenke Dr. Maciej Zawodniok

PUBLICATION THESIS OPTION

This thesis consists of the following two published or to be published papers, formatted in the style used by the Missouri University of Science and Technology, listed as follows:

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Paper II, Pages #21-#35, Y. R. Zheng, Z. Yang, M. Yue, B. Han, Z. Chen, and J. Wang, "DSP Implementation of Direct-Sequence Spread Spectrum Underwater Acoustic Modems with Networking Capability," *MTS/IEEE OCEANS 2014*, St. John's, NL, Canada, Sep. 14-18, 2014, pp.1-5. Published.

ABSTRACT

This thesis designs a low-complexity dual Pseudorandom Noise (PN) scheme for identity (ID) detection and coarse frame synchronization. The two PN sequences for a node are identical and are separated by a specified length of gap which serves as the ID of different sensor nodes. The dual PN sequences are short in length but are capable of combating severe underwater acoustic (UWA) multipath fading channels that exhibit time varying impulse responses up to 100 taps. The receiver ID detection is implemented on a microcontroller MSP430F5529 by calculating the correlation between the two segments of the PN sequence with the specified separation gap. When the gap length is matched, the correlator outputs a peak which triggers the wake-up enable. The time index of the correlator peak is used as the coarse synchronization of the data frame. The correlator is implemented by an iterative algorithm that uses only one multiplication and two additions for each sample input regardless of the length of the PN sequence, thus achieving low computational complexity. The real-time processing requirement is also met via direct memory access (DMA) and two circular buffers to accelerate data transfer between the peripherals and the memory. The proposed dual PN detection scheme has been successfully tested by simulated fading channels and real-world measured channels. The results show that, in long multipath channels with more than 60 taps, the proposed scheme achieves high detection rate and low false alarm rate using maximal-length sequences as short as 31 bits to 127 bits, therefore it is suitable as a low-power wake-up receiver. The future research will integrate the wake-up receiver with Digital Signal Processors (DSP) for payload detection.

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TABLE OF CONTENTS

PUBLICATION THESIS OPTION	iii
ABSTRACT	iv
ACKNOWLEDGMENTS	v
LIST OF ILLUSTRATIONS	viii
LIST OF TABLES	ix
SECTION	
1. INTRODUCTION	1
PAPER	
I. MICROCONTROLLER IMPLEMENTATION OF LOW-COMPLEXITY WAKE-UP RECEIVER FOR WIRELESS SENSOR NODES IN SEVERE	6
ABSTRACT	6
1 INTRODUCTION	7
2 RECEIVER ALCORITHM	' 0
3 HARDWARE IMPLEMENTATION	9 19
4 DEREORMANCE RESULTS	12
5 CONCLUSION	10 91
5. CONCLUSION	21
II. DSP IMPLEMENTATION OF DIRECT-SEQUENCE SPREAD SPEC- TRUM UNDERWATER ACOUSTIC MODEMS WITH NETWORKING CA-	
PABILITY	22
ABSTRACT	22
1. INTRODUCTION	23
2. SYSTEM DESIGN	25
2.1. SYNCHRONIZATION AND ID DETECTION	27
2.2. RECEIVER ALGORITHMS	28
3. HARDWARE IMPLEMENTATION	30
4. PERFORMANCE RESULTS	33
5. CONCLUSION	36

SECTION

2. CONCLUSION	37
BIBLIOGRAPHY	38
VITA	41

LIST OF ILLUSTRATIONS

Figur	P. P	age
1.1	Recorded UWA multipath channel	2
PAPI	ER I	
1	Frame structure for ID detection and symbol synchronization	9
2	Block diagram of the acoustic underwater wireless communication node	12
3	Two circular buffers and three DMAs are used to trade for high processing speed.	13
4	Program flow of ID detection and coarse timing synchronization	15
5	Measured Tx and Rx signals demonstrating the effect of multipath channel.	16
6	Correlator output in different channels. (A) AWGN channel.(B) Multi- path fading channel.	17
7	Receiver operating characteristic (ROC) curves for dual 31, 63, and 127 bits PN ID detection in a 60-taps multipath channel	18
8	Normalized mean square error of coarse synchronization results with different PN lengths in AWGN and multipath fading channel	20
PAPI	ER II	
1	Physical layer block diagram of the transceiver system	25
2	Frame structure for the designed DSSS system	26
3	Adaptive channel estimation algorithm.	28
4	DSP based transceiver system.	30
5	DSP Implementation.	31
6	Software design flow	32
7	Underwater ISI channels, where h_1 and h_2 are measured from underwater experiments, and h_3 is simulated Rayleigh fading channel.	33
8	Peak values of the cross-correlation and the outputs of $R[n = 63]$	34
9	The cross-correlator outputs $R[n=63]$ for the correct and incorrect ID codes	35

LIST OF TABLES

Table		Page
PAPE	ER II	
1	Parameters of the DSSS system.	. 26

1. INTRODUCTION

Underwater acoustic (UWA) sensor network is a means of underwater data acquisition and has been found a broad range of applications such as disaster relief, navigation assistance, environmental monitoring, and underwater infrastructure monitoring [1–3]. UWA sensor network uses acoustic wave to communicate among nodes that are placed underwater, rather than radio frequency (RF) waves commonly used in wireless sensor networks in air.

Acoustic signal has a great advantage to RF signal and is widely adopted in underwater communications. Radio wave always decays much faster than sound in water. It suffers a heavy attenuation in water due to the conductivity of water [4,5]. The attenuation of operation in the lowest frequency amateur band (1.8 MHz) in sea water reaches as high as 46 dB per meter [4]. On contrast, acoustic signal can propagate a very long distance up to tens of miles depending on the carrier frequency and has a smaller attenuation comparing to RF signal. For example, an acoustic signal at the frequency of 115 kHz in sea water, only has propagation loss about 104 dB per kilometer.

However, the application of UWA sensor networks is challenged by many practical problems, such as the low cost and low power consumption requirement of underwater nodes, the detrimental effects of UWA multipath channel, and the low power consumption requirement of ID detector.

The first challenge is the low cost and low power consumption requirement of underwater nodes. The low cost requirement is crucial for practical use, especially for some large-scale monitoring applications. In those applications, the cost of a node reflects the total cost of the entire system. Additionally, the lifetime of a underwater node is restricted by its power consumption, since the nodes are always powered by batteries and are expected to work underwater for more than 10 years. Therefore, low power consumption devices, such as micro-programmed control unit (MCU), have been widely adopted. However, the signal processing capability of these devices is usually weak.

The second challenge is the UWA channel. UWA channels are characterized by path loss, multi-path, fading, and delay [3]. Fig. 1.1 shows a UWA multipath channel which was recorded during the field experiment July, 2013 in Roubidoux Creek, Waynesville, MO. We can hardly distinguish a dominant path from Fig. 1.1.



Figure 1.1: Recorded UWA multipath channel.

UWA multipath channels always cause inter-symbol interference (ISI) and the Doppler effect on point-to-point communication. To combat UWA channels, several advanced signal processing algorithms are adopted to cancel those effects, such as channel estimation, equalization, coding, and orthogonal frequency division multiplexing (OFDM). Most algorithms are computationally intensive, so that they are always implemented in the high end digital signal processor (DSP) or field programmable gate array (FPGA). However, they are both expensive and high power consumption. Thus, there is a trade-off between the cost and the communication performance.

The third challenge is the low power consumption of the ID detector. The capability of networking and remoting by human are crucial to UWA sensor networks. Since the limited memory space and weak processing ability of the node, the acquired data has to be transmitted to the onshore base station for a further analysis. Thus, in order to wake up and fetch data from a specific node, the underwater node is required to have the capability of ID detection. In the practical systems, ID detection is usually conducted by DSP after the node is waken up. Due to the binary bits serving as ID, the accuracy of ID detection is influenced by the UWA multipath channels which cause a serious ISI. Thus, additional signal processing algorithm such as equalization has to be adopted to combat the ISI, which can only be implemented in DSP and will consume the power as well. Besides, every time when a signal is transmitted in the channel, each node would be waken up to check the ID even though it might be the signal transmitted to other nodes. This process results in a lot of energy waste.

The former two challenges can be solved by adopting a wake-up receiver on underwater node. It has been widely adopted in many practical systems to resolve the conflict between the cost and the performance. The wake-up receiver usually consists of a low power device and front-end. To design the lifetime expectancy of the node, the node should keep in sleep most of the time and be woken when required. If the node contains high power consumption devices such as DSP and FPGA, those devices can remain off and only turn it on by the wake-up receiver when required.

The existing approaches of the UWA wake-up receiver are mainly achieved in two ways, i.e. energy detection and carrier sensing. Before the transmission of the data, a wake-up signal is transmitted. The wake-up signal usually uses a period of the carrier or a period of chirp signal. Energy detection is the most widely and commonly used in the current UWA communication systems. It calculates the energy of a period of signal. The system is waken up when the energy of the detected signal exceeds the threshold. Carrier sensing is also used in UWA wake-up receiver. The wake-up receiver, such as the commercial integrated circuit (IC) AS3933 [6], detects the frequency based on a zero crossing counter and uses the clock generator as a time base.

However, both of those wake-up methods cannot jointly detect the ID. As a result, the energy is wasted when the node is waken up by the signal to other nodes. Although the AS3933 has the capability to detect the ID, the ID detection works as a function after the carrier is detected and cannot combat the multipath. Until now, none of the experiment results show the ID detection capability of AS3933 in UWA applications.

To avoid this situation, the ID detection should be conducted in the wake-up receiver, instead of the DSP, with the capability of combating the UWA multipath channel. When the node stand-by in a sleep mode, the wake-up receiver is always listening to the channel for its ID. Thus, the ID detection has to be conducted in realtime. Due to the low processing power of the MCU and the influence of the UWA multipath channel, the desired wake-up and ID detection algorithm should combat UWA multipath channel with low complexity and can be executed in real-time.

In the thesis I propose a novel method which can jointly achieve wake-up, ID detection, and coarse synchronization with very low complexity and self-adapting to severe multipath channels by utilizing a dual pseudo-noise (PN) sequences. Compare to the existing approaches, the algorithm can greatly reduce the power consumption of the nodes by reducing chance of the nodes mistakenly woken up by other's ID. The length of the gap between the two PN sequences represents an ID of node. The ID detection is based on the energy detection and conducted by calculating the auto-correlation from two apart portions of the received signal. When an ID

is matched a peak will be detected, and the index of the maximum value of the correlation peak corresponds to the starting index of the frame. I further optimize the method of calculating the correlation. After reducing the complexity, the algorithm is successfully implemented in an MCU MSP430F5529 and can be executed in real-time. Our wake-up receiver implemented by MSP430F5529 has a very low power consumption which is only 7 mW when working at 8 MHz and will only wake-up by the correct ID. By comparison, the practical wake-up receivers using the commercial energy measurement ICs have a higher power consumption. For example, the power consumption of ADE7566 is 14 mW. The practical wake-up receivers will wake-up the DSP for ID detection every time when a signal is received.

This thesis contains two conference papers. Paper I explains the proposed joint ID detection and coarse synchronization algorithm, demonstrates the implementation in MSP430F5529, and evaluates the algorithm by MATLAB simulations. It shows the contribution in jointly achieving wake-up, ID detection and coarse synchronization in the MCU and combating the UWA multipath channel with very low complexly. Paper II presents the proposed ID detection algorithm serving as a part of the functions in a DSP implementation of direct-sequence spread spectrum underwater acoustic modems.

I. MICROCONTROLLER IMPLEMENTATION OF LOW-COMPLEXITY WAKE-UP RECEIVER FOR WIRELESS SENSOR NODES IN SEVERE MULTIPATH FADING CHANNELS

Ming Yue, Y. Rosa Zheng, Zhenrui Chen, Yunfeng Han

ABSTRACT—This paper proposes a low-complexity dual pseudorandom noise (PN) scheme for identity (ID) detection and coarse frame synchronization. The two PN sequences are identical and are separated by a specified length of gap which serves as the ID for different sensor nodes. The receiver ID detection is implemented on a microcontroller MSP430F5529 by calculating the correlation between the two segments of the received signal with the specified separation gap. When the gap length is matched with the ID, the correlator outputs a peak which sets the wake-up enable. The time index of the correlator peak is used as the coarse synchronization of the data frame. An iterative algorithm is used that requires only one multiplication and two additions for each sample input regardless of the length of the PN sequences, thus achieving low computational complexity. The proposed dual PN detection scheme has been successfully tested by simulated fading channels and real-world measured channels. The results show that, in long multipath channels with more than 60 taps, the proposed scheme achieves high detection rate and low false alarm rate using maximal-length sequences as short as 31 bits to 127 bits, therefore it is suitable as a low-power wake-up receiver.

1. INTRODUCTION

Underwater acoustic (UWA) sensor networks have been applied to many important fields [1–3], such as underwater infrastructure monitoring [7, 8], aided navigation, oceanographic data collection. Among those applications, UWA wake-up receiver with a capability of identity (ID) detection plays an important role in reducing the power consumption and extending the battery life. However, the design of UWA wake-up receiver is challenged by the low-cost constraint and severe UWA channels. Low power devices are utilized to extend the battery life, thus the nodes in UWA sensor networks typically have weak processing ability. On the other hand, UWA multipath channels and slow propagation of sound in water cause serious inter-symbol interference (ISI). Some extraordinary signal processing algorithms are necessary to combat the effect of the ISI.

Several advanced signal processing algorithms are adopted to combat the UWA multipath channels, such as the turbo equalization technique [9, 10], orthogonal frequency division multiplexing (OFDM) using frequency domain oversampling [11] or with padding training sequence [12]. These advanced algorithms are proved to be effective to combat the effect of the ISI, but at the cost of high computational complexity, or in other words, high power consumption. For instance, the turbo equalization contains matrix inversions and several iterations, which require high end digital signal processor (DSP).

A low-power and low-complexity solution is to convert the carrier and ID detection IC AS3933 to handle acoustic hydrophone inputs [6]. The chip AS3933 is a commercial integrated circuit (IC) which is designed for active RFID tags with a low power consumption. It will be waken-up if the particular carrier has been sensed, and then check the following binary bits which means the ID of the receiver node. An experiment on the sea was conducted to evaluate the performance of the wake-up receiver by sensing carriers without ID detection, however, no strong ISI was observed

during the experiment. Since the AS3933 uses binary bits as ID without any built in mechanism to deal with the ISI, this low power solution is not suitable to combat multipath ISI channel.

This paper proposes a low-complexity wake-up receiver for UWA sensor networks. Joint ID detection and coarse frame synchronization are conducted in the wake-up receiver. By using dual pseudorandom noise (PN) sequences, the joint algorithm is designed based on auto-correlation to reduce the complexity. We optimize the calculation of auto-correlation and further reduce the computation complexity. The proposed wake-up receiver is implemented using a TI MCU named as MSP430F5529, whose power consumption is comparatively low among commercial MCUs. The performance of the wake-up receiver is verified by AWGN channels and real-world measured channels. The simulation results demonstrate a strong capability for joint ID detection and coarse frame synchronization with low complexity.

2. RECEIVER ALGORITHM

The data frame structure is depicted in Fig. 2, where in the receiver two identical PN with length of N_1 are separated by a guard interval of N_2 -bit length and a specified x-bit length for each node ID. Guard intervals are inserted into the frame to prevent the ISI from merging into either the second PN in the frame or the data at the payload. We use the length of the first zero padding (ZP) x to represent different ID. That means the start of the second PN sequence in the frame is unique to each node.

PN	Guard	ZP	RN	ZP	Guard	Payload
$\langle \dots \rangle$	k >	$ \rightarrow $	$\langle \dots \rangle$	\leftrightarrow	$\langle \rangle$	<>
N ₁	I N ₂	I X	N ₁	N ₃ -x	I N ₂	N ₄
			1	N		1

Figure 1: Frame structure for ID detection and symbol synchronization.

Let the PN sequence be b_n with $n = 0, 1, ..., N_1 - 1$ and its BPSK symbols be $c_n = 2b_n - 1$. The baseband signal corresponding to the first and the second PN sequences are given as

$$x_{b1}(t) = \sum_{n=0}^{N_1 - 1} c_n p(t - nT_0), \qquad (1)$$

$$x_{b2}(t) = x_{b1}(t - t_2), (2)$$

where p(t) is the shaping pulse, T_0 is the symbol duration and $t_2 = (N_1 + N_2 + x)T_0$. Thus, the baseband ID signal is written as

$$x_b(t) = x_{b2}(t) + x_{b1}(t - t_2).$$
(3)

The corresponding passband signal is expressed as

$$x_p(t) = Re\{x_b(t)e^{j2\pi f_c t}\}\tag{4}$$

where $j = \sqrt{-1}$, f_c is the carrier frequency, and $Re\{\}$ is the real part of the complex variable.

Assume the baseband equivalent multipath channel is time invariant and is denoted as $h_b(t)$, then the passband channel is

$$h_p(t) = Re\{h_b(t)e^{j(2\pi f_c t + \theta)}\}$$
(5)

where θ represents the unknown phase delay. The received passband signal is then

$$y_p(t) = x_p(t) \otimes h_p(t) + \eta_p(t) \tag{6}$$

where $\eta_p(t)$ is the additive white Gaussian noise and \otimes denotes linear convolution. After bandpass sampling at $f_{samp} = 1/T_s$, the received samples are

$$y[k] = y_p(t = kT_s)$$

$$= Re\{x_b(kTs) \otimes h_b(kT_s)e^{j(\omega_F k + \theta)}\} + \eta_p(kT_s)$$
(7)

where ω_F is the normalized angular frequency at the folded frequency.

Let $K_D = D(N_1 + N_2 + x_R)$ where $D = T_o/T_s$ is the upsampling factor, then the correlation between two segments y[k] and $y[k - K_D]$ is calculated as

$$R_{y}[k] = \sum_{m=0}^{DN_{1}-1} y[k-m]y[k-m-K_{D}]$$
(8)

Let $x_R = x$ and assume the channel is time invariant. Thus the channel experienced by y[k] and $y[k - K_D]$ are the same. Then the two-segment correlator acts like a time-reversal filter. Substituting (3) and (7) into (8), we have

$$R_y[k] = R_x[k] \otimes R_h[k] + R_\eta[k] \tag{9}$$

Note $R_h[k]$ effectively shortens the channel effect and $R_x[k]$ peaks at the time index where the last sample of the second PN is obtained by the ADC.

3. HARDWARE IMPLEMENTATION

The proposed underwater acoustic sensor node consists of an acoustic transducer, an analog front-end, a Texas Instruments MSP430F5529 MCU, and a TMS320C6713 DSP, as depicted in Fig. 1. The analog front-end contains the signal conditioning circuit for the receiver side and the power amplifier (PA) for the transmitter side. On the receiver side, an instrumental amplifier (INA) with a 10 dB gain converts the differential input signal from the transducer to a single-ended signal. An 8th-order Butterworth band-pass filter after the INA then filters the noise outside the pass band and a low noise amplifier with a gain of 40 dB amplifies the signal further before sending it to the level shifting circuit to match the input range of the unipolar ADC. At the transmitter side, a class-D power amplifier was utilized to amplify the modulated signals. The advantage of the class-D amplifier is its high conversion efficiency. The pulse width modulation output of the MCU is used as the carrier signal and rectangular pulse is used as the pulse shaping filter for On-Off Keying (OOK) or Binary Shift Keying (BPSK). Therefore, no digital-to-analog converter (DAC) is required at the transmitter, simplifying the implementation.



Figure 2: Block diagram of the acoustic underwater wireless communication node.

The MCU MSP430F5529 is responsible for protocol implementation, which involves generating transmit signals, listening to the media for carrier, detecting node



Figure 3: Two circular buffers and three DMAs are used to trade for high processing speed.

ID, waking up the DSP if needed, coarsely synchronizing the data frame, collecting and storing sensing data. The DSP is used to process the payload signals with complex communication algorithms, for example, fine synchronization, fading channel estimation and equalization, spread spectrum symbol detection, and decoding.

The proposed wake-up receiver is implemented in the MCU, which includes the two functions: carrier sensing and ID detection. The major challenge of lowpower wake-up receiver design is that the correlation between the two segments of the preamble signals has to be calculated in real time as the samples from the ADC becomes available. This means that $2(N_1 + N_2)D$ samples of the 12-bit ADC outputs have to be stored and the correlation coefficient $R_y[k]$ has to be calculated in the $T_s = 1/f_{samp}$ time period. To reduce the computational complexity, we propose a low-complexity algorithm for correlator implementation:

$$R_{y}[k] = R_{y}[k-1] + y[k]y[k-K_{D}]$$

- y[k - DN₁]y[k - DN₁ - K_D]
= R_y[k - 1] + MPY[k]
- MPY[k - DN₁] (10)

where MPY[] represent the multiplication result in the multiplier buffer.

The recursive algorithm for $R_y[k]$ calculation requires two multiplications and two additions at each time instant k. In contrast, if a single PN is used and crosscorrelation between a local PN and the received signal is to be calculated, then N_1 multiplications and N_1 additions are required, as shown in (7). The proposed recursive algorithm can be implemented by two circular buffers, a multiplier (MPY), and an adder, as illustrated in Fig. 3. The first circular buffer stores the ADC output samples y[k] through $y[k-2(N_1+N_2)D)]$ via DMA1 (direct Memory Access). The multiplier MPY fetches the samples y[k] and $y[k - K_D]$ simultaneously via DMA2 and DMA3 computes the multiplication in three MCLK cycles, and then stores the multiplication output to the second circular buffer, which is denoted as MPY[k]. The multiplication of $y[k - DN_1]y[k - K_D - DN_1]$ is calculated prior to $y[k]y[k - K_D]$ and is stored in $MPY[k - ND_1]$ in the second buffer. A 4-byte memory unit is required to store the correlator output and its delayed sample $R_y[k-1]$ is sent to the adder. The adder also fetches MPY[k] and $MPY[k-DN_1]$ via timer interrupts and calculates the two additions in 24 MCLK cycles. The proposed implementation uses memory to trade for processing speed.

We used an 8 MHz oscillator as the main clock of the MCU and adopted a 50 kHz sampling frequency at the ADC. All of the operations had to be completed before the next sample was accepted, which was within 160 clock cycles. The memory space of the MCU is scarce and we reduced the size of the MPY buffer by truncation. Our ADC is 12 bits and the multiplication result is 24 bits which is 4 bytes in memory. We set the ADC to be left justified (the result saves in the higher 12 bits of the 16-bit register), thus only the highest 24 bits of the multiplication are valid. We then abandoned the lower 16 bits of the MPY32 result register which include 8 invalid bits. As a result, the storage of the multiplication results is reduced to only 2 bytes memory per sample.

The software flow of the ID detection algorithm is presented in Fig. 4. We set a threshold to detect the peak of the correlator output. The peak values were saved in a variable for DN_1 samples, even after a wake up. The index of the frame start corresponds to the index of the maximum peak value. Since the dual PN correlation may be distorted by channel correlation and the proposed recursive algorithm cannot produce a sharp peak, the index can be treated as coarse synchronization output.



Figure 4: Program flow of ID detection and coarse timing synchronization.

4. PERFORMANCE RESULTS

The UWA channels are characteristic of both long delays and severe multipaths. The channel we used in the simulation was recorded during the field experiment July, 2013 in Roubidoux Creek, Waynesville, MO. The channel had 60 symbol-spaced taps with a symbol duration $T_s = 0.1ms$. The multipath causes serious ISI, and leads to the signal overlap itself. We transmitted an OOK signal to demonstrate the influence of ISI in the Fig. 5 for observation purposes.



Figure 5: Measured Tx and Rx signals demonstrating the effect of multipath channel.

The peak values of the auto-correlation, when the ID was matched and when it was not, are illustrated in Fig. 6. The left subfigure of Fig. 6 is the theoretical value when the channel is an AWGN channel without multipath. The right subfigure is the result under the UWA multipath channel. Two remarkable results are observed in the simulation. The first observation is that, the correlation result perform as a noise when the ID is not matched. The value of the correlation peak is small when compared to the value when the ID is correct. In this case, we can easily set a suitable threshold to detect. The second observation is that the trend of correlation result in the multipath channel is consistent with the value in the AWGN channel and only one significant peak is observed. Therefore, the algorithm can successfully overcome the influence of severe multipath.



Figure 6: Correlator output in different channels. (A) AWGN channel.(B) Multipath fading channel.

We simulated the performance in our channel with different signal noise ratios (SNR). The SNR was defined at the receiver after the signal was downsampled by the ADC, and we normalized the SNR to each symbol [13]. We evaluated the probability of correct detection and the probability of false alarm. The probability of correct detection was defined as the probability of the node being successfully waken-up by its corresponding ID. We also defined the probability of false alarm to be the sum of the probability of being mistakenly waken-up by other users IDs and the probability of mistakenly waken-up when nothing is transmitted. We obtained the probability of correct detection and the probability of false alarm by changing the level of threshold. The receiver operating characteristic (ROC) curve, is shown in Fig. 7.



Figure 7: Receiver operating characteristic (ROC) curves for dual 31, 63, and 127 bits PN ID detection in a 60-taps multipath channel.

The ROC curves highlight the tradeoff between the probability of correct detection and the probability of false alarm when selecting the threshold. The performance of the receiver is better when the curve is near the left, top corner of ROC plot. In contrast, the performance deteriorates as the curve follows the bottom, right region of ROC plot. The performance becomes better with the increasing length of PN sequence. When the receivers adopts 63 bits PN and 127 bits PN, the performance is greatly improved with SNR equals 5 dB comparing to the situation when the receivers adopts 31 bits PN, as shown in see Fig. 7. We can easily identify a proper threshold, which can keep the correct detection rate above 90%, meanwhile, ensure the false alarm rate below 1%. For the other cases in Fig. 7, the performance is also acceptable. According to the ROC curve, we can still find a threshold that ensures the probability of correct detection above 80% and the probability of false alarm below 10%. The threshold and the length of PN sequence can be selected according to the need. As a result, our proposed dual-PN ID detection algorithm is robust to AWGN and UWA multipath channels with low SNR.

We simulated the performance of the coarse synchronization as well. The timing error of coarse synchronization was normalized using the symbol duration. The index of the maximum peak corresponds to the starting index of the frame as shown in Fig. 6. However, since the correlation peak is not present in an impulse with the time index, the index of the maximum peak is susceptible to the noise and the accuracy of synchronization is equally influenced by the noise, regardless of the length of PN sequence. Thus, as shown in Fig. 8, the performances are the same for different lengths of PN sequence under the AWGN channel. We can also observe the similar phenomenon from the case of multipath channel. Comparing to the curves of AWGN channel, we can find that the multipath channel has a great effect on the correlation peak, and the performance has limited promotion with the improvement of SNR. Nevertheless, it can provide a coarse frame starting index while the normalized

timing errors are within several symbol durations. Additionally, the MCU can provide the DSP with a rough data block and reduce the amount of data to be processed in the DSP. If a fine synchronization is required, it can be operated by the DSP using correlations of received signal and local PN sequences.



Figure 8: Normalized mean square error of coarse synchronization results with different PN lengths in AWGN and multipath fading channel.

5. CONCLUSION

This paper proposes a low-complexity wake-up receiver with joint ID detection and coarse frame synchronization. Dual identical PN sequences are adopted in the frame structure. By using the auto-correlation, ID detection and coarse frame synchronization are achieved with low complexity. The proposed wake-up receiver is implemented on a TI MCU MSP430F5529. The dual PN detection scheme has been verified by simulated fading channels and real-world measured channels. The results show that, the proposed scheme is suitable as a low-power wake-up receiver. Power consumption of the system will be evaluated with more details in future studies. A field test is to be conducted to verify the performance of the proposed wake-up receiver in the real-world UWA channel.

PAPER

II. DSP IMPLEMENTATION OF DIRECT-SEQUENCE SPREAD SPECTRUM UNDERWATER ACOUSTIC MODEMS WITH NETWORKING CAPABILITY

Y. Rosa Zheng, Zengli Yang, Ming Yue, Bing Han, Zhenrui Chen, and Jingtao Wang

ABSTRACT—This paper presents the hardware implementation of a Direct-Sequence Spread Spectrum (DSSS) modem with networking capability for underwater acoustic sensor networks. The hardware platform uses the Texas Instrument Digital Signal Processor (DSP) for physical layer transmission/receiving and microcontroller for network layer control and node ID detection. The system uses 125 kHz single carrier with Binary Phase Shift Keying (BPSK) for ID code modulation and DSSS For payload data detection, adaptive channel estimation is for payload data. implemented to track the time-varying frequency-selective channel and rake receiver is used with simple Zero-Forcing (ZF) equalization. For node ID detection, dual Pseudo-random Noise (PN) sequences are inserted with gaps of variable length that relates with the ID code. The cross-correlation of the two PN blocks is used to detect the ID code while providing carrier and symbol synchronization. The system is tested under real-world underwater channels with severe multipath up to 12 ms. The performance of the design is satisfactory and the computational complexity is affordable by a single DSP.

1. INTRODUCTION

Underwater acoustic sensor networks find important applications [1–3] in oceanographic data collection, underwater civil structure monitoring [14], assisted navigation, etc. Major challenges in the design of underwater acoustic sensor networks include stringent cost constraint, long-life low-power requirements, hostile underwater acoustic (UWA) channels, and slow propagation of sound waves. In particular, the reliability of physical-layer transceiver has been the bottleneck due to severe UWA channels. Also, network layer implementations remain very scarce [15–17], although many designs, such as TDMA, FDMA, CDMA, and CSMA, are available through simulations [18–20].

UWA channels are characterized by severe multipath delays and significant Doppler spreads, leading to doubly selective (time-selective and frequency-selective) channels. In single-carrier systems, multipath delays cause severe inter-symbol interference (ISI) and Doppler spreads cause time-varying frequency modulation, thus requiring advanced turbo equalization techniques [9]. In multicarrier systems like orthogonal frequency division multiplexing (OFDM) [11], ISI can be effectively eliminated by the long duration of OFDM symbols, but significant Doppler spreads lead to severe inter-carrier interference (ICI), requiring ICI compensation [21]. Yet, another viable solution for low-power underwater communication is direct-sequence spread spectrum [22], in which spreading codes are used to enhance the receiver robustness against multipath and Doppler.

Hardware implementation for high-data rate UWA transceivers are available for single carrier, multi-carrier, and OFDM systems [23, 24], which often require multiple DSPs running in parallel. Low-cost low data-rate systems are mostly singlecarrier Frequency Shift Keying (FSK) or DSSS systems. Although non-coherent detection of FSK system has proven to be satisfactory, coherent receivers are mostly challenged by the reliability of carrier/symbol synchronization. This paper proposes a low-cost low data-rate DSSS receiver implemented on a TMS320C6713 DSP and a MSP430 microcontroller of Texas Instruments. The system uses 125 kHz single carrier with Binary Phase Shift Keying (BPSK) for ID code modulation and Direct-Sequence Spread Spectrum (DSSS) for payload data. For ID detection, coherent demodulation and time correlation are used to detect the BPSKmodulated dual Pseudo-random Noise (PN) sequence. The PN sequence also serves for symbol and carrier synchronization. For payload data detection, adaptive channel estimation is implemented to track the time-varying frequency-selective channel and coherent rake receiver is used with simple Zero-Forcing (ZF) equalization. The system is tested under real-world underwater channels with severe multipath up to 12 ms. The performance of the design is satisfactory and the computational complexity is affordable by a single DSP. Without using atomic clocks in the transceivers, the hardware costs under \$1500 US for a single-input single-output system.

2. SYSTEM DESIGN

The block diagram of the physical layer transceiver is shown in Fig. 1. For the transmitter, payload information bits are coded by a rate-1/2 non-systematic convolutional channel encoder with generator polynomial $[G_1, G_2] = [7, 5]_{\text{oct}}$. A block interleaver (II) is adopted to combat burst errors encountered in UWA fading channels. The interleaved bits are mapped to binary phase-shift keying (BPSK) symbols, and then multiplied with a spreading code which are pseudo-random noise (PN) sequences.



Figure 1: Physical layer block diagram of the transceiver system.

The transmitted signal structure is shown in Fig. 2, where BPSK-modulated PN sequences, gaurd intervals, and zero padding (ZP) sequences are added before the payload block. The dual PN sequences are an identical m-sequence (maximum length sequence) for each sensor node, while different m-sequences are utilized for IDs of different sensor nodes. The m-sequences are BPSK modulated without spreading. Guard intervals are also inserted to avoid the ISI smearing into the next PN block



sequence.

or payload. The payload consists of BPSK symbols multiplied by the spreading

Figure 2: Frame structure for the designed DSSS system.

The parameters of the DSSS system are listed in Table 1, where the length of the PN and time gaps are chosen to cover the typical UWA channel length up to 60 taps. The variable length x is specific to each ID code. The payload length can be changed flexibly.

Table 1: Parameters of the DSSS system.

Parameters	Values
Length of one frame	N = 1000 symbols
Length of PN	$N_1 = 64$
Length of ZP	$N_2 = 64$
Length of Payload	$N_3 = 740$
Symbols per second	$R_s ym = 1000$
Chips per second	$R_chip = 5000$
Sampling frequency	$f_s am = 55 \mathrm{kHz}$
Carrier frequency	$f_c = 125 \mathrm{kHz}$
Coding rate	1/2

2.1. SYNCHRONIZATION AND ID DETECTION

The dual PN sequences in the frame header are used for synchronization and ID detection. Using the correlations of received signal, synchronization and node ID detection are operated. The synchronization method adopted in this hardware platform is a simplified version of the two-dimensional auto-correlation algorithm in [25]. The use of two identical PN sequence achieves the channel shortening effect similar to time reversal schemes [26].

Let the sampling interval be $T = T_{sym}/D$ with D being the upsampling factor. Denote y[t] as the received baseband signal after bandpass sampling and lowpass filtering. Two receiver buffers store the received signal blocks that are $(N_2 + x)D$ samples apart. The cross-correlation of the two stored data blocks is calculated as

$$R(t) = \sum_{m=0}^{DN_1 - 1} y^*(t+m)y(t+m+N_D)$$
(1)

where $N_D = (N_1 + N_2 + x)D$. To reduce implementation complexity, the correlations in (1) can be computed recursively by circular buffer computing only two products: the product of the first samples of the data buffer at time t and the product of the new samples that are shifted into the data buffer at time t + 1, such that

$$R(t+1) = R(t) - y^{*}(t)y(t+N_{D}) + y^{*}(t+DN_{1})y(t+DN_{1}+N_{D}),$$
(2)

Note that the buffer for the correlator output is of length $2DN_1 - 1$. Peak detection of the correlator output can be implemented by the five-point comparator as detailed in [27]. If the correlator output peaks at DN_1 -th element in the output buffer, then the time index corresponding to the peak is selected as the start of the data frame. If not, then the node ID is incorrect and no further signals are processed. To balance between buffer size and desired resolution, the correlator output may be down sampled and stored as R[n] = R(t = nD) for peak detection.

2.2. RECEIVER ALGORITHMS

The receiver algorithms for payload detection include adaptive channel estimation and channel equalization. Although UWA channels are very long, field measurements show that the channels are often very sparse with most energy of the channel impulse respond concentrated on a few taps and most taps submerged by noises. Rather than using the normalized least-mean-square (NLMS) algorithm, we adopt the improved proportionate NLMS (IPNLMS) [28] algorithm for the adaptive estimator and equalizer, as shown in Fig. 3. By utilizing the sparse nature of underwater acoustic channels, the IPNLMS method can track the time-varying frequency-selective channels, as detailed in [29].



Figure 3: Adaptive channel estimation algorithm.

To adapt the equalizer coefficients, zero forcing (ZF) equalization is adopted as te first version of the implementation. The advantage of ZF equalization is its low computation complexity. However, the performance of the underwater system can be further improved, if sufficient hardware resources are available to implement advanced equalization methods, such as Turbo equalization [9].

3. HARDWARE IMPLEMENTATION

The hardware system consists of the TI TMS320C6713 DSP starter board, TI MSP430 microcontroller launchpad, front-end daughter board, power amplifier, and acoustic bi-directional transducers. As shown in Fig. 4, the front-end daughter board integrates two analog-to-digital converters (ADC), one dual-channel digital-to-analog converter (DAC), a global positioning system (GPS) timing module, two low-noise amplifiers (LNA), and two bandpass filters.



Figure 4: DSP based transceiver system.

The transmitter synthesizes the carrier sinusoid of frequency $f_c = 125$ kHz by a lookup table stored in DSP memory. The transmitted bit ones are sent from the memory bank directly to the DAC via external memory interface (EMIF), while the bit zeros are transferred after the signs of the memory contents are flipped. The receiver implementation is shown Fig. 5, where a sampling rate of $f_s = 55$ kHz at the ADCs yields the bandpass sampled signal with a carrier frequency 15 kHz and a sampling rate of 11 samples/chip, all controlled by the timer on the DSP. Instead of using the multichannel buffered serial port (McBSP), the 12-bit ADCs communicate with DSK6713 board through the EMIF, transferring the converted digital data to EDMA. The EDMA sends an interrupt to the CPU once a frame of data is filled and data processing is initiated by software interrupts through interrupt service routines (ISR).



Figure 5: DSP Implementation.

The TI MSP430 microcontroller (MCU) is adopted for the transceiver control and power management. The MCU communicates with the digital signal processor (DSP) via the host-port interface (HPI). The MCU implements transmit/receive scheduling for the DSP and polling (or CSMA) for medium access control.

We follow the 3-step design flow for the development of the embedded programs, as shown in Fig. 6. To ensure smooth development and easy debugging, we run Matlab simulation first, then convert successful simulation to desktop C in Visual C++. The final step is to convert the desktop C to embedded C in CCS (Code Composer Studio). This flow enables easy collaboration among team members and fast progress of the final project.



Figure 6: Software design flow.

As of the writing of the paper, the hardware implementation was still a few steps away from finishing the designed project although the major functionalities were implemented and successfully debugged. Areas of improvement include: using the MCU for watchdog reception through carrier sensing, control of sleep mode/active mode for the DSP, channel codeing and decoding in DSP.

4. PERFORMANCE RESULTS

Underwater acoustic channels between a base station and two sensor nodes are shown in Fig. 7 as h_1 and h_2 , respectively. These two channels are recorded during the field experiment in July, 2013 in Roubidoux Creek, Waynesville, MO. We also simulated a severe ISI channel h_3 with an additive white Gaussian noise of 5 dB below signal power.



Figure 7: Underwater ISI channels, where h_1 and h_2 are measured from underwater experiments, and h_3 is simulated Rayleigh fading channel.

Figure 8 demonstrates the symbol-spaced cross-correlation results when the node ID is matched or mismatched with the desired node ID. The value of the cross-correlation at n = 63 indicated the peak way above the threshold if the received PN matched the correct ID, while the value R[n = 63] was very small if the received PN mismatched the correct ID, although a small peak was shown at n = 95.



Figure 8: Peak values of the cross-correlation and the outputs of R[n = 63].

The difference between the correlator outputs R[n = 63] with the matched and mismatched IDs are shown in Fig. 9, where the correct ID has an shift x = 0 and the mismatched ID has a variable shift x = 1:63. The difference of the R[n = 63] values between the matched and mismatched IDs is greater than 29 for x > 1. The results for other two channels were similar to this figure, demonstrating the robustness of the ID detection scheme against different ISI channels. However, when the PN sequences are shorter than the channel length, the effect of ISI channels can be significant, thus degrading the detection performance.

The difference between the correlator outputs R[n = 63] with the matched and mismatched IDs are shown in Fig. 9, where the correct ID has an shift x = 0 and the mismatched ID has a variable shift x = 1: 63. The difference of the R[n = 63] values between the matched and mismatched IDs is greater than 29 for x > 1. The results



Figure 9: The cross-correlator outputs R[n = 63] for the correct and incorrect ID codes. Note the scale of the difference is [-5:45] on the right side of the figure. A threshold can be set at 20 to detect the correct ID.

for other two channels were similar to this figure, demonstrating the robustness of the ID detection scheme against different ISI channels. However, when the PN sequences are shorter than the channel length, the effect of ISI channels can be significant, thus, degrading the detection performance.

5. CONCLUSION

This paper proposes a direct-sequence spread spectrum (DSSS) system with networking capability for underwater acoustic sensor networks. Digital signal processor (DSP) and microcontroller are the key components of this DSSS system. Direct-sequence spread spectrum is used to get the processing gain and improve the bit error rate (BER) performance. By polling in this system, the base station broadcast request to all users, and the corresponding node will be wake up to respond this request. Adaptive channel estimation is used to track the time-varying frequencyselective channels, By utilizing the sparse nature of underwater acoustic channels. The system has been tested with channels recorded in field experiment.

SECTION

2. CONCLUSION

ID detection is important to UWA sensor networks. The thesis proposes a joint low complexity ID detection and coarse frame synchronization algorithm with a dual PN frame structure. Since the dual PN structure achieves the auto-correlation of the channel coefficients at the receiver, it is much more robust than the traditional binary ID and can self-adapt to the server UWA multipath channels. Besides, as a wake-up receiver, it can also provide a coarse frame starting index in real-time, and further fine synchronization can be processed off-line with the local PN.

The calculation complexity of the cross-correlation is reduced by utilizing the dual PN structure. The using of DMA and dual circular buffer design ensure the algorithm can be implemented in a low processing power device, MSP430F5529, in real-time.

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VITA

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