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Analysis of factors affecting station capacitor bank switching transients

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ANALYSIS OF FACTORS AFFECTING STATION
CAPACITOR BANK SWITCHING
TRANSIENTS

by

MAHMOUD DAVARPANAH, 1941-

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A

THESIS

submitted to the faculty of the

UNIVERSITY OF MISSOURI-ROLLA

in partial fulfillment of the requirements for the

Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Rolla, Missouri

1971

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Approved by

(advisor) _____

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ABSTRACT

The problem presented here is a study using a computer program which predicts the transient response when energizing a station capacitor bank of a power system. The computer program gives the wave shape and magnitudes of switching surges obtained while energized capacitor banks at one location and showing the effect of switching a bank while adjacent banks are already energized. The over voltages are given in line-to-ground voltages on the line side of the capacitor banks as well as at lower voltage levels down to the customer 120 volts service voltages.

The purposes are to obtain the optimum values of pre-insertion resistors, the effect of time differences of the pole closures of the three phases in a two-step switching of capacitor banks, and the effect of impedance between banks as an aid in determining the location of future capacitor banks in the station. The effect of distance between banks on the frequency of transients and on magnitude of maximum voltages is investigated.

ACKNOWLEDGEMENTS

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CHAPTER I
INTRODUCTION

The purpose of the research presented in this thesis is to determine the optimum values of pre-insertion resistors and the effect of time differences of the pole closures of the three phases in a two-step switching of capacitor banks and the effect of impedance between banks as an aid in determining the location of future capacitor banks on a system.

Optimum values of pre-insertion resistors not only limit the capacitor bus voltages and currents but also limit the voltages on inductively couple circuits. These voltages may have natural frequencies which result in relatively higher voltages than those on the main bus. Resistors of suitable values very effectively limit the surge current between parallel capacitor banks for both closing and opening operations(1)*.

There are transients in three distinct frequency ranges in switching capacitor banks. The lowest one is near the 60 hertz system frequency caused by minor changes in the reactive power requirement of the power system. This transient is not given any consideration in this work because it has little effect on the customer voltage. The highest range of frequency transients is

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*Number in parentheses are references to the Bibliography

about one megahertz. These transients are referred to as
the distributed parameter transients(2). Since these
highest frequency transients are present on the bus;
the transmission lines; and the transformer, the effect
of them in capacitor switching, especially on the switching
equipment and on the customer voltage is negligable due
to attenuation and filtering by the system. The
switching of a capacitor bank is not nearly as large a
change in the system as the energization of de-
energization of transmission lines, therefore the tran-
sients are small in magnitude and quick to dissipate.

The only transients that are considered in switching
capacitor banks are mid-range transients, which range in
frequency from 100 hertz to several kilohertz. These
transients have the largest magnitudes and persist the
longest. These lumped parameter transients represent
the frequencies involved in the actual switching process
and are capable of being transmitted to the customer(3).

CHAPTER II
REVIEW OF THE LITERATURE

A. Historical Background

The use of static shunt capacitors in power systems
dates back to about 1914. For a long time thereafter
they were used to a very limited extent to supply
reactive kilovolt-amperes to loads in industrial plants
where the power factor was very low and where extra-
ordinary savings in power billing were possible through
power factor improvement. These early capacitor banks
had relatively low KVA ratings because of high cost,
large size, and excessive weight. They were located
electrically and physically close to the load.

In the period from 1924 to the present, improvements
have taken place in paper, foil, impregnants, terminal
design, processing, and testing so that the capacitors
made recently are only about one-tenth as large and
costly per kvar.

Since 1941 utilities have extended the use of capa-
citors to large blocks of 10,000 kvar or more located
at the substation. These are used alone, or in conjunc-
tion with synchronous condensers for supplying reactive
kvar to large segments of the distribution system and
for controlling voltage. The released system capacity
is generally worth many times the cost of the capacitors

required. Because of this the use of capacitors in this manner has been quite general. The reduced first cost, losses, attendance, and maintenance, compared with synchronous condensers, make this a very attractive solution of the reactive load problem. The fact that individual installations can be made as small as desired with very little increase in cost per kvar permits selection of sizes and locations to the best advantages in releasing system capacity.

B. Previous Investigation

Since the early capacitor banks were a permanent part of the system, early studies of the effects of static capacitor banks were confined to sinusoidal steady-state conditions. In an early paper Butler and Pope(4) presented a comprehensive analysis of the transients associated with the switching of capacitor banks.

Early studies in the area of capacitor switching transients were devoted primarily to the selection of suitable circuit breakers and devising switching schemes to protect existing circuit breakers (1,6,7). In these early works an ideal voltage source followed by a simple series impedance was a sufficiently accurate representation of the system. It has been proposed that for capacitor banks supplied by a transmission line, the series

impedance representation be the surge impedance of the line(8). It has also been stated that for any network configuration, the short circuit inductance should be used to represent the series impedance of the system(5).

In a more accurate representation of the system the sources are represented as a constant voltage behind a subtransient reactance. All the transformers are represented by their series reactance. The line is represented by an equivalent network and the load is modeled in lumped form. Approximately 60% of the load at each load bus is modeled as motor load which is represented as a constant voltage behind a subtransient reactance. The remaining 40% of the load at each bus is modeled as lighting load, which is represented as a shunt resistance. The loads are assumed to be located relatively close to the sub-transmission buses and are represented as being connected to the bus by a short line which is modeled as a series R-L circuit and the equivalent capacitive reactance to ground lumped at the bus(3,9,10). The representation of this model is shown in Figure 1.
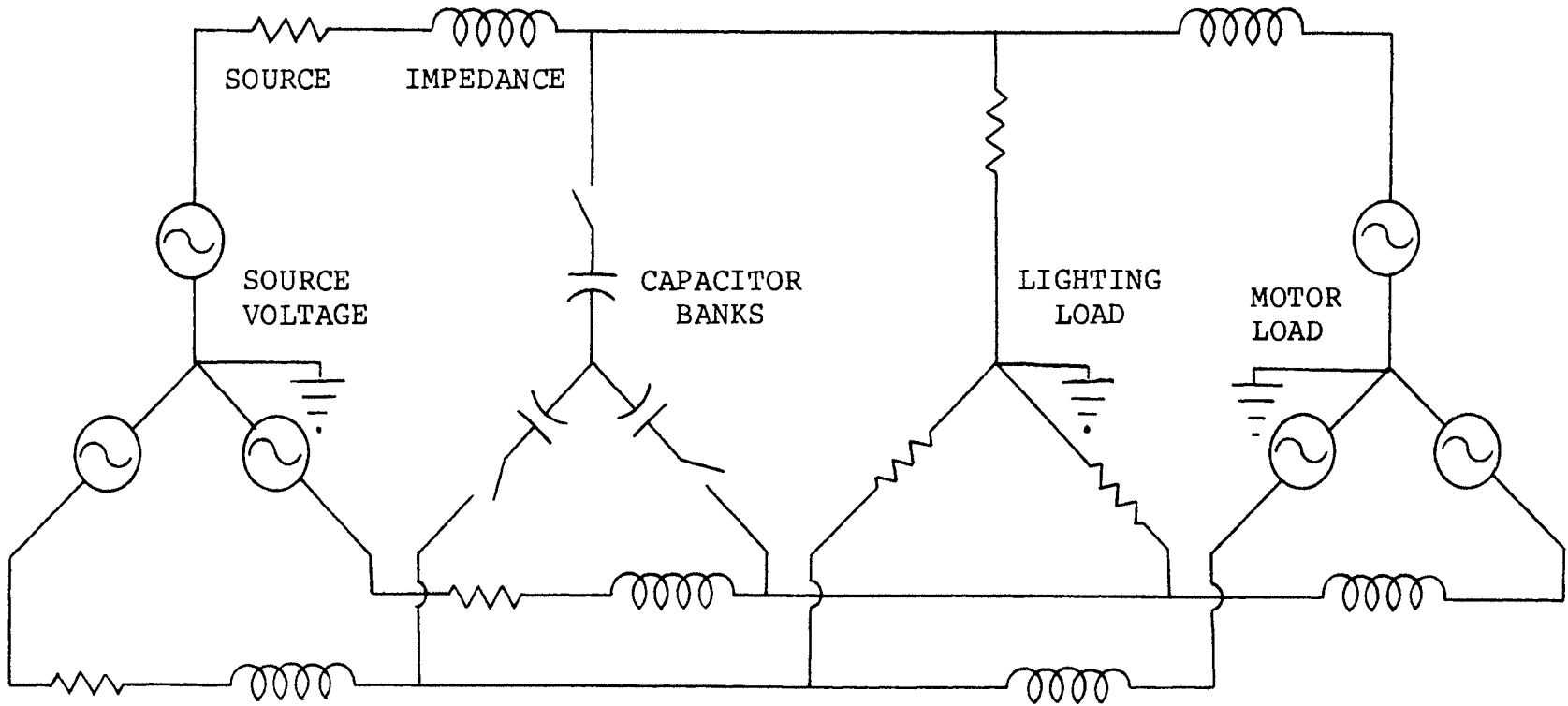
Figure 1. Three-Phase Model

CHAPTER III
DEVELOPMENT AND SOLUTION OF THE MODEL (3,10)

A. Determining the Source and Load Representation

In this part the element values from references
are presented for a specific system. The model is
applied to subtransmission station capacitor banks of a
typical company system. The subtransmission stations
of the system are supplied by one or more 120 kV lines
which with delta to grounded-wye transformers step-
down at the station to 41.6 or 24 kV.

To find the source impedance under transient condi-
tions, the effect of the magnetizing reactance of the
step-down transformers at the station should be included.
The saturated value of the magnetizing reactance of each
subtransmission station transformer is assumed to be
equal to five times the total leakage reactance of the
transformer. Both the load impedance and the magnetizing
reactance of the step-down transformer, under the steady
state condition, are larger than the source impedance.
The steady state Thevenin impedance at the subtransmission
voltage bus is approximately equal to the impedance
of the source without including the magnetizing reactance
of the step-down transformers.

For a source reactance varying from 0.2 to 1.0 times the transformer reactance, the reactance on the receiving side of the transformer under transient conditions would vary from 89.5% to 81.9% of the steady-state Thevenin reactance at the receiving side of the transformer. A reasonable value for transient reactance of the source is 70% of the steady state Thevenin reactance at the capacitor bus. The source resistance is made equal to the Thevenin resistance at the subtransmission voltage bus. To model the equivalent load, 40% of the total load is assumed to be lighting load and 60% motor load. The equivalent reactance of the motor load representation is determined by assuming the equivalent motor to have a subtransient reactance of 20% and that the equivalent motor bus is operating at 80% rated MVA.

B.   Addition of Local Parameters

Figure 1 shows a model when there is no previously energized capacitor bank in the system. To extend this model to the case when there are one or more previously energized capacitor banks, several components are added to the model. These are the supply lines from the capacitor bus to the capacitor bank, the representation of the previously energized capacitor banks at the same station and a general representation of the circuit breaker.

1. Supply Lines

If there is only a single capacitor bank in the station the supply lines have little effect on the transient response. Therefore its effect is negligible(9). However, when one or more energized banks exist in the same station, capacitor switching transients depend to a large extend on the impedance between the banks.

2. Parallel Banks

As has been mentioned, if there is a previously energized bank in the station, the representation of supply lines should be added to each phase of the model of Figure 1. In the case of more than one previously energized bank in the same station, they should be combined to a single equivalent bank, where the MVA rating of the equivalent bank is the sum of all MVA rating of the banks. To find the equivalent supply lines, an equivalent resistance is formed by taking the parallel combination of resistances of each supply line and an equivalent reactance by taking the parallel combination of reactances of each supply lines. The combining of the previously energized banks is justified because there is only small interaction between these banks under transient conditions.

3. Circuit Breaker

There is a possibility of non-simultaneous operation

of the breaker poles. In addition, pre-insertion resistors
are used in some capacitor bank circuit breakers. In
modeling the system to include pre-insertion resistors, a
two-step resistance type switching is used. In this
switching, the breaker closes in two steps. The first
inserting a resistance and the second by passing it after
a period of time. Figure 2 shows a two-step resistance
type switching. One phase of the complete model is
shown in Figure 3.

C.   The Computer Solution

    1.   Calculation of the Network Elements

    The values of the source impedances can be calculated
from the Thevenin equivalent steady state impedance.
Since the normal specification of the Thevenin impedance
is in percent, additional information is needed in order
to compute the source impedances. This additional data
is the percent Thevenin impedance; the MVA base on which
the percent impedance was calculated, and the capacitor
bus voltage in kV. Then the value of the 60-hertz source
impedance is determined in ohms and referred to the capa-
citor bus. As has been mentioned, the lighting load is
40% of the total load and motor load is 60% of the total
load. Therefore the load on the capacitor bus is used to
determine the values of the resistance for lighting load
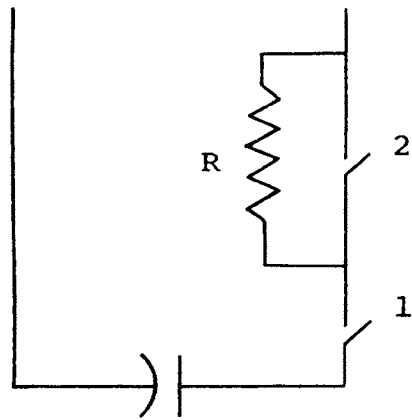
Figure 2.   2-Step Resistance-Type Switching
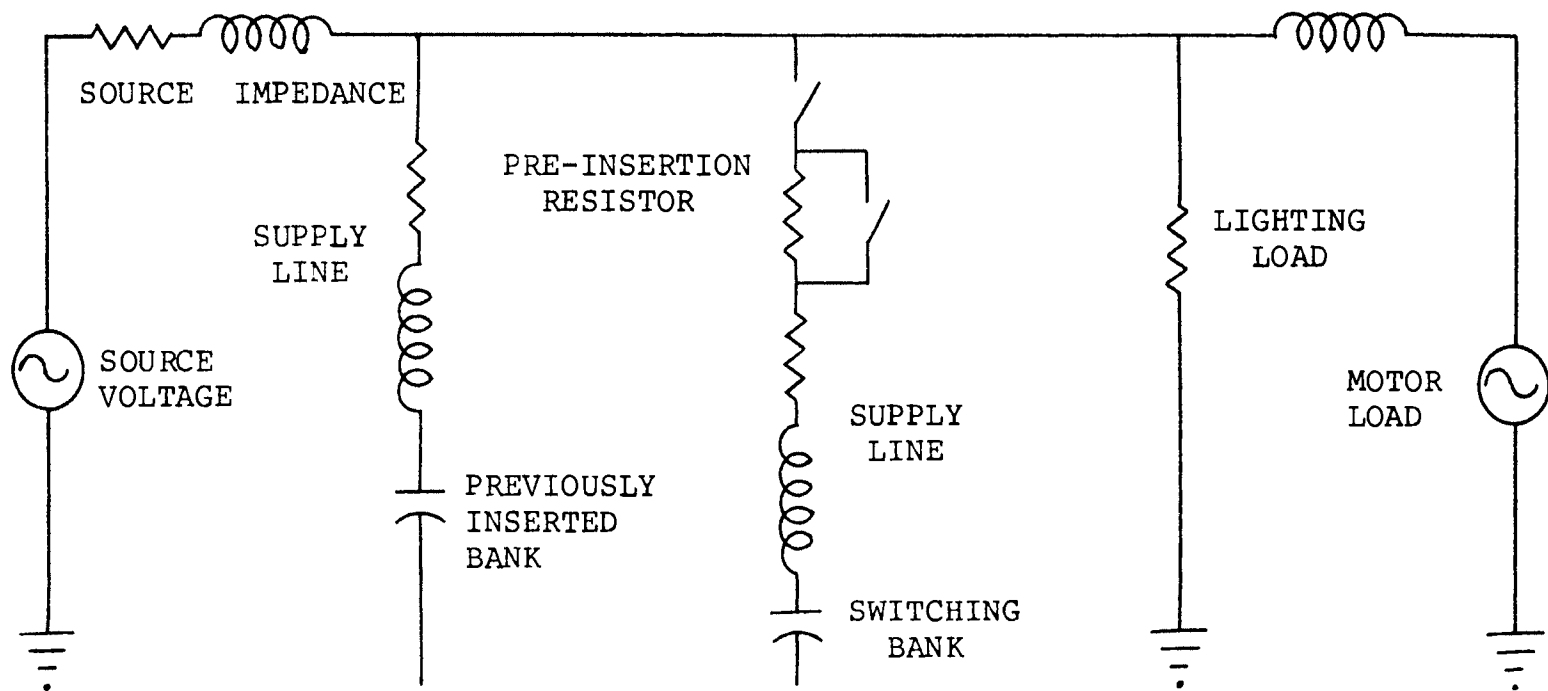
Figure 3. One Phase of the Complete Capacitor Switching
Model

and the reactance for motor load. Other information that
is needed for determining the load parameters are the bus
voltage in kV, and the load in MW and MVAR. To consider
the equivalent parallel capacitor bank, the number of
energized banks and, for each bank, the MVA rating, the
length of feeders, and the type of feeders is needed.
This step is ignored if no banks are energized. The ele-
ment values of all three phases are assumed to be the same
in the steady state condition because the network is
assumed to be balanced.

2. The Steady State Solution

The problem of finding the steady state solution
reduces to solving a single-phase circuit, since the net-
work prior to capacitor switching is in a balanced state.
The angle of the capacitor bus voltage of phase A at the
time the capacitor is to be energized is required by the
program. For non-simultaneous switching the capacitor
bank is considered to be energized when the second pole
of the breaker closes. The initial voltages and the
currents of the A-phase elements are then determined as
are the values of the Thevenin equivalent source and the
source representing the motor load of phase A. The values
of voltages and currents of phase B and phase C are then
calculated by multiplying the A-phase values by $-.5-J.86603$
and $-.5+J.86603$, respectively.

3. The Transient Solution

The transient solution is obtained by trapezoidal integration (3,10). The network configuration at any time depends on the presence or absence or pre-insertion resistors, the existance of energized banks and whether or not the breaker poles operate simultaneously.

In the case of presence of pre-insertion resistors, first the value of the supply line resistance is increased to simulate pre-insertion, and then decreased to indicate the final pole closure. The pre-insertion time of each pole is forced to be the same although there is the possibility of non-simultaneous pole closure. The length of the pre-insertion time and the value of the pre-insertion resistors are required by the program.

In the case of the existence of parallel banks the number of nodes and elements of the network will be increased and also will produce a higher frequency transient. Therefore, if energized banks are present, the program gives the values of voltage in time steps of .02 milliseconds instead of time step of .05 milliseconds when there is no energized bank. In either case, the program provides voltages for 10 milliseconds after switching.

In the case of non-simultaneous switching the A-phase pole is assumed to be closed first. This can be done without the loss of generality, because the definition of

the phase A is arbitrary. The time of closure of the
B-phase pole and the time of closure of the C-phase
pole are required by the program.

There is a possibility of non-simultaneous pole
operation of breakers employing pre-insertion resistors.
This is the most complicated switching sequence which will
occur in such a system. The time of pole A closing is
defined as time zero. The time of pole B closing and
pole C closing are TB and TC, respectively. The time of
pre-insertion is called TPRE. In this case five changes
in the network, or five switching operations occur.
However, with the ungrounded capacitor bank, closing a
single pole has no effect on the capacitor bus voltages.
Therefore, the time zero is redefined as the time of the
second pole closure. This time zero is T2 which is the
minimum of TB and TC. Now if T3 is the time of the
third pole closure, it is the maximum of TB and TC, and
in the redefined time is T3 minus T2. This switching
operations is shown in Table 1.

The program arranges all the operations in the order
of time of occurence. To calculate the transient, the
operations are performed at the appropriate times. If
there is a negative value of time, some necessary opera-
tions are performed before the transient solution is
begun.

TIME	OPERATION	NETWORK CHANGES
-T2	Initial Pole 1 Closure	Add Phase 1 Elements
0	Initial Pole 2 Closure	Add Phase 2 Elements
T3-T2	Initial Pole 3 Closure	Add Phase 3 Elements
TPRE-T2	Final Pole 1 Closure	Modify Line Resistor Phase 1
TPRE	Final Pole 2 Closure	Modify Line Resistor Phase 2
TPRE+T3-T2	Final Pole 3 Closure	Modify Line Resistor Phase 3

Table 1. Switching Operations

The program provides the three line-to-neutral voltages at the capacitor bus and the three line-to-line voltages divided by $\sqrt{3}$. Note that the line voltages divided by $\sqrt{3}$ are the line-to-neutral voltages on the distribution circuits, because a wye-delta transformation is used to step the subtransmission voltages down to the distribution voltages. These voltages are given in per unit, defining the pre-capacitor line to neutral switching voltage as one per unit.

A flow chart of this program is shown in Figure 4. A complete listing of the program is found in reference 3.
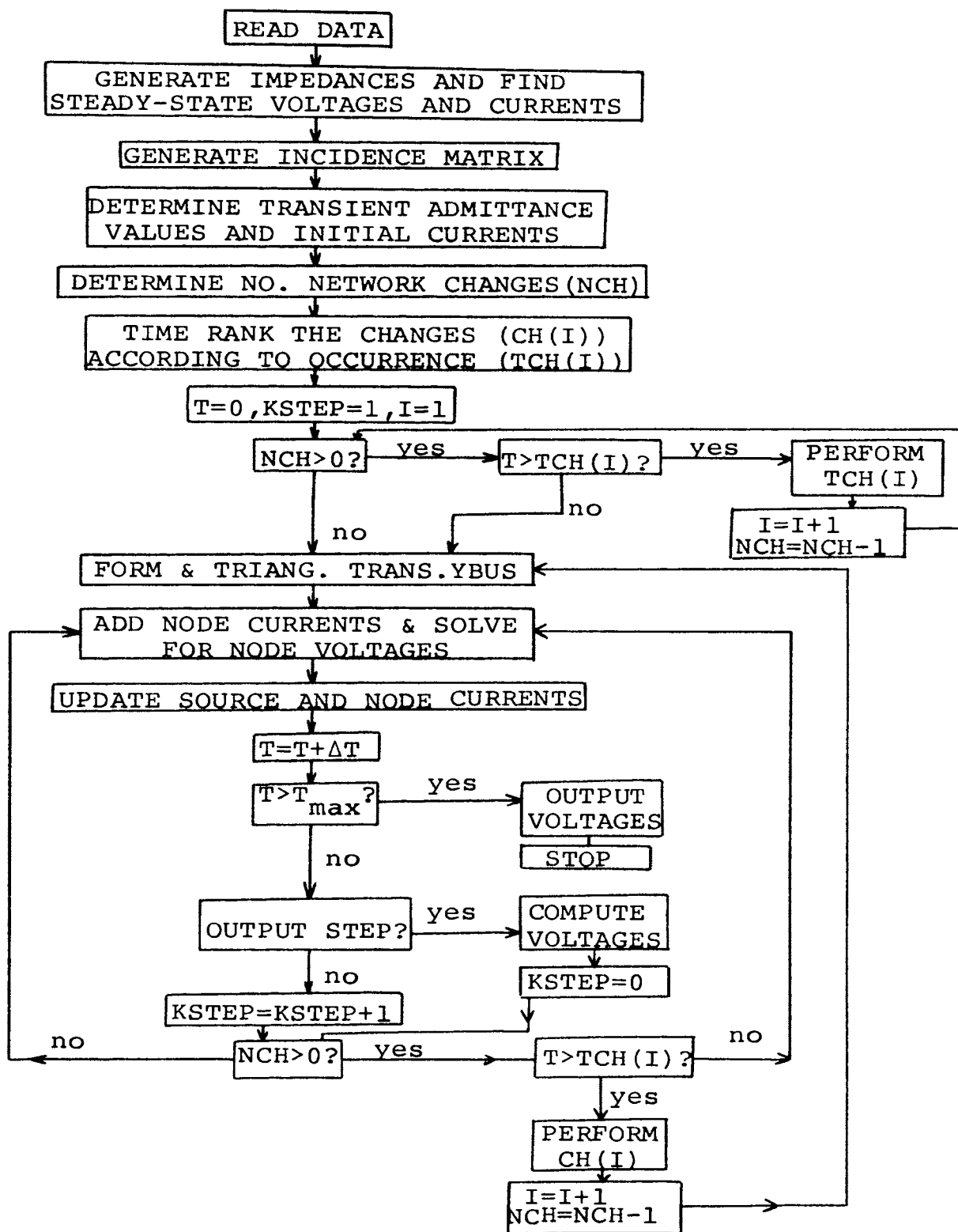
Figure 4. Capacitor Switching Program Flow Chart

CHAPTER IV
DETERMINATION OF OPTIMUM VALUE OF PRE-INSERTION RESISTORS

To determine the optimum value of pre-insertion resis-
tors, the system of Figure 5 is considered. This station
is supplied by 120 kV transmission lines. The voltage is
stepped down to the subtransmission voltage with a delta
to grounded-wye transformer connection and typically
includes a distribution station as an integral part of
the station. The capacitor bank is connected ungrounded
wye and the station has trunks and tie lines supplying
other subtransmission stations and distribution substations.
The subtransmission voltage is 41.6 kV and the capacitor
bank is 18 MVA. The bank is energized by an oil circuit
breaker equipped with pre-insertion resistors and with a
supply line of nearly 50 feet of 3/0 ACSR. Other necessary
information for this station are as follows:

1. Poles A and B are assumed to close simultaneously.
2. Pole C is assumed to close .75 milliseconds after
   closing of poles A and B.
3. The pre-insertion time is 4 milliseconds per pole.
4. The Thevenin impedance is .174+J.721 percent on a
   10 MVA, 41.6 kV base, and initial angle of $+50^{\circ}$
   for the initial closure of the A phase pole is
   also supplied to the program.
5. The load is 105 MW and 23 MVAR.
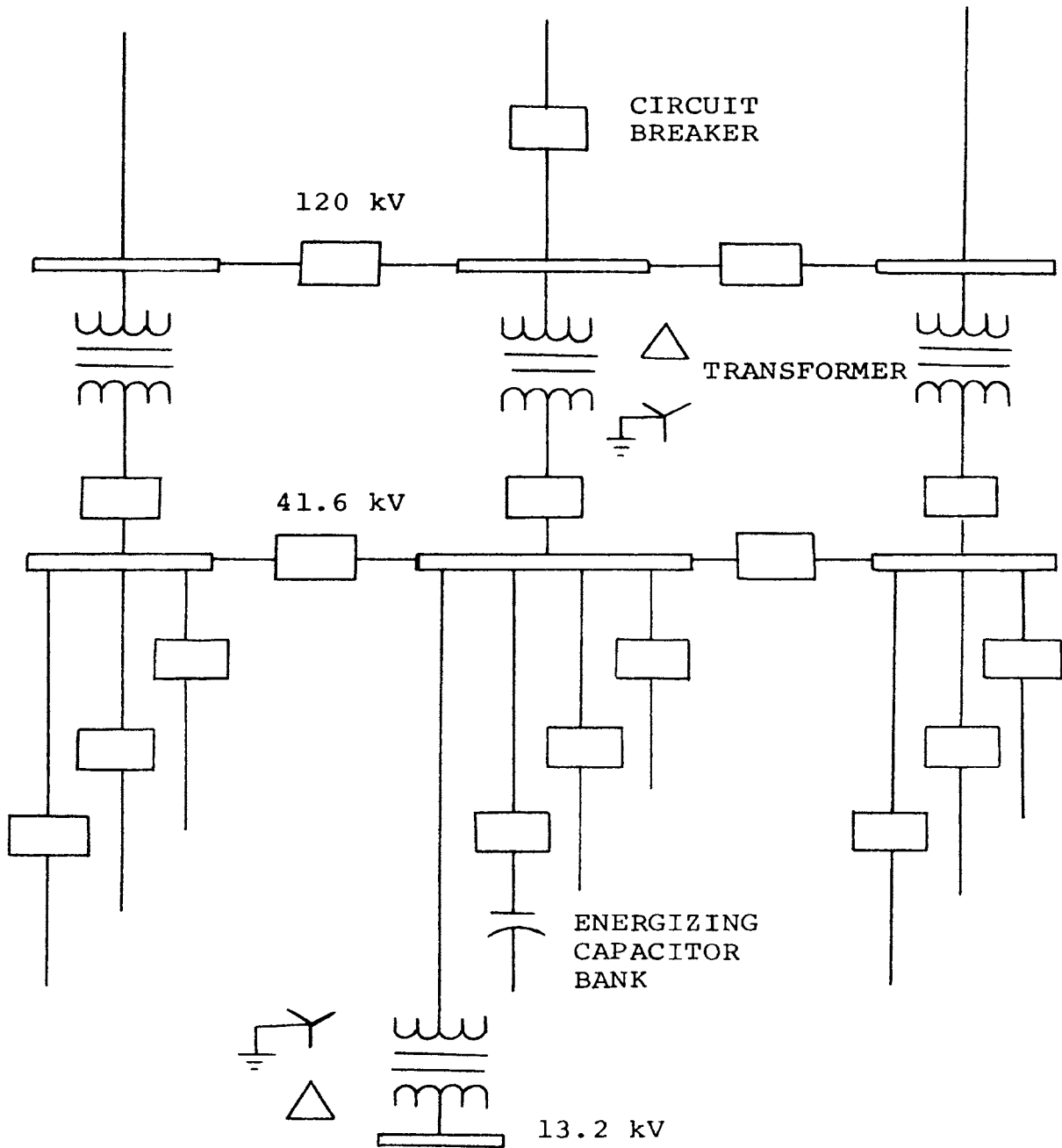
Figure 5. Simplified One-Line Diagram of a
Capacitor Bank Station

To investigate the optimum value of pre-insertion resistors which is used to keep the magnitude of transient voltage below a definite value (which is different for each capacitor bank size) and minimizing the corresponding current inrush, the following tests - each with a specific capacitor bank size - have been performed.

Test 1

The computer program is run for this test where the size of the capacitor bank is 18 MVA. The value of pre-insertion resistors varies from 0.5 ohms to 9000 ohms in this test. The results of test 1 are shown in Table 2. In this table, the first column is the value of pre-insertion resistors in ohms, the next three columns are the maximum magnitudes of the per unit line-to-neutral capacitor bus voltages with the pre-switching line-to-neutral voltage as a base. The last three columns are the maximum magnitudes of the line-to-line per unit capacitor bus voltages with the pre-switching line-to-line voltage as a base. From Table 2 it can be seen that the optimum value of pre-insertion resistor is 20 ohms per phase, because the maximum value of capacitor bus voltage among the three line-to-neutral voltages of the capacitor bus is 1.08 P.U. and the maximum value of the distributed voltage is 1.12 P.U., and they are minimum among all other maximum voltages. Note that in Table 2 the maximum value of the

Value of Pre-Insertion Resistors	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
R	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
0.5	1.54	1.15	1.17	1.45	1.09	1.22
5	1.28	1.03	1.02	1.16	1.04	1.11
20	1.07	1.08	1.01	1.04	1.12	1.03
32	1.04	1.12	1.01	1.06	1.17	1.02
40	1.03	1.14	1.01	1.07	1.18	1.01
50	1.03	1.16	1.01	1.08	1.18	1.01
100	1.05	1.18	1.00	1.09	1.18	1.00
150	1.05	1.18	1.00	1.08	1.17	1.00

Table 2. The Effect of the Value of Pre-Insertion Resistors on the Maximum Magnitude of the Transient Voltage

Value of Pre-Insertion Resistors	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
R	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
200	1.06	1.17	1.00	1.08	1.16	1.00
250	1.06	1.16	1.01	1.08	1.16	1.00
300	1.06	1.15	1.04	1.08	1.17	1.00
350	1.06	1.14	1.07	1.07	1.20	1.00
400	1.07	1.13	1.10	1.07	1.22	1.00
1000	1.07	1.10	1.20	1.06	1.33	1.02
5000	1.07	1.15	1.28	1.05	1.40	1.03
9000	1.08	1.16	1.29	1.05	1.41	1.03

Table 2 (continued). The Effect of the Value of Pre-Insertion Resistors on the Maximum Magnitude of the Transient Voltage

capacitor bus voltage is underlined and the maximum value

of the distributed voltage is double underlined. The

computer solution of B-phase transient, where R = 20 ohms,

is shown in Figure 6. Note that the maximum magnitude of

transient voltage in Figure 6 is 1.08 P.U. The value of

inrush current for each pre-insertion resistance can be

calculated by the following formula:

$$I = \frac{V}{\sqrt{R^2 + X_c^2}} \qquad (1)$$

where

    I is the magnitude of inrush current in amperes

    V is the maximum magnitude line-to-neutral
    capacitor bus voltage in volts

    R is the value of pre-insertion resistor per
    phase in ohms

    X_c is the line-to-neutral impedance of the
    capacitor bank in ohms.

For this test the value of pre-insertion resistor and

the maximum magnitude line-to-neutral voltage can be found

in Table 2. In order to convert the per unit transient

voltage to volts, the per unit values should be multiplied

by $\frac{41.6 \times 1000}{\sqrt{3}}$. The line-to-neutral impedance of a

capacitor bank is calculated by the following formula:

$$X_c = \frac{(kV)^2}{MVA} \qquad (2)$$

where
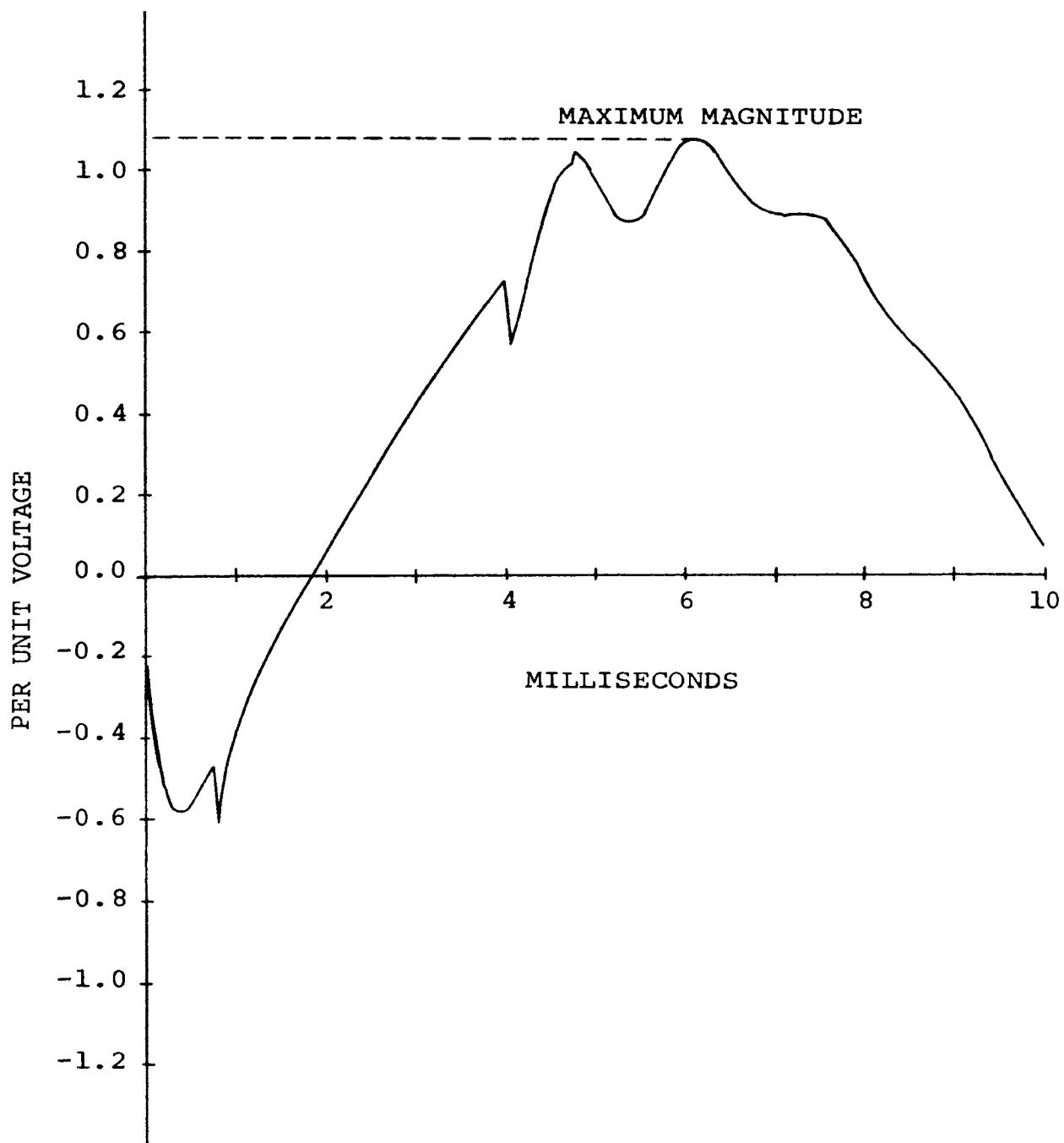
Figure 6. B-Phase Voltage Transient Response
(where R=20 ohms and bank size = 18 MVA)

X_C is line-to-neutral impedance in ohms

KV is the rated capacitor bus voltage in kilovolts

MVA is the capacitor bank size in megavolt-amperes

The impedance per phase of the capacitor bank in this test is, by Eq. (2) at the dominant frequency of 60 hertz

$$X_C = \frac{41.6 \times 41.6}{18} = 96 \text{ ohms}$$

Therefore, the value of inrush current for each pre-insertion resistance can be calculated by Eq. (1). The values of the voltage transients and inrush current for each pre-insertion resistance are shown in Table 3, and graphically in Figure 7. Since the maximum magnitude value of voltage transient is always greater than one per unit, the graphs in Figure 7 are of voltage and current magnitudes. In this figure when R = 20 ohms, the voltage transient is minimum. Due to the trouble that could be caused by the transient voltage in customer equipment, the magnitude of transient voltage has been limited up to 1.1 per unit for this test. For a range of resistances between 16 to 28 ohms, the transient voltage is less than 1.1 unit. For this range the current inrush is also minimum when R = 20 ohms. Therefore, the optimum value of pre-insertion resistors is 20/96 or 20.8 percent of the impedance of the capacitor bank.

Pre-Insertion Resistance (ohms)	Voltage Transient (per unit)	Current Inrush (amperes)
0.5	1.54	385
5	1.28	320
20	1.08	265
32	1.12	267
40	1.14	265
50	1.16	257.5

Table 3. The Maximum Voltage Transient and Current Inrush for Each Value of Pre-Insertion Resistor When Bank Size is 18 MVA

Figure 7. The Maximum Voltage Transient and Current Inrush for Each Value of Pre-Insertion Resistor When Bank Size is 18 MVA

To see the effect of the optimum value of pre-insertion
resistors on voltage transients over a four to one range of
capacitor bank sizes, the program was run by changing 18
MVA first to 4.5 MVA and second to 72.0 MVA. The result
is shown in Table 4.

Test 2

In this test the capacitor bank size is 36 MVA. The
computer program result for determination of the optimum
value of pre-insertion resistors is shown in Table 5.
From this table it can be seen that 10 ohms is the optimum
value of pre-insertion resistors. The computer solution
of A-phase transient, where R = 10 ohms, is shown in
Figure 8. Note that the maximum magnitude of transient
voltage in Figure 8 is 1.12 P.U. The line-to-neutral
impedance of the capacitor bank in this test is, by Eq.
(2) at the dominant frequency of 60 hertz

$$X_c = \frac{41.6 \times 41.6}{36} = 48 \text{ ohms}$$

Therefore the value of inrush current for each pre-
insertion resistance can be calculated by Eq. (1). The
value of the voltage transient and inrush current for each
pre-insertion resistance are shown in Table 6, and
graphically in Figure 9. Since the maximum magnitude
value of voltage transient is always greater than one per
unit, the graphs in Figure 9 are of voltage and current
magnitude. In this figure when R = 10 ohms, the voltage

Bank Size	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
MVA	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
4.5	1.12	1.00	1.00	1.04	1.01	1.03
18	1.07	1.08	1.01	1.04	1.12	1.03
72	1.19	1.40	1.01	1.21	1.27	1.02

Table 4. The Effect of the Optimum Value of Pre-Insertion Resistors (20 ohms) Over a Four to One Range of Capacitor Bank Size on the Maximum Magnitude of the Transient Voltage

Value of Pre-Insertion Resistors	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
R	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
6	<u>1.19</u>	1.04	1.01	1.06	1.09	<u>1.11</u>
10	<u>1.12</u>	1.10	1.10	1.10	<u>1.14</u>	1.07
16	1.07	<u>1.18</u>	1.02	1.14	<u>1.19</u>	1.04
25	1.09	<u>1.25</u>	1.01	1.19	<u>1.22</u>	1.02

Table 5. The Effect of the Value of Pre-Insertion Resistors on the Maximum Magnitudes of the Transient Voltage
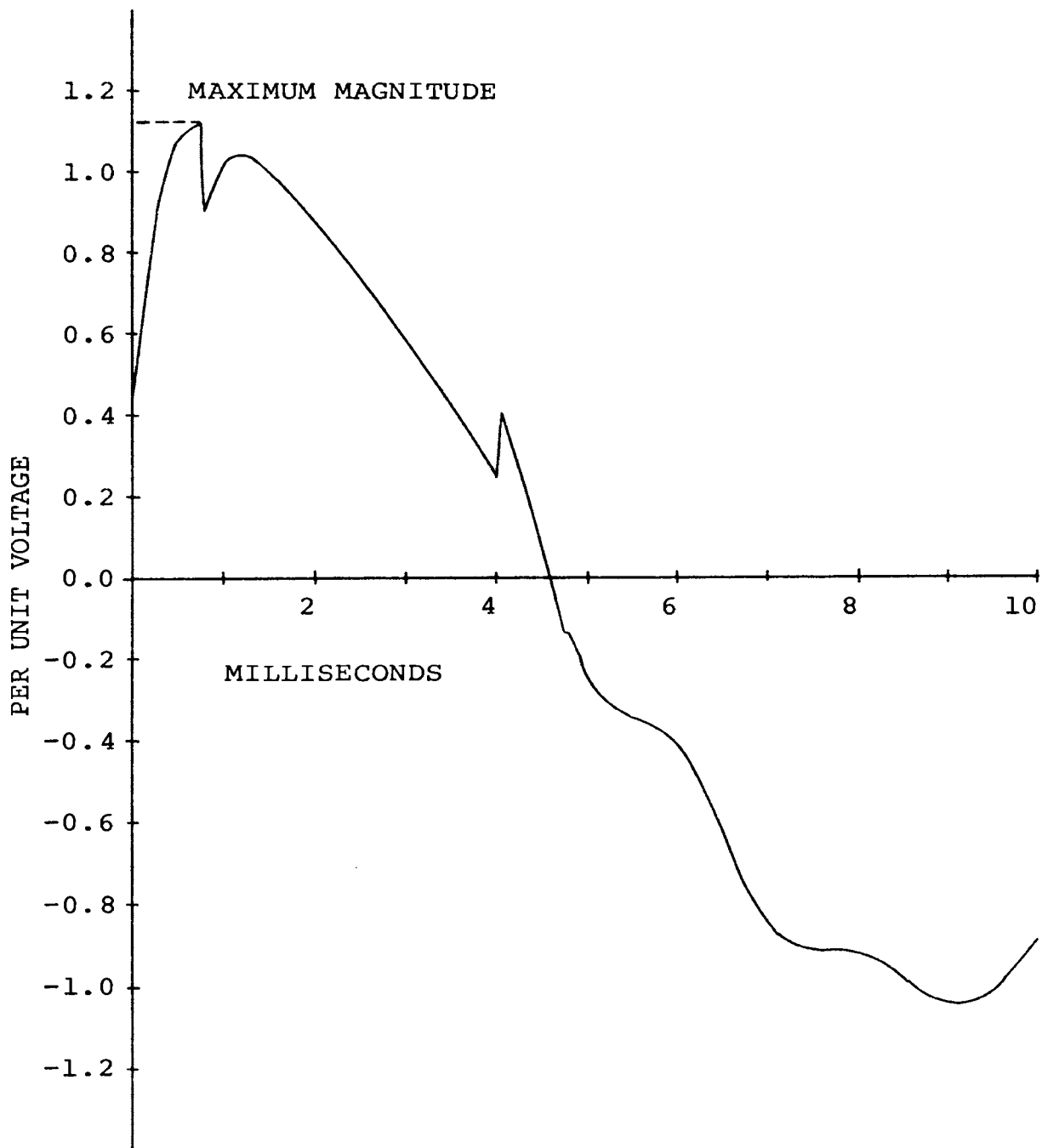
Figure 8.   A-Phase Voltage Transient Response (where
             R = 10 ohms and Bank Size = 36 MVA)

Pre-Insertion Resistance (ohms)	Voltage Transient (per unit)	Current Inrush (amperes)
6	1.19	596
10	1.12	549
16	1.18	564
25	1.25	564

Table 6.   The Maximum Voltage Transient and Current Inrush for Each Value of Pre-Insertion Resistors When Bank Size is 36 MVA
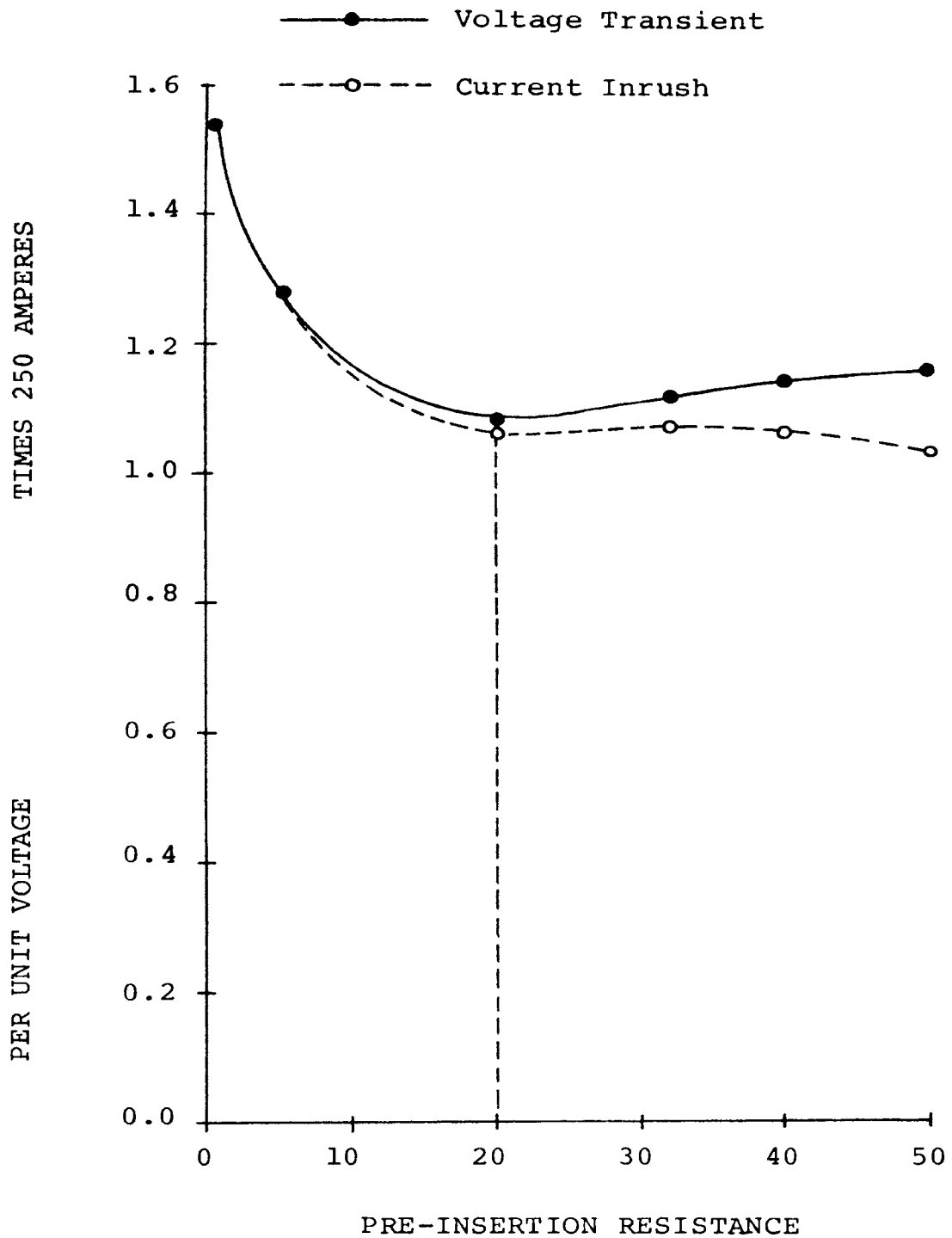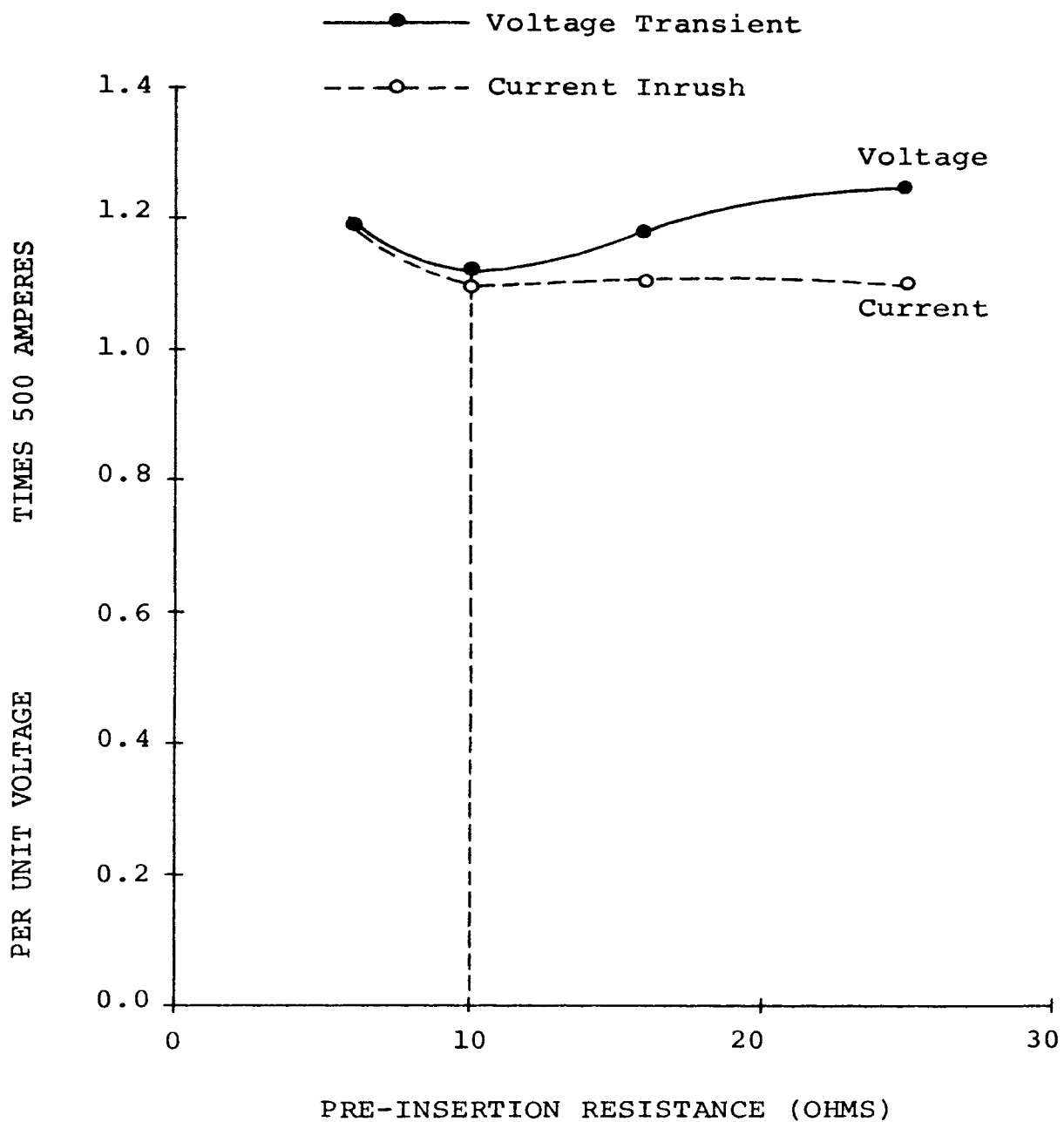
Figure 9. The Maximum Voltage Transient and
Current Inrush for Each Value of
Pre-Insertion Resistor When Bank
Size is 36 MVA

transient is minimum. Due to the trouble that could be caused by the transient voltage in customer equipment, the magnitude of transient voltage has been limited up to 1.2 per unit for this test. For a range of resistances between 7.5 to 14.5 ohms, the transient voltage is less than 1.2 per unit. For this range the current inrush is also minimum when R = 10 ohms. Therefore, the optimum value of pre-insertion resistors is 10/48 or 20.8 percent of the impedance of the capacitor bank.

The effect of the optimum value on voltage transients over a four to one range of capacitor bank sizes is shown in Table 7.

Test 3

In this test the capacitor bank size is 72 MVA. The computer program result for determination of the optimum value of pre-insertion resistors is shown in Table 8. From this table it can be seen that 5 ohms is the optimum value of the pre-insertion resistors. The computer solution of B-phase transient, where R = 5 ohms, is shown in Figure 10. Note that the maximum magnitude of transient voltage in Figure 10 is 1.16 P.U. The line-to-neutral impedance of the capacitor bank in this test is, by Eq.(2) at the dominant frequency of 60 hertz

$$X_c = \frac{41.6 \times 41.6}{72} = 24 \text{ ohms}$$

Bank Size	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltage			Maximum Line-to-Line Per Unit Capacitor Bus Voltage		
MVA	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
9	<u>1.19</u>	1.00	1.00	<u>1.10</u>	1.02	1.07
36	<u>1.12</u>	1.10	1.10	1.10	<u>1.14</u>	1.07
144	1.12	<u>1.50</u>	1.03	<u>1.36</u>	1.29	1.08

Table 7. The Effect of the Optimum Value of Pre-Insertion Resistors (10 ohms) Over a Four to One Range of Capacitor Bank Size on the Maximum Magnitude of Transient Voltage

Value of Pre-Insertion Resistors	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
R	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
3	<u>1.18</u>	1.10	1.11	1.06	1.08	<u>1.21</u>
5	1.10	<u>1.16</u>	1.05	1.09	1.13	<u>1.13</u>
8	1.15	<u>1.25</u>	1.03	1.14	<u>1.19</u>	1.08
15	1.19	<u>1.37</u>	1.02	1.20	<u>1.25</u>	1.03

Table 8. The Effect of the Value of Pre-Insertion Resistors on the Maximum Magnitudes of the Transient Voltage
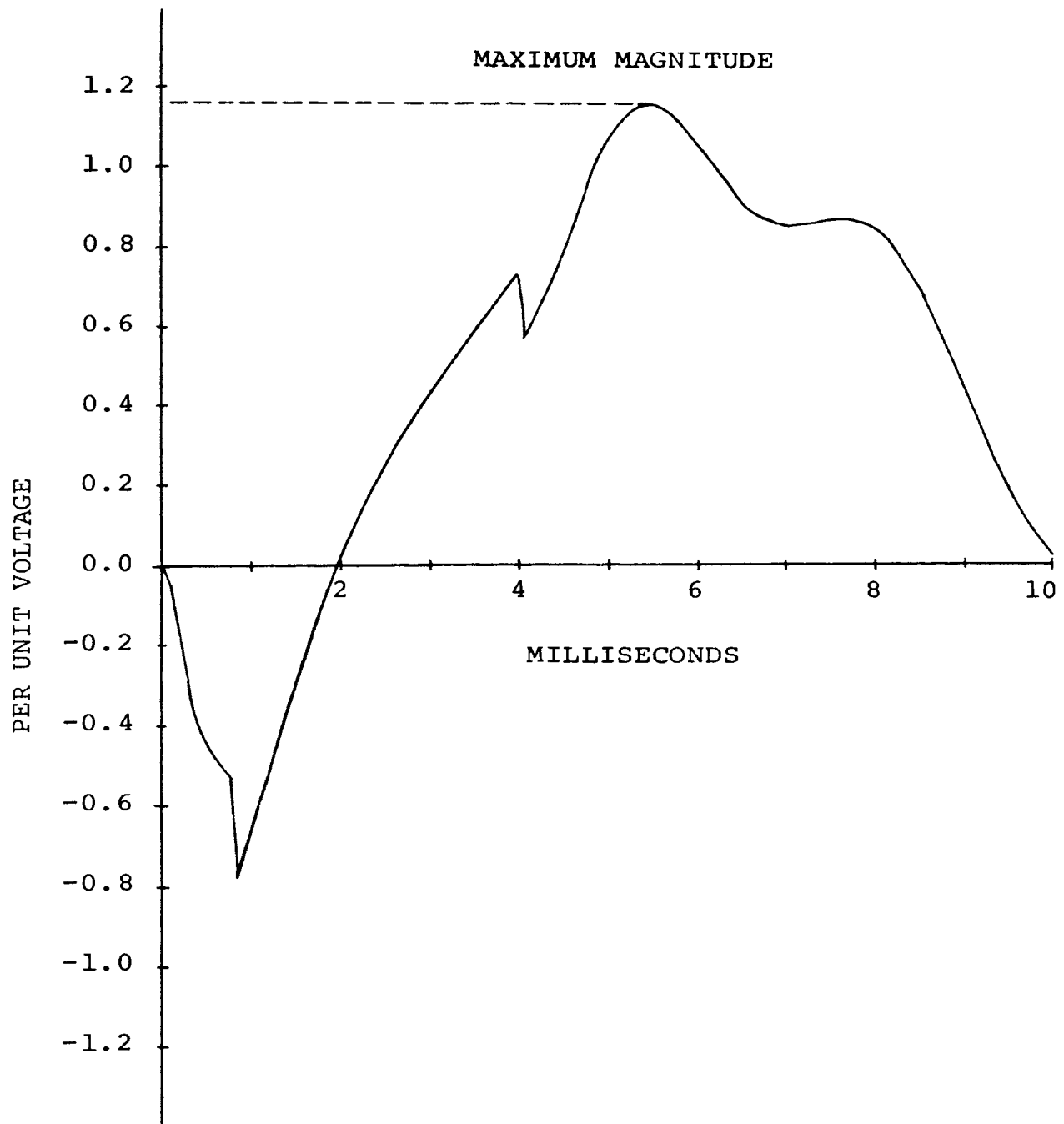
Figure 10. B-Phase Voltage Transient Response
(Where R = 5 ohms and Bank Size =
72 MVA)

Therefore the value of inrush current for each pre-insertion resistance can be calculated by Eq. (1). The value of the voltage transient and inrush current for each pre-insertion resistance are shown in Table 9, and graphically in Figure 11. Since the maximum magnitude value of voltage transient is always greater than one per unit, the graphs in Figure 11 are of voltage and current magnitude. In this figure when R = 5 ohms, the voltage transient is minimum. Due to the trouble that could be caused by the transient voltage in customer equipment, the magnitude of transient voltage has been limited up to 1.2 per unit for this test. For a range of resistance between 3 to 6 ohms, the transient voltage is less than 1.2 per unit. For this range the current inrush is also minimum when R = 5 ohms. Therefore, the optimum value of pre-insertion resistors is 5/24 or 20.8 percent of the impedance of the capacitor bank.

The effect of this optimum value on voltage transients over a four to one range of capacitor bank sizes is shown in Table 10.

Test 4

In this test the capacitor bank size is assumed to be 100 MVA. The computer program result for determination of optimum value of pre-insertion resistors is shown in Table 11. From this table it can be seen that the optimum

Pre-Insertion Resistance (ohms)	Voltage Transient (per unit)	Current Inrush (amperes)
3	1.18	1183
5	1.16	1155
8	1.25	1183
15	1.37	1135

Table 9. The Maximum Voltage Transient and Current Inrush for Each Value of Pre-Insertion Resistors When Bank Size is 72 MVA

Figure 11. The Maximum Voltage Transient and
Current Inrush for Each Value of
Pre-Insertion Resistor When Bank
Size is 72 MVA

Bank Size	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
MVA	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
18.0	1.28	1.03	1.02	1.16	1.04	1.11
72.0	1.10	1.16	1.05	1.09	1.13	1.13
288	1.30	1.59	1.11	1.57	1.29	1.14

Table 10. The Effect of the Optimum Value of Pre-
Insertion Resistors (5 ohms) Over a Four
to One Range of Capacitor Bank Size on
the Maximum Magnitude of Transient Voltage

Value of Pre-Insertion Resistors	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
R	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
2	1.24	1.09	1.19	1.07	1.03	1.27
3.6	1.13	1.18	1.10	1.03	1.12	1.17
5	1.18	1.29	1.05	1.13	1.19	1.10
10	1.21	1.40	1.03	1.22	1.25	1.07

Table 11. The Effect of the Value of Pre-Insertion Resistors on the Maximum Magnitude of the Transient Voltage

value of pre-insertion resistor is 3.6 ohms. The computer
solution of B-phase transient, where R = 3.6 ohms, is
shown in Figure 12. Note that the maximum magnitude of
transient voltage in Figure 12 is 1.18 per unit. The
line-to-neutral impedance of the capacitor bank in this
test is, by Eq. (2) at the dominant frequency of 60 hertz

$$X_c = \frac{41.6 \times 41.6}{100} = 17.3 \text{ ohms}$$

Therefore the value of inrush current for each pre-
insertion resistance can be calculated by Eq. (1). The
value of the voltage transient and inrush current for each
pre-insertion resistance are shown in Table 12, and gra-
phically in Figure 13. Since the maximum magnitude value
of voltage transient is always greater than one per unit,
the graphs in Figure 13 are of voltage and current magni-
tude. In this figure when R = 3.6 ohms the voltage tran-
sient is minimum. Due to the trouble that could be caused
by the transient voltage in customer equipment, the
magnitude of transient voltage has been limited up to 1.24
per unit for this test. For a range of resistance between
2 to 4.3 ohms, the transient voltage is less than 1.24 per
unit. For this range the current inrush is also minimum
when R = 3.6 ohms. Therefore, the optimum value of pre-
insertion resistors is 3.6/17.3 or 20.8 percent of the
impedance of the capacitor bank.
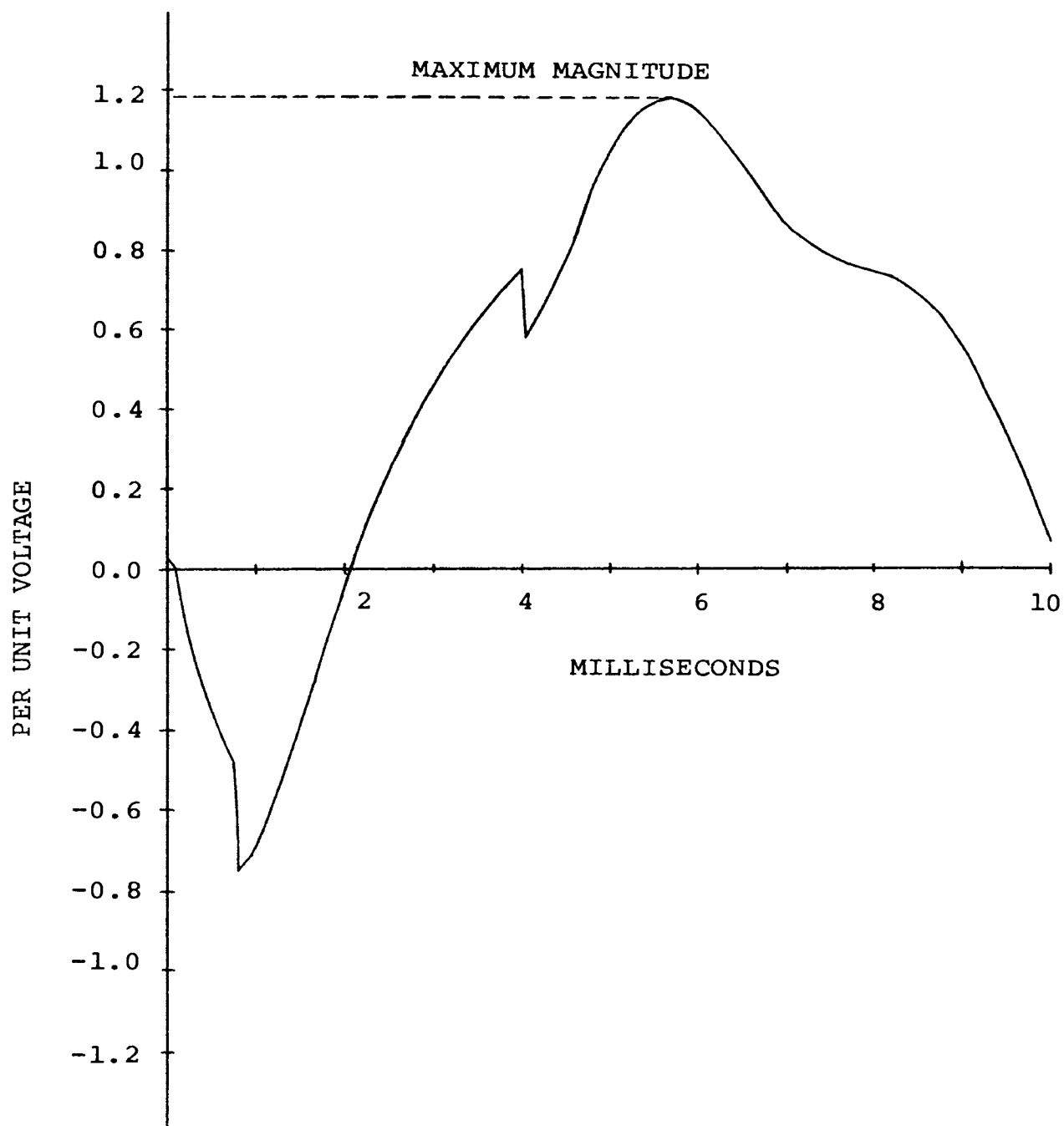
Figure 12.   B-Phase Voltage Transient Response
              (Where R = 3.6 ohms and Bank Size =
              100 MVA)

Pre-Insertion Resistance (ohms)	Voltage Transient (per unit)	Current Inrush (amperes)
2	1.24	1715
3.6	1.18	1585
5	1.29	1685
10	1.40	1685

Table 12. The Maximum Voltage Transient and Current Inrush for Each Value of Pre-Insertion Resistor When Bank Size is 100 MVA
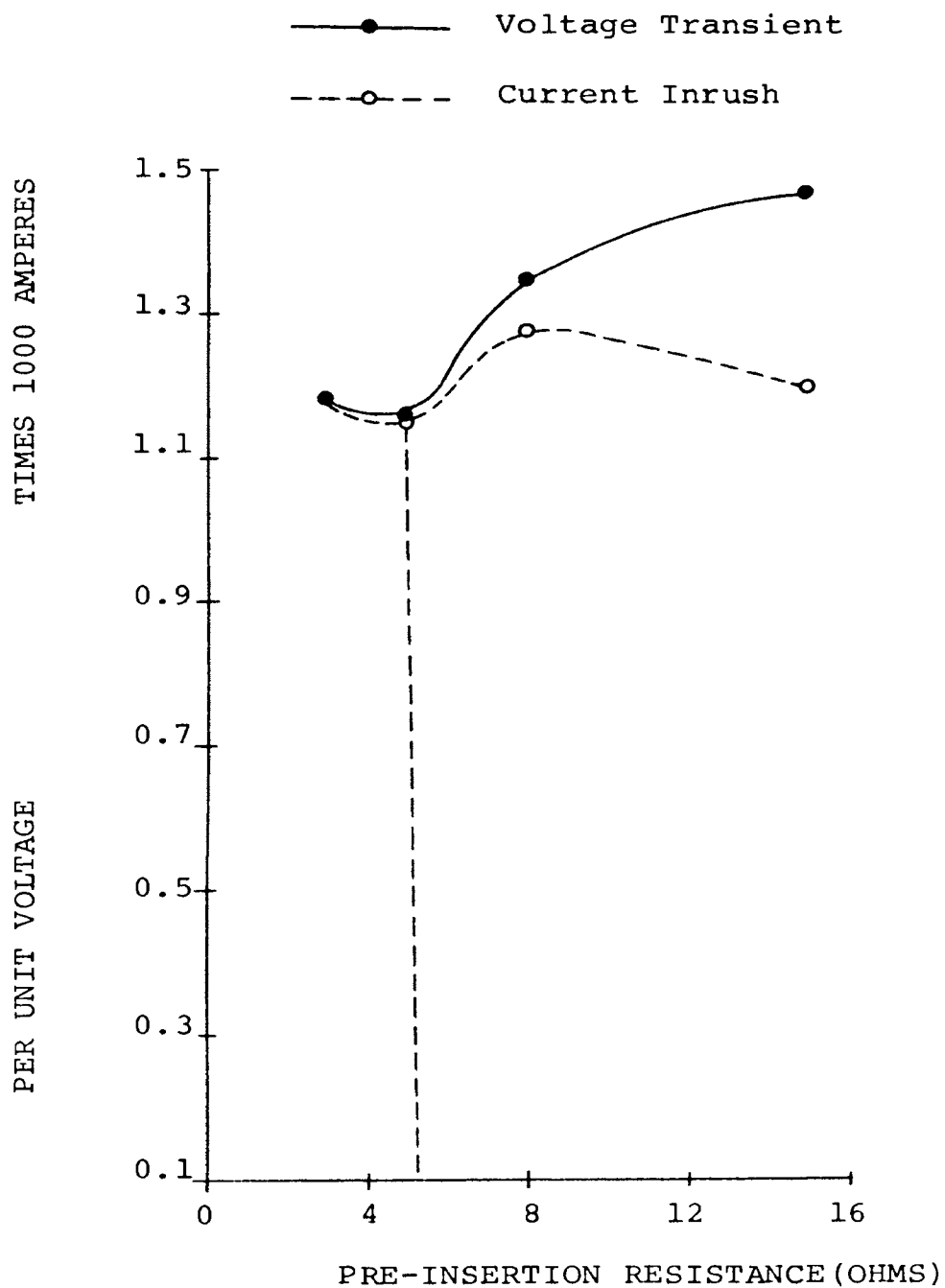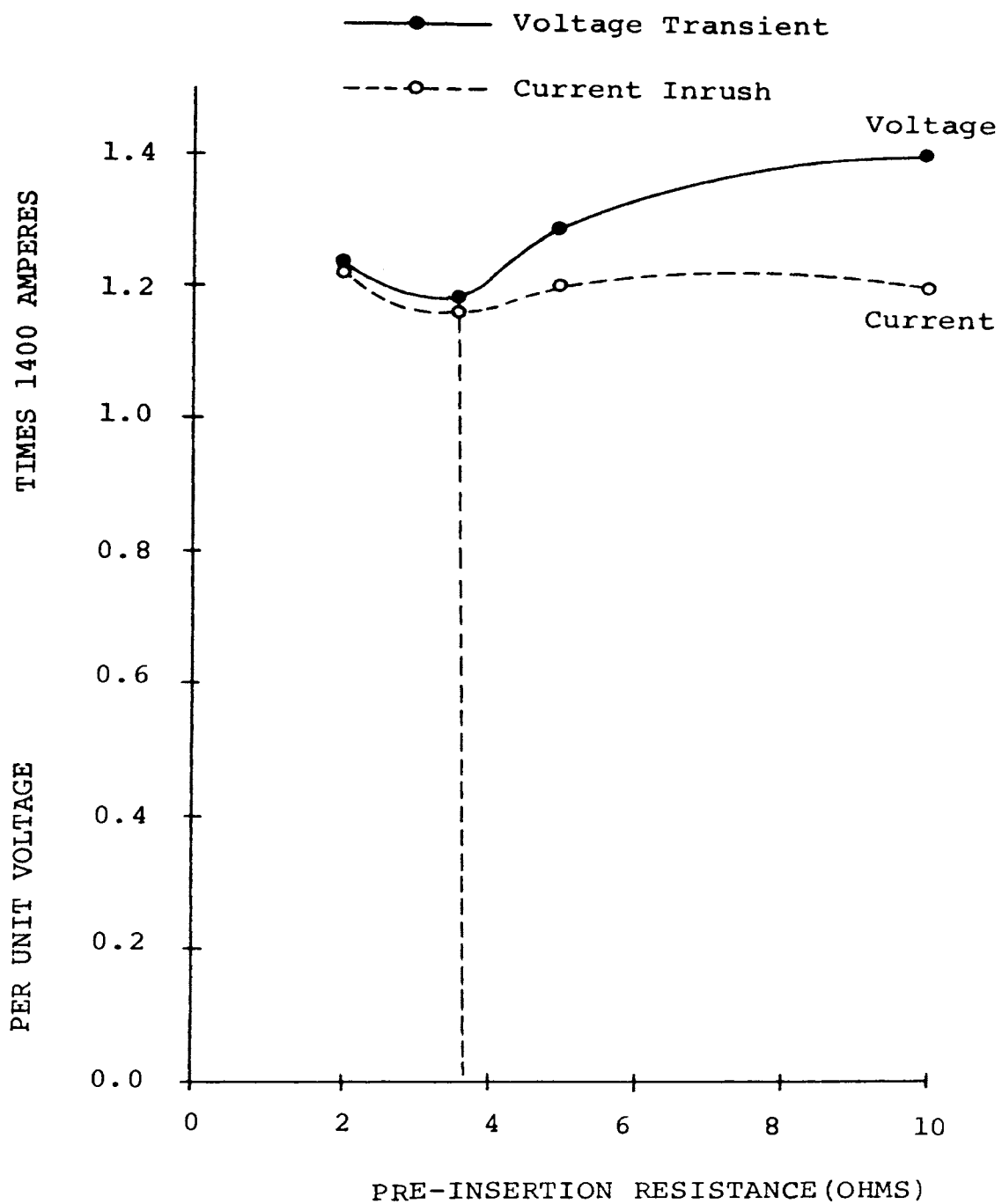
Figure 13. The Maximum Voltage Transient and
Current Inrush for Each Value of
Pre-Insertion Resistor When Bank
Size is 100 MVA

The effect of this optimum value on voltage transients over a four to one range of capacitor bank size is shown in Table 13.

If Table 2 is considered more carefully, it looks like that for the optimum value of pre-insertion resistor 18 ohms is somewhat better than 20 ohms, because for 18 ohms, by interpolation VPU A; VPU B and VPU BC are about 1.10, however VPU C; VPU AB and VPU CA remain less than 1.10. Therefore, the optimum value for test one may be 19/96 or 18.7 percent of the impedance of the capacitor bank. For other tests the value a little less than the optimum value of pre-insertion resistor which is mentioned before looks like better. As a general result, it can be stated that the optimum value of pre-insertion resistor is about 20 percent of the impedance of the capacitor bank.

Bank Size	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
MVA	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
25	<u>1.31</u>	1.02	1.03	<u>1.18</u>	1.04	1.13
100	1.13	<u>1.18</u>	1.10	1.03	1.12	<u>1.17</u>
400	1.48	<u>1.62</u>	1.20	<u>1.66</u>	1.29	1.35

Table 13. The Effect of the Optimum Value of Pre-Insertion Resistors (3.6 Ohms) Over a Four to One Range of Capacitor Bank Size on the Maximum Magnitude of Transient Voltage

CHAPTER V

THE EFFECT OF TIME DIFFERENCES OF THE POLE CLOSURES OF THE
THREE PHASES IN A 2-STEP SWITCHING OF CAPACITOR
BANKS

To see the effect of time differences of the pole
closures of the three phases in a 2-step switching of
capacitor banks, two computer program tests are run for
the capacitor bank station of Figure 5. It should be
noted that the program gives the results for a period of
10 milliseconds after the second pole closes.

Test 1

In this test the value of pre-insertion resistors is
32 ohms for an 18 MVA capacitor bank. The pre-insertion
time is 4 milliseconds per pole. Since the poles A and
B are assumed to be closed simultaneously, TA and TB are
set to zero. The program result of this test by changing
TC from 0.75 to 6 milliseconds is shown in Table 14. A
good result (when the maximum magnitude of transient
voltage is minimum among all others) is obtained when TC =
6 milliseconds. Since the program gives the result for a
period of 10 milliseconds after the second pole closes,
it is quite possible to get a better result when TC is
greater than 6 milliseconds.

Three Phases Pole Closure Times (In Milliseconds)			Maximum Line-to-Neutral Per Unit Capacitor Bus Voltage			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
TA	TB	TC	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
0.0	0.0	0.75	1.04	1.12	1.01	1.06	1.17	1.02
0.0	0.0	2.0	1.04	1.17	1.02	1.06	1.12	1.01
0.0	0.0	4.0	1.09	1.11	1.00	1.06	1.17	1.05
0.0	0.0	6.0	1.04	1.09	1.00	1.06	1.11	1.01

Table 14. The Effect of Time Differences of the Pole Closures of the Three Phases in a 2-Step Switching of Capacitor Bank (18 MVA) On the Maximum Magnitude of Transient Voltage (Where the Value of Pre-Insertion Resistor is 32 ohms)

Test 2

In this test the value of pre-insertion resistor is 20 ohms, optimum value, for the same capacitor bank size of test 1. The pre-insertion time is 4 milliseconds per pole. The program result of test 2 is shown in Table 15. To get the best result (when the maximum magnitude of transient voltage reaches as low as one per unit) in this test, the time differences of the pole closures of the three phases are random. However, a very good result can be obtained when TA = 0; TB = 2 and TC = 8 milliseconds. Note that for TB = TC = 4 milliseconds and TB = TC = 8 milliseconds, the results are exactly the same. This is because the pre-insertion time for each pole is 4 milliseconds.

Three Phases Pole Closure Times (In Milliseconds)			Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
TA	TB	TC	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
0.0	0.0	0.0	1.08	1.07	1.01	1.04	1.07	1.01
0.0	2.0	2.0	1.08	1.05	1.01	1.02	1.07	1.04
0.0	2.0	4.0	1.07	1.09	1.07	1.02	1.05	1.07
0.0	2.0	6.0	1.07	1.04	1.02	1.02	1.15	1.04
0.0	2.0	8.0	1.07	1.05	1.00	1.02	1.04	1.03
0.0	4.0	4.0	1.26	1.05	1.01	1.08	1.07	1.11
0.0	8.0	2.0	1.04	1.11	1.02	1.07	1.01	1.01
0.0	8.0	8.0	1.26	1.05	1.01	1.08	1.07	1.11

Table 15. The Effect of Time Differences of the Pole Closures of the Three Phases in a 2-Step Switching of Capacitor Bank (18 MVA) On the Maximum Magnitude of Transient Voltage. (When the Value of Pre-Insertion Resistor is 20 ohms)

CHAPTER VI

THE EFFECT OF IMPEDANCE BETWEEN BANKS AS AN AID IN DETER-
MINING THE LOCATION OF FUTURE CAPACITOR BANK
ON A SYSTEM

To determine the effect of the impedance between
banks on transient voltage, the capacitor bank station
of Figure 5 is again considered with an additional 18
MVA bank which is assumed to be energized while switching
the capacitor bank. A simple one-line diagram of this
station is shown in Figure 14. In this figure bank C1
is energizing with bank C2 on the line.

Test 1

The purpose of this test is to investigate the
effect of the impedance between capacitor banks on voltage
transients. Here the distance of energizing bank (C1)
from capacitor bus was set to 50 feet of 3/0 ACSR and
the distance of the previously energized bank (C2) from
the capacitor bus is set to 10, 50, 100 and 200 feet of
3/0 ACSR for each run. Therefore the line length
between banks are 60, 100, 150 and 250 feet for each run.
The program results for this test are shown in Table 16.
The A-phase voltage transients versus time are plotted in
Figures 15, 16, 17 and 18, corresponding to their line
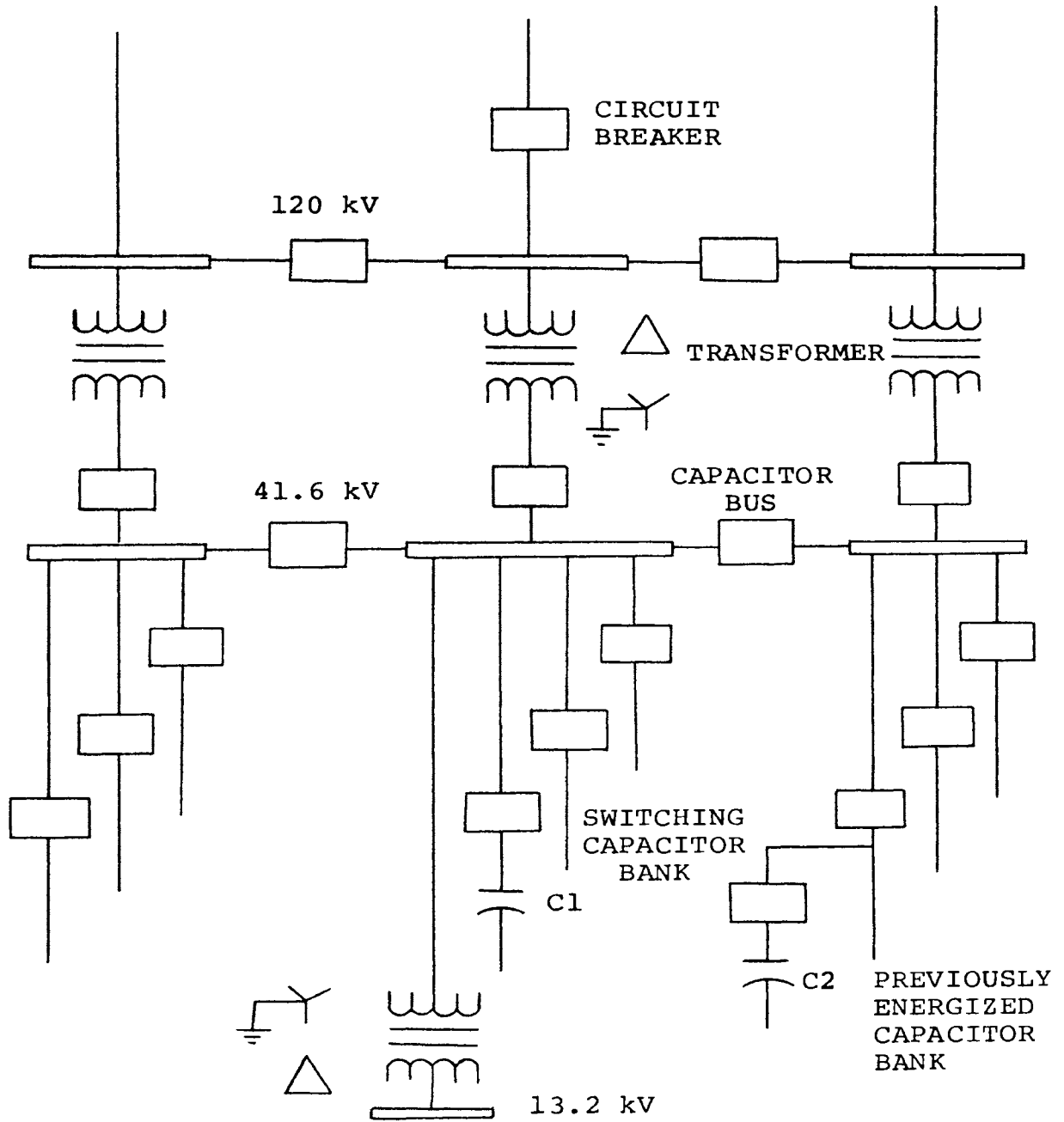length between banks (60, 100, 150 and 250 feet). The

Figure 14. Simplified One-Line Diagram of
Capacitor Bank Station

Line Length Between Banks (In Feet)	Maximum Line-to-Neutral Per Unit Capacitor Bus Voltages			Maximum Line-to-Line Per Unit Capacitor Bus Voltages		
L	VPU A	VPU B	VPU C	VPU AB	VPU BC	VPU CA
60	1.09	1.07	1.02	1.08	1.10	1.06
100	1.09	1.05	1.02	1.06	1.08	1.06
150	1.10	1.02	1.02	1.05	1.07	1.06
250	1.08	1.06	1.02	1.07	1.10	1.06

Table 16. The Effect of the Line Length Between Capacitor Banks on the Maximum Magnitude of Transient Voltage
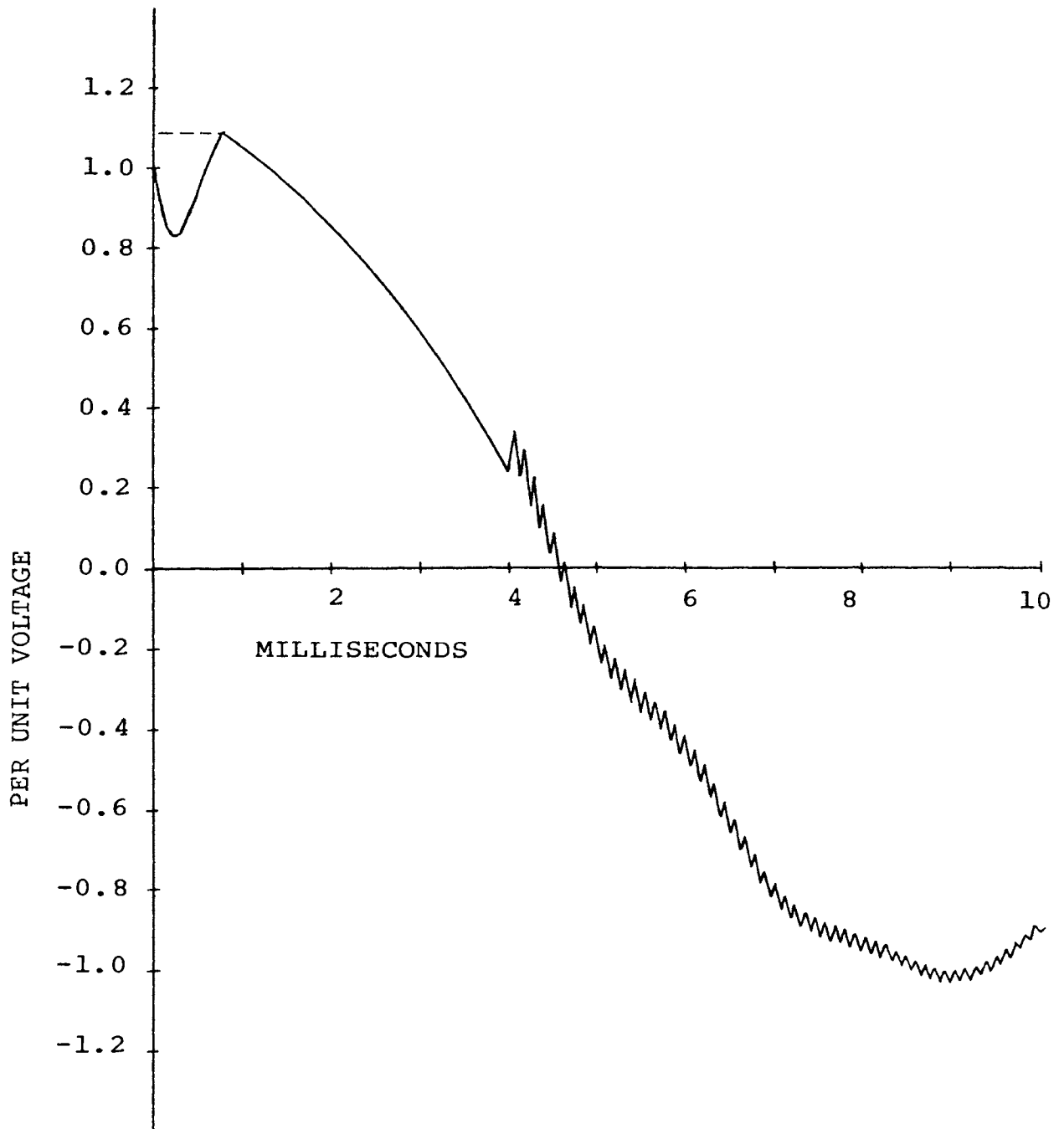
Figure 15.   A-Phase Voltage Transient Versus Time
When the Distance Between Banks is 60
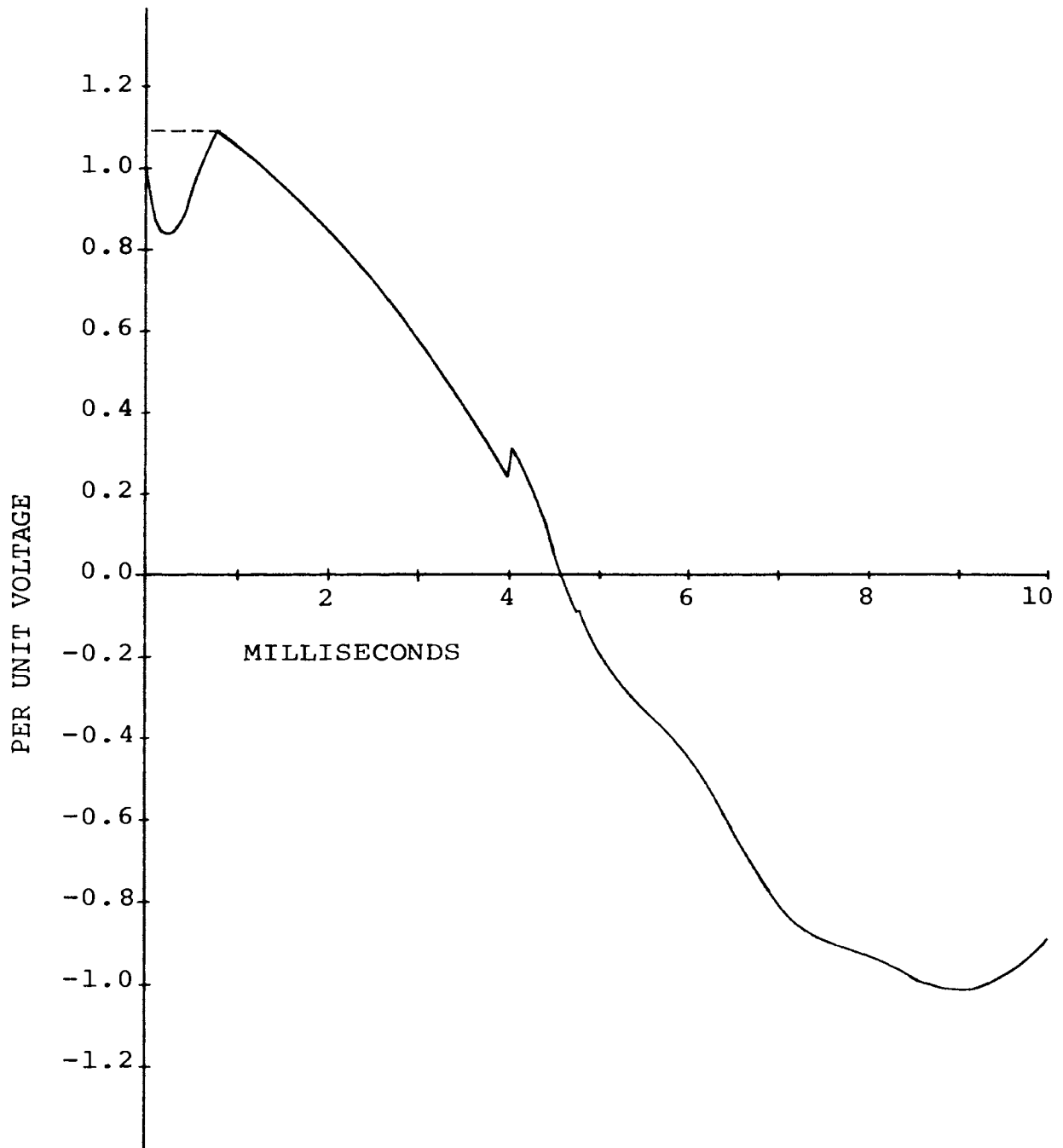Feet of 3/0 ACSR

Figure 16.   A-Phase Voltage Transient Versus Time
            When the Distance Between Banks is 100
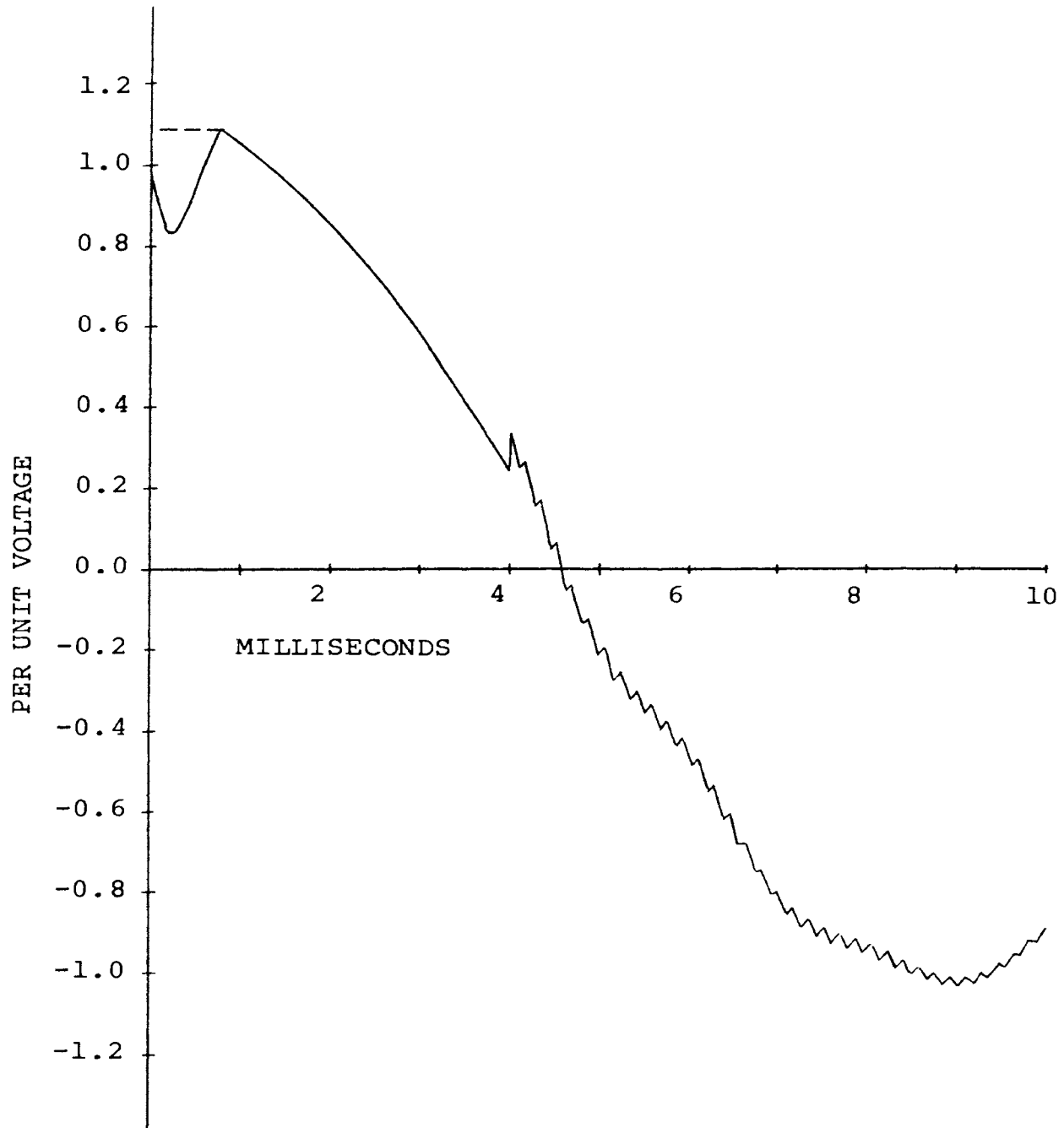   Feet of 3/0 ACSR

Figure 17. A-Phase Voltage Transient Versus Time When the Distance Between Banks is 150 Feet of 3/0 ACSR
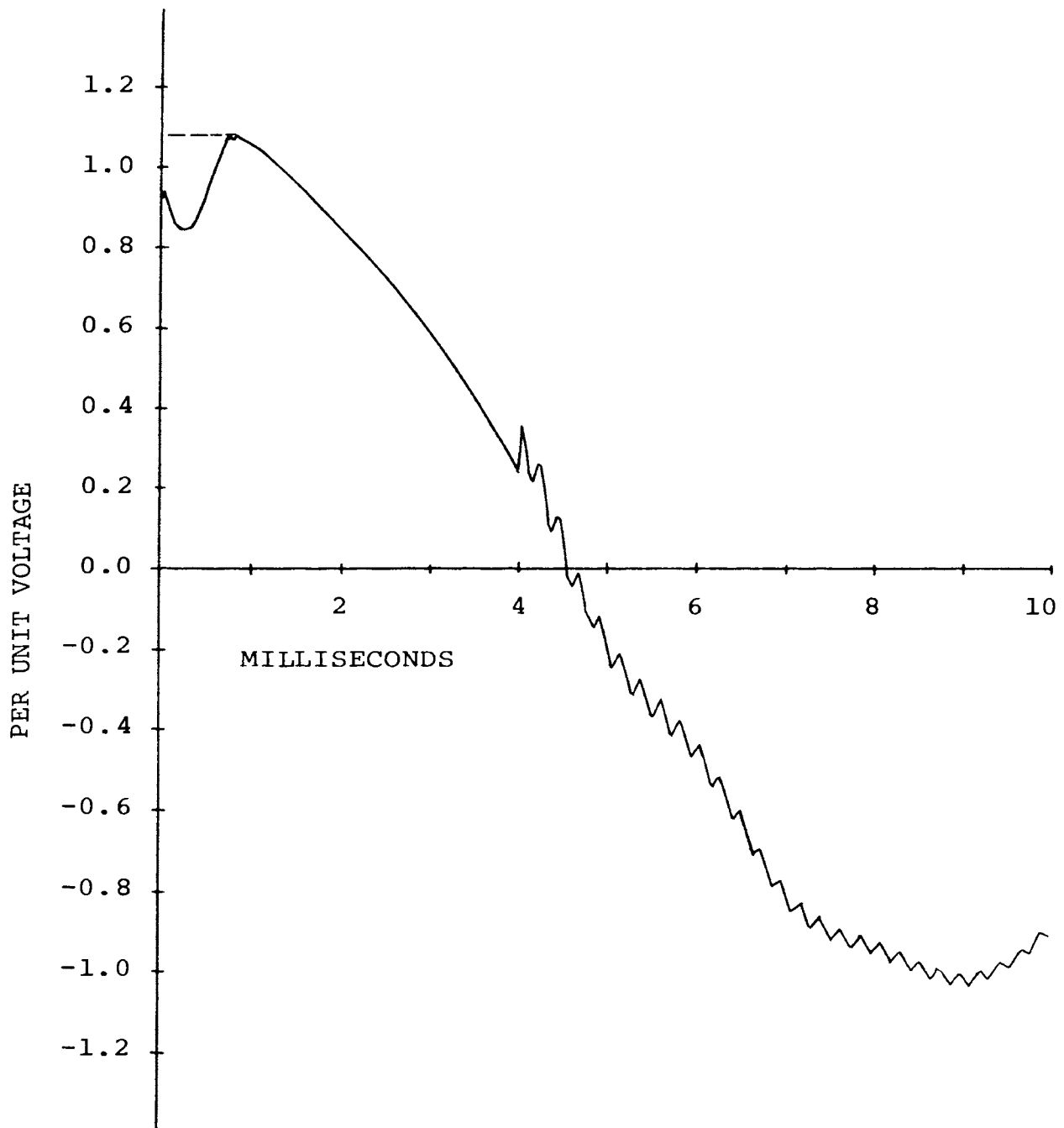
Figure 18.   A-Phase Voltage Transient Versus Time
When the Distance Between Banks is 250
Feet of 3/0 ACSR

maximum magnitude of transient voltage as a function
of distance between banks is shown in Figure 19. From
this figure it can be seen that the effect of distance,
or impedance, between banks on transient voltage is not
significant.

To observe the effect of distance, or impedance,
between banks on the transient frequency, the transient
frequency as a function of distance between bank is
shown in Table 17, and graphically in Figure 20. The
impedances, $X_c = 1/2\pi fc$, of the capacitor banks at
these high nature frequencies are very small, and the
transient currents which can flow between capacitor
banks may be over 100 times the normal current of the
capacitor bank which is switched. To keep the transient
current as low as possible, the distance between banks
should be chosen 100 feet for this test.
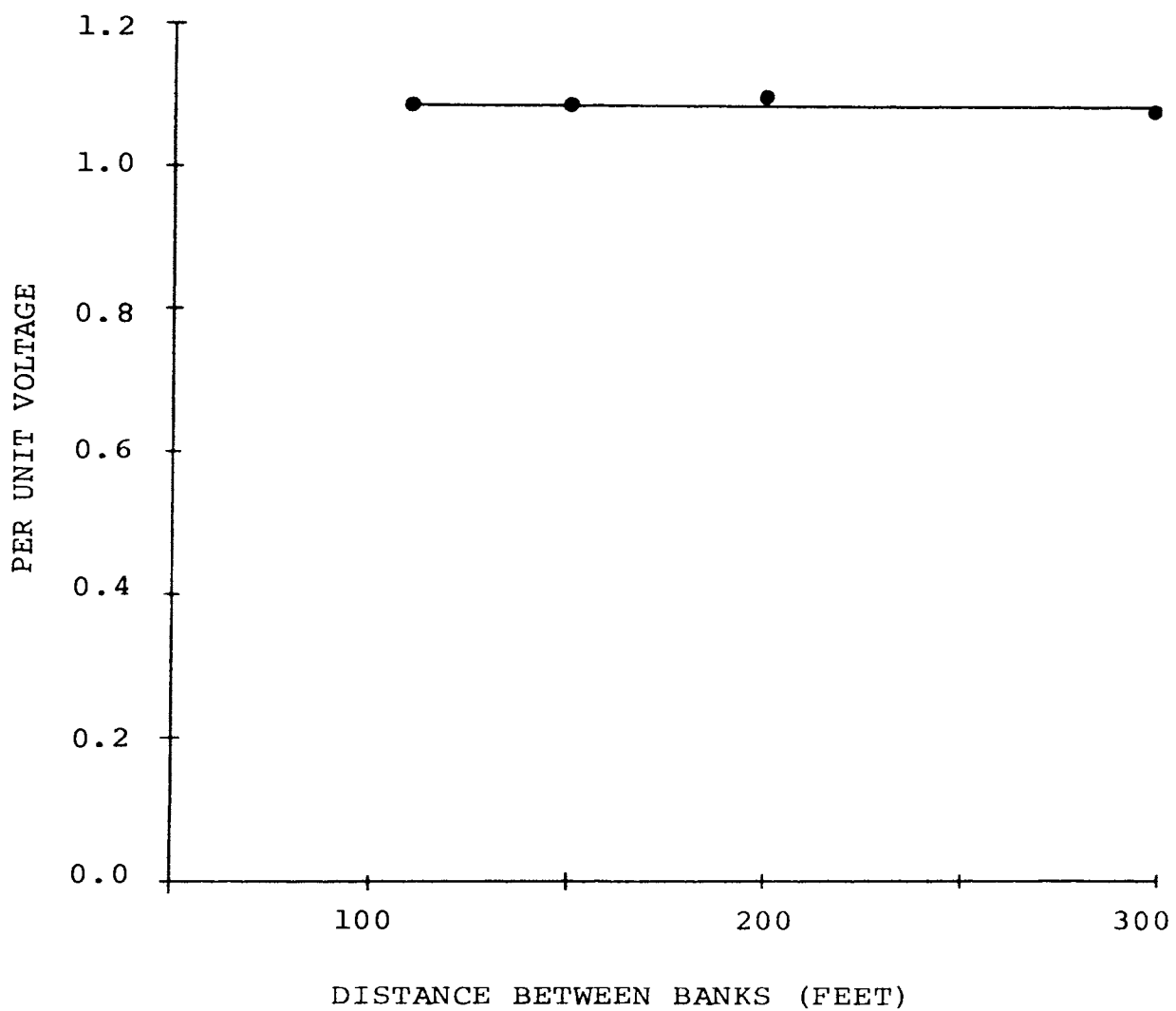
Figure 19. The Maximum Magnitude of Transient
Voltage as a Function of Distance
Between Banks

Line Length Between Capacitor Banks (feet)	Transient Frequency (cps)
60	9000
100	1000
150	5666
250	4500

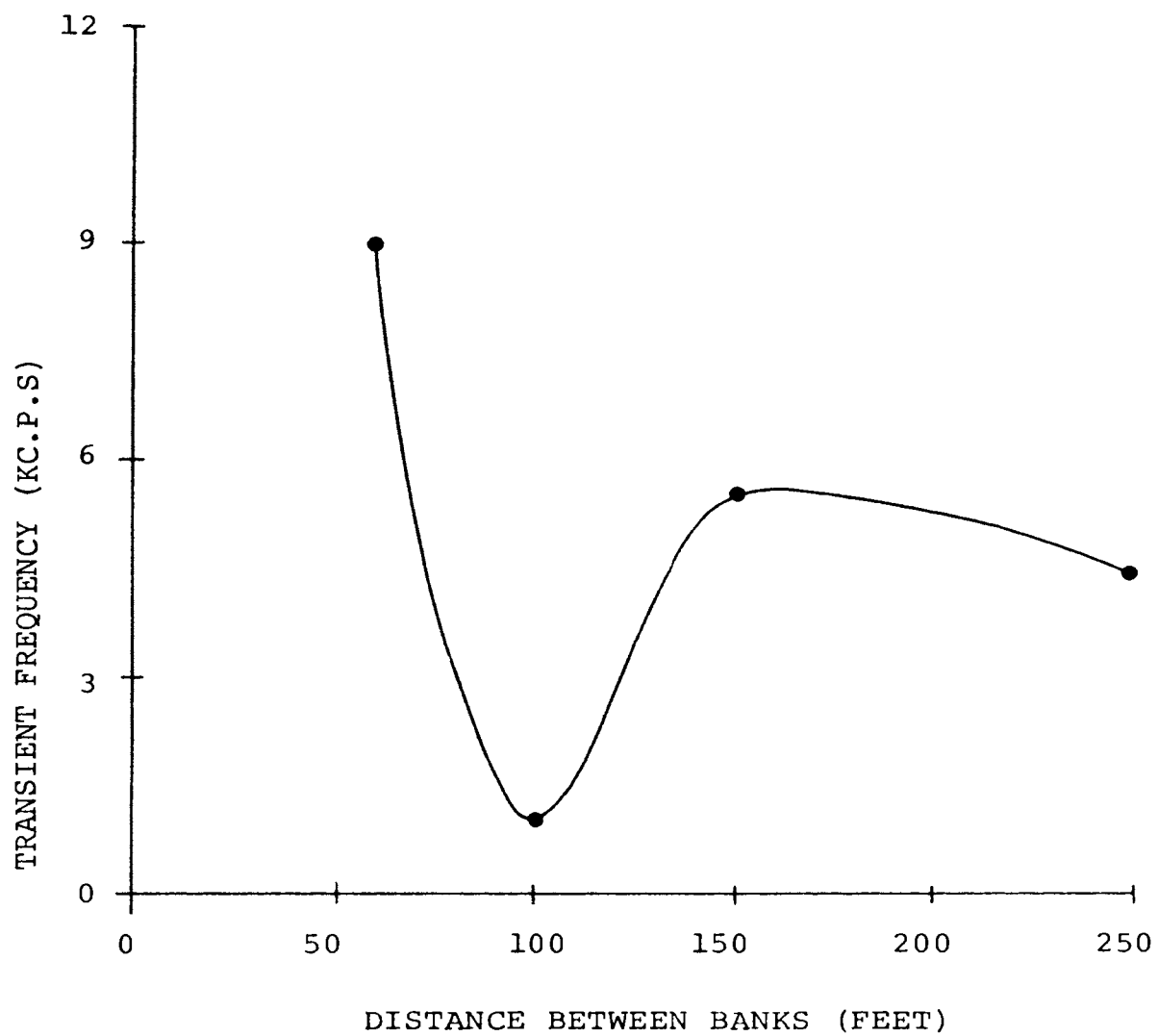Table 17. Transient Frequency as a Function
of Distance Between Banks

Figure 20. Transient Frequency as a Function of
Distance Between Banks

CHAPTER VII
RESULTS AND CONCLUSIONS

The results of this thesis are presented in tables
2 through 17, and in Figures 6 through 13, and
15 through 20. Both voltage transient and current
inrush can be limited to very low values by 2-step
switching inserting resistance smaller than the impedance
of capacitor bank. As has been stated earlier in this
work, the optimum value of pre-insertion resistor is
about 20 percent of the impedance of the capacitor bank,
but a breaker equipped with resistors will give satis-
factory operation over a range of capacitor bank four
to one.

To keep the voltage transient and current inrush at
a very low value, the time differences of the pole closure
of the three phases are random. However, a good result
can be obtained if TB and TC differ 2 to 6 millisecond
from each other. Both TB and TC should not exceed the
pre-insertion time on any occasion (TA is assumed to be
zero).

The effect of distance, or impedance, between banks
on transient voltage is not significant. However, a
change in distance, or impedance, between banks causes
the transient frequency changes inversely. To keep the

transient current which can flow between banks as
low as possible, the transient frequency should be very
low (about 1000 hertz), therefore for a 1000 hertz fre-
quency the distance between energizing bank and
future bank should be chosen 100 feet of 3/0 ACSR for
the capacitor bank station in Figure 14.

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VITA

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