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Locating current paths via time synchronized measurements in a multiphase DCDC buck converter and a high frequency analytical model for the common-mode impedance of a ferrite choke

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LOCATING CURRENT PATHS VIA TIME SYNCHRONIZED MEASUREMENTS IN A MULTIPHASE DCDC BUCK CONVERTER

AND

A HIGH FREQUENCY ANALYTICAL MODEL FOR THE COMMON-MODE IMPEDANCE OF A FERRITE CHOKE

by

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ABSTRACT

In the first section, it introduces a novel method to localize current from multiple sources. The identification of return current paths is often a key element in understanding the root cause of a product's radiated emissions. In a complex system, multiple sources can contribute to the current at the same location and frequency. The source of the current can be identified by correlating the current to different sources. However, the multiphase buck converter phases do not switch at the same time. Thus, synchronizing to a specific phase makes it possible to determine how the current from a specific phase spreads throughout the board. With the objective of localizing current, one can determine whether the capacitor placement is optimal and improve the layout and placement solutions for a multiphase buck converter.

In the second section, it presents a novel analytical model to model the ferrite choke. Ferrite chokes are widely used to reduce the common mode current in power systems. For certain systems, changes in total common mode impedance due to a ferrite are important to characterize the behavior of the ferrite. However, the change in impedance due to the ferrite on the structure depends not only on the ferrite frequency response, but also on the system structure and the location of the ferrite This paper presents a novel high-frequency analytical model for the common mode impedance of ferrite chokes. This model was developed based on transmission line theory to predict the impact of various ferrite chokes on common mode currents in wire harnesses using a closed-form equation. It more clearly explains the physical meaning of the internal mechanism of the ferrite and agrees well with experimental results on a wide bandwidth up to 1 GHz.

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1.1. INTRODUCTION

Multiphase buck DC-DC converters (Fig. 1.1) provide very large currents at low voltages.

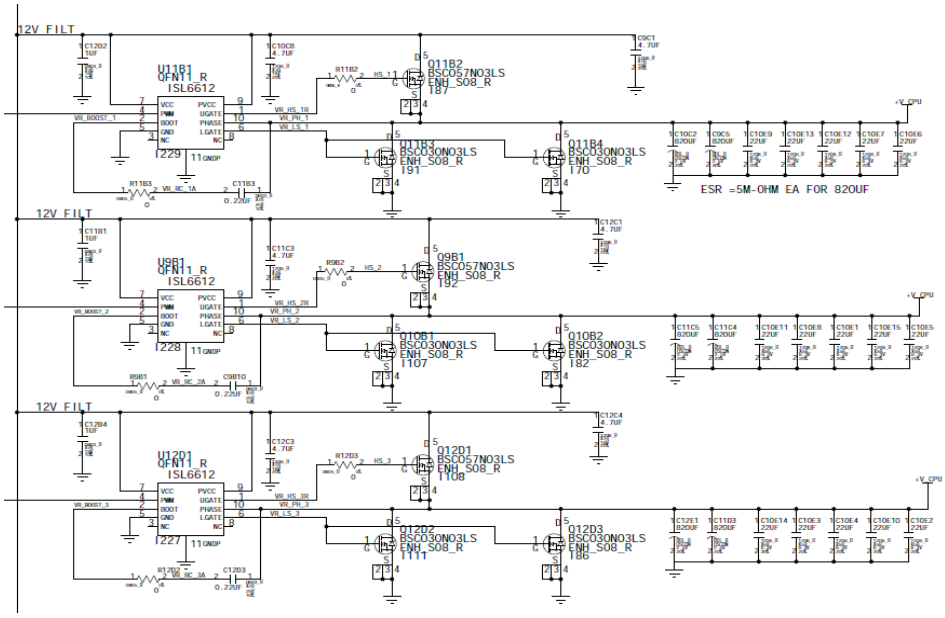


Fig. 1.1 An example of a multiphase buck DCDC converter.

Typically, they provide the core voltage for processors, so values of 100A at 1.3V are not uncommon. In a multiphase configuration, 4-6 converters typically step the voltage down (e.g., from 12V to 1.3V). Each converter may run at the same frequency (e.g., 300 kHz); however, to reduce the size of the output capacitors, the timing of the switching is distributed over the 3-us cycle time. Some randomization may be introduced to reduce the spectral density at the 300 kHz and its harmonics.

Fig. 1.2 shows a schematic of a typical synchronous buck converter. High-side and low-side metal–oxide–semiconductor field-effect transistors (MOSFETs) switch alternatively. In this case, two low-side MOSFETs handle current. The switching of the

MOSFETs is controlled by a controller Integrated circuit (IC) which generates a PWM signal and drives the gates. The node shared by the three MOSFETs and the output inductor is called a phase node. The voltage waveform of the phase node is expected to be a rectangular pulse train with a certain duty cycle, D. The duty cycle of the phase voltage (Fig. 1.3) waveform determines the output voltage of the converter: $V_{out} \approx D \cdot V_{in}$. The output L-C filter averages the phase voltage waveform [3].

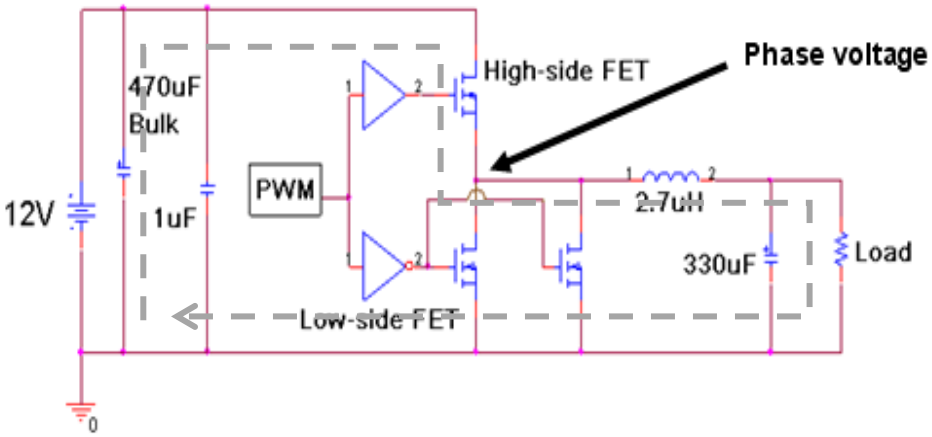


Fig. 1.2 Typical synchronous buck converter [1] [2] schematic.

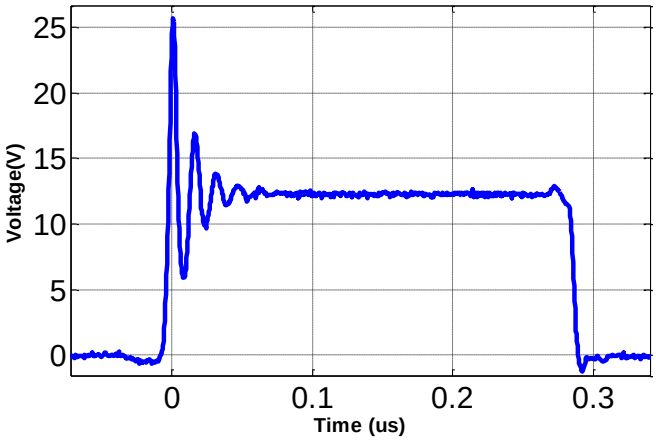


Fig. 1.3 Voltage at the phase node (see Fig. 1.2).

During the switching of a buck converter, the phase voltage will ring when the high-side FET turns on. The ringing frequencies are in the range of 50-200 MHz, and the currents associated with this ringing may reach 25 A [4]. The signal is spectrally distributed and pulsed such that the usual value of 5uA for a narrowband current cannot be applied here. If a maximum of 1mA of current is accepted on an attached cable as a standard for passing FCC class B, then we see that a suppression of about 88 dB is needed. The various phases of the multiphase converter are all fed from a 12V plane on one side into a 1.3V plane. Due to the high current requirements, the size of the FETs, and the cooling requirements, relatively large planes (often extending through many layers of the PCB) are used. As shown in Fig. 1.1, the 12V input plane especially will carry the ringing current. Many decoupling capacitors are placed on this plane to supply necessary transient currents. Since all phases of the converters are connected to the same 12V plane and share the same capacitors, in principle, the current of each phase can be distributed over a large area of the PCB. From an EMC point of view, it is desirable to minimize the current spread and to minimize the loop areas in the input switching current loop (Fig. 1.2).

This measurement method makes it possible to determine the current contributions of each phase in each capacitor.

1.2. CAPACITOR CURRENT MEASUREMENT

The current in the capacitors is estimated via their magnetic fields by a small loop placed close to the capacitor. The mutual inductance between the probe and the current path at the capacitor is a function of the size of the capacitor; thus, it must be determined for each capacitor size by forcing a known current through a capacitor and measuring the voltage induced in the loop (as shown in Fig. 1.4).

The mutual inductance is determined by:

$$M = \frac{V_{induced}}{j\omega I}.$$

The term M represents mutual inductance between the H-field probe loop and the capacitor, and I is the current flowing through the capacitor. The mutual inductance is not

a strong function of frequency; however, calibration should be performed at a frequency close to the ringing frequency $V_{induced}$ is the voltage induced on the H-field loop. The mutual inductance value between a 1x1 mm probe and the capacitors is generally in the range of 20-40pH. The equivalent circuit model is shown in Fig. 1.5.

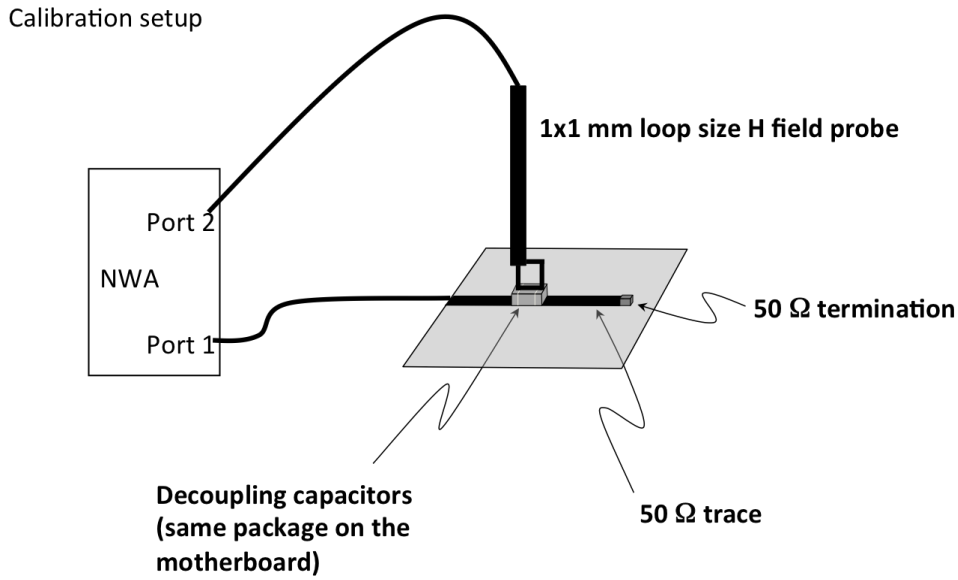


Fig. 1.4 H-field probe calibration setup.

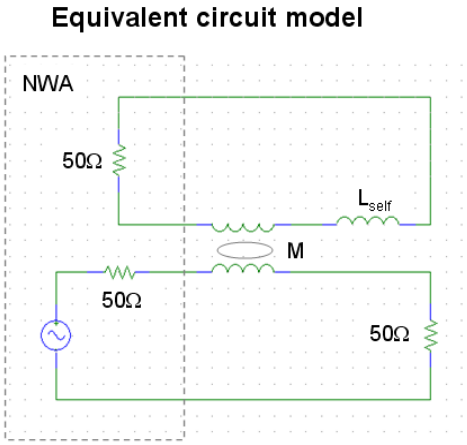


Fig. 1.5 The equivalent circuit model of the calibration setup.

1.3. DEVICE UNDER TEST (DUT) ANALYSIS

The DUT uses a 6-phase buck converter. Its layout is shown in Fig. 1.6 and illustrated in Fig. 1.7 and Fig. 1.8. Fig. 1.8 shows the timing of the switching, illustrating the six switching events that take place during a 3-us cycle.

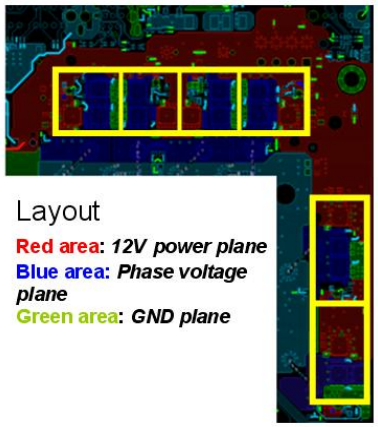


Fig. 1.6 Layout of the 6 phases of the converter.

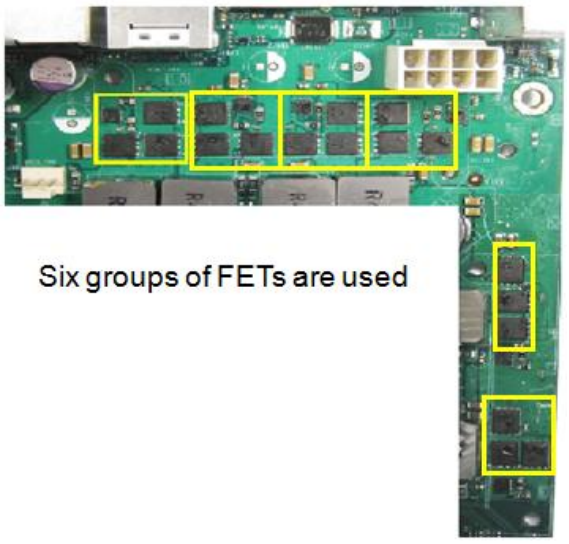


Fig. 1.7 Test structure showing the 6 phases of the converter.

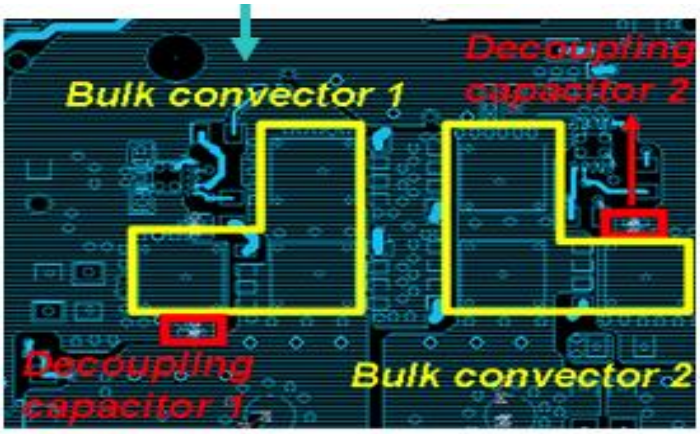


Fig. 1.8 Two of the six phases, each phase uses 3 MOSFETs.

The timing shown in Fig. 1.9 indicates that each of the 6 phases injects ringing current into the 12V plane. The ringing frequency (shown in Fig. 1.3) is based on the loop inductance and the capacitance of the two low side MOSFETs. A total of 34 capacitors are placed on this plane.

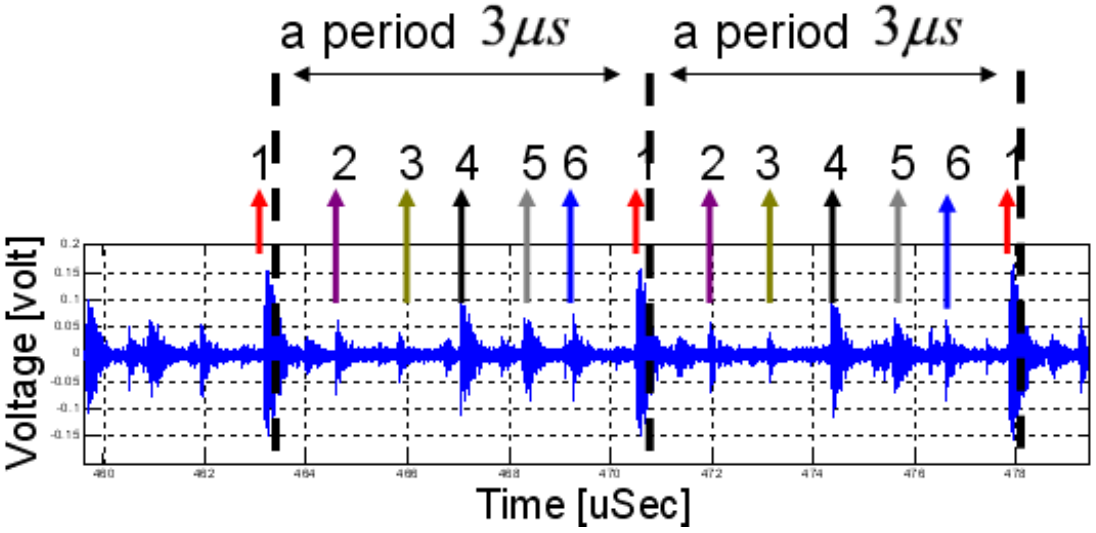


Fig. 1.9 Noise voltage illustrating the timing of the 6 converter legs.

1.4. CURRENT SPREADING SYNCHRONIZED MEASUREMENT

All converters ring at the same frequency range; however, they do not switch at the same moment. Thus, by synchronizing an oscilloscope to a specific phase of the converter, one can determine how the current of the converter spreads over all the possible capacitors.

Fig. 1.10 shows the test setup of the synchronized measurement [5]. One channel of an oscilloscope is connected to a 1x1 mm H-field probe, which is placed on the capacitor of interest. A second probe is placed on one phase; this is the trigger signal, which determines which parts of the current in the capacitor of interest are related to the MOSFET group selected as a trigger source.

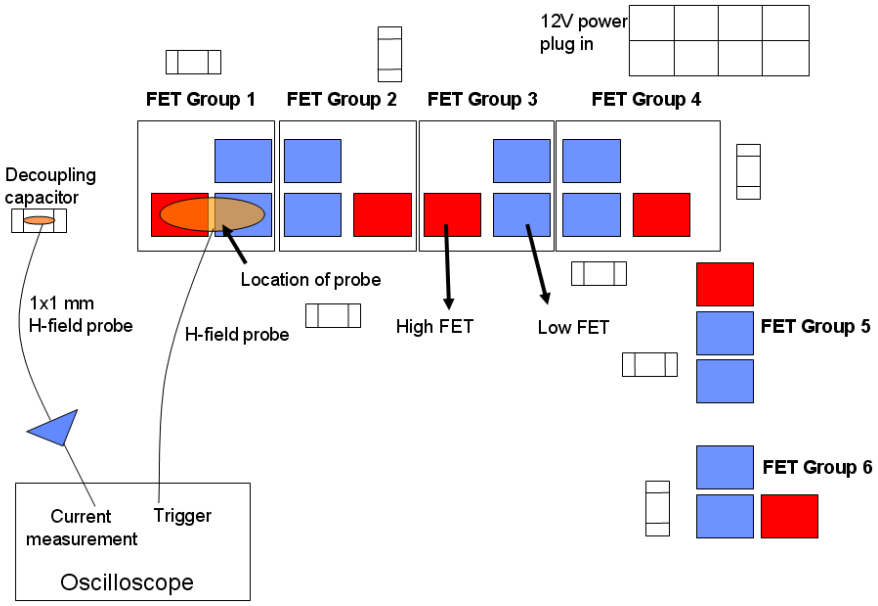
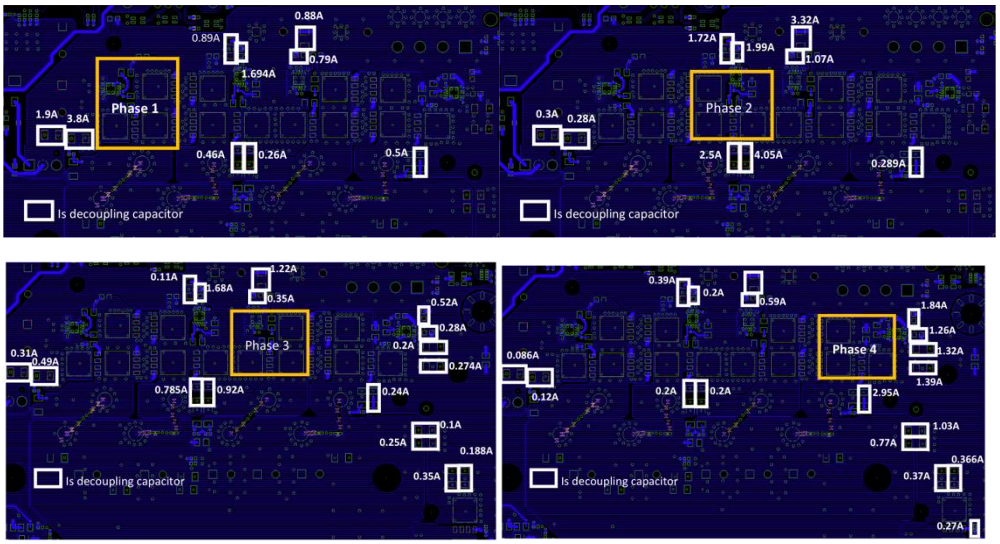


Fig. 1.10 Test setup of the synchronized measurement.

Using the mutual inductance M, one can estimate the current in the capacitor from the voltage induced in the 1x1 mm probe. This measurement must be performed for each of the converter phases and for each capacitor, generating a larger data set, as illustrated in Fig. 1.11.



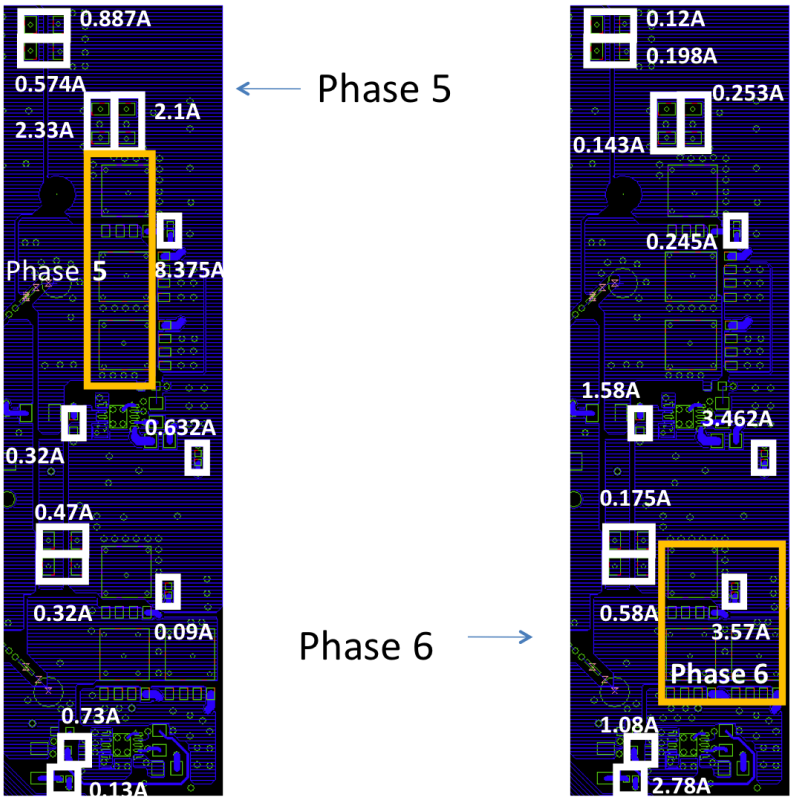


Fig. 1.11 Current spreading from phases 1-6 throughout capacitors.

Fig. 1.11 shows the current spreading for phases 1 through 6. The decoupling capacitors are represented by white rectangles. This measurement showed that the

currents were not well localized. The current spread widely over the whole board, meaning that the loop currents pass many other components.

1.5. LOCALIZATION COEFFICIENT

To judge the localization of the current spreading, a new parameter needs to be defined. The localization coefficient is defined as:

$$LC = \frac{1}{I_{total}} \sum_{i=1}^{n} I_i \cdot d_i$$

Where I is the total current flowing through one phase. This total current is the summation of all the current on the decoupling capacitors. The term I_i is the current flowing on one capacitor from one phase, and d_i is the distance between the capacitor and the center of the MOSFETs group. The term n is the number of decoupling capacitors.

In Fig. 1.12, n is 2, I_1 is 1.5A, I_2 is 2A, d_1 is 2cm, and d_2 is 2.5cm. The localization coefficient (LC) is: $\frac{1.5\times2+2\times2.5}{2+2.5} = 2.3$.

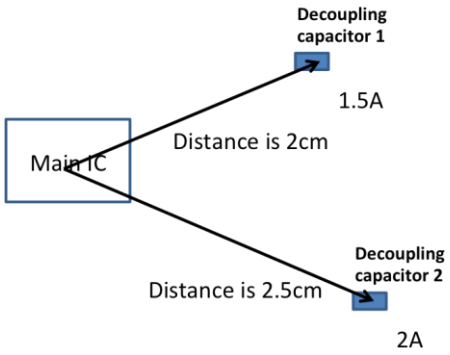


Fig. 1.12 Example to calculate the localization coefficient.

If the value of the localization coefficient is small, the circuit is localized. Otherwise, the currents are spreading widely.

1.6. MOTHERBOARD REDESIGN

The analysis showed that the current is not well localized. A better localization seemed achievable by improved capacitor placement and a reduction of the loop inductance (Fig. 1.13), which was made possible by adding another ground plane.

Fig. 1.13 shows parts of the new design.

The most significant change was the placement of a ground plane in layer 2 to reduce the loop size. The decoupling capacitors were placed for minimal loop size.

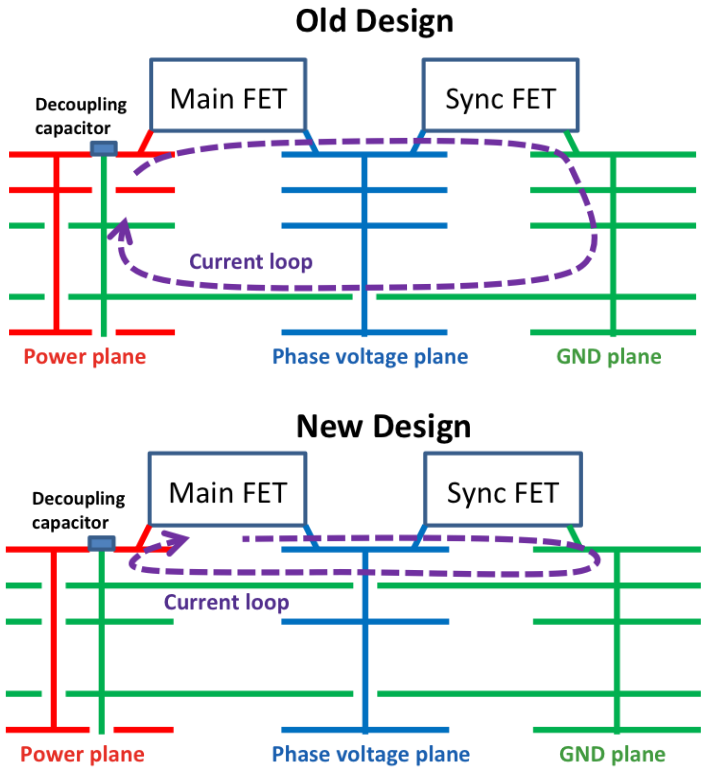


Fig. 1.13 Addition of a second layer as the ground plane to reduce the current return loop size.

The ground planes were connected by many vias such that the magnetic field from the radio frequency (RF) currents flowing vertically through the PCB would be cancelled by the GND loop paths formed by the planes and the vias. Thus, the field could not penetrate between the layers of the PCB beyond the wall of vias.

The synchronized measurement method showed a significant improvement in current localization and an increase in the ringing frequency. The latter indicates a reduced loop inductance. Fig. 1.14 through Fig. 1.19 compare the currents of the new board to those for the older board for phase 1 to 6.

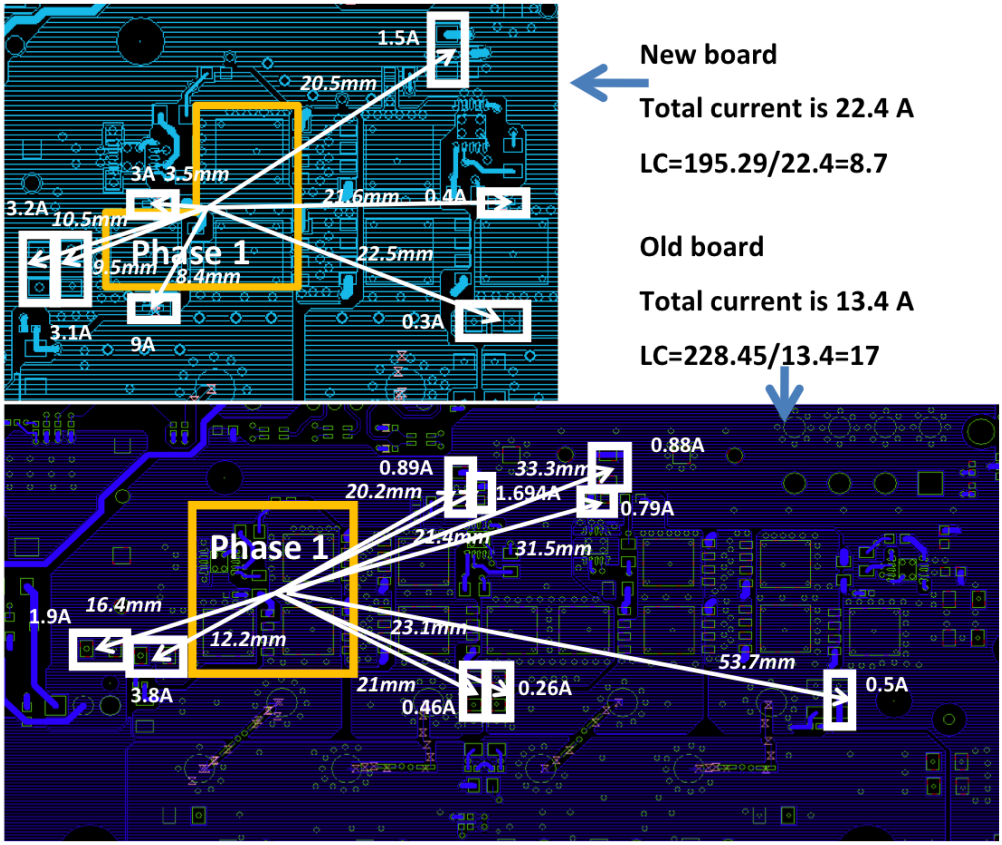


Fig. 1.14 Comparison of the current distribution on new board and old board of phase 1.

The return current path was controlled close to the MOSFETs. Less current spreading over the whole board would lead to fewer far-field emissions.

The far-field measurement of the new board confirmed the improvement of the radiated emissions, which were reduced by 8 dB.

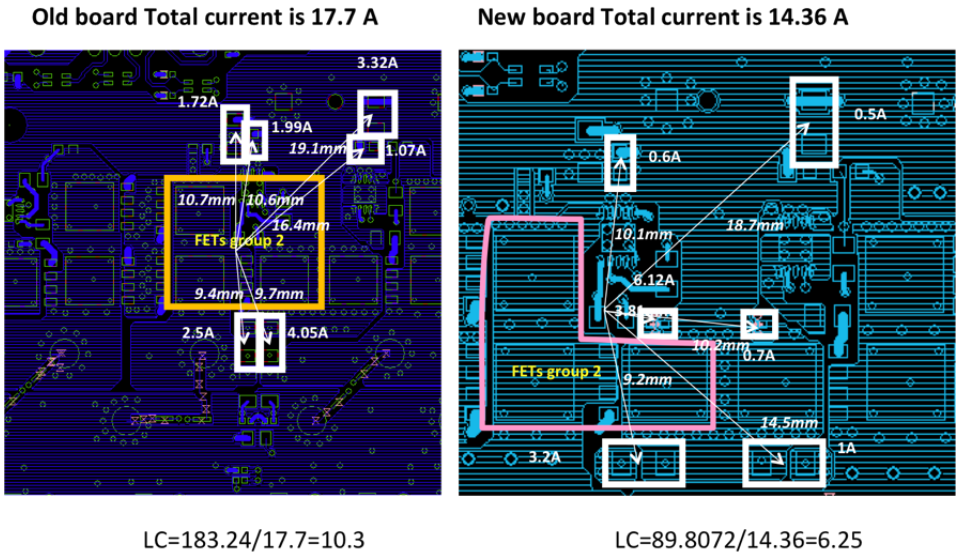


Fig. 1.15 Comparison of the current distribution on new board and old board of phase 2.

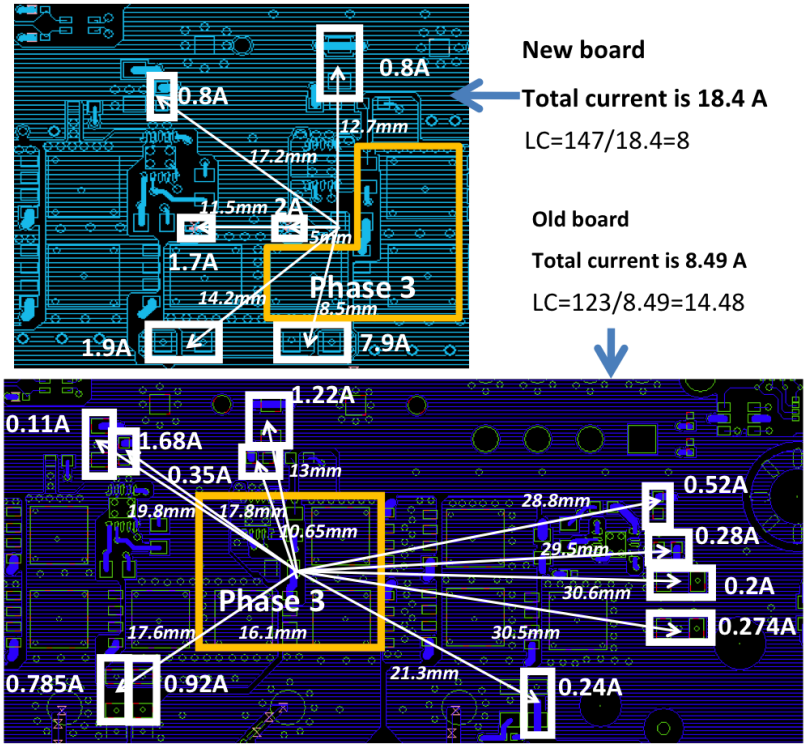


Fig. 1.16 Comparison of the current distribution on new board and old board of phase 3.

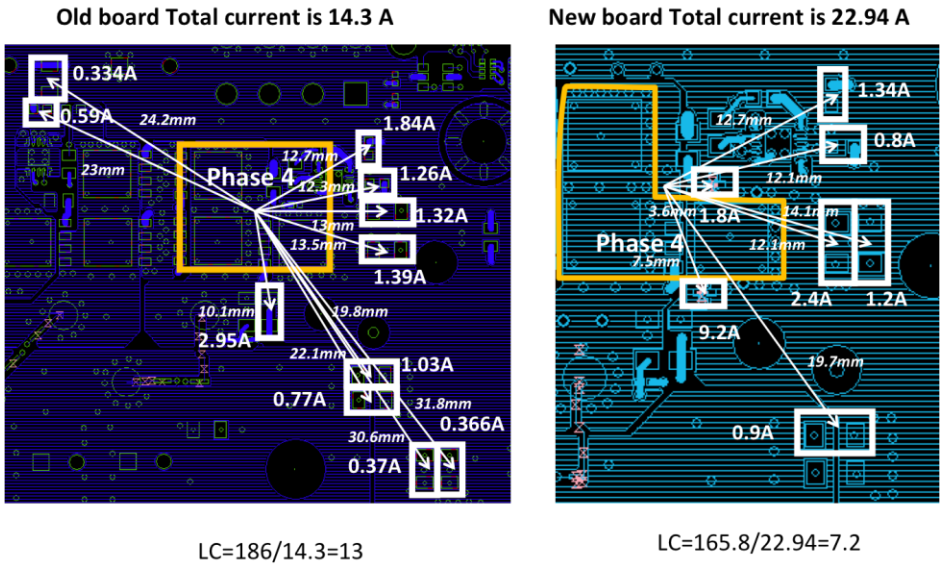


Fig. 1.17 Comparison of the current distribution on new board and old board of phase 4.

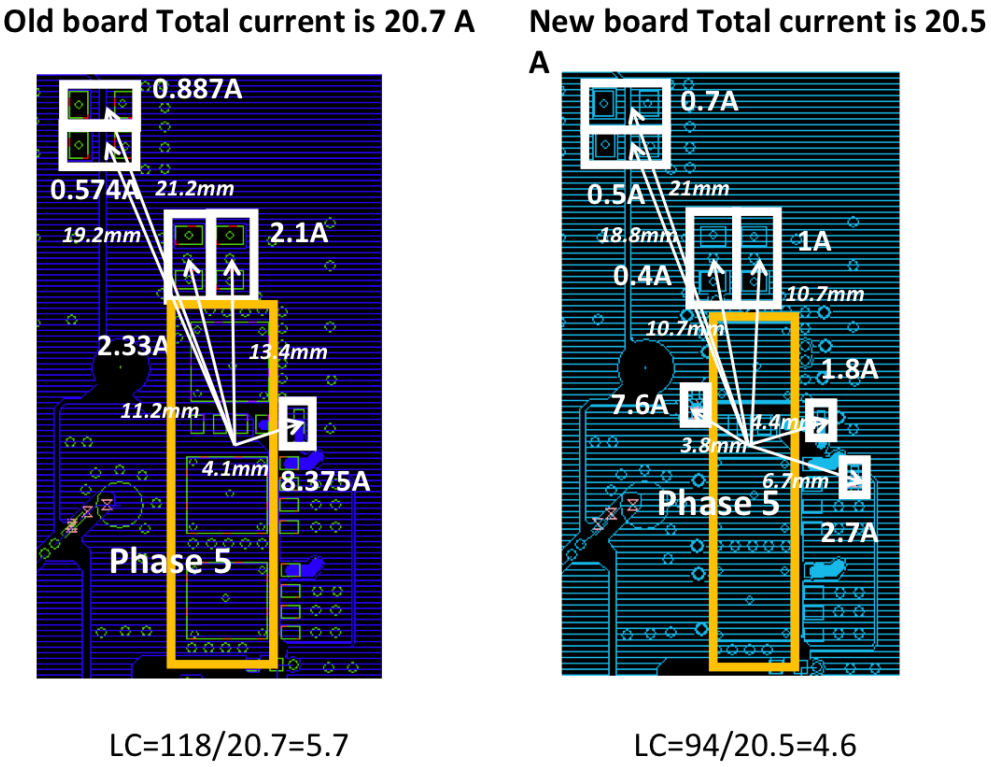


Fig. 1.18 Comparison of the current distribution on new board and old board of phase 5.

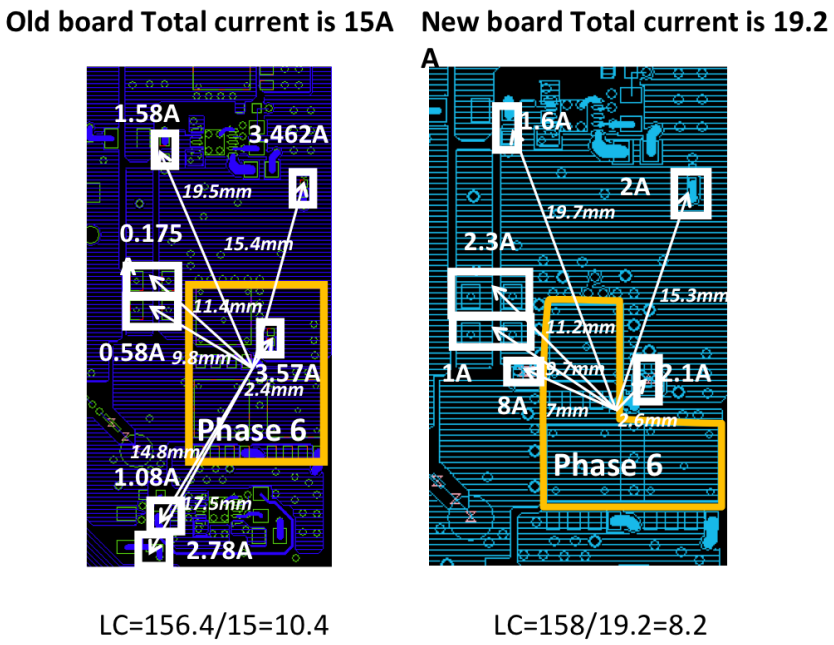


Fig. 1.19 Comparison of the current distribution on new board and old board of phase 6.

1.7. FIELD SCANNING TO ASSIST CURRENT DISTRIBUTION ANALYSIS

Automatic field scanning is a useful methodology to analyze current distribution and assist in PCB design [6~8]. Combined with synchronized measurement, this method can track the current originating from one phase of the DC/DC convertor on the outside of the PCB.

During the scanning, the z-direction is defined as the direction normal to the board. A 7-mm diameter shielded horizontal H-field probe was used to capture the z-component of the magnetic field (H_z) signal using an oscilloscope, which was triggered by another H-field probe placed on the MOSFETs group. (Fig. 1.20)

Fig. 1.20 compares the distribution of the vertical magnetic field on the back side of the PCB board around the DC/DC convertor area over two phases.

These two data were measured using the synchronized measurement methodology. The trigger positions on the front side are presented by white crosser in the figure indicating the positions of the MOSFETs. The scanning result from the previous design

(In Fig. 1.21, majority of the current is inside the circled region.), demonstrates that the currents spread widely, but remained around the trigger points located at various phases of the buck converter.

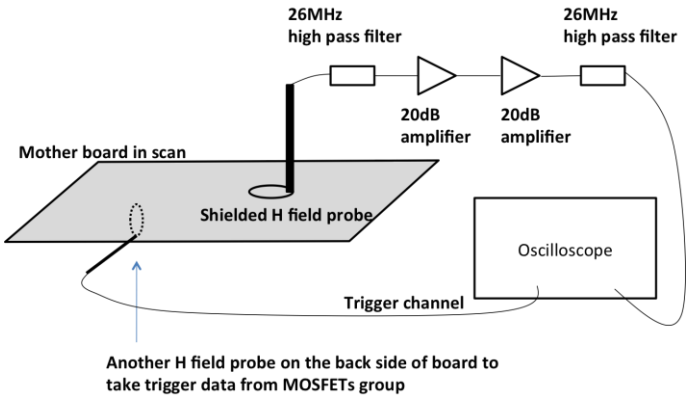


Fig. 1.20 Automated scanning test setup for Hz measurement over the board.

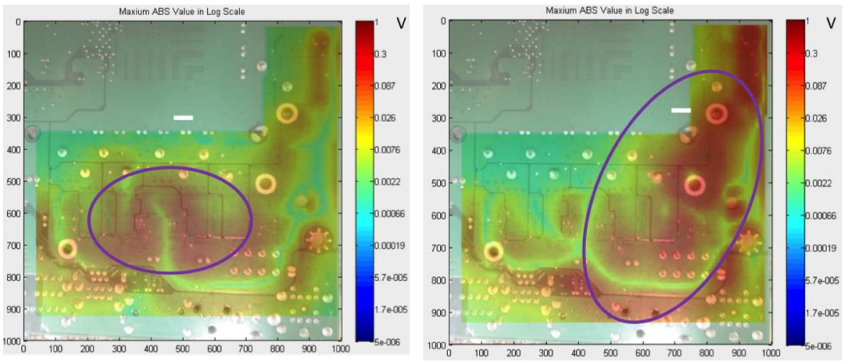
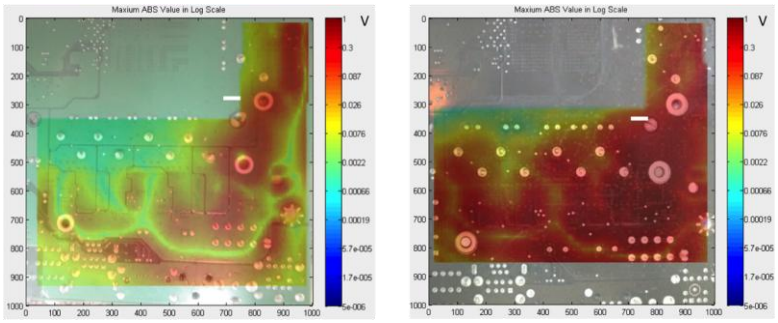


Fig. 1.21 Comparison of the Hz-field measured around 60 MHz using an automatic scanning system. Shown is the back side of the board for two different trigger conditions: (a) Hz field captured by triggering to Phase 2 and (b) Hz field captured using a trigger from Phase 4.

Fig. 1.22 compares the H_z-field on the bottom layer from boards of two different designs by triggering at the same phase. Since the earlier design (Fig. 1.22b) had reference plane on layer 2, most of the current returned through layer 5, which was close to the bottom

layer. More Hz-field was been detected on the earlier design. The new design was much improved by control of the current around the local area and reduction of the amplitude of the H_z-field on the bottom layer.



(a) (b)

Fig. 1.22 Comparison of the Hz-field measured using an automatic scanning system. Shown are the back sides of the board from (a) the new design and (b) the old design. The Hz-field was captured by the same trigger to Phase 4.

Synchronized measurement clarifies the current distribution. A good design should control the current in a small region around the trigger point.

1.8. CONCLUSION

Time-synchronized measurement makes it possible to determine the current paths for systems that have sources distinguishable by timing. Understanding of the noise current distribution facilitates circuit and layout optimization and thus improves our understanding of counter EMI methods.

2. A HIGH FREQUENCY ANALYTICAL MODEL FOR THE COMMON-MODE IMPEDANCE OF A FERRITE CHOKE

2.1. INTRODUCTION

With the increased use of the digital equipment, electromagnetic compatibility problems are becoming increasingly important. To solve the electromagnetic interference (EMI) problems and electromagnetic immunity problems, ferrites chokes are widely used to reduce common mode current by increasing the common mode impedance in a certain frequency range. However, the working frequency range of a ferrite choke on a system is difficult to predict; not only does it depend on the ferrite material and geometry, but it also relies on the system structure and the location of the ferrite. More importantly, although much work has been published on single lumped element models of ferrite cores [9-13], these models fail at high frequency because the ferrite is no longer electrically short. To ensure agreement between measured and analytical results at high frequency, discrete lumped element models have been developed for ferrite cores [14-18].These models, however, do not clearly explain the internal mechanism of the ferrite.

To ensure close agreement at high frequencies and have more physical meaning, this work developed a novel transmission line model based on the Maxwell equation. The model calculates the change in impedance of the cable bundle case with a ferrite choke attachment. This work aimed to establish an analytical model for ferrite chokes placed on a brass tube located above a metallic plane. This paper introduces a method of modeling a ferrite choke attached to a brass tube over a current return plane structure using transmission line theory approximation. One test structure was built to measure the change in common mode impedance due to ferrite. The same test structure was also used to verify the ferrite modeling results with experimental measurements.

2.2. THEORY

A test structure was modeled since ferrite behavior is based on its location in the system and on the structure of the system. The test structure was designed based on the general use of ferrite chokes in a real power system with 3-phase power cables connecting the power inverter and motor with the chassis (Fig. 2.1 Ferrites are used in a real system with multiphase power cables). Power cables often bring common mode currents, causing EMI problems. In most cases, the common mode current returns from the ground (i.e., the current return path). In this test structure, the ferrite was placed on the power cables to reduce the common mode current.

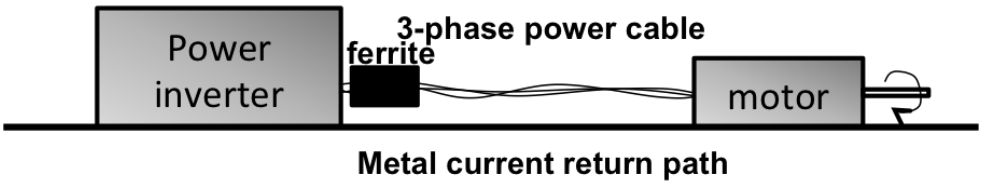


Fig. 2.1 Ferrites are used in a real system with multiphase power cables.

To simplify the problem, a brass tube was used to replace the multiphase power cables since these cables carry common mode currents together. The current return path was modeled as a solid metallic plane located beneath the brass tube. The test structure was composed of a brass tube passing over a solid metallic plane, and this structure was treated as a transmission line system since there are only two conductors. This model considers a TEM wave. It simplifies all waves as a single TEM wave when the ferrite

choke is clamped on the system as shown in Fig. 2.2. Higher modes appear in the higher frequency range, which is not discussed here.

To characterize the system behavior, the total system impedance [18] had to be calculated. For the simplified test structure (Fig. 2.3) modeled from the real case (Fig. 2.1), this paper uses the input impedance from one port as a common mode load impedance to characterize the ferrite behavior as well.

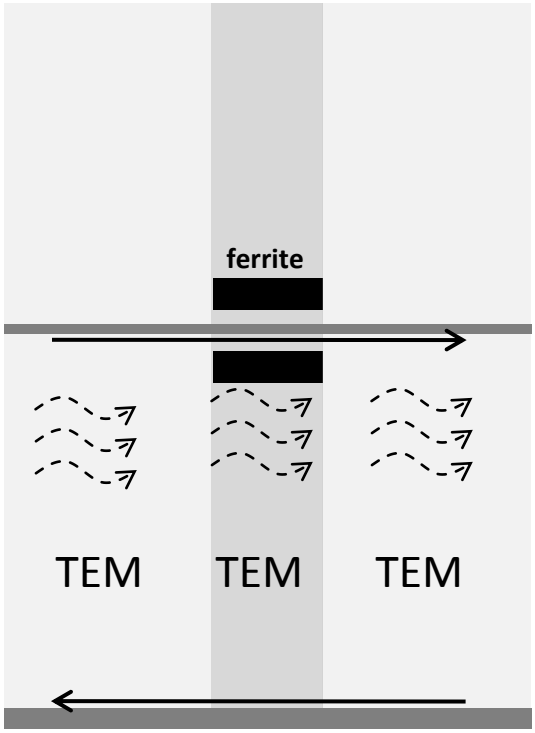


Fig. 2.2 Cross section of brass tube over current return path system with ferrite clamped on. In real-world cases, all waves can be simplified as a single TEM wave. The results indicate that this is an acceptable simplification.

RLGC parameters and transmission line theory [19] were used to calculate the input impedance of the brass tube over the current return path system. Once the RLGC

parameters have been calculated, the characteristic impedance can be expressed by

$$Z = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{1}$$

and the propagation constant by

$$\gamma = \sqrt{(R + j\omega L) \cdot (G + j\omega C)}. \tag{2}$$

The RLGC parameters for the brass tube over current return path system in air (with no dielectric loss) and with no ferrite attaching condition can be calculated using the following equations:

$$R = R_{conductor\_loss} \tag{3}$$

$$L = \frac{\mu_0}{2\pi} \cdot \ln\left(\frac{r_{wire}}{h}\right) \tag{4}$$

$$C = \frac{2\pi\varepsilon_0}{\ln\left(\frac{r_{wire}}{h}\right)} \tag{5}$$

$$G = 0, \tag{6}$$

where $R_{conductor\_loss}$ is the conductor loss of the brass tube, r_{wire} is the radius of the brass tube, and h is the height of the brass tube over ground. RLGC is represented here per unit length parameters. When the ferrite choke was placed on the brass tube, the RLGC parameters were calculated based on the geometry and material properties of the ferrite, as shown in the following sections.

2.2.1. Inductance Per Unit Length (L) Calculation. The inductance per unit length was defined as:

$$L = \frac{\psi}{I \cdot l} = \frac{\int B \cdot dS}{I \cdot l}. \tag{7}$$

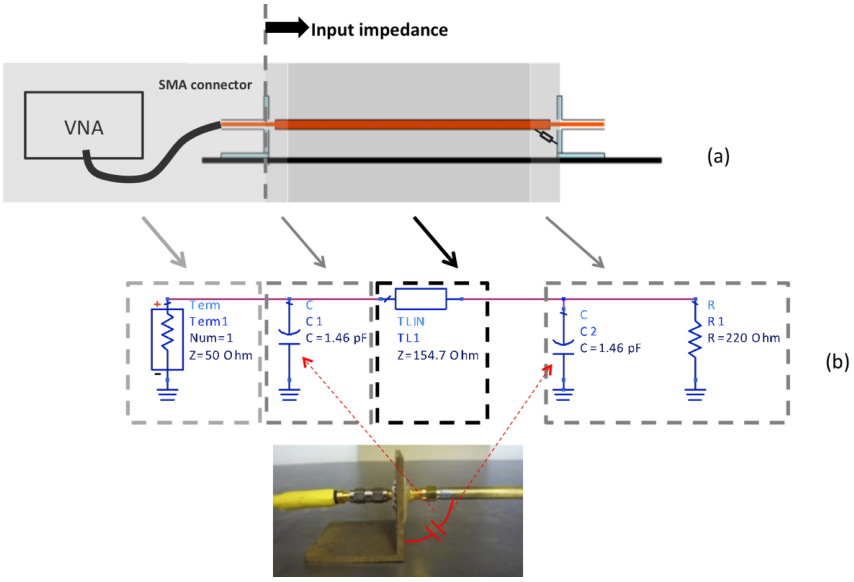


Fig. 2.3 Model for the real system (a) Simplified structure based on the real system, (b) SPICE model for the structure and the capacitor between brass tube and brass stand.

The integral area for flux was estimated; this was the total flux in the area between the brass tube and the current return path (pink region in Fig. 2.4 Inductance per unit length parameter calculation method with ferrite choke on the brass tube). Since the test structure was composed of a wire over a current return path system, the system can be treated as a mirror system. By removing the current return path, a mirror brass tube and a mirror ferrite are added to the system (Fig. 2.4). The flux in the integral area caused by the brass tube current and the mirror brass tube current was calculated to obtain the equivalent inductance per unit length. However, most of the magnetic field from the mirror current was attracted by the mirror ferrite; therefore, the flux in the integral area caused by the mirror current can be disregarded. The final flux considered in the integral area contained only current from the brass tube.

Several parameters were defined in the structure: r_{in} is the inner radius of the ferrite, r_{fert} is the outer radius of the ferrite, H is the height of the brass tube away from the current return path, r_{wire} is the radius of the brass tube, μ_r is the permeability of the ferrite (Fig. 2.5 Geometry parameter definition and the cross section of the structure showing the flux of the areas to be calculated).

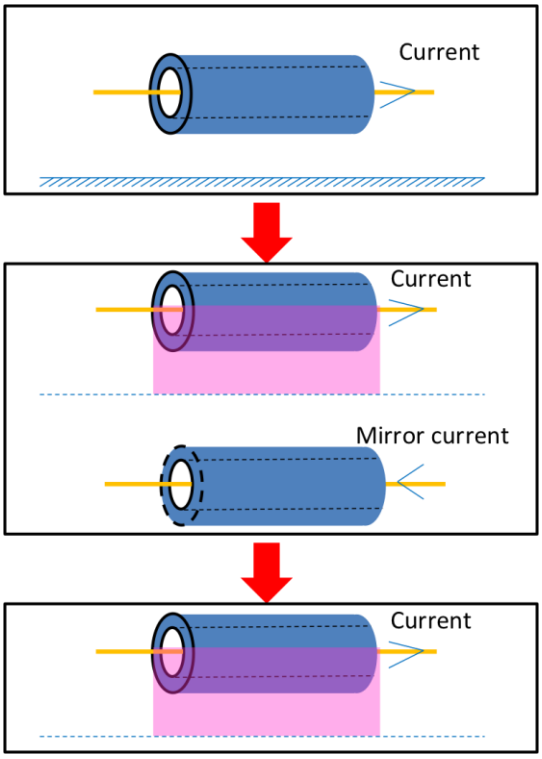


Fig. 2.4 Inductance per unit length parameter calculation method with ferrite choke on the brass tube.

To calculate the inductance in the integral region (Fig. 2.4), the areas of three parts of the integral region had to be calculated individually: the area between the brass tube and the ferrite (S1), the area inside the ferrite (S2), and the area between the ferrite

and the current return path (S3) (Fig. 2.5).

From the equations

$$B = \frac{I \cdot \mu_0}{2\pi r} \tag{8}$$

and

$$dS = l \cdot dr, \tag{9}$$

the flux per unit length in area 1 (S1) can be calculated as

$$\psi_1 \approx \int_{r_c}^{r_{in}} \frac{I \cdot \mu_0}{2\pi r} \cdot dr. \tag{10}$$

Similarly, the flux of other two areas (S2, S3) can be calculated as

$$\psi_2 \approx \int_{r_{in}}^{r_{fert}} \frac{I \cdot \mu_0 \cdot \mu_r'}{2\pi r} \cdot dr \tag{11}$$

and

$$\psi_3 \approx \int_{r_{fert}}^{h} \frac{I \cdot \mu_0}{2\pi r} \cdot dr. \tag{12}$$

By summing the results of (10), (11), (12), the total flux can be obtained:

$$\psi \approx \frac{\mu_0 \cdot I \cdot l}{2\pi} \left[\ln\left(\frac{r_{in}}{r_{wire}}\right) + \ln\left(\frac{h}{r_{fert}}\right) + \mu_r' \cdot \ln\left(\frac{r_{fert}}{r_{in}}\right)\right]. \tag{13}$$

Then, from equations (7) and (13), the inductance per unit length can be calculated as:

$$L = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{r_{in}}{r_{wire}}\right) + \ln\left(\frac{h}{r_{fert}}\right) + \mu_r' \cdot \ln\left(\frac{r_{fert}}{r_{in}}\right)\right]. \tag{14}$$

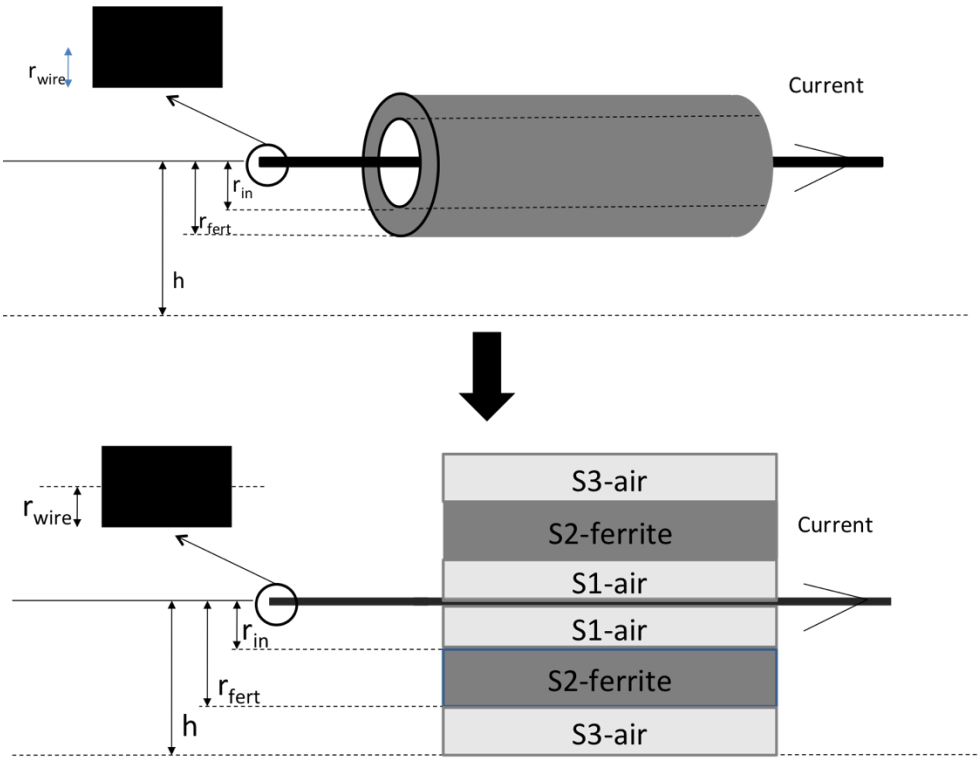


Fig. 2.5 Geometry parameter definition and the cross section of the structure showing the flux of the areas to be calculated.

2.2.2. Calculations of Resistance Per Unit Length Calculation. The resistance per unit length of the structure with ferrite had two parts: the resistance of the brass tube, which can be calculated based on the skin effect method [18], and the other part was contributed by the ferrite since a lossy term was contained in the imaginary part of ferrite's permeability. Since the resistance of the ferrite was a result of the rotation energy loss of the magnetic dipole, the resistance calculation can be part of the inductance calculation with the imaginary ferrite's permeability. In the calculating the resistance, $\boldsymbol{\mu_r}'$ was replaced by $\boldsymbol{\mu_r}''$ in (14):

$$R_{ferrite} = 2\pi\omega L \approx \frac{\omega\cdot\mu_0}{2\pi}\left[\mu''_{r\_air}\cdot\ln\left(\frac{r_{in}}{r_{wire}}\right)+\mu''_{r\_air}\cdot\ln\left(\frac{h}{r_{fert}}\right)+\mu''_{r\_ferrite}\cdot \text{lnrfertrin}.\right. \quad (15)$$

Thus , $R_{ferrite}$ is calculated as:

$$R_{ferrite} \approx \omega\cdot\mu_0\cdot\mu''_{r\_ferrite}\cdot\ln\left(\frac{r_{fert}}{r_{in}}\right), \quad (16)$$

and R as

$$R \approx R_{skin} + \omega\cdot\mu_0\cdot\mu''_{r_{ferrite}}\cdot\ln\left(\frac{r_{fert}}{r_{in}}\right). \quad (17)$$

2.2.3. Calculation of Capacitance and Conductance Per Unit Length Calculation. Capacitance per unit length was calculated in three steps shown in Fig. 2.6 and Fig. 2.7. The electrical fields were not perpendicular to the surface of the ferrite because the latter was not a perfect electric conductor (PEC), and the field distribution was not homogeneous. Thus, the capacitance was difficult to calculate analytically, making an approximation necessary. The main assumption was that the electric field between the brass tube and the inner radius of the ferrite, and the electric field between the inner and outer radius of the ferrite are symmetric. Thus, the coaxial capacitance formula can be used here to calculate the capacitance per unit length:

$$C_1 \approx \frac{2\pi\varepsilon_0}{\ln\left(\frac{r_{wire}}{r_c}\right)} \quad (18)$$

and

$$C_2 \approx \frac{2\pi\varepsilon_0\varepsilon'_r}{\ln\left(\frac{r_{fert}}{r_{in}}\right)}, \quad (19)$$

where ε_r' is the real part of the permittivity of the ferrite, and C_3 can be considered the capacitance of the brass tube over the ground system, which can be expressed as

$$C_3 = \frac{2\pi\varepsilon_0}{\cosh^{-1}(\frac{h}{r_{fert}})}. \tag{20}$$

The total capacitance per unit length is

$$C = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}} \quad . \tag{21}$$

Since the contributed loss of the conductance was from ferrite, G can be calculated as

$$G = \omega \cdot C_2 \cdot \frac{\varepsilon_r''}{\varepsilon_r'} . \tag{22}$$

The characteristic impedance and propagation constant was obtained using (1) and (2). This model can be used in a real system and the total system impedance can be obtained once the system details are known.

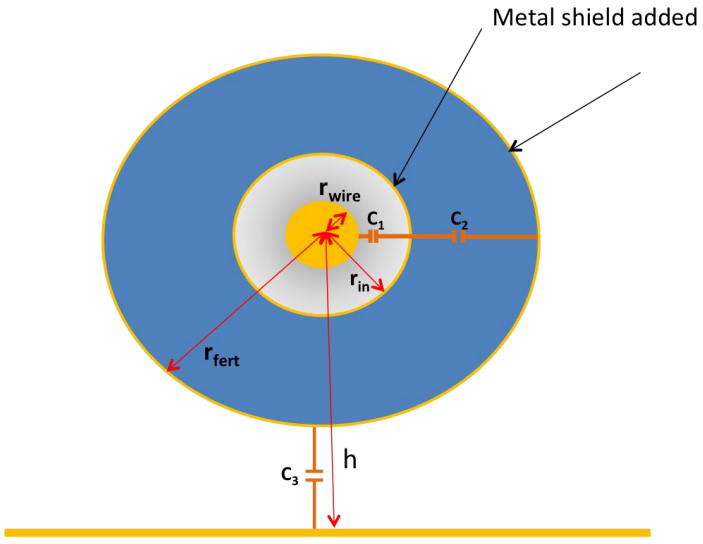


Fig. 2.6 Cross section of the brass tube over the ground system with ferrite.

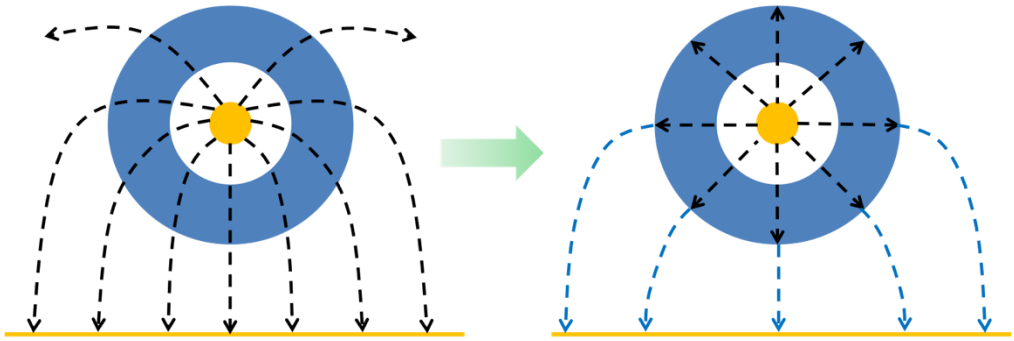


Fig. 2.7 Approximation of the E-field of the structure: which the model considers a radial symmetry distribution.

2.3. STRUCTURE

To test and verify the analytical model for ferrite, a simple test structure similar to the brass tube over current return plane system (Fig. 2.1) was designed and tested (Fig. 2.8). At this stage, the analytical model for the test structure was built. Since all the details of the test structure details were known, the input impedance from one side of the system was calculated analytically. For experimental verification, a vector network analyser (VNA) was used to measure the input impedance from one side of the whole system through a Z11 measurement. A ferrite choke was then placed on the test structure, and the new input impedance was measured. The ferrite model was implemented to the model of the test structure to calculate the new analytical input impedance. This impedance was then verified by the experimental results.

2.3.1. Analogy to a Real Power System. As shown in Fig. 2.1, a brass tube was incorporated in the test structure to simulate the common mode current on the 3-phase power cables, The signal passing through the brass tube was used to model the common mode current on the power cables. In most cases, in a real power system, the inverter and motor are covered by enclosures, which can be modeled by the brass stand in the test

structure. Here, the brass stand was in an L shape (Fig. 2.8), which ensured good contact with the ground plane and modeled the enclosure of the inverter and the motor. To reduce the common mode current in a real system, a ferrite choke was placed on all the power cables. In the test structure, the ferrite was placed on the brass tube to reduce the signal running on the tube.

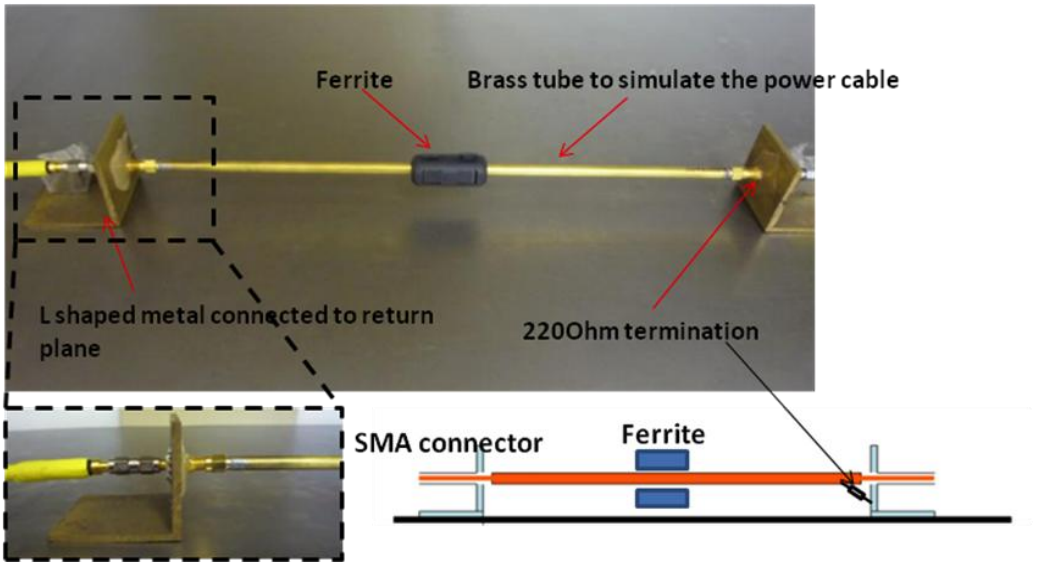


Fig. 2.8 Simplified test structure based on a real power system.

2.3.2 Modeling the Test Structure. Once the test structure was built, verification of the analytical ferrite model required knowledge of all the details of the test structure so that the measured input impedance could be compared with the results of the analytical calculation of the whole structure with the ferrite choke. The test structure was divided into several parts for modeling (Fig. 2.9). VNA was used to measure the input impedance. Fig. 2.9 shows the voltage source including the VNA. This part was modeled as a 50-ohm

source. Two critical capacitors were placed between the brass tube and the brass stand, labeled respectively in Fig. 2.9 as C1 and C2. The middle part of the brass tube over the ground system was modeled as a transmission line system. When the system without ferrite was terminated, the frequency response of Z11 was flat. The working frequency range of the ferrite was easily obtained from the elevated region of the Z11 curve with the ferrite attached to the system. Thus, a 220-ohm resistor was used at the end of the structure to match the whole system based on the characteristic impedance of the brass tube over ground system (23)

$$Z = \sqrt{\frac{L}{C}}. \tag{23}$$

Since it was extra, the capacitance between the brass tube and the brass stand (Fig. 2.9) was crucial to the structure's response. Two locations in the system, the termination end and the source end had this capacitance; the values were the same for both. Fig. 2.10 shows the details of the connection between the brass tube and the brass stand, chich were joined by an SMA connector. The structure was divided into three parts, and the capacitance of each part was calculated individually. Part 1 was the capacitance between the brass tube and the brass stand. Part 2 was the capacitance between the connector and the brass stand. Part 3 was the capacitance between the inner conductor and the brass stand.

Part 1 (Fig. 2.11) was contributed by a portion of the brass tube and a portion of the brass stand. The length of the brass tube to be used in the calculation was difficult to determine because most of the tube contributed to the capacitance of the transmission line. Because all the electric field lines came for this capacitor came from the tube to end at the stand, a rough approximation was made, assuming that the length of the tube was the

same as that of the stand, which equalled the distance from the lower edge of the connector to the current return plane. This approximation fails when higher propagating orders appear, which was not the case here. The capacitance between a cylinder and a sheet was difficult to derive.

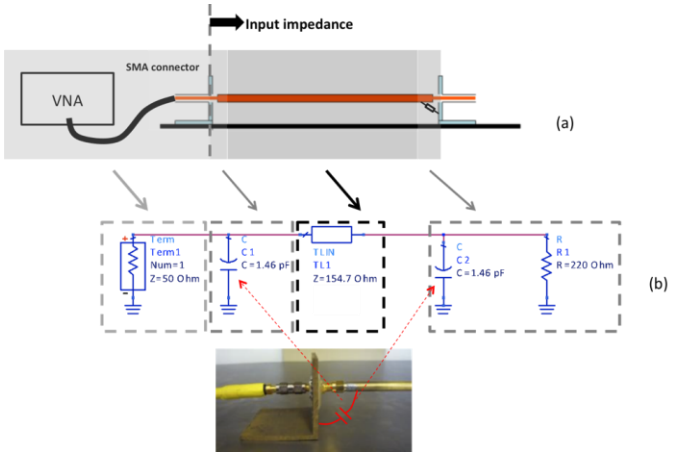


Fig. 2.9 Test setup and model of the test structure.

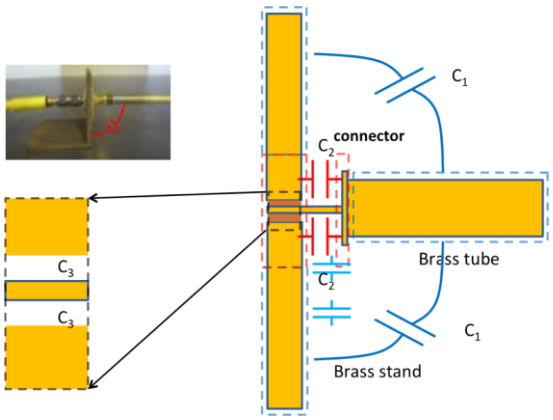


Fig. 2.10 Detail of the connector between the brass stand and the brass tube, showing three capacitance parts.

It was calculated by unrolling the brass tube so that it became a sheet. The capacitance between the brass tube and the brass stand then became the capacitance between two perpendicular sheets. The capacitance [20] was calculated by

$$C = \varepsilon_0\left(\frac{K'(k_{in})}{K(k_{in})} + \frac{K'(k_{out})}{K(k_{out})}\right). \quad (24)$$

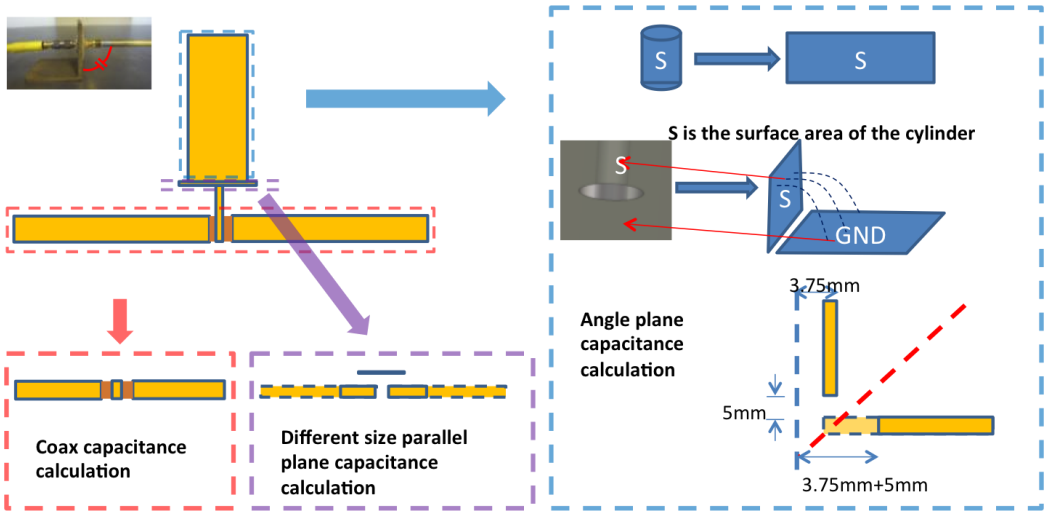


Fig. 2.11 Method to calculate the capacitance between part of the brass tube and the brass stand.

Part 2 was contributed by the SMA connector and the remaining part of the brass stand (Fig. 2.12). The area of the brass stand counted in Part 1, but it was not included in the capacitance calculation in Part 2. The capacitance between two parallel plates with different areas can be approximated based on the electrical field distribution (Fig. 2.13). Since the area of the brass stand (lower plate in Fig. 2.13) was larger than that of the connector (higher plate in Fig. 2.13), the E-field lines started from both the top and bottom surfaces of the connector end on the top surface of the brass stand. So that the top

area of the connector could be considered in the calculation of capacitance, the area of the connector was assumed to be the same as that of the brass stand. Therefore, the brass stand area (i.e., the larger area) was selected for calculation of the parallel-plane capacitance. The capacitance for Part 2 can be obtained from

$$C_2 \approx \frac{\varepsilon A}{d} \tag{25}$$

where A is the remaining area of the brass stand and d was the distance between the connector and the brass stand.

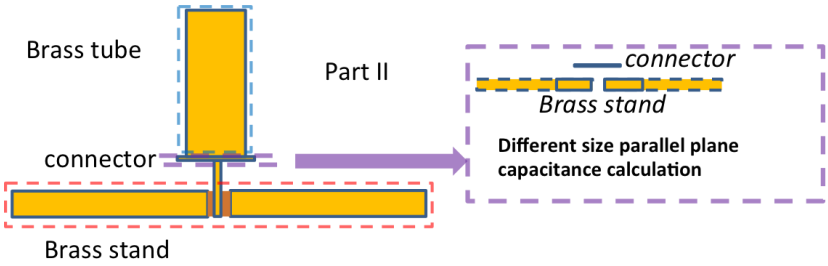


Fig. 2.12 Method to calculate the capacitance between the connector and part of the brass stand.

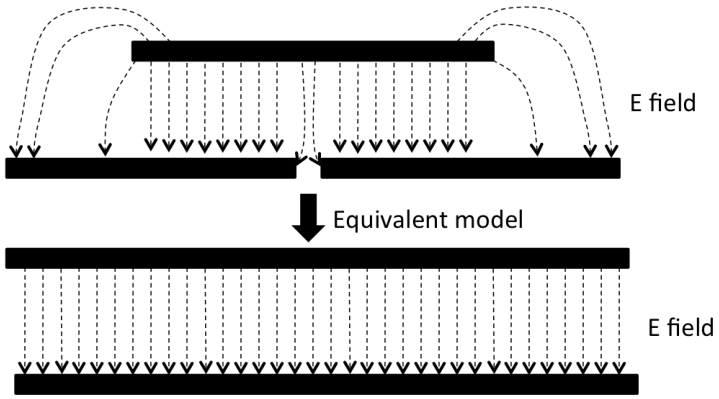


Fig. 2.13 Method to calculate the capacitance between two parallel plates with different areas.

Part 3 (Fig. 2.14) was contributed by the inner conductor of the SMA connector and the brass stand. Since Part 3 was electrically short in 1 GHz, this was a typical coaxial capacitance calculation performed by disregarding the fringing field. The capacitance value can be calculated as

$$C_3 \approx \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_{inner}}{r_{stand}}\right)}. \tag{26}$$

The total capacitance between the brass tube and the brass stand was the summation of Parts 1, 2 and 3 because all were connected in parallel:

$$C = C_1 + C_2 + C_3. \tag{27}$$

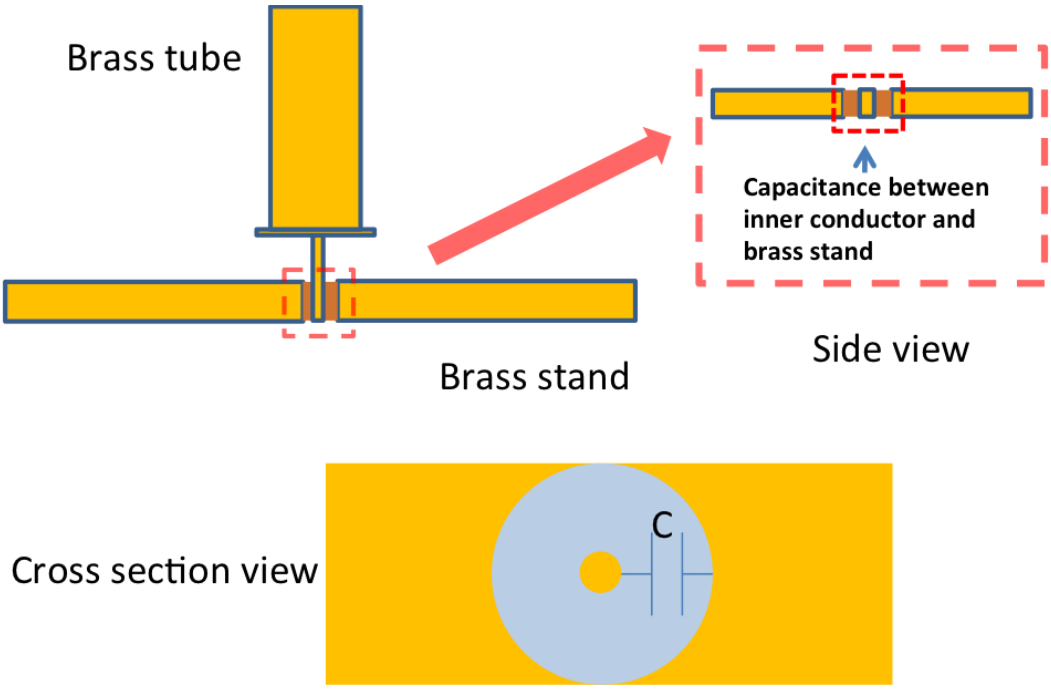


Fig. 2.14 Method to calculate the capacitance between inner conductor and the brass stand.

2.4. ANALYTICAL MODEL VERIFICATION

2.4.1. Modeling of the Simple Test Stucture Without Ferrite Choke. The capacitance between the brass tube and the brass stand was modeled analytically for the structure shown in Fig. 2.9. The capacitances at the two ends were symmetrical and had the same value. The characteristic impedance of the transmission line in the middle was calculated using the RLGC parameters. The input impedance from the source end was calculated analytically and step-by-step from the termination end, which had a 220-ohm resistor:

$$Z_{input} = Z_0 \frac{Z_{load} + Z_0 \tanh(\gamma l)}{Z_0 + Z_{load} \tanh(\gamma l)}. \quad (28)$$

In the experimental setup shown in Fig. 2.9, a (VNA) connected to the source end of the structure was used to measure the Z11, which was the input impedance of the whole structure. The radius of the brass tube was 2.16 mm; Its total length was 30 cm, and its height was 2.3 cm. Fig. 2.15 and Fig. 2.16 show the amplitude and phase result of Z11 (the input impedance from the source end). The measured input impedance was similar to the analytical result; the two curves matched closely. This test setup was then used to verify the ferrite model when ferrite was placed on the brass tube.

2.4.2. Modeling of Simple Test Structure With Ferrite Choke. The ferrite choke model was verified using the test structure previously built. The ferrite choke was placed at the brass tube on different locations, and the VNA was connected to the source end of the test structure to measure the input impedance. The analytical input impedance was obtained from the ferrite model combined with the structure model. The ferrite was placed at different locations along the brass tube, and the total input impedance of the

system from the source end was calculated using equation (26). In the simplest case, the ferrite was placed in the middle of the brass tube (Fig. 2.17). The length of the ferrite was 1.3cm, Its inner radius was 1.2cm, and its outer radius was 1.8cm.

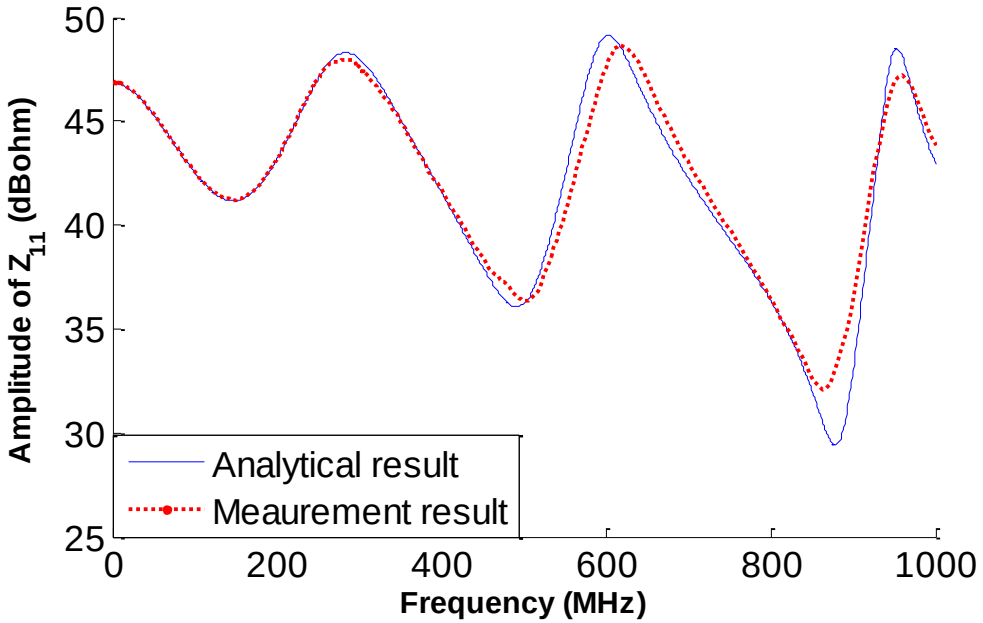


Fig. 2.15 Comparison of the calculated and measured input impedance amplitude of the structure.

Fig. 2.18 and Fig. 2.19 show the permeability and permittivity of the ferrite as indicated by the manufacture. To calculate the characteristic impedance of the middle part (shown in Fig. 2.17), RLGC parameters were used in the analytical model. Fig. 2.20 shows the measured and analytical results for the input impedance of the system with ferrite placed in the middle of the brass tube.

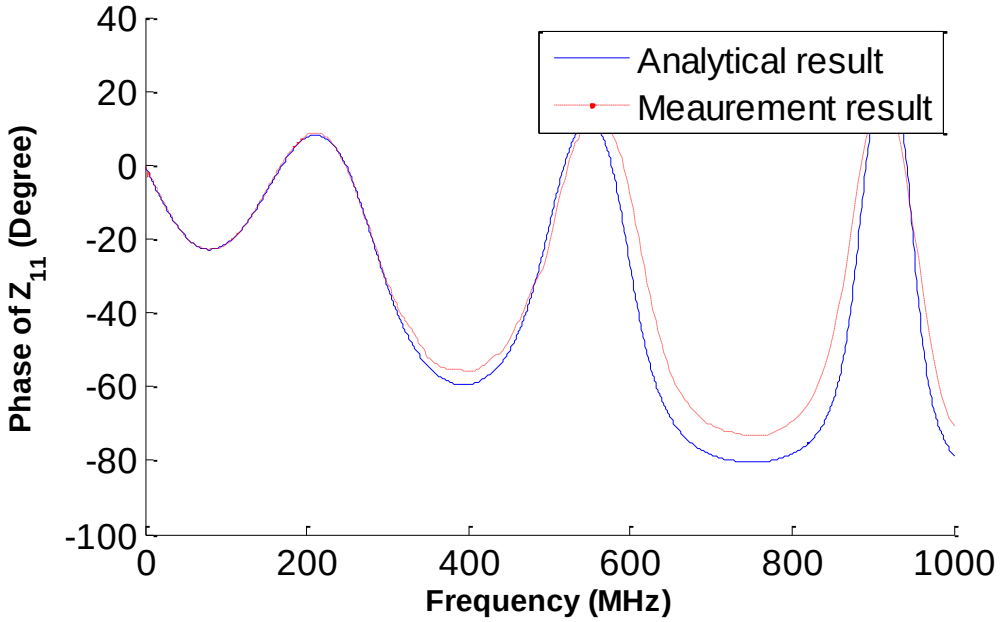


Fig. 2.16 Comparison of the calculated and measured input impedance phase of the structure.

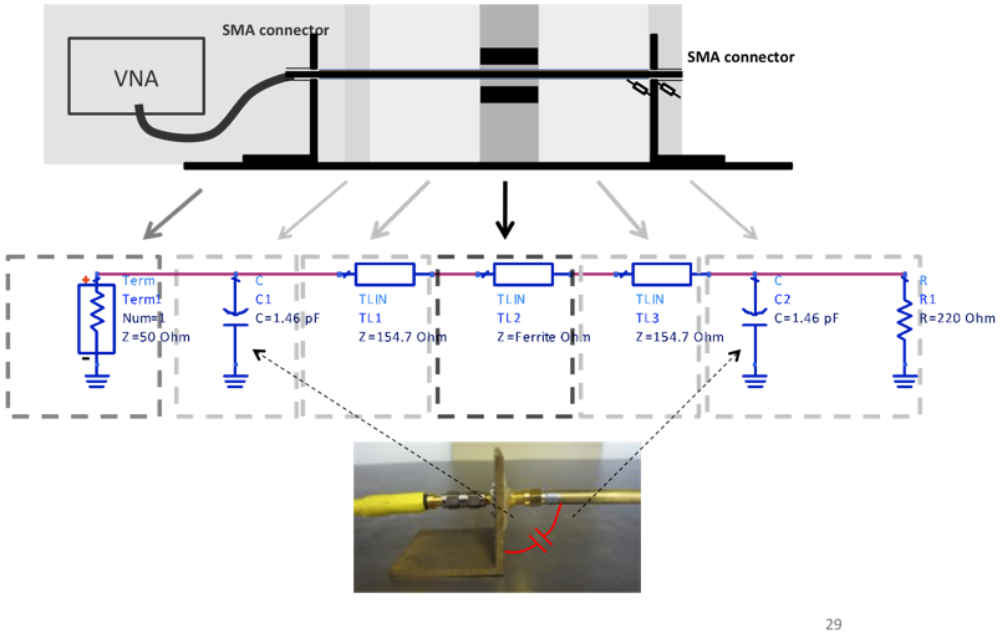


Fig. 2.17 Test setup and equivalent model with the ferrite was placed in the middle of the brass tube.

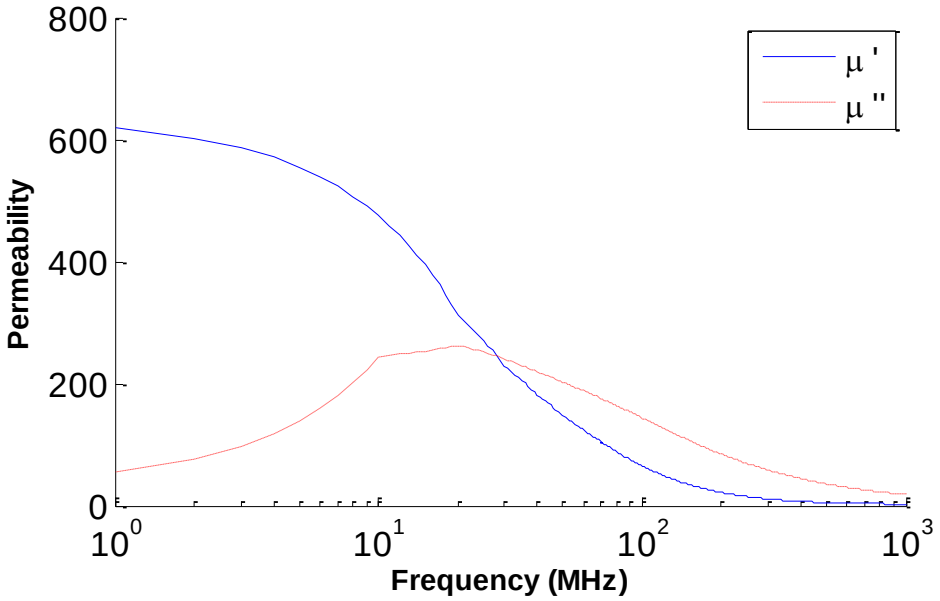


Fig. 2.18 Permeability of the ferrite used in the experiment.

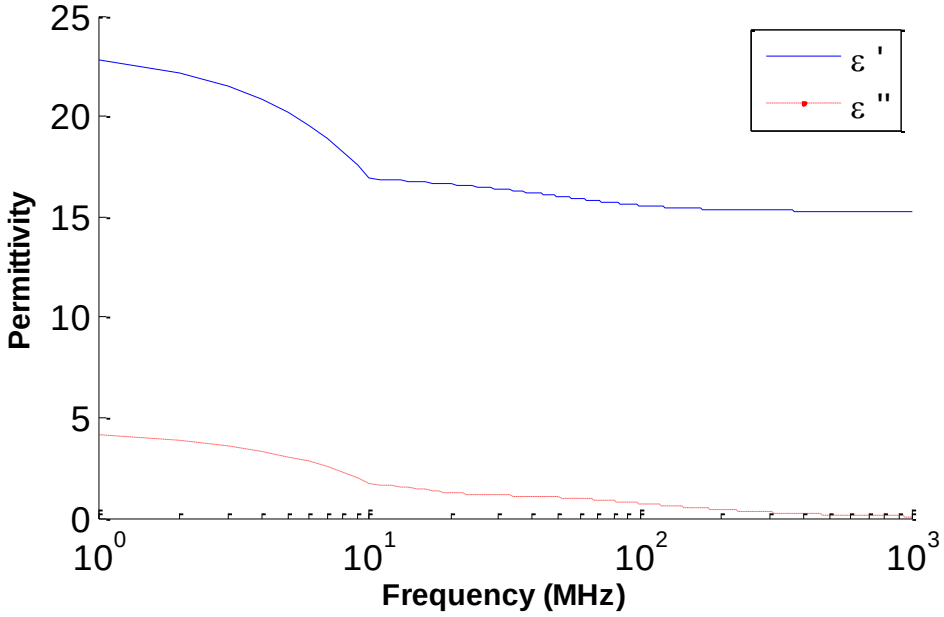


Fig. 2.19 Permittivity of the ferrite used in the experiment.

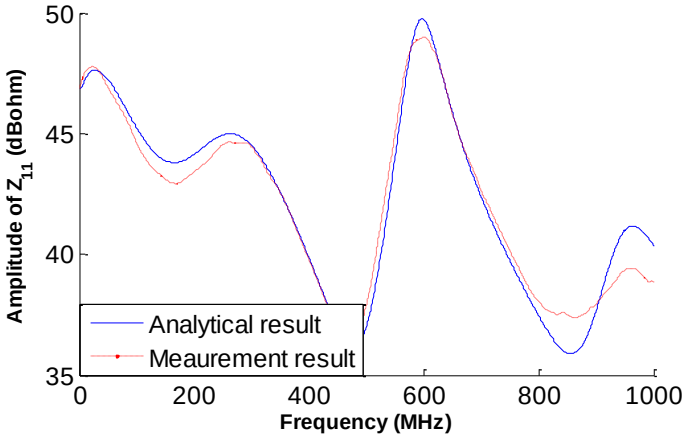


Fig. 2.20 Comparison of analytical and measured results for input impedance with ferrite placed in the middle of the brass tube.

Further verification relied on placement of the ferrite at different locations. The ferrite was placed close to the brass stand to simulate actual conditions in which ferrite is placed close to the power inverter chassis. Fig. 2.21 shows the test setup. Same method was used to calculate the input impedance of the system using (24). Fig. 2.22 shows the comparison curves.

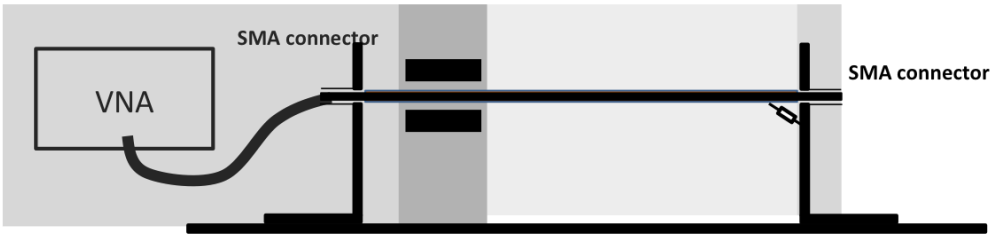


Fig. 2.21 Test setup when the ferrite was close to the brass stand to simulate placement of ferrite was placed close to the chassis in a real system.

Various heights of the brass tube were also tested, with the ferrite placed close to the brass stand. Fig. 2.23 shows the test setup with the brass tube a 7.7 cm; Fig. 2.24 shows the results. Two curves matched very closely when the ferrite was placed at different heights as well. This match suggests that the model is robust for the brass tube over a current return path system below 1GHz.

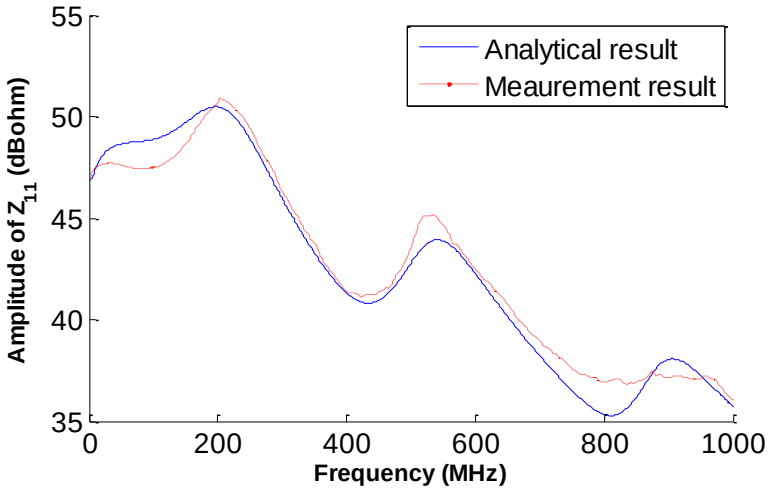


Fig. 2.22 Comparison of analytical and measured results for input impedance when ferrite was placed close to the brass stand on the brass tube.

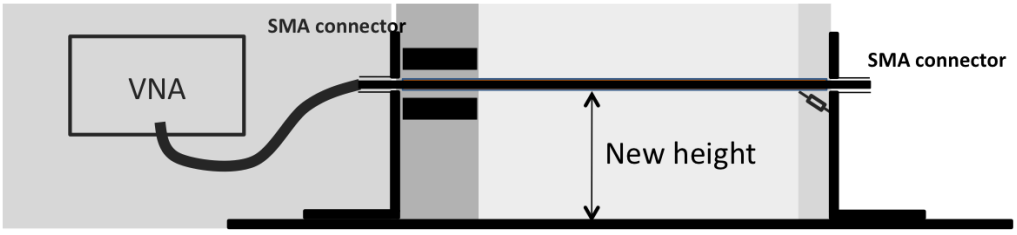


Fig. 2.23 Test setup when the ferrite was close to the brass stand and the height of the brass tube was doubled to simulate placement of the ferrite was placed close to the chassis in a real system.

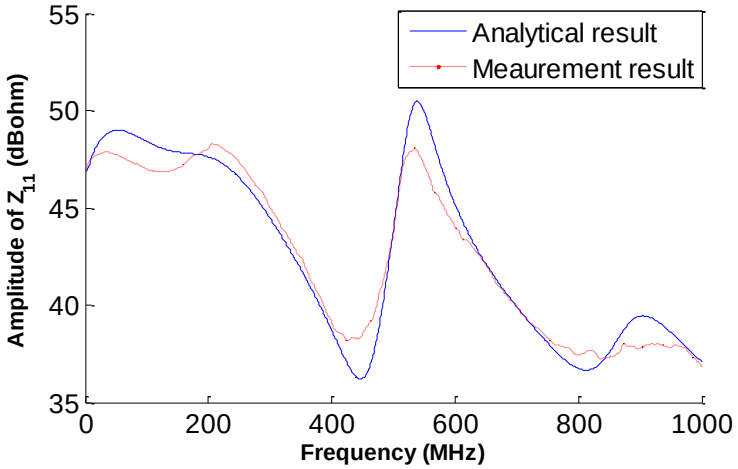


Fig. 2.24 Comparison of analytical and measured input impedance amplitude of the structure with ferrite placed close to the source brass stand at a new height (7.7 cm).

2.5. CONCLUSION

This work developed a novel analytical model on ferrite based on transmission line theory. It provides a robust method to predict the common mode input impedance. It proved better physics indication of the effect of the ferrite. The model can apply ferrite with working frequency range up to 1GHz. This paper also built test structure based on real power system. The test structure is consisting of the brass tube, brass stand and a current return path. Ferrite choke was placed on the brass tube. The brass tube was representing multi-phase power cables. The paper also developed analytical model for the test structure, to which the analytical model for ferrite was implemented. The input impedance of the test structure was calculated by the analytical model, as well as measured through experiment using VNA. The input impedance was calculated and measured with the ferrite being placed in several different locations of the test structure. The analytical result and experiment result were compared and found match very well, which proved the accuracy of the model. To calculate the common mode impedance

behavior of the system with a ferrite choke, characteristic impedance was needed and was calculated using RLGC parameters which can be obtained from the ferrite choke geometry, material properties, and structure information. This model offers more clear physics meaning then the lumped element ferrite model since it applies the Maxwell equation to calculate RLGC parameters and use wave propagation theory to explain the ferrite behavior.

This ferrite analytical model could be used in real power systems and any other conditions have wire over current return plane problems. The input impedance from the common mode source could be calculated by using this ferrite choke model.

Since this model uses the transmission line theory, two conductors were defined (the brass tube and current return path). In reality, the current return path for common-mode current was occasionally difficult to find. In these cases, the model cannot predict the common-mode impedance of the system with ferrite chokes. Normally, however, if there are few structures around the power cable, the current return path should be the ground (current return path). Another limitation of this work lies in common mode current with a higher frequency. Because the fundamental approximation made in this model is that the wave propagation mode was a TEM wave, this approximation fails at high frequency (>1GHz) when the higher mode waves appear. The cut-off frequency of this approximation is difficult to derive and will be studied in future work.

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