Summer 2007

Process development and applications of a dry film photoresist

Phaninder R. Kanikella

Department:

PROCESS DEVELOPMENT AND APPLICATIONS OF A DRY FILM PHOTORESIST

by

PHANINDER REDDY KANIKELLA

A THESIS

Presented to the Faculty of the Graduate School of the

UNIVERSITY OF MISSOURI-ROLLA

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN MATERIALS SCIENCE AND ENGINEERING

2007

Approved by

Matthew J. O'Keefe, Advisor	Chang-Soo Kim

F. Scott Miller

PUBLICATION THESIS OPTION

This thesis has been prepared in the form of two manuscripts for publication. An Introduction section has been included in the thesis to provide background information.

The first manuscript (pages 17-47) is intended for submission in the JOURNAL OF MICROELECTRONIC ENGINEERING.

The second manuscript (pages 48-65) is intended for submission to the IEEE SENSORS JOURNAL

ABSTRACT

In this study, dry film photoresist was patterned using UV lithography and the sidewall profile was optimized to achieve vertical sidewalls. Sidewall verticality of dry film is very important for better pattern transfer. A fractional factorial design (FFD) method was used to identify the significant variables for sidewall optimization. The significant factor was exposure energy. Other factors were not significant in improving sidewall verticality. The sidewall angles ranged from 64 ± 5° to 86 ± 5°. It was found that the sidewall slope increased with a decrease in exposure energy.

The reactive ion etching (RIE) of lithographically patterned dry film is necessary in the fabrication of dry film mask. Dry film RIE with optimized sidewall was carried out using Ar plasma and CF_4–O_2 plasmas. Full Factorial experimental design was used to identify the key factors affecting the process. Oxygen flow rate and RF power were significant variables for dry film RIE using CF_4–O_2 plasmas. Etch rates ranged from ~150 nm/min to ~5000 nm/min. The etch rates increased with an increase in RF power and oxygen flow rate. RF power and time were found to be significant for Ar plasma.

The fabricated dry film molds with nearly vertical sidewalls were used for copper electroplating and Ti lift-off applications. The electroplating process was optimized using fractional factorial design. As expected, current density and plating time were found to be significant. The lower current density resulted in a smoother, fine grained deposit compared to the higher current density. However, the effect of pH value of the plating solution on dry film is yet to be investigated. Dry film molds with increased sidewall slope showed better pattern transfer for copper electroplating and Ti- lift-off.

ACKNOWLEDGMENTS

This thesis would have been impossible without the encouragement and support of many people. I would like to express my gratitude to all of them.

I have been very fortunate to have Dr. Matthew J. O'Keefe as my advisor. I would like to thank him for providing me with an opportunity to work under him. I am extremely grateful to him for his excellent guidance, technical help, motivation, and continued patience throughout this research, through the course of my graduate studies, and during the writing of this thesis.

I would like to express appreciation to my co-advisor, Dr. Chang-Soo Kim, for his financial support and his willingness to share his technical knowledge and expertise. I wish to express my sincere thanks to my committee member, Dr. F. Scott Miller for his valuable discussions and help throughout this study. I extend my gratitude towards Dr. Jay Liu, Dr. Lidia Lee, Dr. Alex Yu and Dr. Anupam Choubey for their support and encouragement during my co-op employment at Vicor Corporation, MA.

I would also like to thank my friends and colleagues who provided me with good assistance, ideas, and valuable suggestions: Dr. Martin Gerardo Perez, Dr. Shaoxin You James N. Reck, Travis McKindra, Jongwon Park, Swetha Kamlapurkar and Phani Krishna.

In addition, a special thanks goes to my parents and sister for their love and understanding throughout my "academic career." Their support and faith in me has always encouraged me and helped me come out stronger for all the hard times so far.

TABLE OF CONTENTS

PAPER II

Process development for Reactive-Ion Etching of Dry Film Photoresist

LIST OF ILLUSTRATIONS

Figure Page

INTRODUCTION

PAPER I

Process development and application of dry film photoresist in MEMS

LIST OF TABLES

1. INTRODUCTION

1.1. PHOTORESIST

Photoresist is a photosensitive material used in the microelectronics industry to form a patterned coating on a substrate surface. The pattern is transferred from a photomask to the wafer using a process called photolithography. In this process, a photoresist is coated on the wafer and exposed to light through a mask. A photochemical reaction occurs in these exposed regions of the resist which is then easily dissolved in a developer solution. The resist pattern depends on the photomask pattern and the polarity of resist. Positive photoresist responds to the light in such a way as to make the exposed regions dissolve more quickly during the development process. In other words, the unexposed regions of the resist will remain unchanged. Negative photoresist responds to light in opposite manner such that the unexposed regions of the resist will dissolve in the developer solution, while the exposed regions remain behind [1].

1.2. TYPES OF PHOTORESISTS

Currently three different types of photoresists are commonly used, namely liquid photoresist, dry film, and SU-8 photoepoxy. Each of these photoresists has its advantages and disadvantages depending on the application.

1.2.1. Liquid Photoresist. Liquid photoresists are the most widely in the microelectronics industry. The resist consists of three components: a resin or base material, a photo active compound, and a solvent that controls the mechanical properties,

such as the viscosity, which is an important parameter for the application of the resist to the wafer. Liquid resists are applied to the wafer through a spin coating technique in which the wafer, along with the resist, is rotated at high speed to form a uniform coating. A typical spin coating process consists of a dispense step in which the resin fluid is deposited onto the substrate surface, a high speed spin step to thin the fluid, and a drying step to eliminate excess solvents from the resulting film (Figure 1). Liquid photoresists are not a permanent part of the structure and are removed once the pattern transfer is complete. Liquid resists were proposed as an alternative to dry film photoresists; the intention being to reduce the material costs in large-volume inner layer production and to automate the in-line manufacture. The liquid resists employed in large-volume inner layer production have essentially proved themselves both technologically and economically, especially when their use has been integrated into a highly automated plant [2]. The inability of liquid resists to cover holes limits its use in certain applications. Therefore, dry film resists are used to bridge and protect vias and through holes [3].

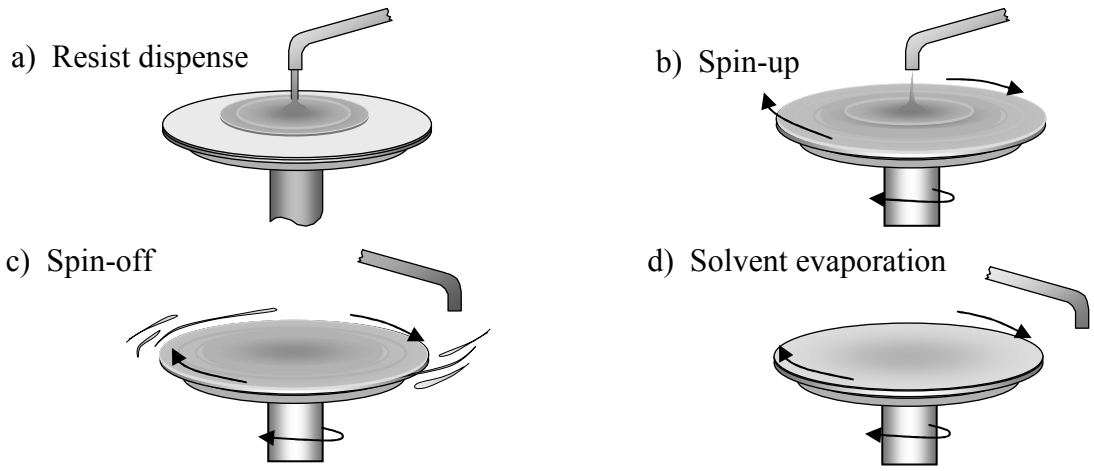
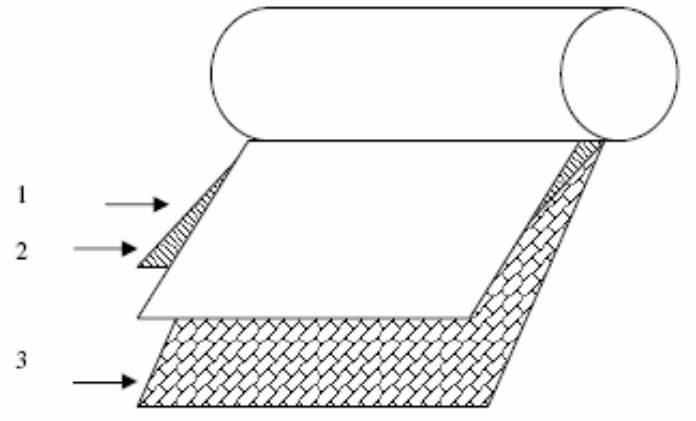
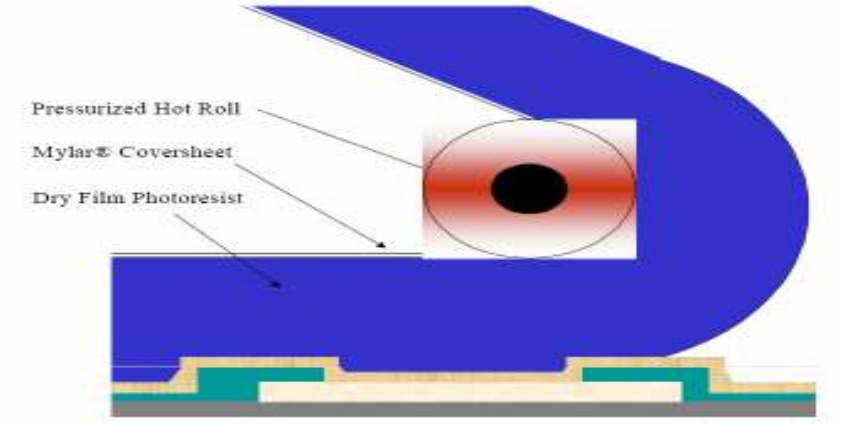


Figure 1: Steps of liquid photoresist spin coating [4].

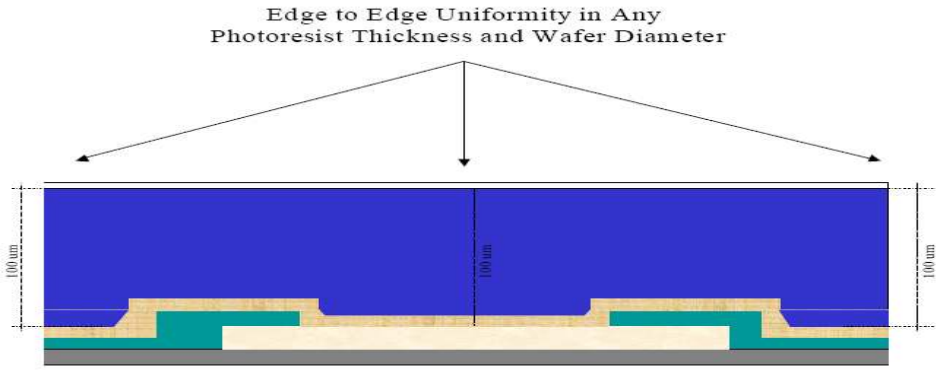
1.2.2. Dry Film Photoresist. Dry film resists (DFRs) were originally developed 30 years ago for printed circuit board (PCB) fabrication. Although application for MEMS (Micro-electro-mechanical systems) fabrication is uncommon, DFRs have been reported to be useful for the fabrication of electroplating molds, for sealing fluidic channels and as a mask for powder blasting of microchannels [5]. Today, DFRs are playing a vital role in the development of MEMS devices. DFRs are typically three-layer structures: a polyester support base membrane; a resist layer, varying in thickness between about 15 and 75 μm depending on the intended application; and on the top of the resist a polyolefin sheet, usually 25 μm thick polyethylene. The dry film is coated as "wide stock," a web about 2 meters in width. The resist is typically coated on the polyester support from a solution, dried, and then covered with a polyethylene foil before winding up the wide stock in rolls of dry film that are several hundred meters long. The polyethylene is needed to prevent the resist from sticking to the polyester of the preceding lap during roll formation. Dry photoresist is applied using dry lamination, where photoresist is evenly rolled across the surface of the wafer with a controlled degree of pressure and temperature (Figure 2). During lamination, the polyethylene is first removed while the resist remains on the polyester support. After lamination and exposure, the polyester has to be peeled off without tearing the resist away from the surface. The hot roll lamination process has the objective of creating smooth and intimate dry contact between the wafer surface and the photopolymer. Adhesion is normally not an issue with dry film photoresist [6].



(a) 1-Polyethylene separation, 2-photoresist and 3-polyester support



(b)



(c)

Figure 2: Dry film photoresist processing. (a) Three-layer structure of dry film photoresist. (b) Dry film lamination on circuitry (c) Edge to edge uniform coverage of dry film [7]

ADVANTAGES OF DRY FILM RESISTS

DFRs offer many advantages over liquid resists, depending on the application. The advantages of dry film include the following:

i. Good conformability

ii. Excellent adhesion on any substrate

iii. No liquid handling because there is no solvent

iv. High process speed

v. Excellent thickness uniformity over a whole wafer

vi. Simple handling

vii. No formation of edge beads

viii. Low exposure energy

ix. Short processing time

x. Near vertical sidewalls

In addition, the set up cost for dry film processing is significantly lower than for liquid resists [8].

1.2.3. SU-8 Epoxy Based Photoresist. SU-8 is a negative, epoxy type, near-UV photoresist that was originally developed and patented by IBM in 1989. Due to its low optical absorption in the UV range, this photoresist can form thick films (40-200 μm). The SU-8 resist contains a few percent of photoacid generator that will produce a strong acid when a photochemical transformation takes place upon absorption of a photon. This photoacid acts as a catalyst in the subsequent crosslinking reaction that takes place during

post exposure bake (PEB), that is, crosslinking occurs only in regions that contains acid catalyst and mainly during PEB [9].

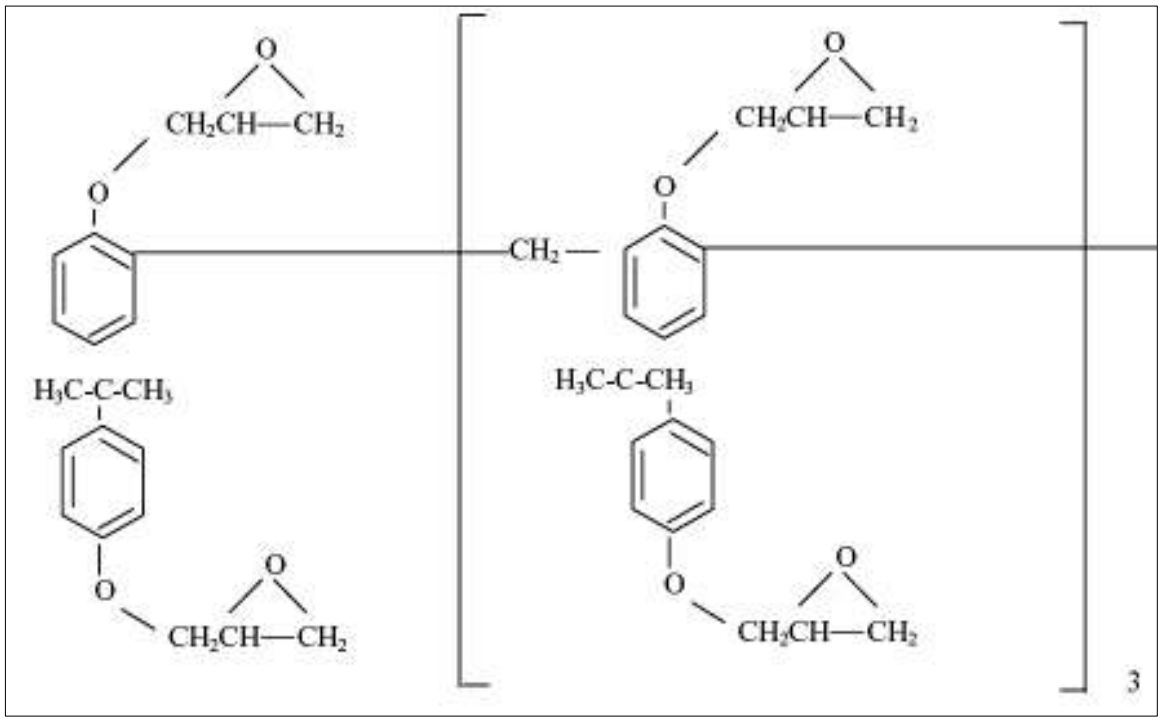


Figure 3: Molecular structure of SU-8 [10]

SU-8 has a high functionality (each SU-8 molecule has eight reactive epoxy groups as shown in Figure 3), which yields good sensitivity, and a low molecular weight, providing high contrast and solubility. These properties, along with a good UV transparency, makes SU-8 a popular choice for fabrication of high aspect ratio structures [11].

Typical SU-8 processing consists of spin coating, exposure, polymerization and development. The SU-8 is spin coated onto a substrate and soft baked in order to evaporate the solvent. In the exposure step the SU-8 film is exposed to near-UV light through a mask. Once initiated by the exposure, the polymerization process is assisted by

thermal energy in the post-exposure bake, or PEB. Finally the unexposed SU-8 is dissolved by organic solvent, leaving only the cross-linked SU-8 structures on the substrate [12]. It has been found that process steps like softbake, exposure, post-exposure bake and development have strong influence in the internal stress of the SU-8 resist structures, resolution and aspect ratio [13].

To date, SU-8 negative photoresist has mainly been used and investigated for various high aspect ratio patterning purposes such as masking for deep RIE etching, electroplating molds, injection molding masters, micro fluidic components and structural parts for micro motors and actuators due to its good mechanical durability, water impermeability, excellent resolution in thick film applications, sensitivity to inexpensive UV sources, high aspect ratio imaging with near vertical sidewalls, and stability as an electroplating mold [14, 15]. However, despite all these advantages, the SU-8 photoresist suffers from three disadvantages, namely adhesion selectivity, stress, and resist stripping.

1. SU-8 adhesion is good on materials such as silicon and gold, but on other materials such as glass, nitrides, oxides and other metals, the adhesion is poor and the resist easily delaminates from such materials surfaces during development.
2. On many surfaces suitable for spinning SU-8, such as silicon or glass, the thermal expansion coefficient mismatch is large (SU-8 has CTE of 52 ppm/K compared to silicon which has CTE of 3 ppm/K). This causes high stress at the material interface due to shrinkage of the resist while crosslinking occurs during curing.
3. As a photoplastic material, SU-8 is chemically stable and resistant to most acids and other solvents. Consequently, it is difficult to remove once crosslinked [16].

1.3. LIQUID PHOTORESISTS VS DRY FILM RESIST

The advantages of liquid resists over dry film are both economic and performance based. Dry film has always been a wasteful process with any resist over hanging the board edges or the space between the boards being non-productive. The resolution of the dry films is limited by the polyester or mylar cover sheet which lies between the phototool and the photoreactive layer. This layer distances the image on the phototool from the resist layer and allows some light scattering, causing spreading of the image and a loss in resolution. In contrast, the liquid resists, with thinner coating capabilities than dry film and direct artwork to resist contact, have better resolution capabilities than the dry films. The UV sensitive constituents of dry film are, by their chemical nature, faster reacting to UV light than those which can be used in liquid resist. The coating related problem with dry films is their inability to successfully fill scratches and imperfections on the substrate surface. This leads to the etchant leaching beneath the resist, causing breaks in fine line patterns. Liquid photoresists, however, are unable to reliably protect plated through holes on double-sided and multilayer boards. Dry resists of the film thickness greater than 38 μm can protect the vias from etching by forming the resist 'tent' over the hole ends, preventing the etchant entry. The major differences between the processes for dry film and liquid resists occur at the next stage in the line-coating. Dry film etch resists are hot laminated onto the substrate, which is fed to the laminator either at ambient temperature or pre-heated (generally 60° - 100°C). Dry film coats both sides of the board concurrently with the resist. Liquid resists require no pre-heating of the laminate before coating which can be carried out using spin coating process that produces

a very uniform thin coat of resist, but the laborious nature of the set up of this process make it unsuitable for volume coating work [17]

1.4. DRY FILM RESIST AS AN ALTERNATIVE TO SU-8 IN MEMS

The possibility of using DFRs for the realization of the key elements of a microfabricated reduction unit was first evaluated by Lorenz et al. in 1995 [18]. Since then, a great amount of research has been done on evaluating dry films for various applications in the production of microfabricated parts. In 2003, Kukharenka et al. [7] evaluated the dry film electroplating process, which opened up new possibilities for low-cost LIGA-type processes for MEMS applications. Recently, SU-8 epoxy-based negative photoresist has been used for many lab-on-a-chip applications. However, this type of photoresist is difficult to process and remove after electroplating. This led to a search for a negative tone resist that can be easily removed after electroplating to realize three dimensional microfabricated parts [18].

1.5. DRY FILM ELECTROPLATING PROCESS

The historic preference for building up the copper deposit by electroplating has to do with lower cost, faster deposition rate, and, in general, better metallurgical properties of electroplated copper. For the first time, Kukharenka et al. evaluated the dry film electroplating process, using nickel sulphamate electrolyte for the realization of 3D parts in MEMS device fabrication [7]. Since then there has been very little information available regarding a dry film copper electroplating process for MEMS fabrication. Figure 4 shows the process map for realizing copper pattern through electroplating on dry film molds. A dry film is laminated and lithographically patterned on the copper seed layer. The patterned dry film molds are electroplated, using a copper sulfate electrolyte. The dry film resist is stripped to realize electroplated three dimensional copper parts.

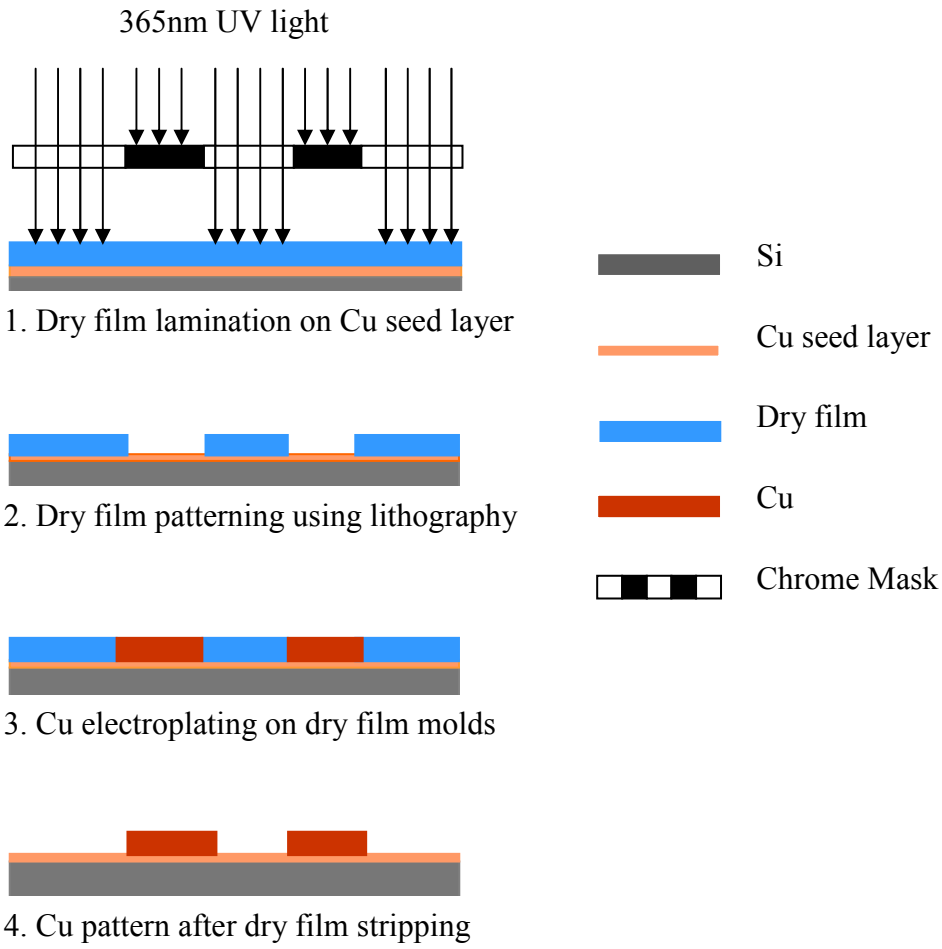


Figure 4: Process map of dry film electroplating process

1.6. DRY FILM LIFT-OFF PROCESS

Metal patterning using a photoresist is one of the key processing technologies in integrated circuit fabrication. For applications which are not easily patterned by conventional lithography and etching techniques, the lift-off method has been widely used as a simple and easy method for patterning materials as films. A pattern is defined on a substrate using photoresist. A film, usually metallic, is blanket-deposited all over the substrate, covering the photoresist and areas in which the photoresist has been cleared. During the actual lift-off, the photoresist under the film is removed with a solvent, taking the film with it, and leaving only the film which was deposited directly on the substrate. Metal lift-off can be performed using positive as well as negative photoresists. Historically, there are three basic ways in which lift-off could be performed: the single-layer method, the multi-layer method, and the surface modified method. The single-layer method, usually using a negative photoresist, is the simplest and involves only one lithography step. The multi-layer method has process complications due to additional polyimide depositions and subsequent etching steps. In the surface-modified method, the top surface of the photoresist is chemically modified by soaking it in chlorobenzene solution so that it will develop at a slower rate than the underlying photoresist [19]. Figure 5 depicts the process for Ti metal lift-off using a negative tone dry film photoresist. The dry film is laminated and lithographically patterned on a SU-8 layer. Titanium metal is then deposited onto the patterned dry film layer. The dry resist is stripped leaving the Ti metal pattern on the SU-8 layer.

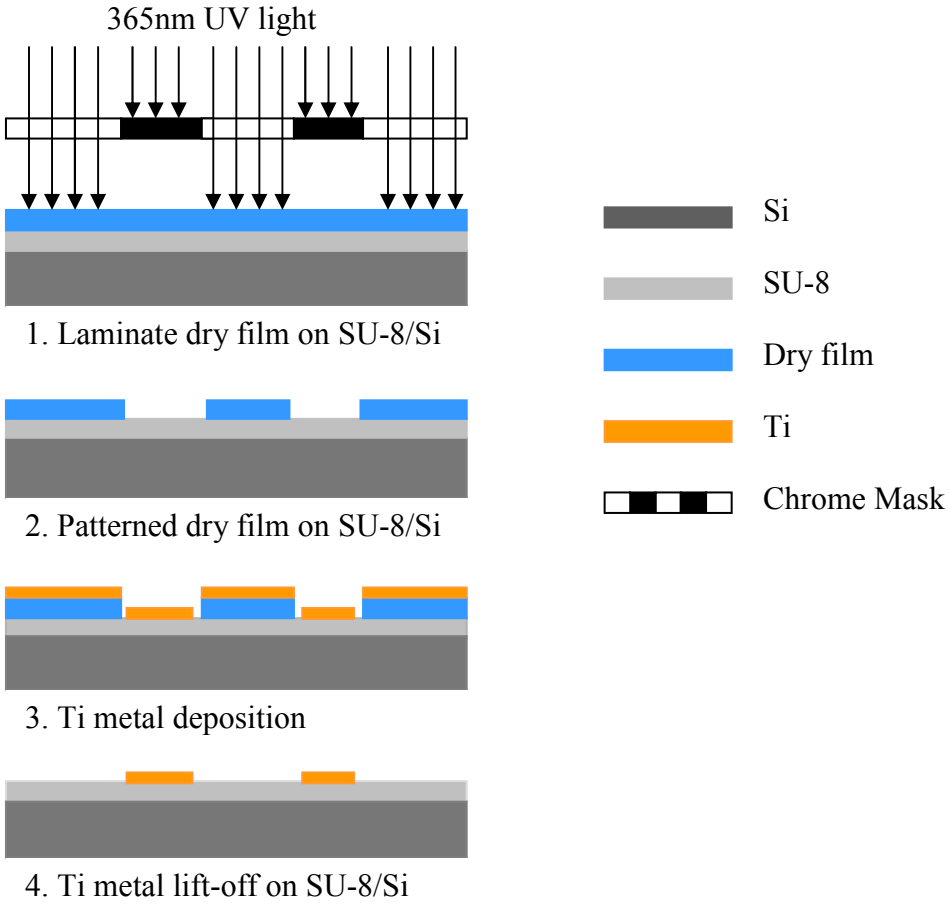


Figure 5: Process map of dry film lift-off process

REFERENCES

[1] Stephen A. Campbell, The Science and Engineering of Microelectronic Fabrication, 2nd Edition, Oxford University Press, New York, 2001.

[2] Klaus Maurischat, "Dry film photoresists–a never ending success story?" *J. Institute of Circuit Technology*, 24 (2), (1998) 34-37.

[3] Wayne M. Moreau, Semiconductor lithography–Principles, Practices and Materials, Plenum Press, New York, 1988.

[4] Michael Quirk and Julian Serda, Chapters 13-15, Semiconductor Manufacturing Technology, Prentice Hall, October 2001.

[5] P. Vulto, N. Glade, L. Altomare, J. Bablet, L. Del Tin, G. Medoro, I. Chartier, N. Manaresi, M. Tartagni and R. Guerrieri, "Dry film resist for fast fluidic prototyping," *8th International Conference on Miniaturized Systems for Chemistry and Life Sciences*, September 26-30, 2004, Malmo, Sweden.

[6] Dr. Karl Dietz, Dry film photoresist processing technology, Electrochemical Publications, British Isles, January 2001.

[7] E. Kukharenka, M. M. Farooqui, L. Grigore, M. Kraft and N. Hollinshead, "Electroplating moulds using dry film thick negative photoresist," *J. Micromech. Microeng,* 13 (2003) S67-S74.

[8] P. Vulto, N. Glade, L. Altomare, J. Bablet, L. Del Tin, G. Medoro, I. Chartier, N. Manaresi, M. Tartagni and R. Guerrieri, "Microfluidic channel fabrication in dry film resist for production and prototyping of hybrid chips," *Lab on a chip*, 5 (2005) 158-162.

[9] J. Liu, B. Cai, J. Zhu, G. Ding, X. Zhao, C. Yang and D. Chen, "Process research of high aspect ratio microstructure using SU-8 resist," *Microsystem Technologies,* 10 (2004) 265-268.

[10] E. Koukharenko, M. Kraft, G.J Ensell, N. Hollinshead, "A comparative study of different thick photoresists for MEMS applications," *J. Material Science: Materials in Electronics*, 16 (2005) 741-747.

[11] Thomas A. Anhoj, Anders M. Jorgensen, Dan A. Zauner and Jorg Hubner, "Optimization of SU-8 processing for integrated optics," *Micromachining Technology for Micro-Optics and Nano-Optics IV, Proc. Of SPIE,* 6110 (2006) 611009.

[12] Thomas A. Anhoj, Anders M. Jorgensen, Dan A. Zauner and Jorg Hubner, "The effect of soft bake temperature on the polymerization of SU-8 photoresist," *J. Micromech. Microeng,* 16 (2003) 1819-1824.

[13] K. D. Vora, A. S. Holland, M. K. Ghantasala and A. Mitchell, "Patterning of SU-8 resist structures using CF_4," *Device and Process Technologies for MEMS, Microelectronics, and Photonics III, Proc. Of SPIE,* 5276 (2004) 162-172.

[14] V. Seidemann, J. Rabe, M. Feldmann and S. Buttgenbach, "SU8–micromechanical structures with in situ fabricated movable parts," *Microsystem Technologies,* 8 (2002) 348-350.

[15] Martin G. Perez, Matthew J. O'Keefe, Phaninder Kanikella, James Reck and Chang-Soo Kim, "Reactive ion etching of SU-8 photoresist using CF_4-O_2 plasmas," *Manuscript submitted to J. Microelec. Eng.* (2007).

[16] Ewan H. Conradie and David F Moore, "SU-8 thick photoresist processing as a functional material for MEMS applications," *J. Micromech. Microeng,* 12 (2002) 368-374.

[17] Primary Imaging Resists–Technical Publication, Coates Circuit Products, Norton Hill, Midsomer Norton, UK.

[18] Hubert Lorenz, Lionel Paratte, Roland Luthier, Nicholaas F. de Rooij, Philippe Renaud, "Low-cost technology for multilayer electroplated parts using laminated dry film resist," *Sensors and Actuators A*, 53 (1996) 364-368.

[19] Hyung Suk Lee and Jun-Boo Yoon, "A simple and effective lift-off with positive photoresist," *J. Micromech. Microeng.* 15 (2005) 2136-2140.

Process development and application of dry film photoresist in MEMS

Phaninder Kanikella[1], Matthew J. O'Keefe[1], Chang-Soo Kim[2]

[1]*Graduate Center for Materials Research, University of Missouri-Rolla, MO 65409 USA*

[2]*Electrical & Computer Engineering, University of Missouri-Rolla, MO 65409 USA*

Abstract

A dry film photoresist (MX 5000 series) commercially available from DuPont Electronic Technologies was selected to fabricate high aspect ratio microstructures using UV lithography and the sidewall verticality was optimized in order to achieve near vertical dry film sidewalls during the process. The lithographically patterned dry film molds with optimized sidewall profile were electroplated with copper and used for sputtered metal lift-off. A fractional factorial design (FFD) was selected to optimize the processing parameters during sidewall angle improvement and copper electroplating. The significant factor in the sidewall optimization was exposure energy and the sidewall angles ranged from 64° to 86°. The results show that with an increase in current density and plating time, the thickness of the deposit increased drastically, as would be expected. Sputtered Ti films of thicknesses ranging from 50 to 500 nm were deposited onto dry film molds to test the dry film lift-off process. A titanium film with a thickness of 200 nm was successfully lifted-off using dry film.

Keywords: Dry film resist, SU-8 photoepoxy, Aspect ratio, Sidewall, Lithography, FFD, Lift-off, MEMS.

1. Introduction

Dry film photoresists (DFRs) were invented almost 30 years ago. Since that time, DFRs have been widely used in the production of printed circuit boards (PCBs) [1]. The application of dry films in micro electromechanical systems technology has been widely reported and is restricted to the fabrication of electroplating molds and masks for powderblasting of microstructures [2]. In the future, dry films are expected to be used in the fabrication and integration of microsystems with a high resolution. However, not enough information exists to address issues such as the limitation of lateral resolution or sidewall verticality when dry films are used in MEMS, and the problems to be encountered are mostly unknown.

MEMS have gained significant importance in recent years. The design of micromachined devices is often limited by the impossibility of layer patterning by resist spinning on a wafer surface containing large steps in height. The standard resist spinning method needs a flat surface for coverage with a uniform layer thickness [3]. A dry film photoresist is used to facilitate flat surfaces. A DFR has numerous advantages such as good conformability, excellent adhesion on any substrate, no liquid handling because there is no solvent, high process speed, excellent thickness uniformity over a hole wafer, simple handling, no formation of edge beads, low exposure energy, low cost, short processing time and near vertical sidewalls [4]. Since the DFR fabrication does not necessarily require a clean-room environment, the technique is extremely suitable for low-cost prototyping. In addition, good compatibility with standard lithography processes and a minimal number of process steps make this technique suitable for industrial applications as well [5]

Previous studies [6] have reported the use of commercially available dry film photoresists, such as Riston®, Ordyl BF 410, Etertec® 5600, DF 4615, DFR-15, and Ordyl P-50100. Riston® was successfully used by Lorenz *et al* [4] for the fabrication of one or multilevel, high-slope and high-thickness electroplated microstructure. Recently, Ordyl P-50100 was used by Kukharenka *et al* [6] to realize a 3D micro-disc by electroplating nickel into a mold of dry film photoresist. This paper reports on process development and applications of a dry film photoresist. For this purpose, an MX 5020 dry film resist from DuPont Electronic Technologies, USA was used. This type of film is a solid negative tone photopolymer sheet available in a three-ply composite format. The photopolymer emulsion, ranging from 10 to 100 μm, is protected by two other layers. The top layer is an extra clear polyester film with a thickness of 18.5 μm. The bottom layer, or base, is a low-density polyethylene film [7].

2. Experimental

2.1. Standard dry film processing

A standard 4-inch (100 mm) single-side polished Si wafer was cleaned for three minutes in acetone followed by 30 seconds air dry, three minutes in ethanol followed by 30 seconds air dry, and three minutes in a DI water rinse followed by 90 seconds spin dry as per the standard lab procedure. The wafer was subjected to a dehydration bake at 200°C for five minutes. After the cleaning step, the wafer surface was free from dust particles and other contaminants. In the case of copper electroplating, a Cu seed layer was sputtered on silicon substrate at 300 W power and 3 mTorr argon pressure using Denton Discovery® 18 sputter system. The thickness of the Cu seed layer was measured using an

alpha-step Tencor® profilometer. The average thickness of the sputtered copper seed layer was measured to be 55 nm. The wafer was then heated to 100°C on a hot plate. The dry film resist polyolefin sheet was first removed; the film was then brought in contact with the wafer, with the resist facing the polished surface. A 4-inch wide soft rubber roller was used manually to laminate the dry film. Conformation was achieved by heating the wafer under pressure. The wafer was subjected to a post-lamination bake at 100°C for 15 minutes to enhance film adhesion on extra smooth surfaces and for aggressive applications. The processed wafer was exposed to UV light using a Karl-Suss MA/BA-6 mask aligner. A chromium mask with 250 μm wide columns was used to form patterns on dry film. The wafer was exposed at 60 mJ/cm^2 for 60 seconds depending on the intensity of the UV bulb. The post-exposure bake was done at 90°C for 30 minutes to enhance the photoresist resolution and development latitude leading to a clean surface after development and very straight photoresist sidewalls. The polyester cover sheet was removed before development. The wafer was placed on the vacuum chuck of a CEE® 100 model spin coater from Brewer Science Inc. D4000 IC developer concentrate was used for developing the resist. The wafer was spin developed manually for three minutes followed by DI water rinse for two minutes at 1000 rpm and then dipped in D4000 IC developer concentrate for two minutes followed by rinsing in DI water for two minutes. A combination of spin development and immersion development was used to achieve excellent sidewall profiles in the dry film. The wafer was further spin dried at 3000 rpm for 45 seconds. The post development bake was done at 90°C for 20 minutes to enhance polymer film resolution and processing latitude, thus leading to straighter film sidewalls and higher resistance to aggressive chemistries. The sidewall angle was measured using a

Nikon optical microscope and ImageJ software. The dry film molds thus formed were used for copper electroplating and 200 nm thick Ti metal lift-off. The dry film was stripped using a Dynaloy PR 7200 photoresist stripper to obtain 3D microstructures.

A Fractional Factorial Design (FFD) was applied to identify and optimize the critical processing conditions for the sidewall verticality and electroplating copper onto laminated dry film molds with near vertical sidewalls. In this study, MINITAB statistical software was used to design and analyze the fractional factorial experiments. An Analysis of Variance (ANOVA) determined the statistical significance of each factor and the interaction between the different factors at 90% confidence level ($\alpha = 0.10$). Results were considered statistically significant if the P-value < α [7]. The factors that were considered for FFD experiment to improve sidewall angle were exposure energy, post exposure bake temperature (PEB_{Temp}), post exposure bake time (PEB_{Time}), develop time (D_{Time}), post development bake temperature (PDB_{Temp}), and post development bake time (PDB_{Time}). Three factors, namely current density (CD), plating time, and temperature were selected as factors for copper electroplating process.

2.2. Electroplating Setup

A standard copper sulfate solution (36 g/L Cu, 150 g/L H_2SO_4) was used as an electrolyte. The electroplating cell consisted of a glass beaker, $CuSO_4$ electrolyte, a copper anode, and a patterned wafer cathode. A Keithley® current source was used for the DC supply ranging from 100 nA to 100 mA. A hot plate with a magnetic stirring facility was used for uniform process control. High purity silver paint and epoxy were used to make electrical connections to both the anode and cathode. The temperature of the bath ranged from 40°C to 60°C. The current density varied from 30 mA/cm^2 to 70

mA/cm^2, and the plating time ranged from 25 to 40 minutes. Each factor was set at two levels, low (-) and high (+), in such a way that they covered the usual operating range to obtain significant plating uniformity.

3. Results and discussion

3.1. Sidewall Angle Optimization

The factors and levels for the fractional factorial design in sidewall optimization are presented in Table 1. The high and low levels were selected based on the manufacturer's initial process parameters. The sidewall angles measured for different processing conditions of the dry film resist with the design matrix in the 2_{IV}^{6-2} FFD experiment is shown in Table 2. Figure 1 shows the normal probability plot of the standardized effects from this experiment. All of the effects that lie close to the line are negligible, whereas the significant effects lie away from the line [8]. The important effect that emerges from this analysis is exposure energy. However, according to the sparsity of effects principle, where there are several variables, a process is likely to be driven by some of the main effects and interactions. Since the three-factor and higher interactions don't appear to be significant, it was concluded that exposure energy was the most important effect. Also, the P-value is much less than 0.10 (α = 90% confidence level), indicating that exposure energy is a significant effect.

The effect of exposure energy on the sidewall angle is shown in Figure 2. It shows a sharp decrease from 86° to 64° with increasing exposure energy. This is also supported by the P-values in which exposure energy factor is the most important variable affecting the sidewall angle. However, there are several other factors which slightly affect the

sidewall angle, such as post exposure bake temperature (PEB_{Temp}), develop time (D_{Time}), post development bake temperature (PDB_{Temp}), and post development bake time (PDB_{Time}). As expected, the sidewall angle increases with an increase in PEB_{Temp}, D_{Time} and PDB_{Time}. There is a need to address correlation between PDB_{Temp} and sidewall angle since the result is quiet contradictory to the manufacturer's initial process recipe which states that an increase in PDB_{Temp} leads to straighter film sidewalls [9]. Figure 2 shows that the sidewall angle remains virtually the same with a change in post exposure bake time (PEB_{Time}). Figure 3 presents a residual plot for the sidewall angle. The residuals from the experiment were examined to determine if the data collected met the criteria for analysis used. The results showed that the residuals were structureless, normally distributed with no major outliers. The normal probability plot indicates that the plot is a slightly skewed from the line.

Figure 4 presents the results of interactions among all the process variables. Any plot with a positive slope indicates a higher sidewall angle, while a negative slope is a lower sidewall angle. The intersection quadrant between two labels represents the interaction between two factors (i.e. the PDB_{Time}–exposure energy interaction is the upper right-hand quadrant, while the upper left-hand quadrant is the PEB_{Temp}–exposure energy interaction). The first row indicated that the sidewall angle was typically larger at low level exposure energy, with an increase in all the other variables, and vice versa at high level exposure energy. The ANOVA results indicated that all the interactions were significant and required an in-depth explanation.

Figure 5 shows the sidewall images of dry film at various processing conditions. The near vertical sidewall at 86° was obtained at 60 mJ/cm^2, while the 64° sidewall

obtained at 90 mJ/cm^2. This can be explained by the higher exposure energy resulting in a narrower microchannel width and more sloped sidewall (i.e. lower sidewall angle). The presence of a polyester layer between the chrome mask and the top of the dry film leads to UV light refraction causing the increased path length and change of light propagation direction. Refraction shifts the UV light away from the dark field. Also, the reflection at the substrate surface and diffraction at the edge of dark field lines of the mask makes significant difference in the channel widths and taper angle [10]. Thus, the dependence of sidewall profile on the exposure could be due to the diffraction of incident UV light at the edge of the dark field lines of the mask, refraction of light at the polyester layer/dry film interface, and the reflection from the silicon wafer surface. It was difficult to focus optical images of the sidewalls because the dry film peeled off from the silicon surface during cleavage and cross sectioning of samples.

3.2. Optimized Copper Electroplating Process

The thickness of electroplated copper deposit was measured for various levels of processing conditions with the design matrix in the 2_{III}^{3} FFD experiment (two replicates) is shown in Table 3. The deposition rates ranged from ~ 390 nm/min to ~ 1250 nm/min as shown in Table 4. Figure 6 shows the normal probability plot of the standardized effects from this experiment. The effects of current density and plating time were significant, with low P-values. The temperature of the electroplating bath was shown to not be significant during process evaluation as it lies close to line.

The effect of current density and plating time on the thickness of the deposit is shown in Figure 7. As expected, it shows a sharp increase with increasing current density

and plating time. This is also supported by P-values in Table 4 in which current density and plating time factors are important variables affecting the deposit thickness. However, the surface morphology of the deposit varies greatly with the changes in temperature.

Figure 8 presents the results of interactions among all the process variables. As expected, for higher current density, the thickness of the deposit increases with increasing plating time and temperature. However, for the lower current density the results indicated a decrease in thickness with increasing temperature. It is not clear why thicker deposits are formed at lower temperatures, but may be related to a shift in deposition mechanisms at the substrate interface.

Figure 9 presents the residual plot for the deposit thickness. The residuals from the experiment were examined to determine if the data collected met the criteria for analysis used. The results showed that the residuals were structureless, normally distributed with no major outliers. The residuals versus fitted values plot do not show a curve, which means the constant variances assumption is valid. Therefore, the plot is satisfactory.

3.3. Microstructural Analysis

The microstructures of the electroplated deposits for various processing conditions were examined using optical microscope and SEM. The optical images of the lithographically patterned dry film before and after electroplating are shown in Figure 10. A reasonably sharp Cu pattern and no delamination were observed after electroplating. However, dry film discoloration was found after electroplating. This may be due to the chemical effect (pH) of plating solution on dry film. Figure 11 depicts a copper deposit

obtained with a 86° sidewall angle of dry resist. The deposit edges look well defined at the center of the pattern. However, at the pattern edges, outside the plated area, residual copper has been identified. This can be attributed to a distorted dry film pattern before electroplating. Some areas near the edges were uncovered during electroplating which lead to the formation of copper outside the intended pattern after the dry film has been stripped. Figure 11 shows a near vertical sidewall copper deposit with some copper. This implies that the copper deposit has a vertical sidewall after the dry film has been stripped.

Figure 12 presents the variation in surface morphology of the deposit with increasing current density. The surface looks smoother with a few cracks at the lower current density and plating time. As expected, the surface was rougher and faceted at higher levels of current density and plating time. Figure 13 shows the variation in surface morphology with decreasing current density. The lower current density resulted in a smoother, fine grained deposit compared to the higher current density.

3.4. Dry Film Lift-off Process

Dry film was investigated as a lift-off material for metal deposition using different sidewall profiles. Figure 14 shows images of the dry film lift-off results using the 86° and 64° sidewall angles obtained during sidewall optimization experiments. The titanium lift-off using a 86° dry film sidewall had clear, straight edges (Fig. 14(a)). Figure 14 (b) presents titanium lift-off using a 64° dry film sidewall angle in which the edges are unclear and jagged after lift-off. This result indicated that at lower sidewall angles the edges of the pattern were fully covered with the thin film metal layer, making it difficult to remove during stripping and creating the uneven edges. A confirmation lift-off

experiment was run with SU-8 as a substrate material instead of silicon. Figure 14 (c) shows a clear titanium lift-off on SU-8 resist using a dry film with 86° sidewall angle and 200 nm thick Ti layer.

4. Conclusion

Using fractional factorial design, the effect of six factors, exposure energy, post-exposure temperature, post-exposure bake time, develop time, post-development bake temperature, and post-development bake time on the sidewall angle of dry film photoresist was studied. The sidewall angle is predominantly determined by exposure energy. The sidewall angles ranged from 64° to 86°, increasing the slope with a decrease in exposure energy. Dry film resist was successfully used to pattern molds using UV-lithography and electroplated with copper. The effect of current density, plating time, and temperature were studied using fractional factorial design and it was found that current density and plating time were significant to control the process. It was also demonstrated that the process could be used for lift-off of sputter metal, with a well defined patterned transfer for 200 nm thick Ti films obtained for 86° sidewalls.

Acknowledgments

We wish to acknowledge Dr. Martin G. Perez and Clarissa Wisner of University of Missouri-Rolla for providing technical support in designing the experiments and SEM imaging. The authors would also like to thank Dr. Thomas O'Keefe, and Jongwon Park of the University of Missouri-Rolla, and Pedro Goncalo C. T. Jorge of DuPont Electronic Technologies, USA for their valuable suggestions

References

[1] Klaus Maurischat, "Dry film photoresists–a never ending success story?" *J. Institute of Circuit Technology*, 24 (2), (1998) 34-37.

[2] P. Vulto, N. Glade, L. Altomare, J. Bablet, L. Del Tin, G. Medoro, I. Chartier, N. Manaresi, M. Tartagni and R. Guerrieri, "Microfluidic channel fabrication in dry film resist for production and prototyping of hybrid chips," *Lab on a chip*, 5 (2005) 158-162.

[3] V.L. Spiering, J. W. Berenschot and M. Elwenspoek, "Planarization and fabrication of bridges across deep groves or holes in silicon using a dry film photoresist followed by an etch back," *J. Micromech. Microeng,* 5 (1995) 189-192.

[4] Hubert Lorenz, Lionel Paratte, Roland Luthier, Nicholaas F. de Rooij, Philippe Renaud, "Low-cost technology for multilayer electroplated parts using laminated dry film resist," *Sensors and Actuators A*, 53 (1996) 364-368.

[5] P. Vulto, N. Glade, L. Altomare, J. Bablet, L. Del Tin, G. Medoro, I. Chartier, N. Manaresi, M. Tartagni and R. Guerrieri, "Dry film resist for fast fluidic prototyping," *8th International Conference on Miniaturized Systems for Chemistry and Life Sciences*, September 26-30, 2004, Malmo, Sweden

[6] E. Kukharenka, M. M. Farooqui, L. Grigore, M. Kraft and N. Hollinshead, "Electroplating moulds using dry film thick negative photoresist," *J. Micromech. Microeng,* 13 (2003) S67-S74.

[7] Minitab, Inc. *Minitab 14 Users Manual* from the Help menu, "Analyzing Full Factorial Design with Replicates and Blocks," State College, PA, 2004.

[8] D.C. Montgomery, Design and analysis of experiments, 5th edn, 2000.

[9] Microlithographic Polymer Film DuPont™ MX5000™ Series Data Sheet & Processing Information (www2.dupont.com/APL/en_US/products/mx/index.html).

[10] Jun Zhang, Mary B. Chan-Park and R. Conner, "Effect of exposure dose on the replication fidelity and profile of very high aspect ratio microchannels in SU-8," *Lab on a chip,* 4 (2004) 646-653.

Table 1: Factors and levels for 2_{IV}^{6-2} FFD experiment in sidewall optimization.

Factor	Level	
	Low (-)	High (+)
A=Exposure energy (mJ/cm^2)	60	90
B=PEB temp (°C)	90	110
C=PEB time (min)	20	30
D=Develop Time (spin + dip) sec	230	300
E=PDB temp (°C)	90	110
F=PDB time (min)	20	30

Table 2: Sidewall angles measured for 2_{IV}^{6-2} FFD experiment

Run order	Exposure Energy (mJ/cm^2)	PEB temp (°C)	PEB time (min)	Development time (sec)	PDB temp (°C)	PDB time (min)	Avg. Sidewall angle (X°) (100 samples)
1	60	110	30	230	90	30	84 ± 3
2	90	110	20	300	90	20	81 ± 2
3	90	110	30	300	110	30	81 ± 1
4	60	110	20	230	110	20	80 ± 1
5	90	90	20	230	90	30	75 ± 1
6	60	90	20	300	110	30	77 ± 7
7	90	90	30	230	110	20	74 ± 2
8	60	90	30	300	90	20	86 ± 1
9	90	90	30	230	110	20	64 ± 5
10	90	110	20	300	90	20	68 ± 2
11	90	90	20	230	90	30	83 ± 2
12	90	110	30	300	110	30	82 ± 3
13	60	110	20	230	110	20	81 ± 2
14	60	90	20	300	110	30	84 ± 2
15	60	90	30	300	90	20	80 ± 1
16	60	110	30	230	90	30	79 ± 5

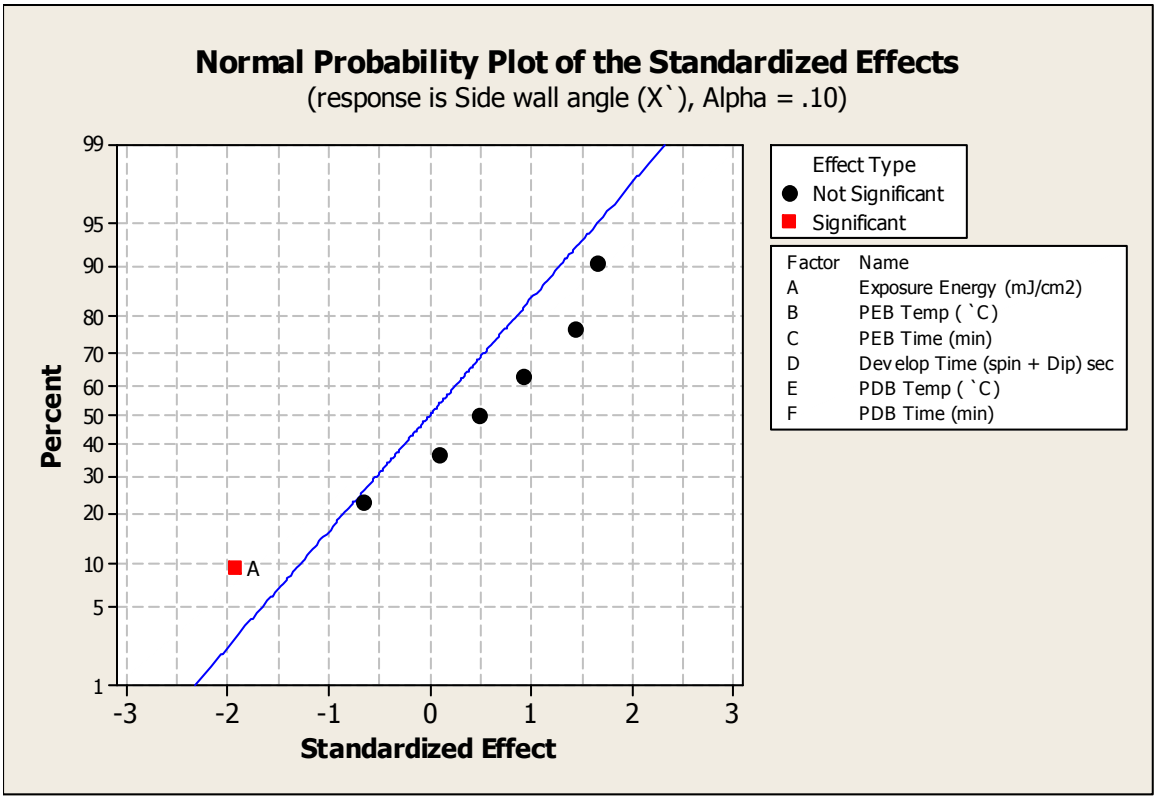


Figure 1: Normal probability plot of standardized effects for sidewall optimization.

(A= exposure energy)

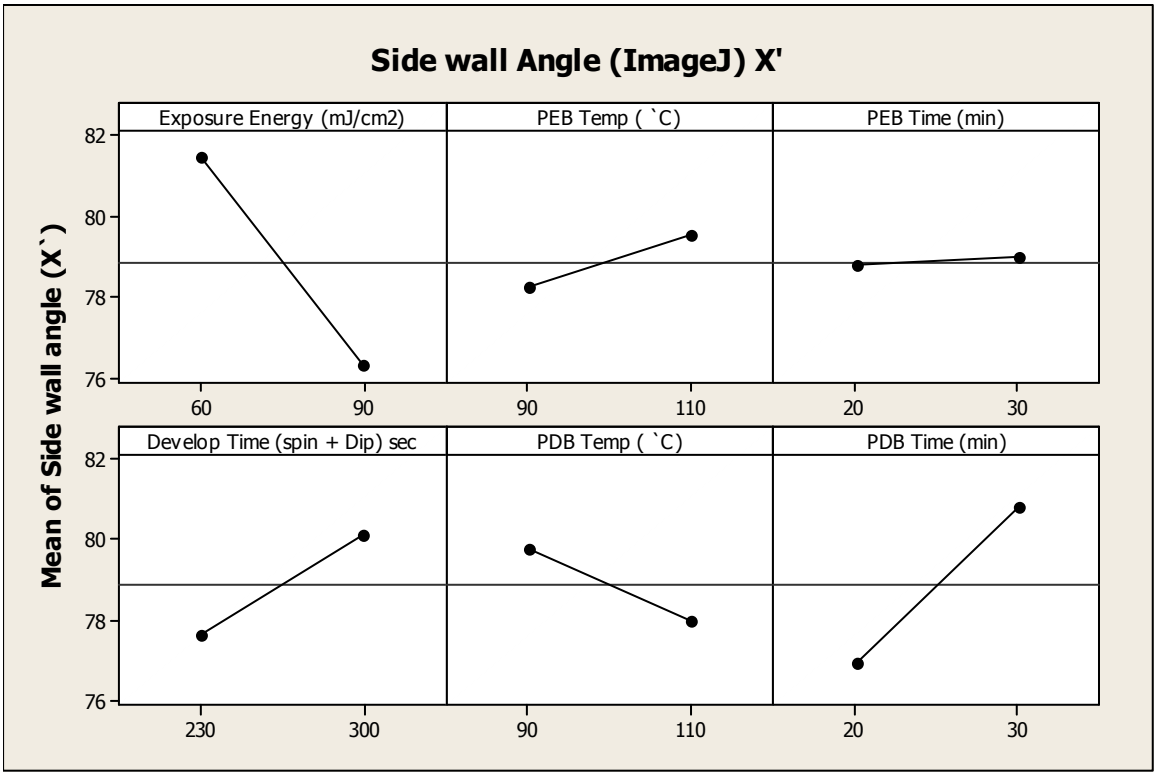


Figure 2: Main effects plot for sidewall angle optimization. The y-axis represents sidewall angle

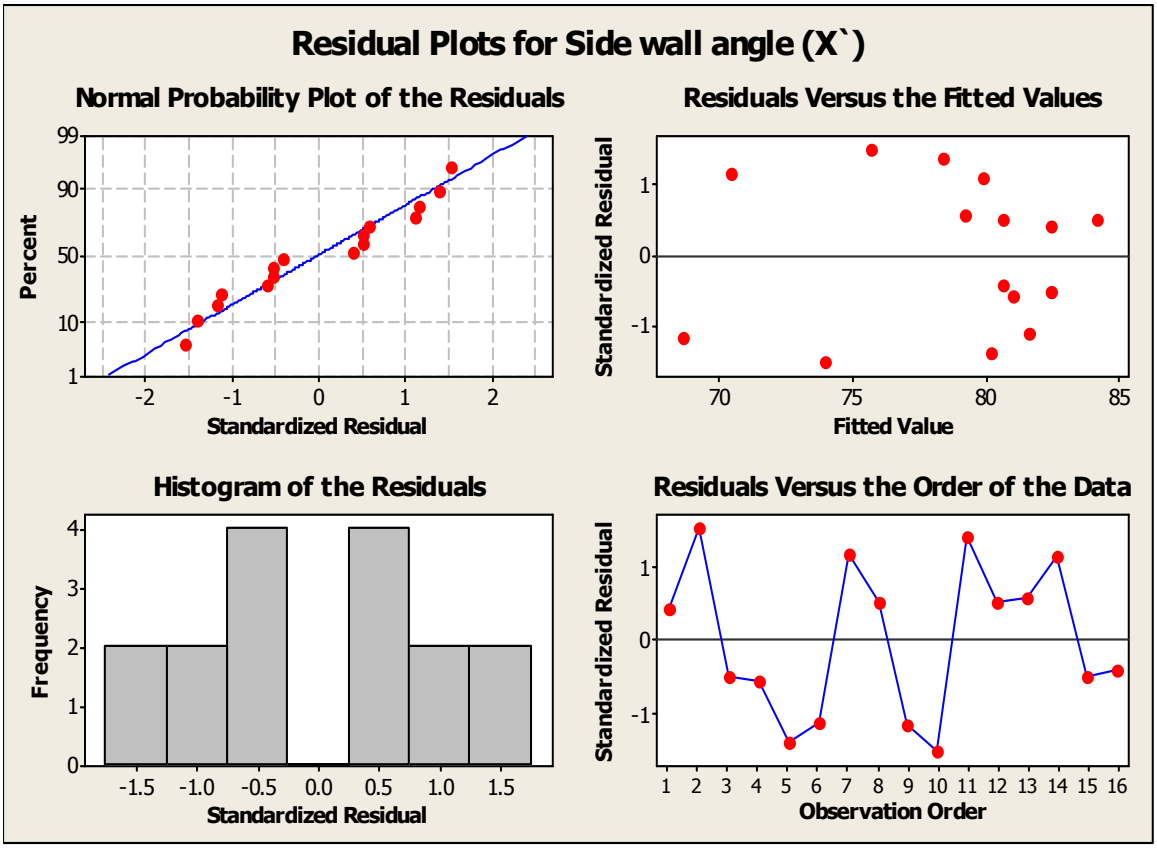


Figure 3: Residual plots for sidewall angle measurements

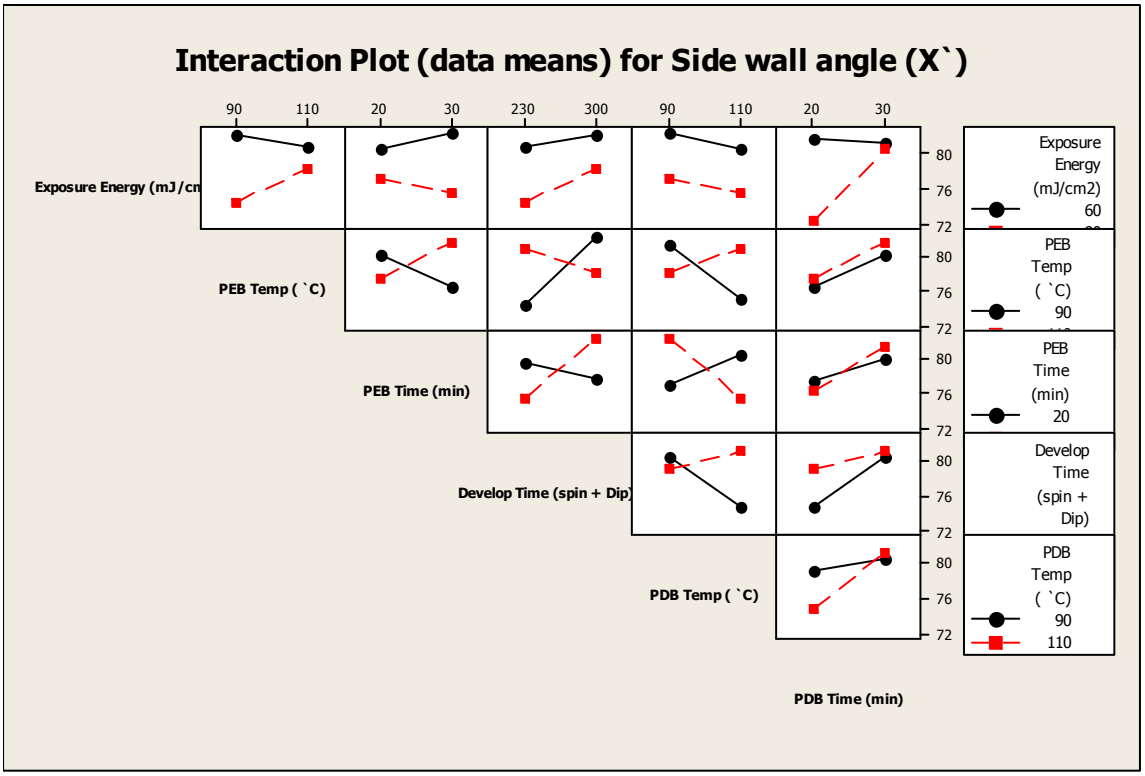
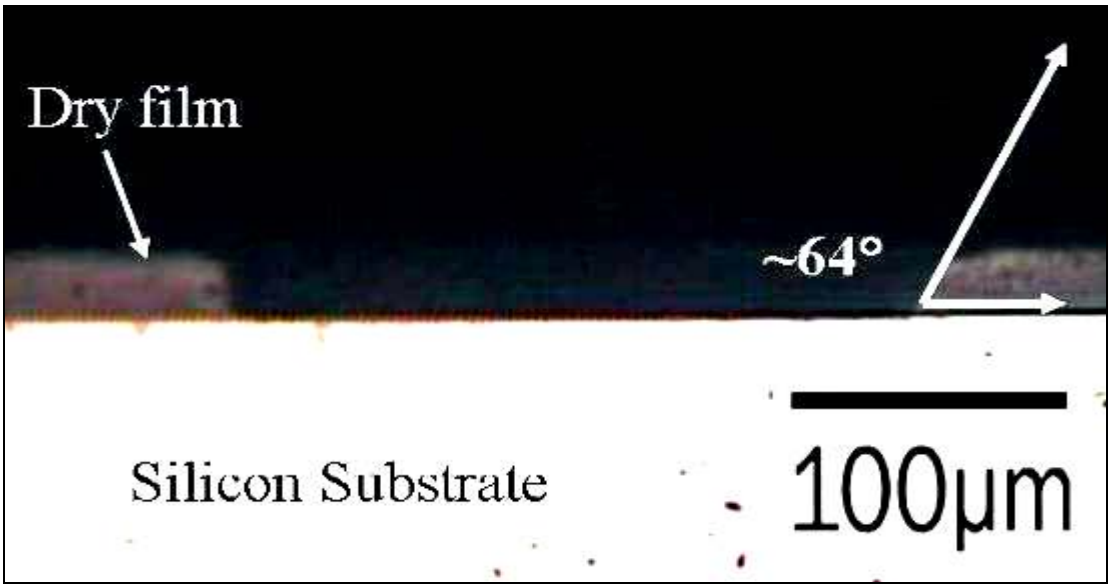
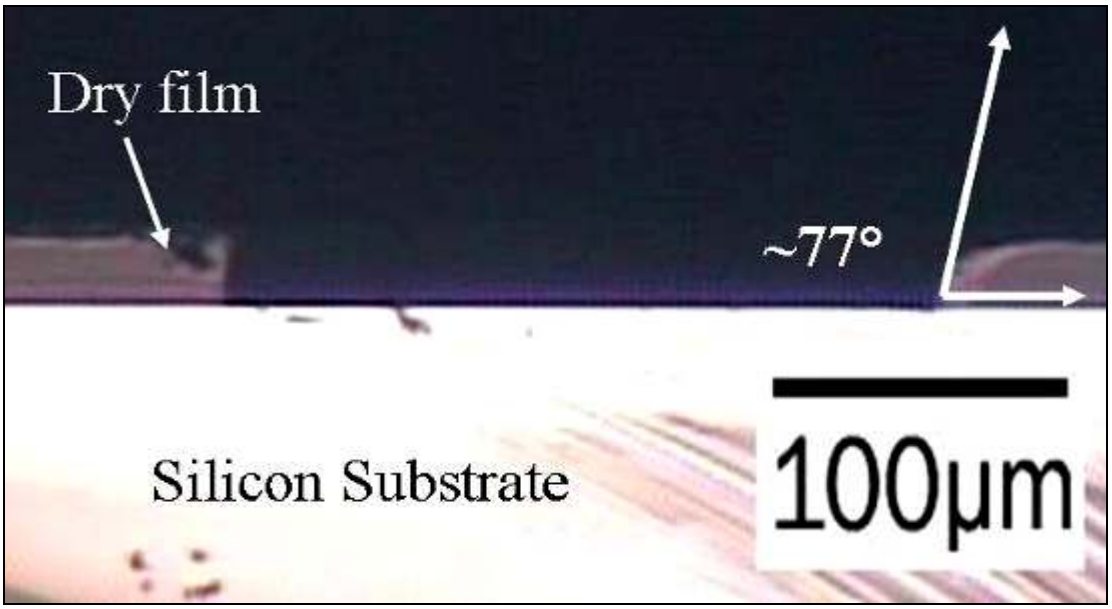


Figure 4: Interaction plot of for sidewall angle optimization

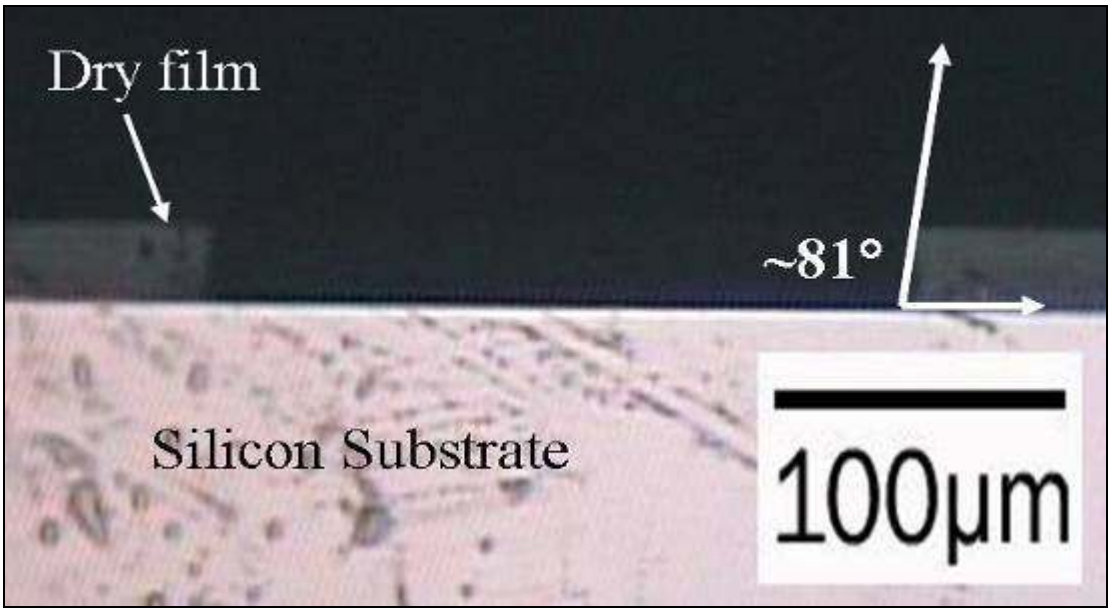


(a) Optical image of 64° sidewall (RIE conditions: 90 mJ/cm^2, 90°C PEB_{Temp}, 30 min PEB_{Time}, 230 sec D_{Time}, 110°C PDB_{Temp}, 20 min PDB_{Time}).

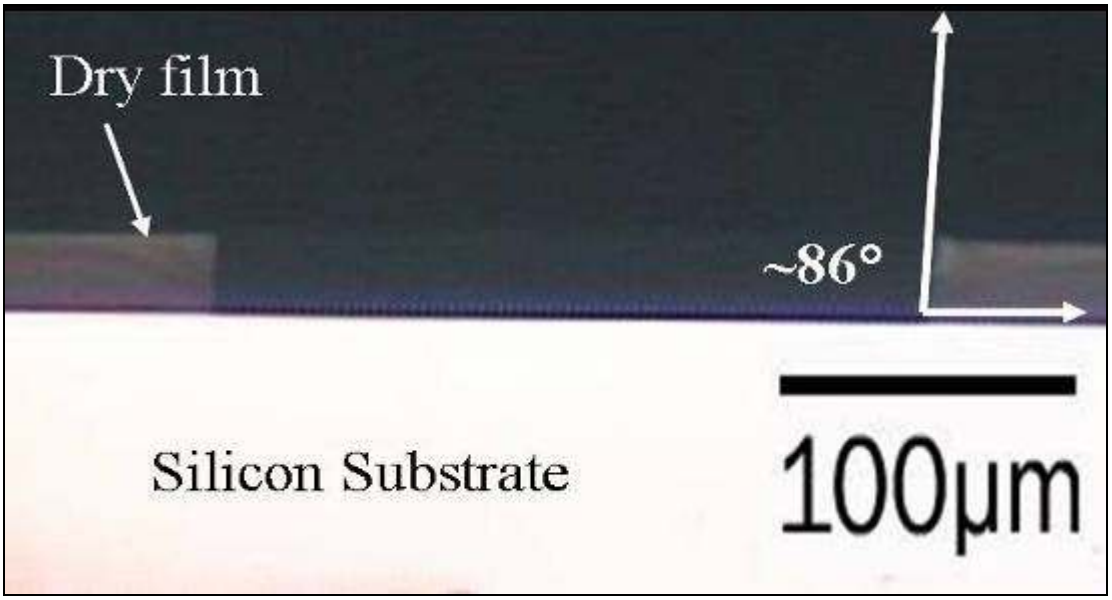


(b) Optical image of 77° sidewall (RIE conditions: 60 mJ/cm^2, 90°C PEB_{Temp}, 20 min PEB_{Time}, 300 sec D_{Time}, 110°C PDB_{Temp}, 30 min PDB_{Time}).

Figure 5: Optical images of sidewalls for 2_{IV}^{6-2} FFD experiment



(c) Optical image of 81° sidewall (RIE conditions: 90 mJ/cm^2, 110°C PEB_{Temp}, 20 min PEB_{Time}, 300 sec D_{Time}, 90°C PDB_{Temp}, 20 min PDB_{Time}).



(d) Optical image of 86° sidewall (RIE conditions: 60 mJ/cm^2, 90°C PEB_{Temp}, 30 min PEB_{Time}, 300 sec D_{Time}, 90°C PDB_{Temp}, 20 min PDB_{Time}).

Figure 5: (Continued) Optical images of sidewalls for 2_{IV}^{6-2} FFD experiment

Table 3: Factors and levels for 2_{III}^{3} FFD experiment in copper electroplating process optimization.

Factor	Level	
	Low (-)	High (+)
A=Current density (mA/cm^2)	30	70
B=Plating time (min)	25	40
C=bath temperature (°C)	40	60

Table 4: Thickness of copper deposit measured for 2_{III}^{3} FFD experiment

Run Order	Current Density (mA/cm^2)	Plating Time (min)	Temperature (°C)	Thickness (nm)
1	30	40	40	15,600 ± 300
2	30	25	60	13,600 ± 400
3	30	40	40	36,700 ± 800
4	70	40	60	37,100 ± 300
5	70	25	40	25,300 ± 700
6	70	40	60	49,800 ± 1400
7	70	25	40	29,300 ± 900
8	30	25	60	16,700 ± 200

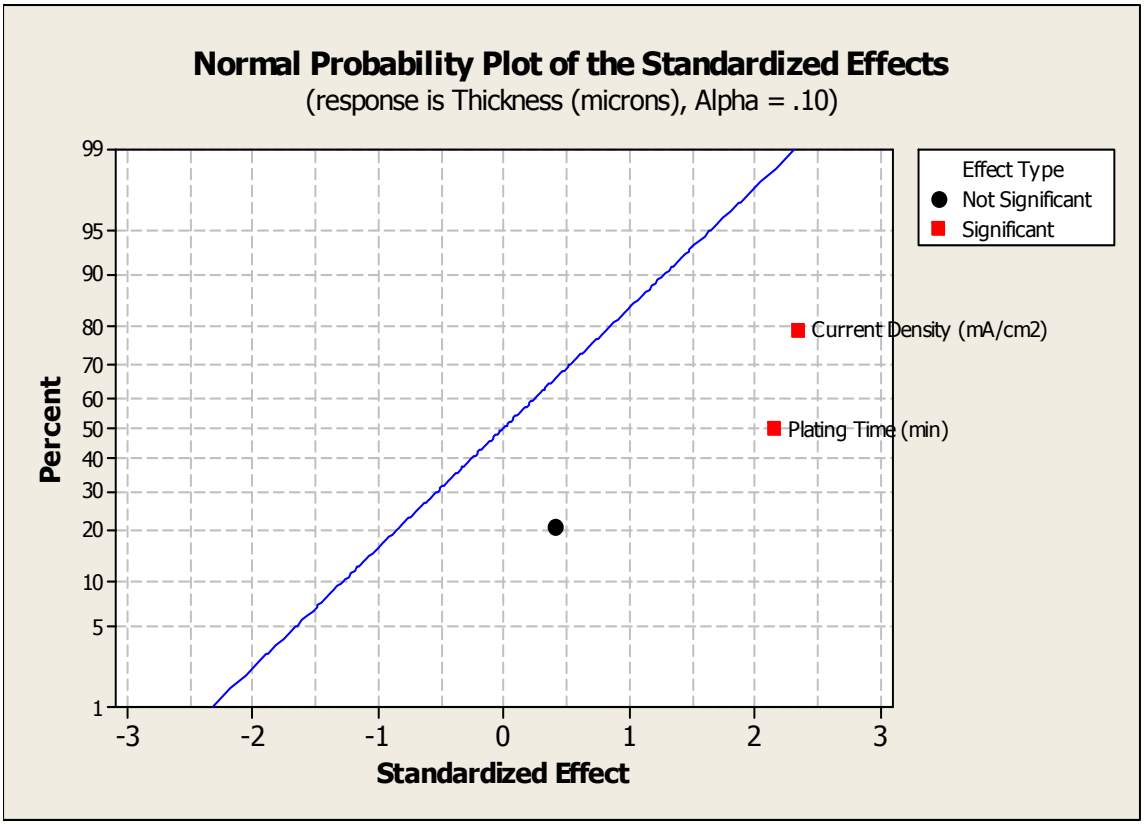


Figure 6: Normal probability plot of standardized effects for copper electroplating.

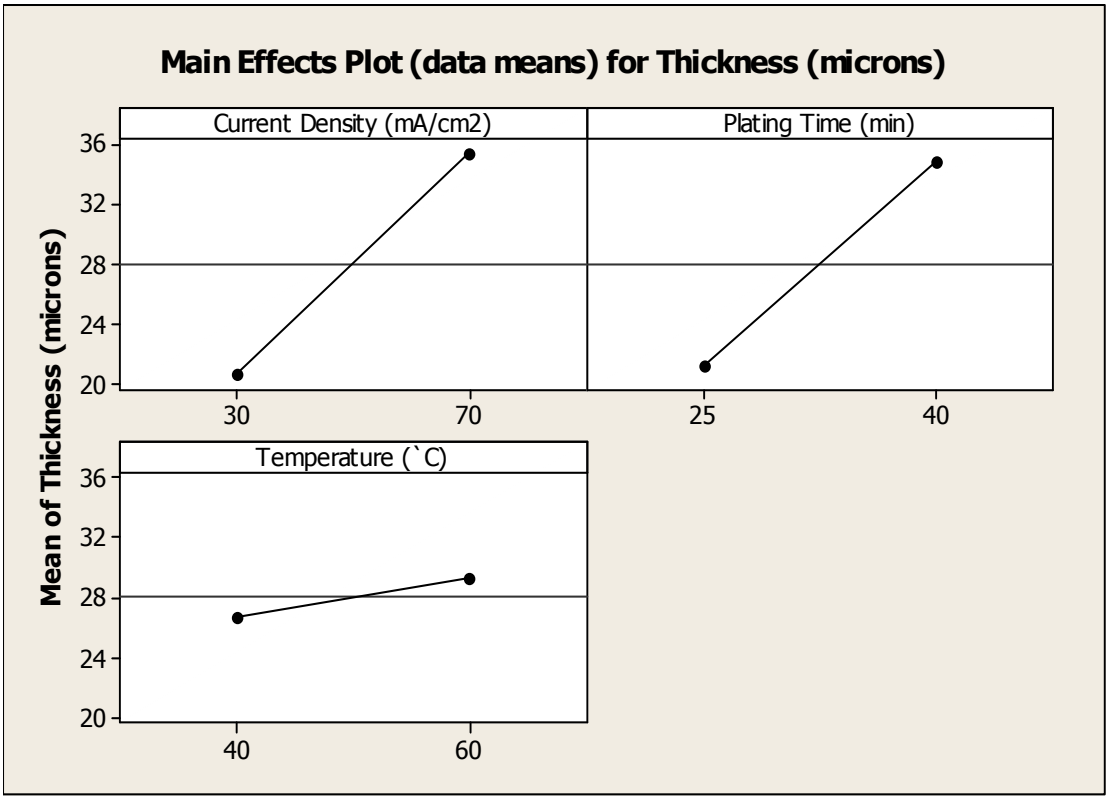


Figure 7: Main effects plot for copper electroplating process optimization. The y-axis represents thickness of copper deposit.

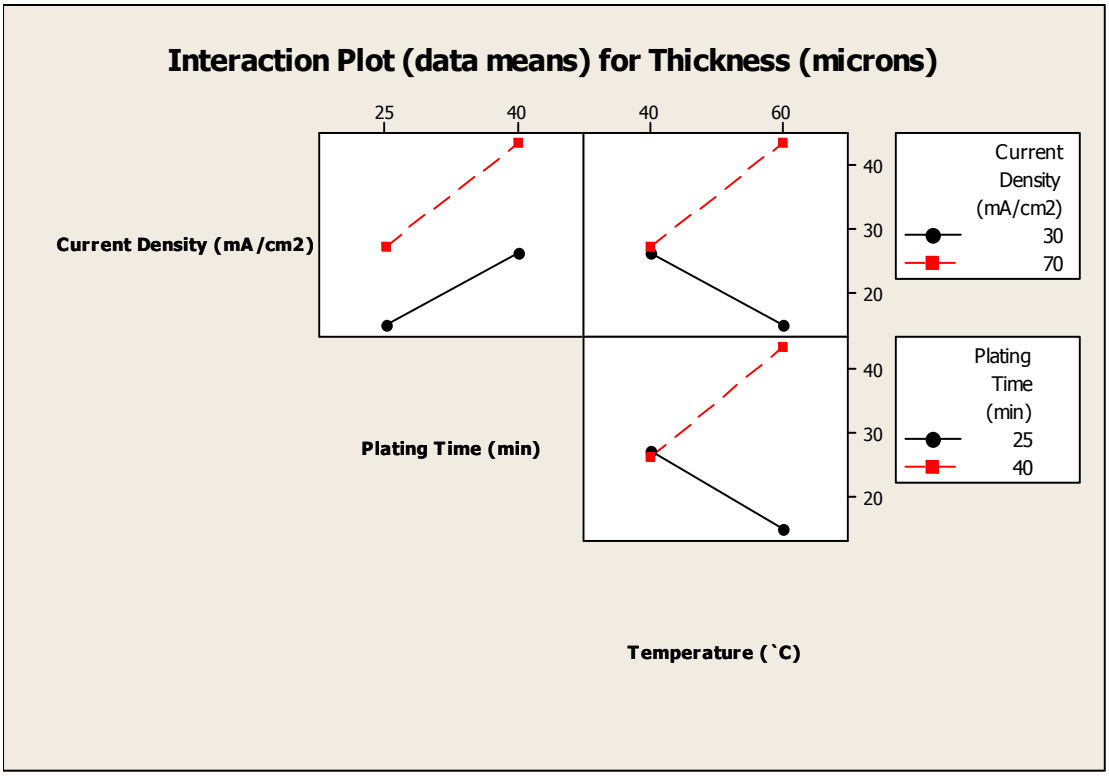


Figure 8: Interaction plot for copper electroplating process optimization

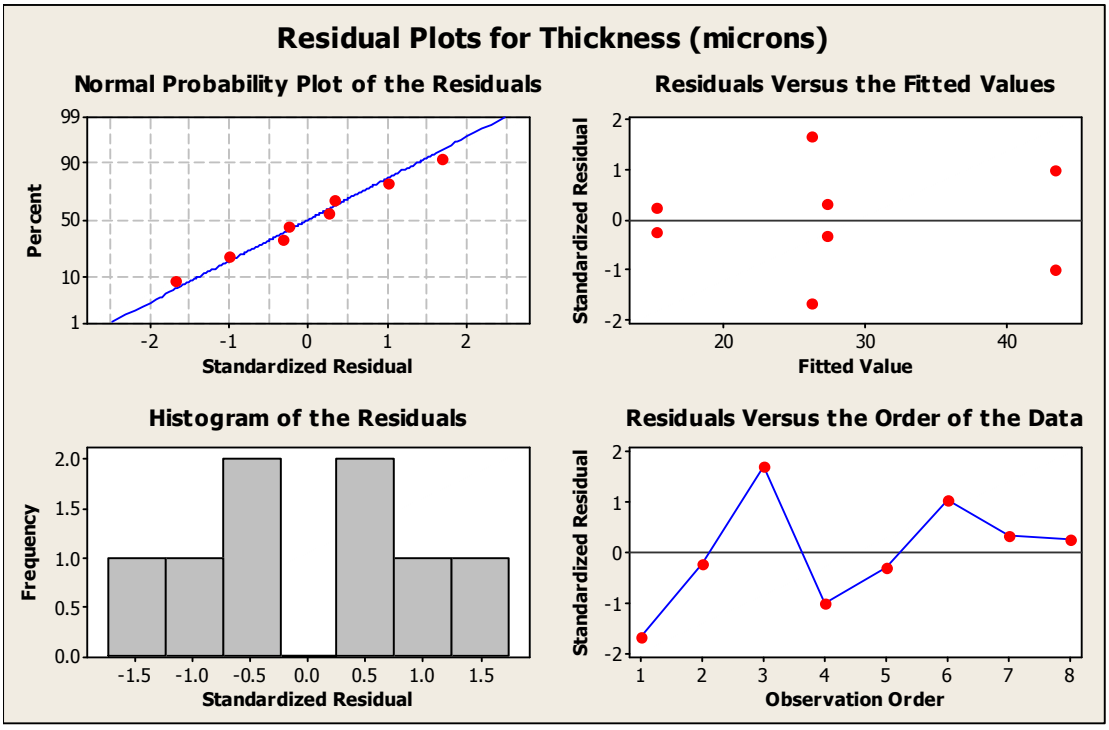
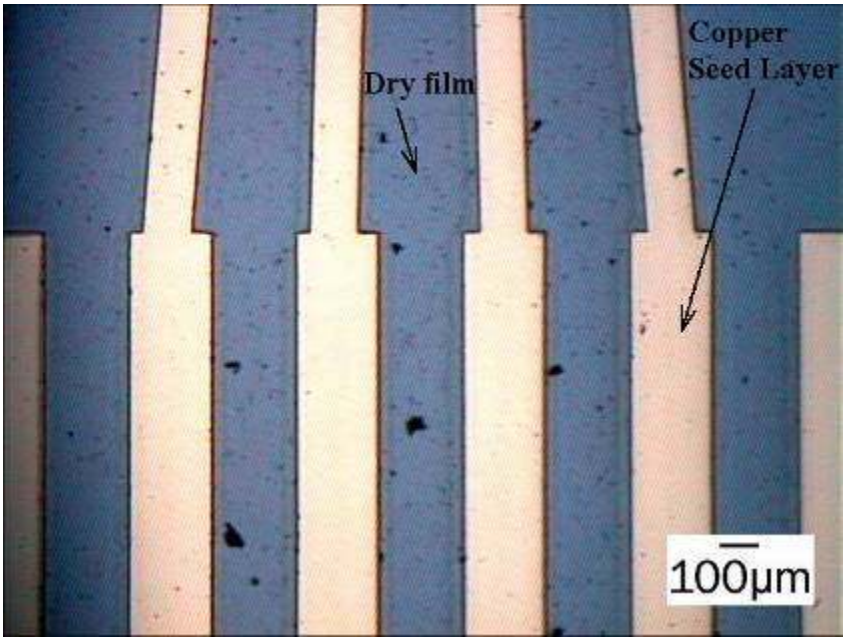
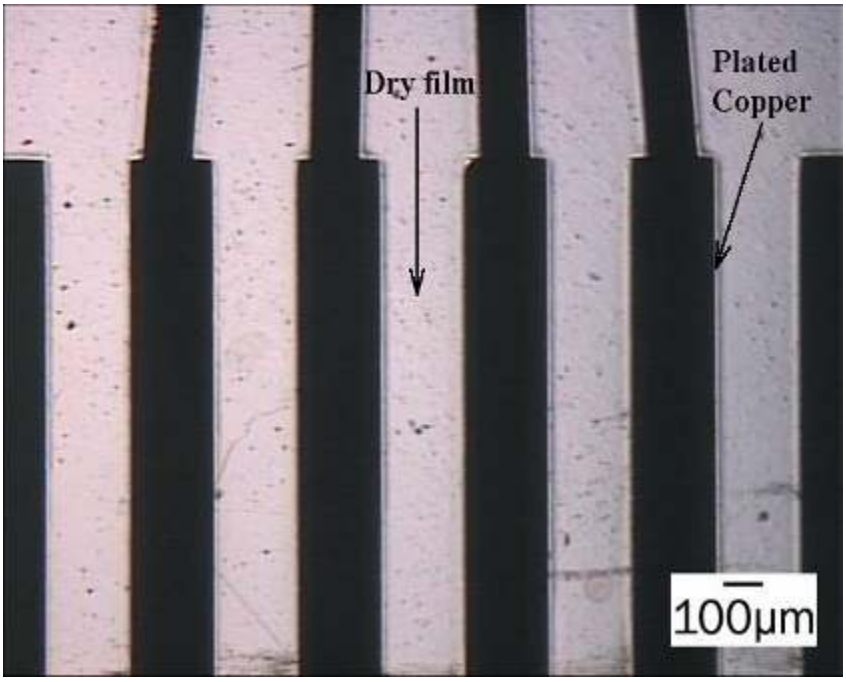


Figure 9: Residual plots for copper electroplating process optimization.

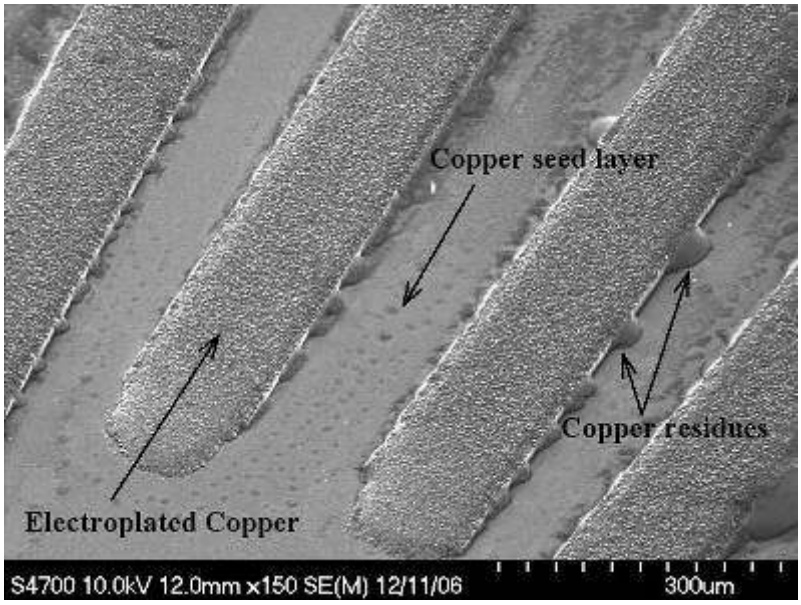


(a) Dry film pattern before electroplating.

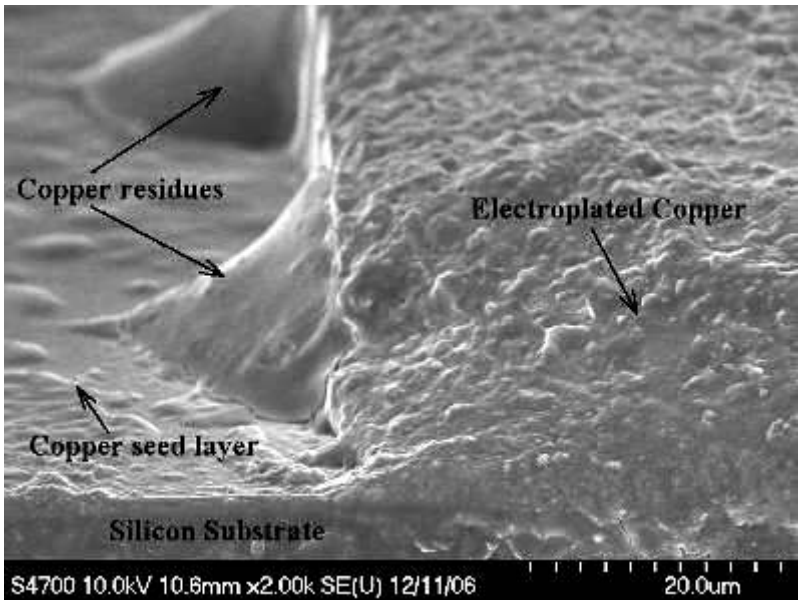


(b) Dry film pattern after electroplating

Figure 10: Optical images of lithographically patterned dry film used for electroplating

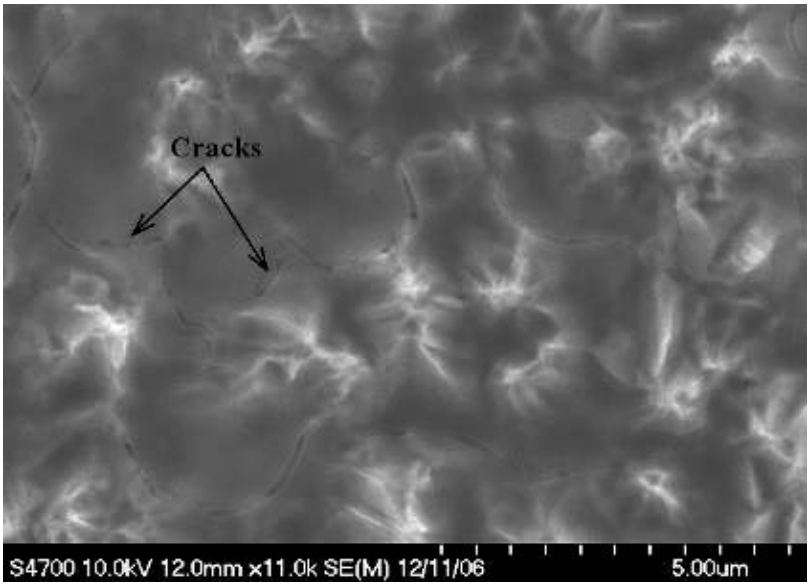


(a) Arial view of electroplated copper pattern after dry film stripping

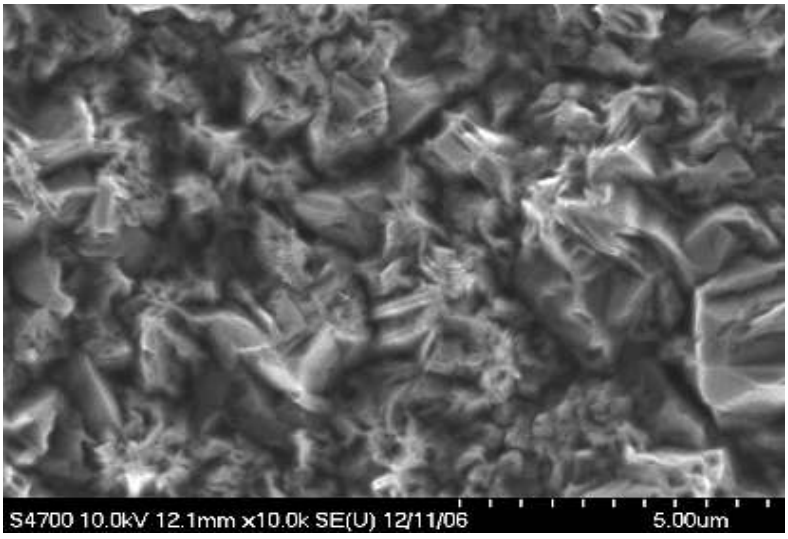


(a) Front view of electroplated copper pattern after dry film stripping

Figure 11: FESEM images of electroplated copper deposit obtained at process conditions: 30mA/cm^2, 25 min, and 60°C.

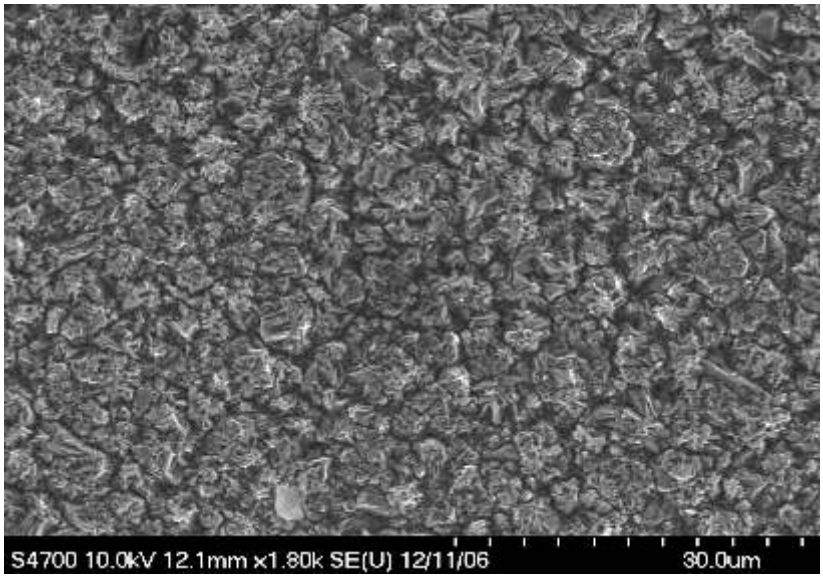


(a) Surface morphology of electroplated copper deposit obtained at process conditions: 30mA/cm^2, 25 min, and 60°C.

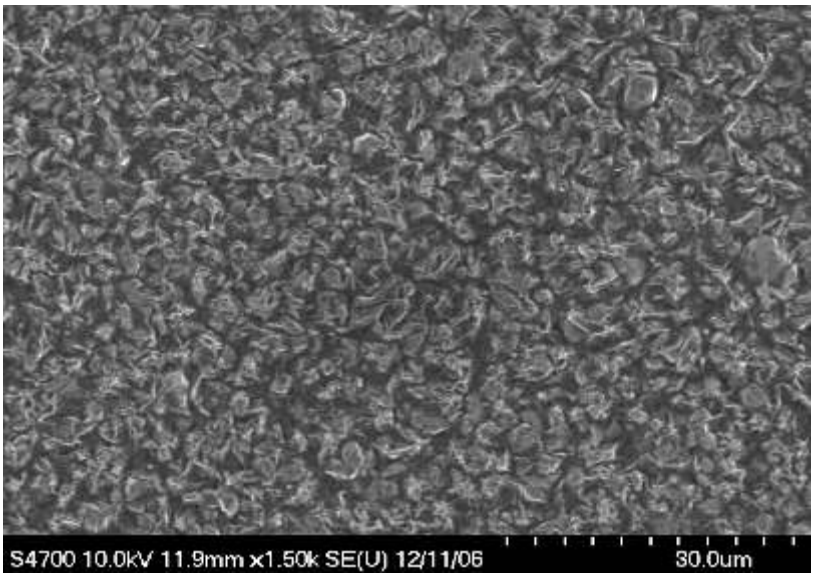


(b) Surface morphology of electroplated copper deposit obtained at process conditions: 70mA/cm^2, 40 min, and 60°C.

Figure 12: FESEM images of electroplated copper deposit obtained at various process conditions.

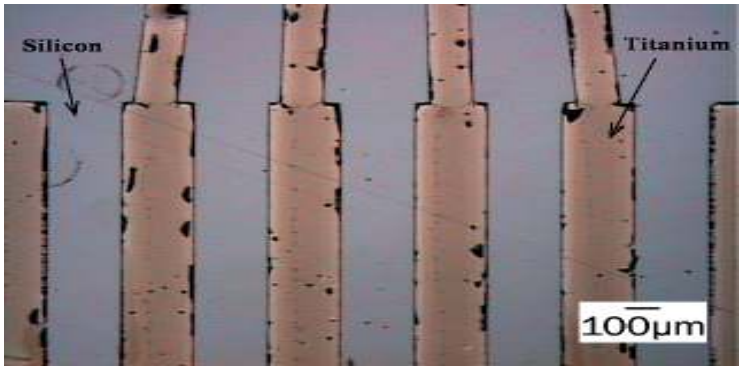


(a) Surface morphology of electroplated copper deposit obtained at process conditions: 70mA/cm^2, 40 min, and 60°C.

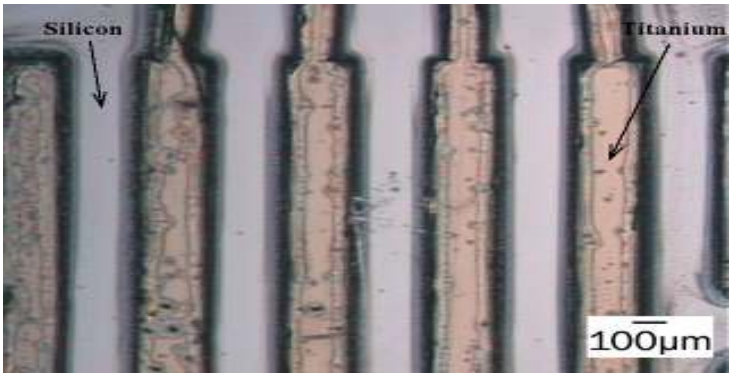


(b) Surface morphology of electroplated copper deposit obtained at process conditions: 30mA/cm^2, 40 min, and 40°C.

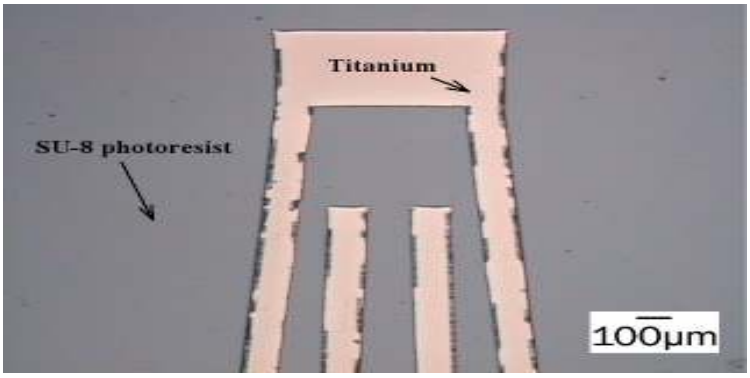
Figure 13: FESEM images of the electroplated copper deposit at decreased current density and bath temperatures.



(a) Ti (200 nm) metal lift-off on silicon substrate using dry film with 86° sidewall



(b) Ti (200 nm) metal lift-off on silicon substrate using dry film with 64° sidewall



(c) Ti (200 nm) metal lift-off on SU-8 photoresist using dry film with 86° sidewall

Figure 14: Optical images of Ti metal lift-off at various angles of dry film sidewall

Process Development for Reactive-Ion Etching of Dry Film Photoresist

Phaninder Kanikella, Matthew J. O'Keefe, Chang-Soo Kim
Department of Materials Science and Engineering
University of Missouri-Rolla, Missouri, USA 65401

Abstract

In this study, plasma etching of dry film was carried out using Ar plasma and CF_4–O_2 plasmas and full factorial designs were run to determine dry film reactive-ion etch rates. This offers the possibility for the fabrication of microchannels in dry film as a replacement for SU-8. MINITAB statistical software was used to design and analyze the full factorial experiments. The factorial designs had different combinations of CF_4 gas flow, O_2 gas flow, RF power and time. Etch rates ranged from ~150 nm/min to ~5000 nm/min. The RF power and oxygen gas flow rate were identified as significant factors contributing to the reactive-ion etch (RIE) process of dry film. The possibility of using dry film as an etch mask was also investigated to etch channels in SU-8 photoepoxy for microfluidic device fabrication based on the etch rates obtained in the experiment.

Index Terms**:** SU-8 photoresist, reactive-ion etch, CF_4–O_2 plasma, full factorial designs, dry film, photomask, microfluidic channels, UV-Lithography

I. INTRODUCTION

Over the last several years SU-8 negative tone epoxy based photoresist has been the subject of development efforts in the field of thick or ultra-thick high aspect ratio MEMS devices with aspect ratios up to 20 [1]. There are many microfabrication

processes that use SU-8 due to its good mechanical durability, water impermeability, excellent resolution in thick film applications, sensitivity to inexpensive UV sources, and nearly vertical sidewalls [2]. However, despite all these advantages, SU-8 photoresist suffers from three major disadvantages, namely adhesion selectivity, stress, and resist stripping. Dry film photoresist has been used as an alternative to SU-8 negative photoresist because it is easier to process and remove after electroplating [3]. Reactive-ion etching of dry film resist for the fabrication of bridges and cantilevers across deep grooves was reported by Spiering *et al* [4]. The dry film photoresist was also used as a simple etch mask for the deep etching of glass substrates in buffered HF solutions, which was used for the production of glass embossing stamps [5].

Photomasks are an integral component in the lithographic process of semiconductor manufacturing. High-purity quartz or glass plates containing precision images of integrated circuits (or chips), photomasks are used as masters to optically transfer these images onto semiconductor wafers coated with a light sensitive material called photoresist. Using negative photoresist the unexposed, or masked, portion of this material is then removed so it can be etched to form channels [6]. There is no information available about the reactive ion etching of dry film using CF_4–O_2 plasmas for microfluidic applications. The selectivity of dry film with respect to SU-8 can be determined to successfully etch channels in SU-8 that would form a part of microfluidic device when dry film was used as an etch mask. This study investigated the possibility of reactive-ion etching of dry film resist. For this purpose, an MX 5020 dry film photoresist (DuPont electronic Technologies Inc, USA) was used because it can be transferred into a rigid structure by a post bake.

II. EXPERIMENTAL

A standard 4-inch (100 mm) single-side polished Si wafer was cleaned for three minutes in acetone followed by 30 seconds air dry, three minutes in ethanol followed by 30 seconds air dry, and three minutes in a DI water rinse followed by 90 seconds spin dry. The wafer was subjected to a dehydration bake at 200°C for five minutes. After the cleaning step, the wafer surface was free from dust particles and other contaminants. The wafer was then heated to 100°C on a hot plate. The dry film photoresist polyolefin sheet was first removed; the film was then brought in contact with the wafer, with the resist facing the polished surface. A 4-inch wide soft rubber roller was used manually to laminate the dry film. Conformation was achieved by heating the wafer under pressure. The wafer was subjected to a post-lamination bake at 100°C for 15 minutes to enhance film adhesion on extra smooth surfaces and for aggressive applications. The processed wafer was exposed to UV light using a Karl-Suss MA/BA-6 mask aligner. A chromium mask with 250 μm wide columns was used to form patterns on dry film. The wafer was exposed at 60 mJ/cm^2 for 60 seconds (depending on the intensity of the UV bulb). A post-exposure bake was done at 90°C for 30 minutes to enhance photoresist resolution and development latitude leading to a clean surface after development and very straight photoresist sidewalls. The polyester cover sheet was removed before development. The wafer was placed on the vacuum chuck of a CEE® 100-model spin coater from Brewer Science Inc. D4000 IC developer concentrate was used for developing the resist, and the wafer was spin developed manually for three minutes followed by DI water rinse for two minutes at 1000 rpm. The wafer was then dipped in D4000 IC developer concentrate for two minutes followed by rinsing in DI water for two minutes. The wafer was further spin

dried at 3000 rpm for 45 seconds. A post- development bake was done at 90°C for 20 minutes to enhance the polymer film resolution and processing latitude, thus leading to a straighter film sidewall and higher resistance to aggressive chemistries. The sidewall angle was measured using a Nikon optical microscope and ImageJ software. The samples were then etched using a Plasma Etch PE-200 RIE system. The reactive ion etching of dry film was carried out using Ar plasma and CF_4/O_2 plasmas. The RF power used in the etch process ranged from 200W to 280W. The flow rate of argon was fixed at 100 sccm for physical etching of dry film resist. The CF_4–O_2 gas flow rates used were in the ratios of 75%:25% and 25%:75% respectively. The thickness of the etched samples was measured using the alpha-step Tencor® profilometer. The etch rates were determined for various combinations of processing conditions. The dry film patterning using UV-lithography was repeated on SU-8 substrate and the reactive-ion etch rates for dry film were used to etch deep channels into SU-8. A full factorial design method was used to identify the significant variables in dry film reactive-ion etch processes. This allows the effect of each variable to be studied at a variety of other variable levels, as well as interactions among the variables. In a full factorial experiment, responses are measured at all combinations of the experimental factors. In general, full factorial designs may be used with small screening experiments or in optimization experiments [7]. In this study, MINITAB statistical software was used to design and analyze the full factorial experiments. An Analysis of Variance (ANOVA) determined the statistical significance of each factor and the interaction between the different factors at a 90% confidence level ($\alpha = 0.10$), called a P-value.

III. RESULTS AND DISCUSSION

(I) DRY FILM ETCHING USING ARGON PLASMA

The factors and levels for a 2^2 full factorial design for RIE of dry film using Ar gas are presented in Table 1. The high and low levels were selected based on the parameter range of the equipment. The dry film etch rates for the 2^2 experiment ranged from ~150 to ~300 nm/min (Table 2). The maximum etch rates were attained at 280W, 100 sccm Ar, and four minutes etch time. The etch rate for these same conditions after one minute of process time were ~1000 nm/minute (1.0 μm/min). The deviation in etch rates with time was thought to be due to the presence of residual air in the plasma etch chamber during the initial stages of plasma processing. The effect of residual air present inside the chamber decreased over time as the chamber was enriched with the process gases [8].

Figure 1 shows the normal probability plot of the effects from the experiment. All of the effects that lie close to the line are negligible, whereas the significant effects lie away from the line. The important effect that emerges from this analysis is RF power. Also, the P-value is much less than 0.10 (α = 90% confidence level), indicating that RF power is a significant effect. The effect of RF power on the etch rate is shown in Figure 2. It shows a sharp increase from ~ 180 nm/min to ~ 300 nm/min. As expected, the etch rate increases with an increasing RF power and etch time.

Figure 3 presents the results of interactions among all the process variables. Any plot with positive slope indicates a higher etch rate while a negative slope is a lower etch rate. It shows that, for higher levels of RF power, the etch rate is higher compared to lower levels of RF power and that the etch rate increases with time for higher levels of

RF power, as would be expected since Ar plasma etching is accomplished by a physical removal mechanism.

(II) DRY FILM ETCHING USING CF_4– O_2 PLASMAS

The factors and levels for 2^4 full factorial design for RIE of dry film using CF_4/O_2 gases are presented in Table 3. The high and low levels were selected based on the parameter range of the equipment. The dry film etch rates for the 2^4 experiment ranged from ~150 to ~5000 nm/min (Table 4). The maximum etch rates were attained at 280W, 25 sccm CF_4, 75 sccm O_2, and four minutes etch time. The ANOVA results from 2^4 factorial experiment indicated that the main factors were RF power and O_2 flow rate, RF-CF_4 interaction, and CF_4–O_2 interaction with P-values less than 0.10 (α = 90% confidence level). Figure 4 shows the normal probability plot of the effects from this experiment. Again, all of the effects that lie close to the line are negligible, whereas the significant effects are away from the line. The important effects that emerge from this analysis are O_2 flow rate and RF power. However, according to the sparsity of effects principle, where there are several variables, a process is likely to be driven by some of the main effects and interactions. The three-factor and higher interactions seem negligible. Also, the P-value is much less than 0.10 (α = 90% confidence level), indicating that O_2 flow rate and RF power are significant effects, indicating that both chemical and physical etching was occurring.

The effect of O_2 flow rate and RF power on the etch rates is shown in Figure 5. It shows a sharp decrease with increasing O_2 flow rate and RF power. This is also supported by the P-values, in which O_2 flow rate and RF power are the most important variables

affecting the etch rates. Figure 5 also shows that the etch rate remains virtually the same with the change in CF_4 flow rate and etch time. The data suggests that the amount of available oxygen species in the plasma has the greatest effect on etch rate, with an increase in RF power and O_2 flow rate increasing oxygen radicals in the plasma.

Figure 6 presents the results of interactions among all the process variables. Any plot with a positive slope indicates a higher etch rate while a negative slope is a lower etch rate. The three important interactions considered to be significant in the normal probability plot were evaluated. It shows that, for higher levels of RF power, the etch rate decreases with increasing CF_4 flow rate. It also depicts that for higher levels of RF power, the etch rate increases sharply with increasing O_2 flow rate. Also, for lower values of CF_4 flow rate, the etch rate increases with increasing O_2 flow rate. This can be explained with the following mechanism: One of the species that may have formed in the CF_4 plasma is CF_2, which is a component of polytetrafluoroethylene (PTFE or Teflon). At higher CF_4 flows and increased times, it is possible that greater amounts of CF_2 may have formed and coated the surfaces of dry film to slow down the etch rate. Trials were conducted for using dry film as a mask material to etch SU-8 with the previously obtained RIE data. It showed that microchannels can be fabricated by using dry film as an etch mask to etch SU-8 [2]. The trench depth and sidewall angle of SU-8 microchannels need to be focused more in future studies when dry film is used as an etch mask.

IV. CONCLUSION

Using a full factorial design, the effect of four factors, RF power, CF_4 gas flow rate, O_2 gas flow rate, and etch time on the etch rate of dry film was studied. Etch rates ranged from ~150 nm/min to ~5000 nm/min. The etch rate is mainly controlled by O_2 gas flow rate and RF power. Increased RF power and oxygen flow increased the etch rate, most likely due to an increase in the formation of oxygen radicals in the plasma. The dry film proved to be a useful etch mask material to etch channels.

ACKNNOWLEDGMENT

The authors would like to thank Dr. Martin Perez of the University of Missouri-Rolla and Pedro Goncalo C. T. Jorge of DuPont Electronic Technologies, USA for their valuable suggestions.

REFERENCES

[1] Marc Rabarot, Jacqueline Bablet, Marine Ruty, Matthieu Kipp, Isabelle Chartier, and Christophe Dubarry, "Thick SU-8 Photolithography For BioMEMS," *Micromachining and Microfabrication Process Technology VIII, Proceedings of SPIE,* Vol. 4979, pp. 382-390, 2003.

[2] Martin G. Perez, Matthew J. O'Keefe, Phaninder Kanikella, James Reck, and Chang-Soo Kim, "Reactive-ion etching of SU-8 photoresist using CF_4–O_2 plasmas," *Manuscript submitted to J. Microeng,* 2007.

[3] E. Kukharenka, M. M. Farooqui, L. Grigore, M. Kraft and N. Hollinshead, "Electroplating moulds using dry film thick negative photoresist," *J. Micromech. Microeng,* Vol. 13, pp. S67-S74, 2003.

[4] V.L. Spiering, J. W. Berenschot and M. Elwenspoek, "Planarization and fabrication of bridges across deep groves or holes in silicon using a dry film photoresist followed by an etch back," *J. Micromech. Microeng,* Vol. 5, pp.189-192, 1995.

[5] M. E. Sandison and H. Morgan, "Rapid fabrication of polymer microfluidic systems for the production of artificial lipid bilayers," *J. Micromech. Microeng,* Vol. 15, pp. S139-S144, 2005.

[6] Chihchen Chen, Danny Hirdes, and Albert Folch, "Gray-scale photolithography using microfluidic photomasks," PNAS, Feb 2003; 100: 1499 - 1504.

[7] Minitab, Inc. *Minitab 14 Users Manual* From the Help menu, "Analyzing Full Factorial Design with Replicates and Blocks," State College, PA, 2004.

[8] Plasma Etch, Inc*., Plasma Etch PE-200 Users Manual*, Reno, NV, 2005.

Table 1: Factors and levels for 2^2 Full Factorial design (dry film RIE using Ar gas)

Factor	Level	
	Low (-)	High (+)
A=RF power (W)	200	280
B=Time (min)	2	4

Table 2: Average Etch Rates for Experimental conditions in the 2^2 Factorial design (dry film RIE using Ar gas)

StdOrder	Blocks	RF Power (W)	Time (Min)	Avg. Etch Rate (nm/min)
4	1	280	4	308 ± 30
1	1	200	2	158 ± 75
6	1	280	2	294 ± 50
7	1	200	4	201 ± 30

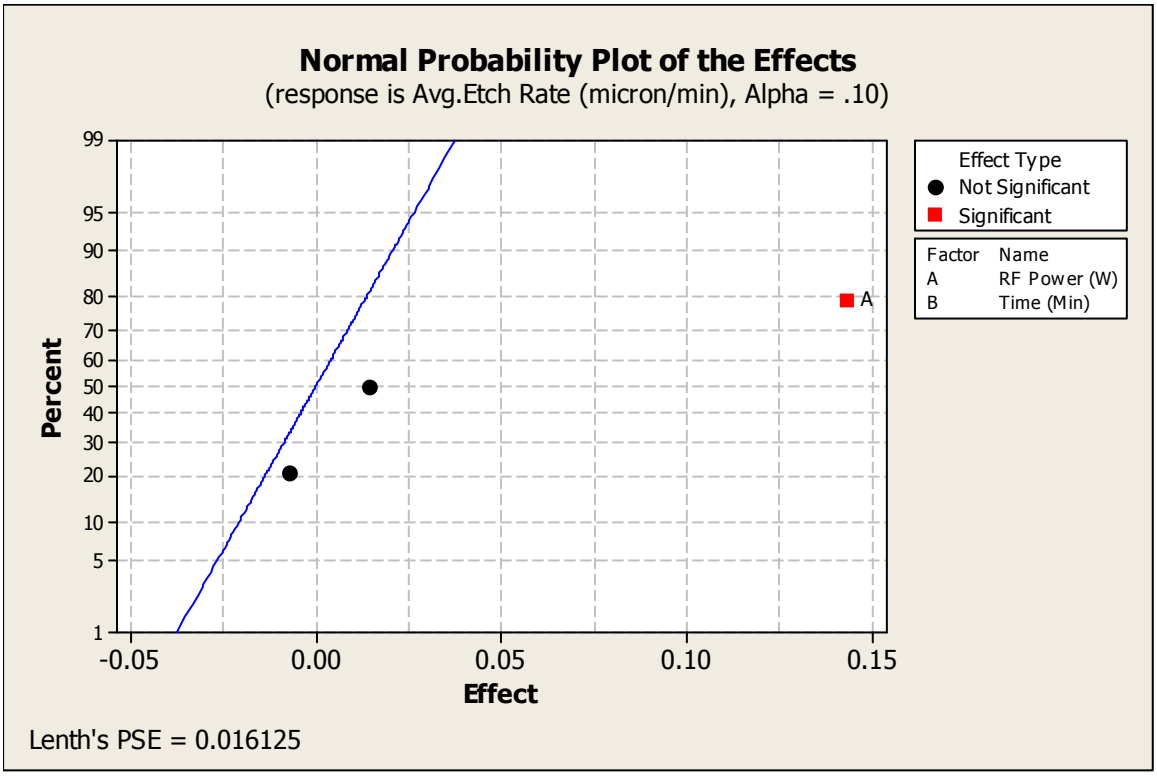


Figure 1: Normal probability plot for RIE of dry film using Ar gas.

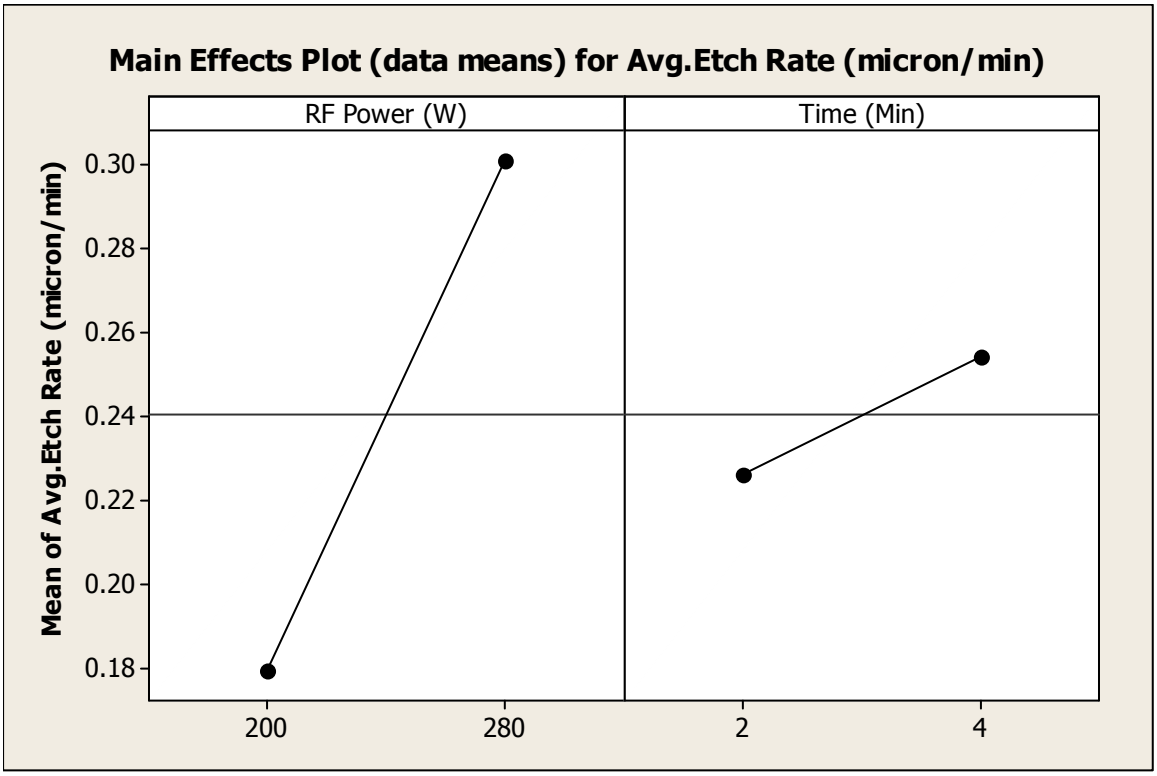


Figure 2: Main effects plot for RIE of dry film using Ar gas.

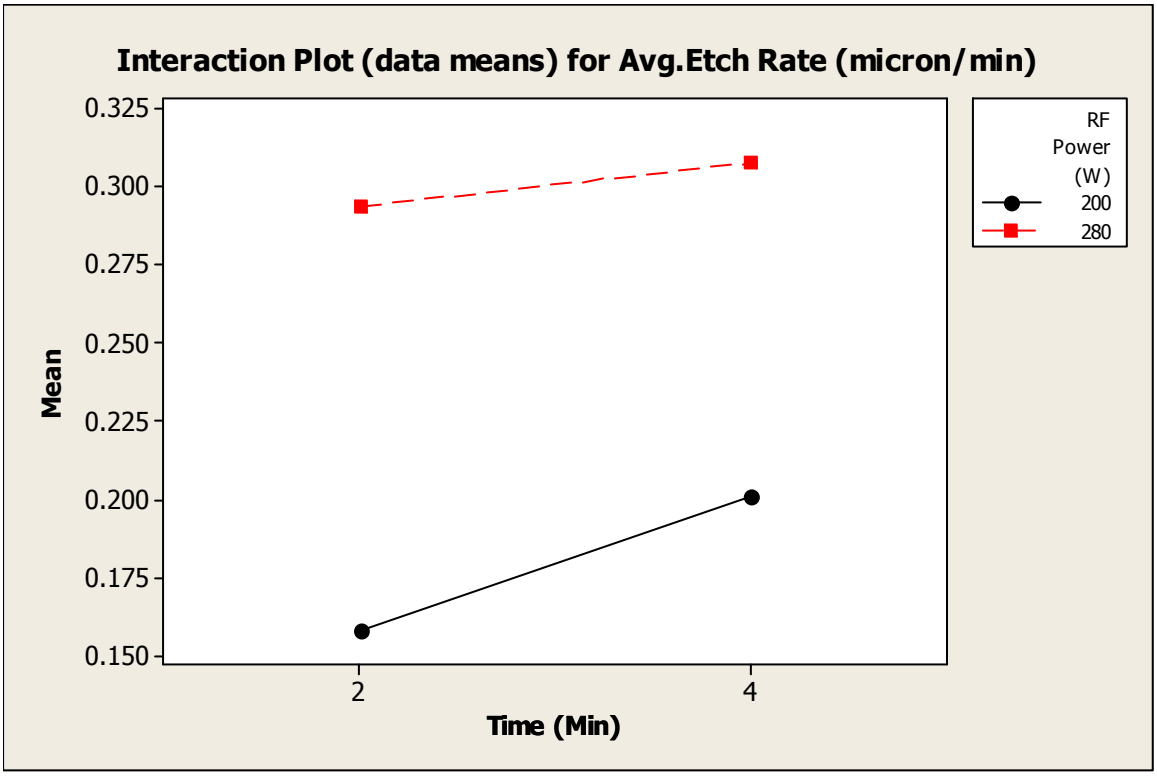


Figure 3: Interaction plot for dry film RIE using Ar gas.

Table 3: Factors and levels for 2^4 Factorial design (dry film RIE using CF_4/O_2 gases)

Factor	Level	
	Low (-)	High (+)
A=RF power (W)	200	280
B=CF_4 (sccm)	25	75
C=O_2 (sccm)	25	75
D=Time (min)	2	4

Table 4: Average Etch Rates for Experimental conditions in the 2^4 Factorial design (dry film RIE using CF_4/O_2 gases)

StdOrder	RF Power (W)	CF_4 (sccm)	O_2 (sccm)	Time (min)	Etch Rate (nm/min)
14	280	25	75	4	4980 ± 8
8	280	75	75	2	3630 ± 70
9	200	25	25	4	1150 ± 60
13	200	25	75	4	1340 ± 40
16	280	75	75	4	3530 ± 25
12	280	75	25	4	147 ± 100
5	200	25	75	2	1620 ± 90
2	280	25	25	2	1160 ± 100
10	280	25	25	4	1620 ± 70
11	200	75	25	4	244 ± 120
6	280	25	75	2	4770 ± 200
4	280	75	25	2	700 ± 60
3	200	75	25	2	490 ± 15
1	200	25	25	2	1340 ± 50
7	200	75	75	2	3680 ± 90
15	200	75	75	4	3030 ± 25

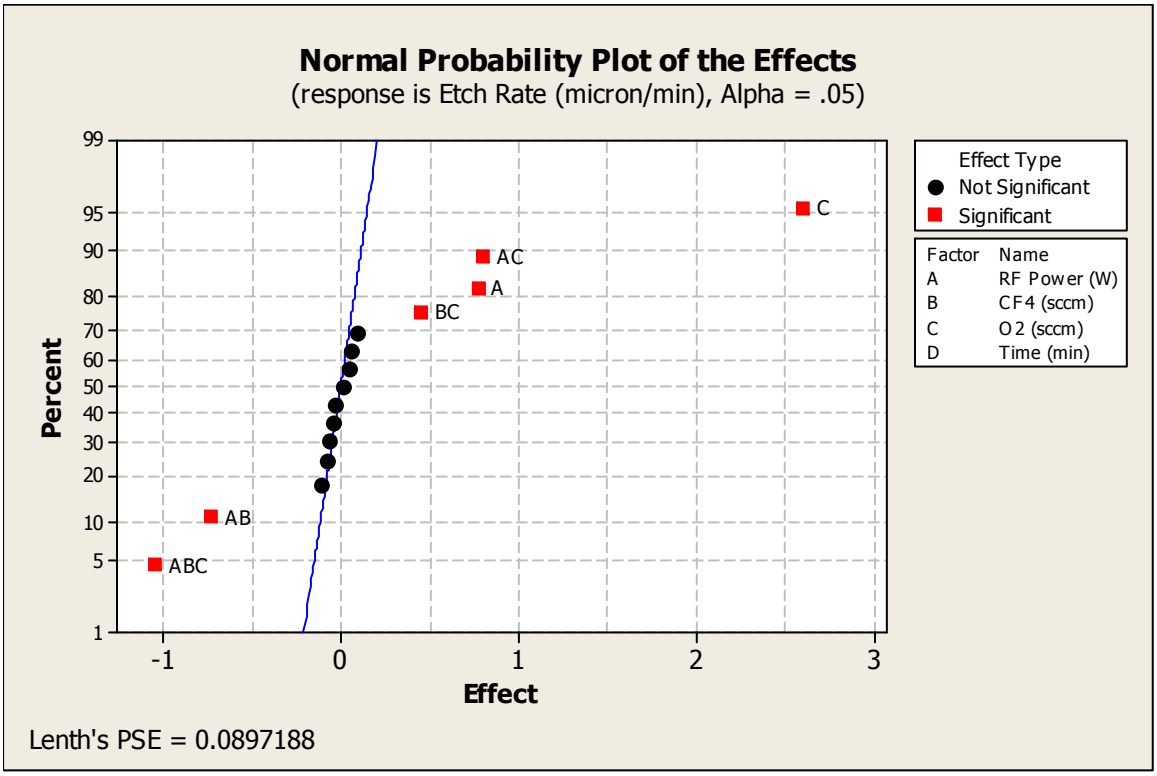


Figure 4: Normal probability plot for RIE of dry film using CF_4/O_2 gases.

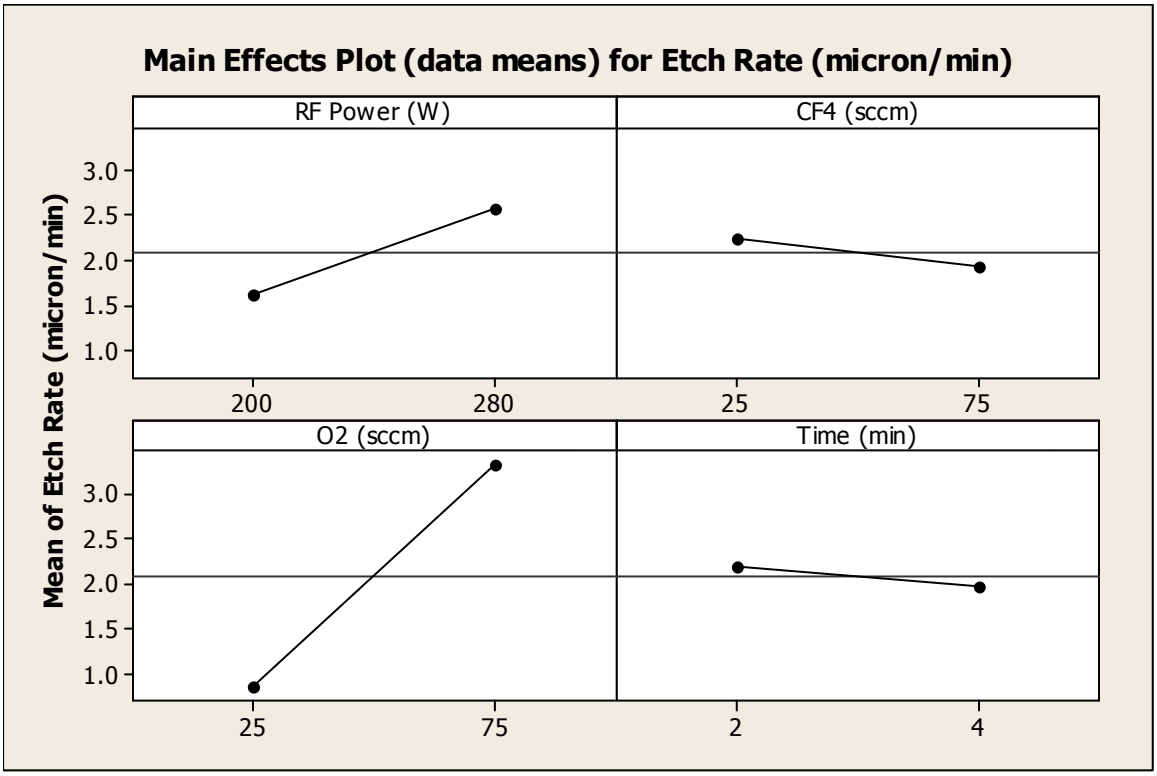


Figure 5: Main effects plot for RIE of dry film using CF_4/O_2 gases.

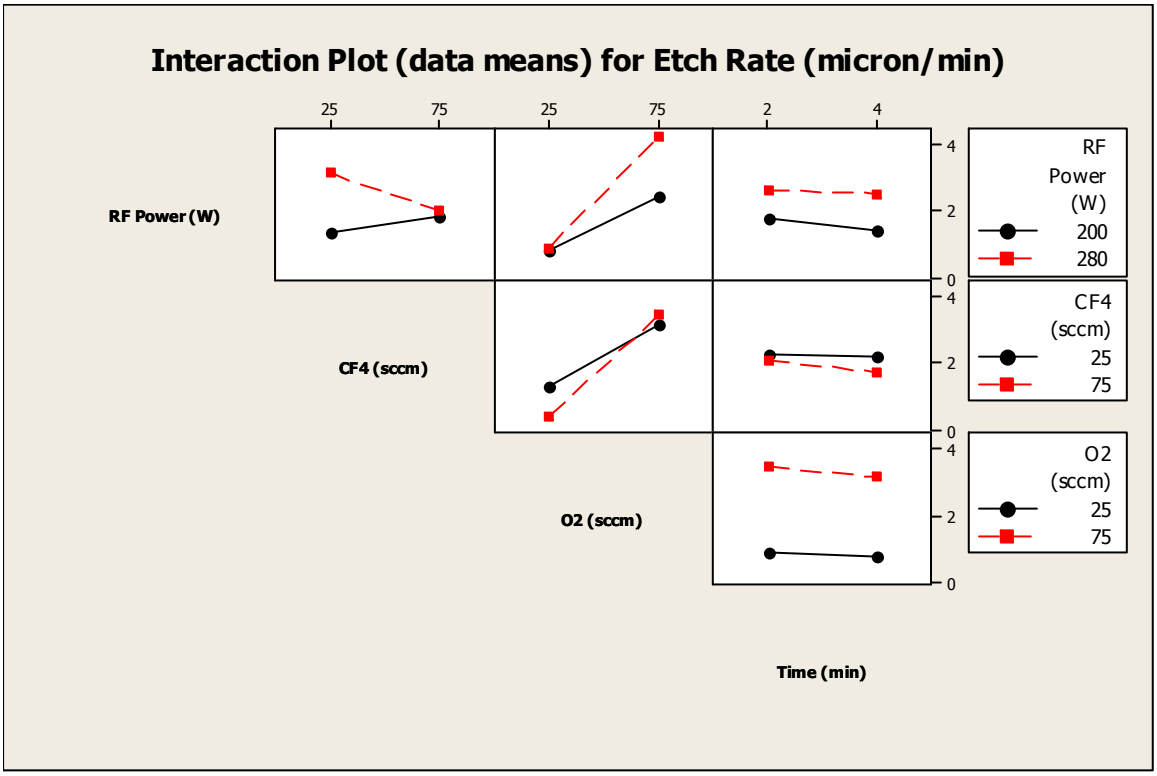


Figure 6: Interaction plot for RIE of dry film using CF_4/O_2 gases.

VITA

Phaninder Reddy Kanikella was born on November 26, 1983 in Hyderabad, India. In June 2005, he obtained a bachelor's degree in Metallurgy and Materials Technology from Jawaharlal Nehru Technological University, Hyderabad, India. In 2005, he received the prestigious JNT University Gold Medal for the best outgoing student in Metallurgy and Materials Technology.

In August 2005, he enrolled at the University of Missouri-Rolla to pursue a master's degree in Materials Science and Engineering under the guidance of Dr. Matthew J. O'Keefe. During his time at UMR, he was employed as a Graduate Research Assistant in the Materials Science and Engineering department. He also worked as a Process Development Engineer through a co-op at Vicor Corporation in Boston, Mass for five months in 2007. He received his master's degree from UMR in July 2007.