1971

The design and experimental investigation of a hybrid phase-lock loop

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Department:

THE DESIGN AND EXPERIMENTAL INVESTIGATION OF A HYBRID PHASE-LOCK LOOP

BY

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THESIS

Presented to the Faculty of the Graduate School of the

UNIVERSITY OF MISSOURI-ROLLA

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Rolla, Missouri

1971

Approved by

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ABSTRACT

This thesis describes the design and the laboratory implementation of a hybrid phase-lock loop. The step-by-step procedure followed in developing this experimental hybrid phase-lock loop, and its optimization with respect to various parameters are given. In regard to the performance characteristics, the loop was used to obtain the phase estimate of a split-phase modulated signal. The phase error probability density function was measured under various input noise conditions and these results are included and compared with previously published theoretical results.

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ACKNOWLEDGEMENTS

The author wishes to express his sincere appreciation to Dr. Rodger E. Ziemer for his very valuable guidance and help in the preparation of this thesis and to Dr. William H. Tranter for his very useful comments in the writing of this thesis.

Appreciation is also extended to Connie Hendrix for her typing efforts.

I. INTRODUCTION

The hybrid phase-lock loop (PLL) is a combination of a Costas loop [1]* and a phase-lock loop [2]. The Costas loop portion responds to the modulation component and the phase-lock loop portion responds to the carrier component of the received signal. In a hybrid loop the phase estimate for coherent detection is derived both from the carrier and data components. The superior performances of the phase-lock loop and Costas loop at low and high signal-to-noise ratios (SNRs), respectively, are therefore combined to obtain a better performance for all SNRs than for a Costas or phase-lock loop alone.

This thesis is concerned with the development of an experimental implementation of a hybrid phase-lock loop which is optimized for minimum mean-square phase error with respect to its design parameters. The design procedure is considered in detail. Also performance is characterized in terms of mean-square phase error versus input SNR.

The hybrid phase-lock loop is presently of interest due to the possibility that it may perform better than conventional tracking loops in non-Gaussian and non-stationary environments such as radio-frequency interference, multipath and fading. Such backgrounds may be severe problems in various synchronous-orbit relay-

*Numbers in [] denote references

satellite systems now under study [3]. Also of interest is possible application in low data-rate systems [4]. Theoretical studies have been made of the performance of a hybrid phase-lock loop as compared to the performance of a Costas or a conventional phase-lock loop [4,5,6]. The well-known Fokker Planck techniques were used in these studies, and a maximum improvement of 1.5dB in SNR was predicted. The optimization of the hybrid loop with respect to its design parameters has been dealt with in detail in [5]. This approach has been used in this study to optimize the experimental model of the hybrid loop developed and will be described in the latter sections. Before doing so, however, the hybrid loop will be described in more detail and its equations of operation developed.

II. DESCRIPTION OF THE HYBRID LOOP AND EQUATIONS OF OPERATION

A block diagram of a hybrid loop is shown in Fig. 1. As previously mentioned it is essentially a combination of a Costas loop and a phase-lock loop. The outer loop (ABCDEFGHI), referred to as the Costas loop portion, is designed to lock on the modulation component of the input signal. The inner loop (ABGHI), referred to as phase-lock loop portion, is designed to respond to the carrier component of the input signal. The error signals from both branches of the loop are added and passed through the loop filter F(p). The output of the loop filter is used as the control voltage of the voltage-controlled oscillator (VCO). The filters with transfer functions G(p) of the outer legs remove the double frequency components resulting from the multiplication operations as well as the low-frequency component due to the carrier component at the input. To permit removal of this low frequency component, the data input should have negligible energy in its spectrum close to the origin; this is true, for example, if split phase modulation is used for transmission of the data, or if the data is placed on a subcarrier.

The equations of operation are easily derived [5]. In Fig. 1, let

$$y(t) = s(t) + n(t) \tag{1}$$

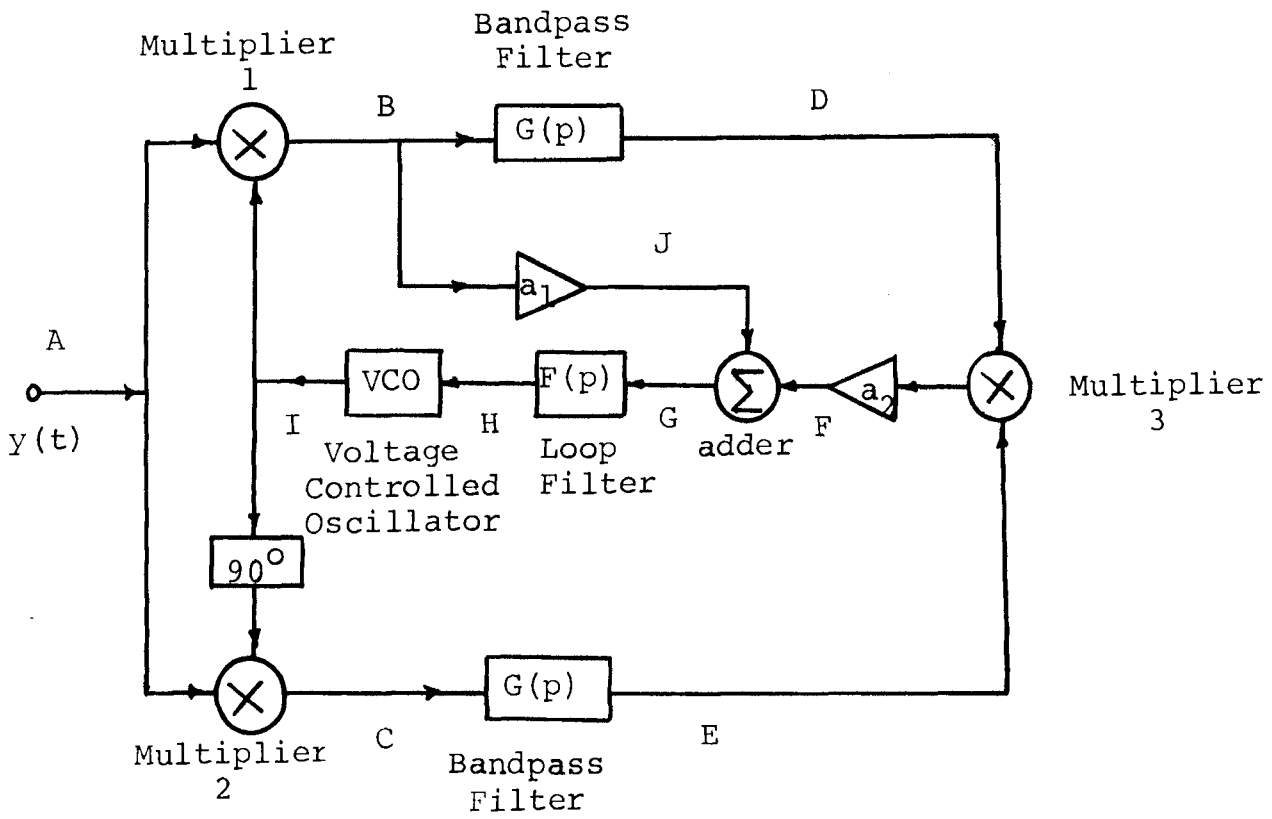


Figure 1. Block Diagram of a Hybrid Phase-Lock Loop

where

$$s(t) = \sqrt{2}\, A\, \mathrm{Sin}(\omega t + x(t)\mathrm{Cos}^{-1} m + \theta) \qquad (2)$$

is the signal, and

$$n(t) = \sqrt{2}\, n_c(t)\mathrm{Cos}(\omega t+\theta) + \sqrt{2}\, n_s(t)\mathrm{Sin}(\omega t+\theta) \qquad (3)$$

represents a Gaussian noise process. In (2), $x(t) = \pm 1$ in T_B - second intervals is the modulation and m is the square-root of the ratio of the power in the reference signal to the total transmitted power. The signal component of the input, s(t), can also be written as

$$s(t) = \sqrt{2}\, Am\, \mathrm{Sin}(\omega t+\theta) + \sqrt{2}\, A\sqrt{1-m^2}\, x(t)\mathrm{Cos}(\omega t+\theta)$$

where the first term is the carrier component and the second term is the modulation component.

The VCO output is assumed to be

$$\sqrt{2}\, k_1\, \mathrm{Cos}(\omega t + \hat{\theta}) \ .$$

This yields

$$y_B(t) = k_o[2k_1 Am\, \mathrm{Sin}(\omega t+\theta)\mathrm{Cos}(\omega t+\hat{\theta}) +$$

$$2Ak_1\sqrt{1-m^2}\, x(t)\mathrm{Cos}(\omega t+\theta)\mathrm{Cos}(\omega t+\hat{\theta}) +$$

$$\sqrt{2}\, k_1\, \mathrm{Cos}(\omega t+\hat{\theta})n(t)] \qquad (4)$$

for the output of Multiplier 1. Similarly, the output of Multiplier 2 is

$$y_c(t) = k_o[2\ k_1\ Am\ Sin(\omega t+\theta)Sin(\omega t+\hat{\theta}) +$$

$$2Ak_1\sqrt{1-m^2}\ x(t)Cos(\omega t+\theta)Sin(\omega t+\hat{\theta}) +$$

$$\sqrt{2}\ k_1\ Sin(\omega t+\hat{\theta})n(t)]. \qquad (5)$$

The filters with transfer function G(p) eliminate the double frequency and dc components. These signals, $y_D(t)$ and $y_E(t)$ are multiplied in multiplier M3 producing the outer loop control voltage

$$e_c(t)= k_0^2k_2\ [\frac{A^2(1-m^2)}{2}]\ k_1^2\ Sin2\phi + Ak_1\sqrt{1-m^2}\ x(t)n_c(t).$$

$$Sin2\phi - k_1A\sqrt{1-m^2}\ x(t)n_s(t)Cos2\phi +$$

$$\frac{k_1^2n_c^2}{2}\ Sin2\phi - k_1^2n_cn_s\ Cos2\phi - \frac{n_s^2k_1^2}{2}\ Sin2\phi], \qquad (6)$$

where $\phi = \theta - \hat{\theta}$ is the phase error.

The control voltage for the phase-lock loop portion is

$$e_p(t) = k_1AmSin\phi + k_1n_c(t)Cos\phi + k_1n_s(t)Sin\phi, \qquad (7)$$

and the total control voltage due to outer and inner loops is

$$e_H(t) = F(p)\ [a_1\ e_p(t) + a_2e_c(t)].$$

Here a transfer function

$$F(p) = \frac{p+a}{p+\varepsilon} \qquad (8)$$

is used, where a and ε are constants. This corresponds to the case of an inperfect second-order loop. The differential equation for the loop can be written as

$$\frac{d\hat{\theta}}{dt} = +k_v F(p) \ [a_1 e_p(t) + a_2 e_c(t)] \tag{9}$$

or

$$\frac{d\theta}{dt} - \frac{d\phi}{dt} = +k_v F(p) [a_1 e_p(t) + a_2 e_c(t)]. \tag{10}$$

Considering only the signal portion of $e_p(t)$ and $e_c(t)$, linearizing the equation by assuming ϕ to be small, substituting $F(p) = \frac{p+a}{p+\varepsilon}$, and simplifying, yields

$$\frac{d^2\phi}{dt^2} + \{k_v k_o k_1 A[m + \frac{a_2}{a_1} k_o k_2 k_1 A(1-m^2)] + \varepsilon\} \frac{d\phi}{dt} +$$

$$k_v k_o k_1 A \, a[m + \frac{a_2}{a_1} k_o k_2 k_1 A(1-m^2)]\phi(t)$$

$$= \frac{d^2\theta}{dt^2} + \varepsilon \frac{d\theta}{dt} . \tag{11}$$

Letting

$$G_o = k_v k_o k_1 A[m + \frac{a_2}{a_1} k_o k_2 k_1 A(1-m^2)], \tag{12}$$

$$\varepsilon + G_o = 2\xi\omega_n, \tag{13}$$

and

$$\omega_n^2 = G_o a \tag{14}$$

allows (11) to be written as

$$\ddot{\phi}(t)+2\xi\omega_n\dot{\phi}(t) + \omega_n^2\phi(t) = \ddot{\theta}(t)+\varepsilon\dot{\theta}(t) . \qquad (15)$$

This is a differential equation for a second-order linear system written in terms of the parameters ξ, the damping factor, and ω_n, the natural frequency. Together with the imperfection factor ε, ω_n and ξ completely characterize the loop response to an arbitrary input, $\theta(t)$, provided that the input is small so that linearization holds. The nonlinear equation of loop operation, (10), can also be expressed in terms of these parameters.

Quite often it is convenient to characterize the loop in terms of its single-sided equivalent noise bandwidth B_L, which can be obtained from

$$B_L = \frac{1}{H^2(0)} \int_0^\infty |H(j\omega)|^2 \frac{d\omega}{2\pi} , \qquad (16)$$

where $H(j\omega)$, the closed loop transfer function is

$$H(s) = \frac{\hat{\theta}(s)}{\theta(s)} = 1 - \frac{\phi(s)}{\theta(s)} \qquad (17)$$

From (15) we obtain

$$H(s) = \frac{G_o s+aG_o}{s^2+(\varepsilon+G_o)s+aG_o} . \qquad (18)$$

Carrying out the integration for B_L yields

$$B_L = \frac{G_o+a}{4(1+\varepsilon/G_o)} . \qquad (19)$$

Design of the loop consists of choosing appropriate values for G_0, a and ε to get the required bandwidth and damping factor. The procedure is outlined in the next section.

III. DESIGN OF THE HYBRID LOOP

The design procedure is based on the theory outlined in the previous section. The design equations for the hybrid loop have been shown to be:

1. Loop Bandwidth; $B_L = \frac{G_o+a}{4(1+\varepsilon/G_o)}$ (20)

2. Loop Damping Factor; $\xi = \frac{1}{2} \cdot \frac{\varepsilon+G_o}{\sqrt{aG_o}}$ (21)

The value of ξ was chosen to be $1/\sqrt{2}$. Jaffe and Rechtin [7] have shown that this choice of ξ minimizes phase error variance due to additive noise at the input, while maintaining a specified maximum transient phase error due to the step changes in input phase. Once the value of ξ is fixed at $1/\sqrt{2}$, the expression for loop bandwidth can be written as

$$B_L = G_o \cdot \frac{1+a/G_o}{4\sqrt{2a/G_o}} \tag{22}$$

where a is the loop filter time constant and ε is the loop filter imperfection factor. Also,

$$G_o = k_v k_3 (a_1 k_o)(k_1 A)[m+\rho(1-m^2)] \tag{23}$$

where

k_v is VCO constant (rad/sec./volt),

k_3 is the loop filter gain factor,

a_1 is inner loop gain,

$$m = \frac{\text{Power in the reference } (P_v)}{\text{Total transmitted power } (P_T)} \quad , \tag{24}$$

and

$$\rho = \frac{a_2}{a_1} k_2 k_o k_1 A. \tag{25}$$

For a given value of loop bandwidth and ξ of $1/\sqrt{2}$, it remains to optimize the loop with respect to m and ρ. Computerized results showing the values of $\rho_{opt.}$ and $m_{opt.}$ for different values of input SNR are given in [5]. The loop filter time constant, a, and the loop imperfection factor, ε, are determined by solving the two equations giving B_L and ξ in terms of loop parameters.

The hybrid loop design is shown in Fig. 2. Detailed design of the various loop components are given in Appendix A, and an illustrative design example is given in Appendix B. A summary of the values of the various parameters pertinent to the design shown in Fig. 2 is given in Table II in Appendix B. For ξ = .707, loop bandwidths of 8.5, 85, 850 and 8500 Hz, are achieved by switching various resistors and capacitors into the feedback loops of the operational amplifiers. By adjusting the potentiometers at the summing junction of the first operational amplifier ρ can be adjusted from 0.05 t0 2.5.

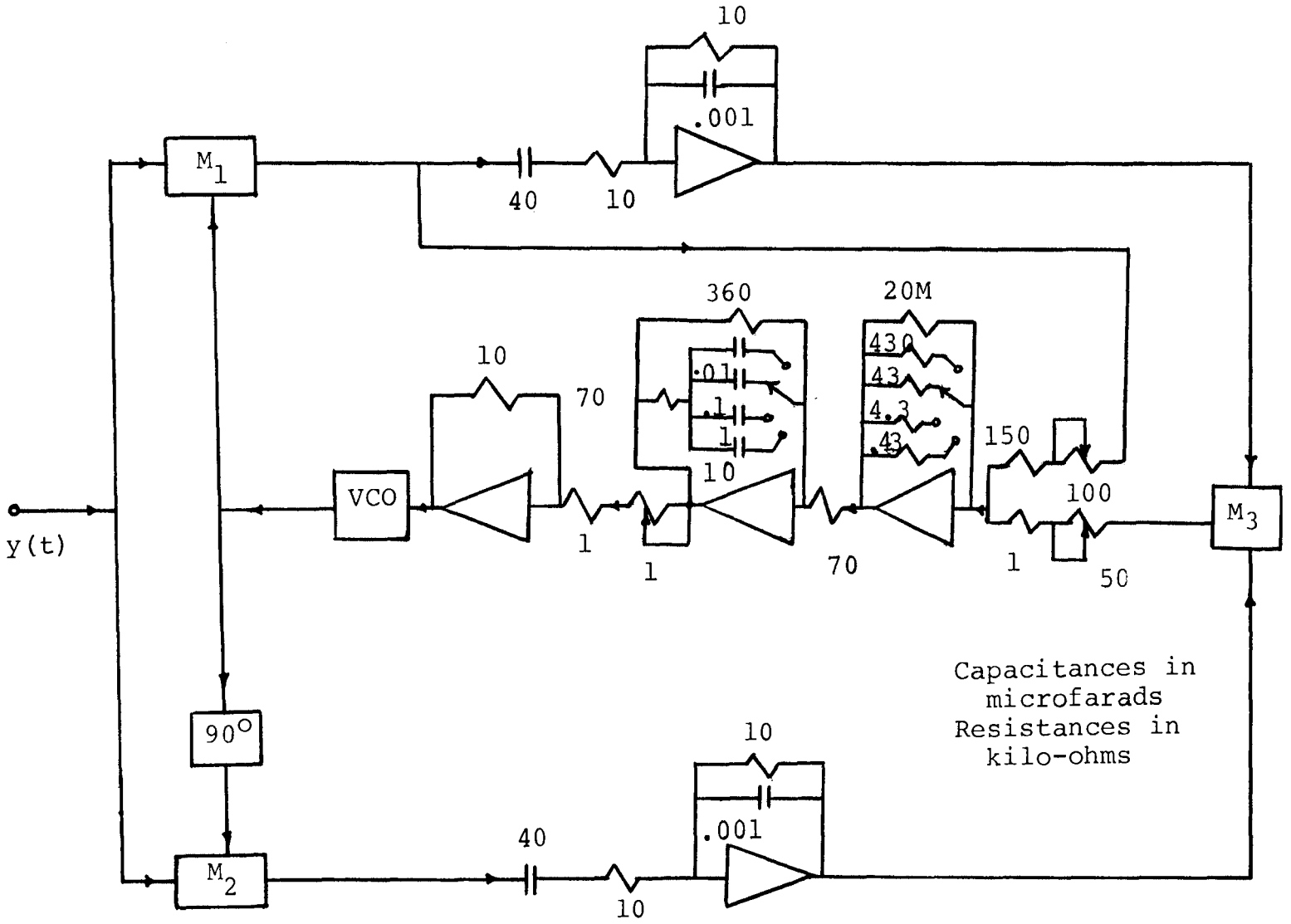


Figure 2. Experimental Hybrid Phase-Lock Loop

IV. RESULTS AND DISCUSSIONS

Performance of the loop was experimentally tested by demodulating a phase modulated signal in the presence of noise, and measuring the phase error probability density function. Details of the experimental set up are given in Appendix C.

In Fig. 3, the modulating PN-sequence and the demodulated PN-sequence, when no external noise was added to the input signal, are shown. The modulating signal is a 63 bit maximal-length PN code with a bit rate of 11.7k Hz.

The input to the loop is a split-phase modulated signal, i.e. a logic one is encoded as a plus-to-minus phase transition and a logic zero as a minus-to-plus transition, or vice-versa.

Phase error probability density functions for various loop and noise conditions are shown in Figures 4-10. The phase error standard deviations obtained from these phase error density plots at different SNRs and for various modulation indices are tabulated in Table I. The last column in Table I represents the value of the phase-error standard deviation of the hybrid loop (σ_H) calculated theoretically from the results of [5]. From [5]

$$\sigma_H^2 = 1 + \frac{\rho^2(1-m^2)\left[1+\frac{1}{z\beta(1-m^2)}\right]}{z[m + \rho(1-m^2)]} \qquad (26)$$

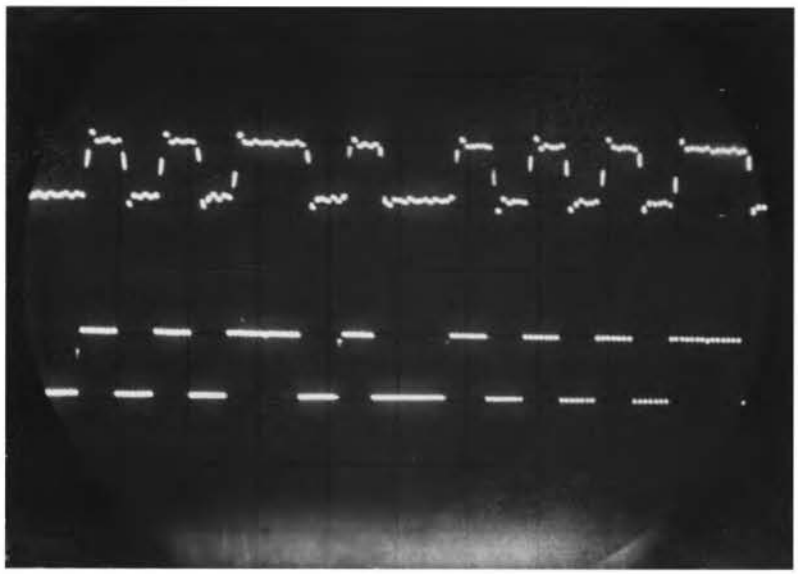
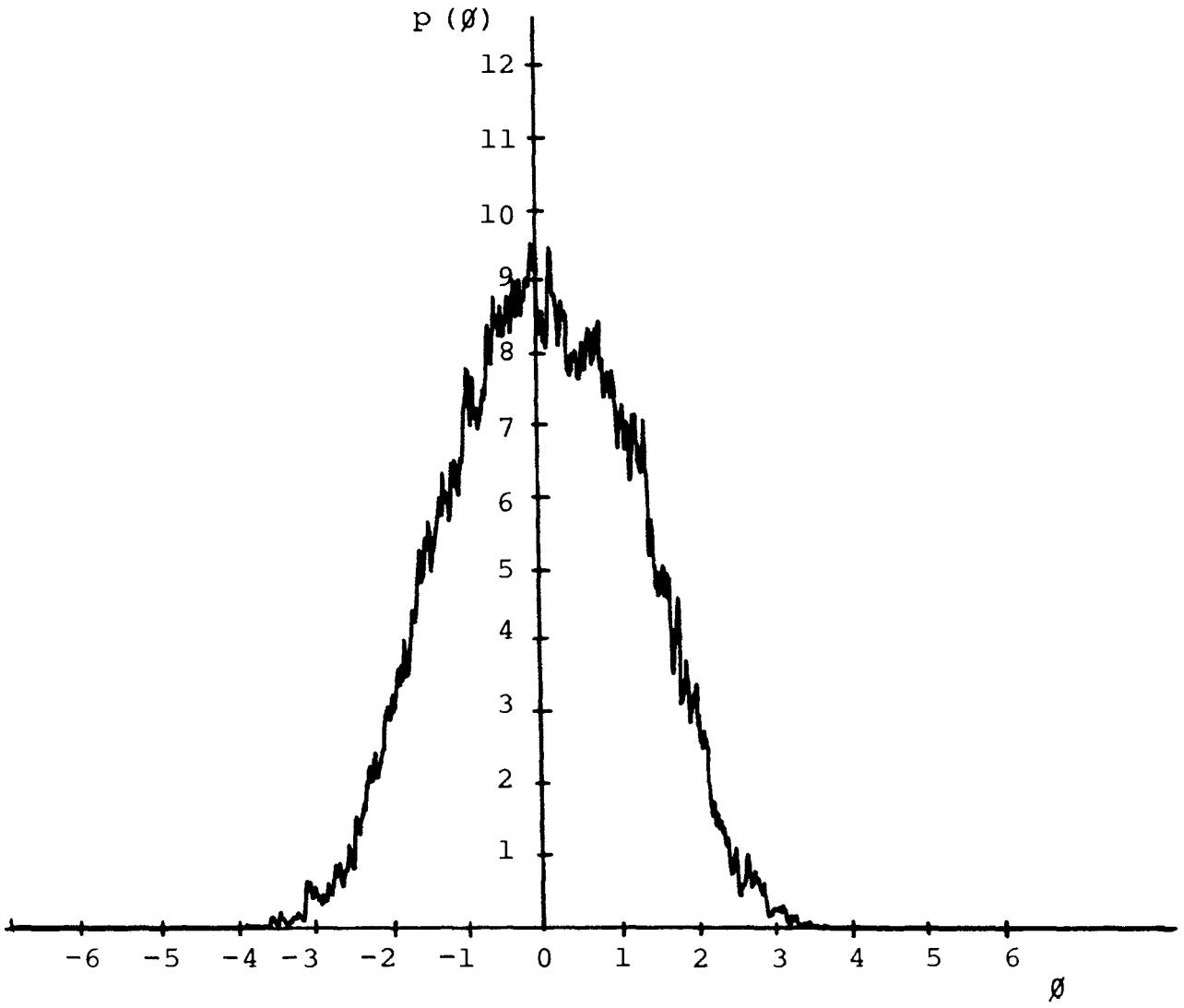
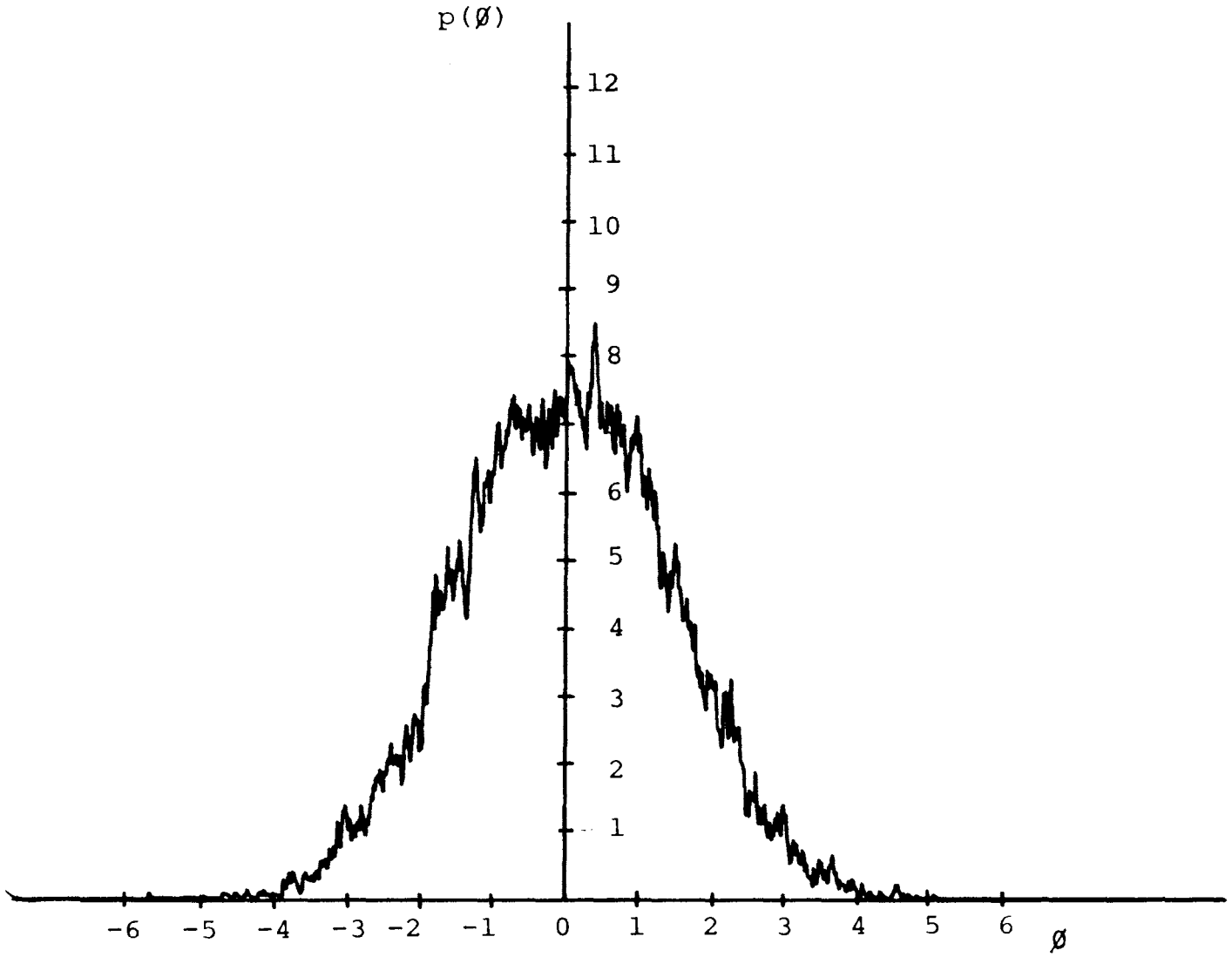


Figure 3. Modulating PN Sequence (lower trace) and Demodulated Output Sequence (upper trace)



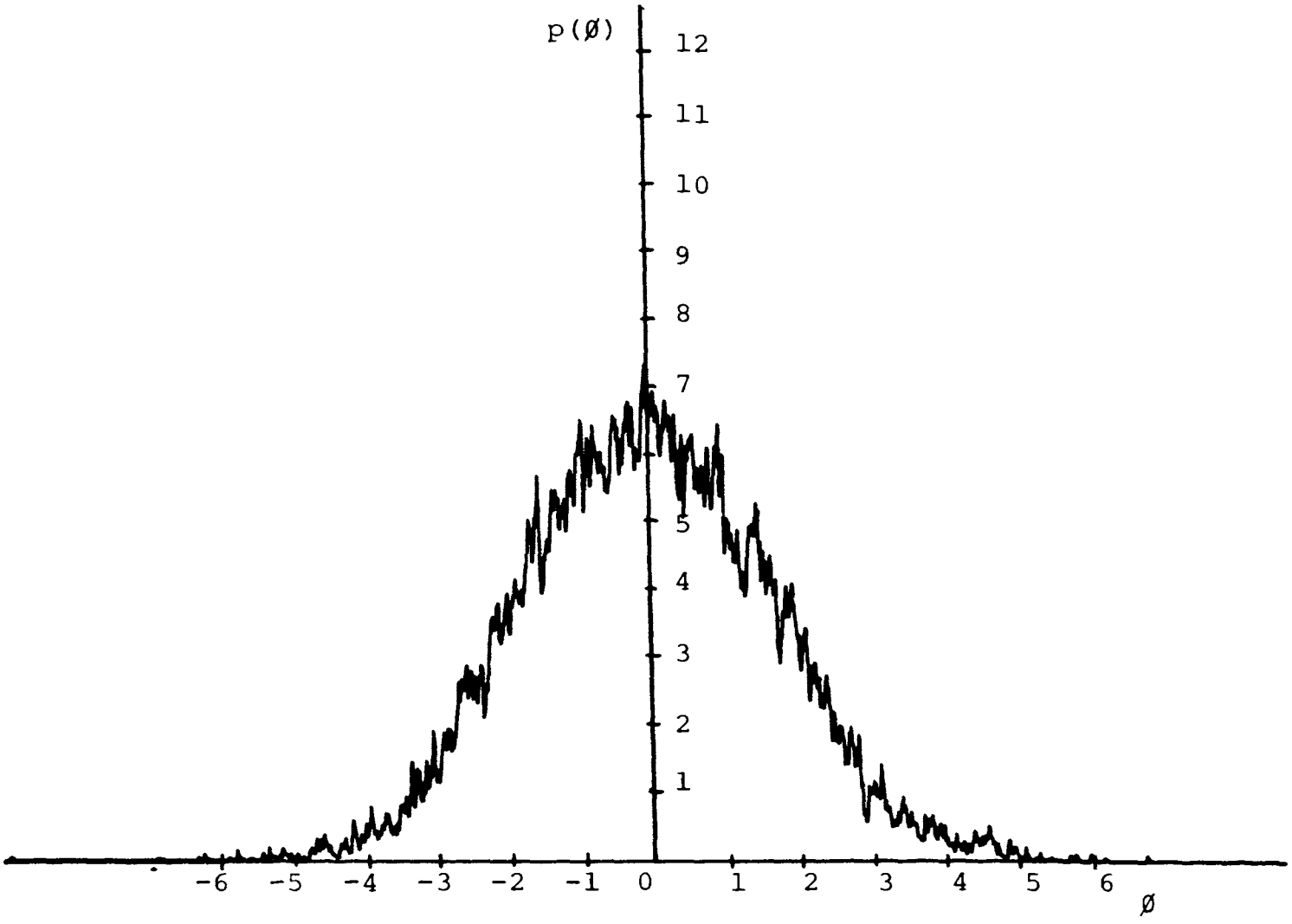
Calibration: Abscissa 1 unit = 1.12 radians
Ordinate 1 unit = .0377 rad.$^{-1}$

Figure 4. Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3; m=1/2, SNR=25dB



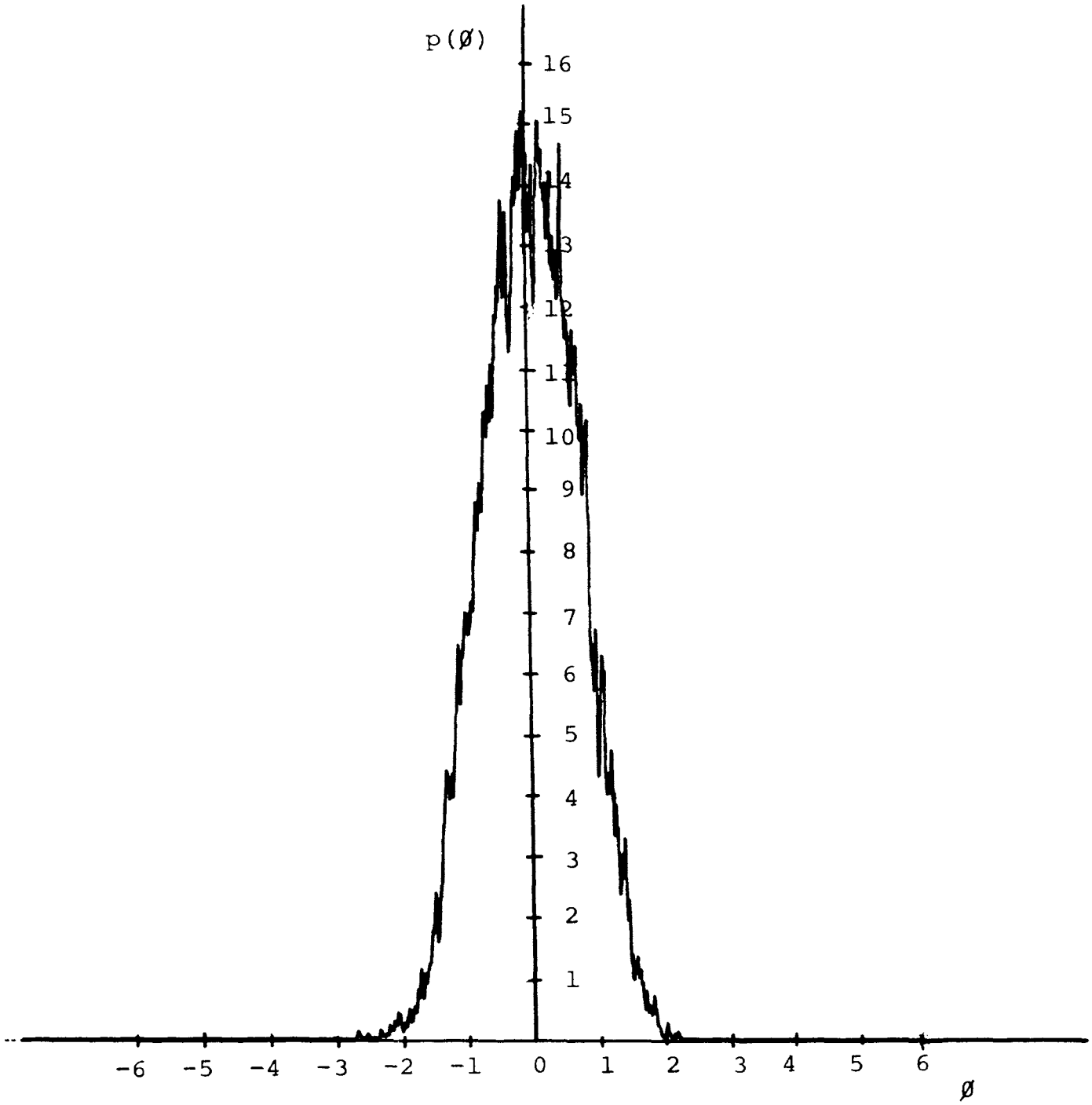
Calibration: Abscissa; 1 unit = 1.12 radians
Ordinate: 1 unit = .0431 rad^{-1}

Figure 5. Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3, m=1/2, SNR=19dB



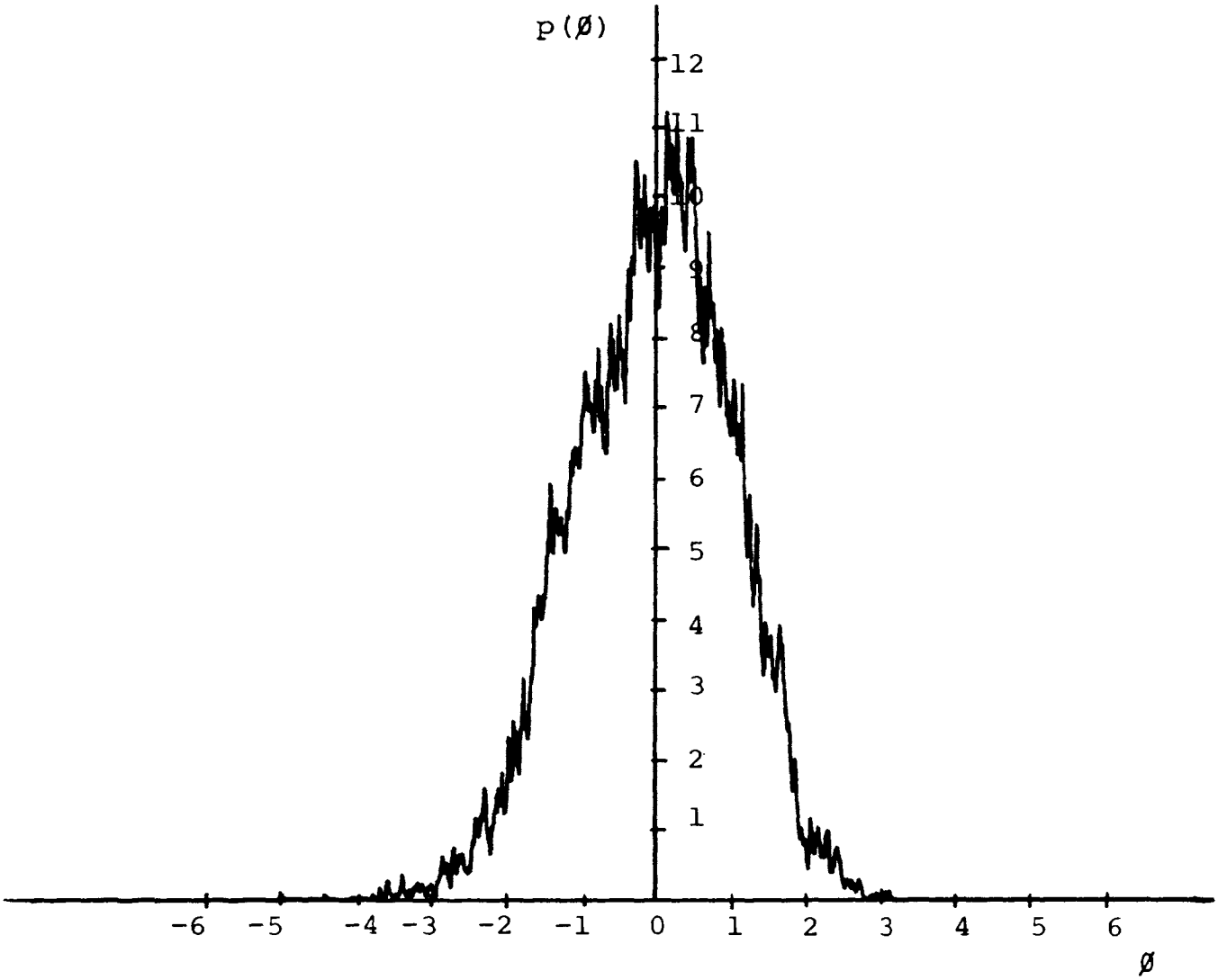
Calibration: Abscissa; 1 unit = 1.12 radians
Ordinate: 1 unit = .0431 rad^{-1}

Figure 6. Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3, m=1/2, SNR=17dB



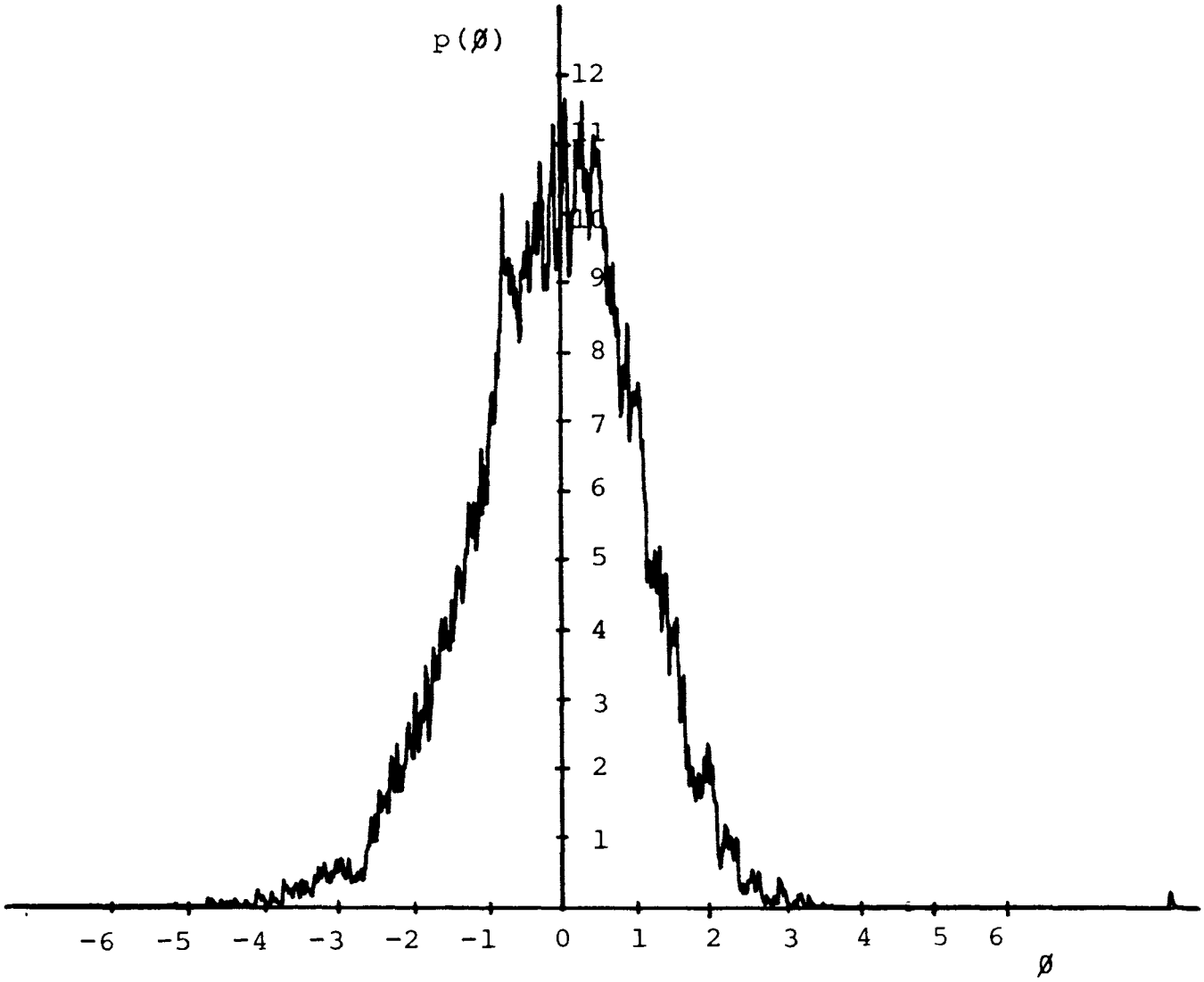
Calibration: Abscissa:1 unit = 1.12 radians
Ordinate:1 unit = .031 rad^{-1}

Figure 7. Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3, m=1, SNR=25dB



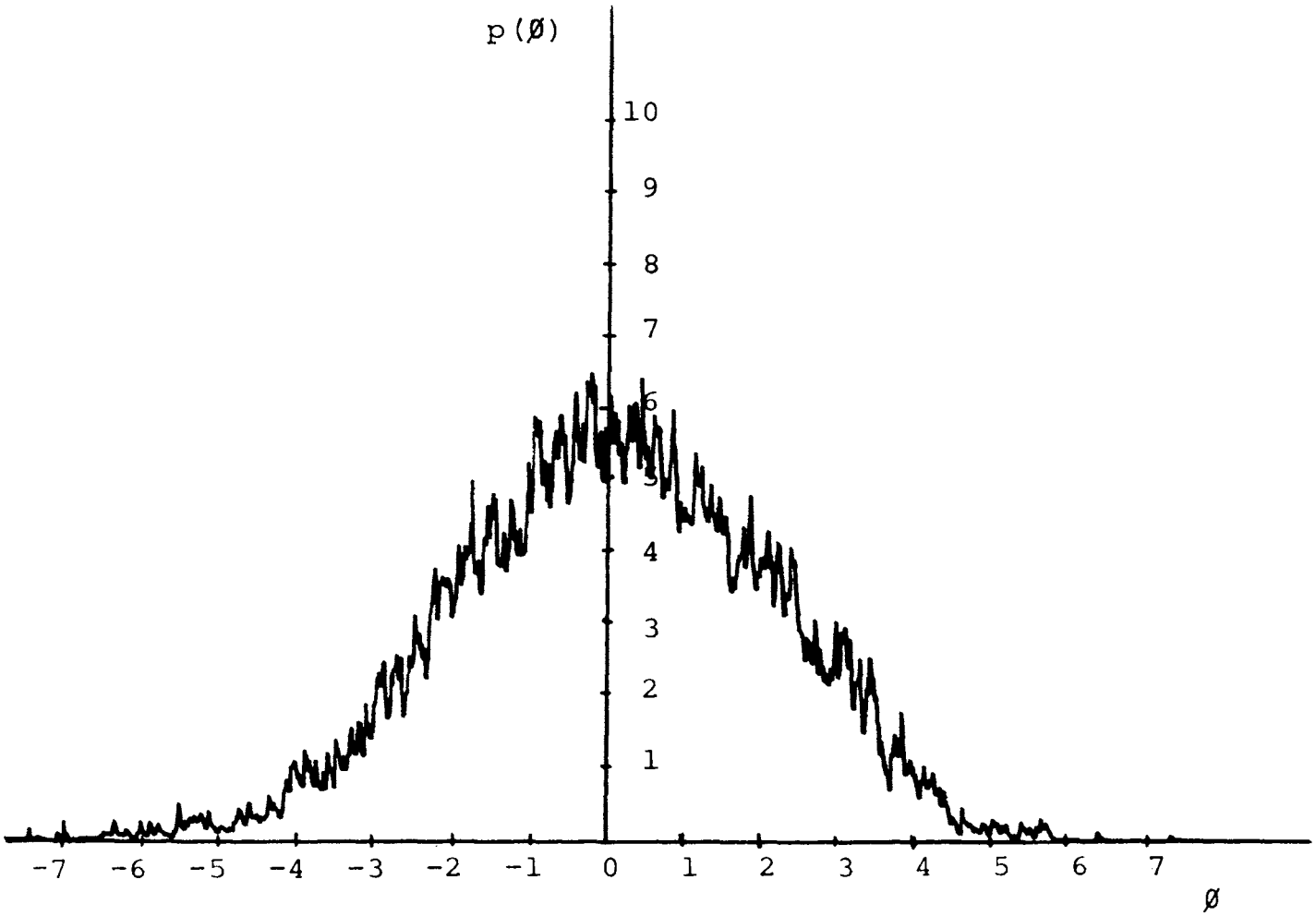
Calibration: Abscissa: 1 unit = 1.12 radians
Ordinate: 1 unit = .0548 rad^{-1}

Figure 8. Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3, m=1, SNR=19dB



Calibration: Abscissa: 1 unit = 1.12 radians
Ordinate: 1 unit = .0375 rad^{-1}

Figure 9: Probability Density Function of Phase Error; B_L=85Hz; ρ=0.3, m=1, SNR=19dB



Calibration: Abscissa: 1 unit = 1.12 radians
Ordinate: 1 unit = .0376 rad^{-1}

Figure 10. Probability Density Function of Phase Error; B_L=85Hz, ρ=0.3, m=0.2, SNR=25dB

where

$$z = \frac{A^2}{N_o B_L} = SNR, \tag{27}$$

$$\beta = B_L/B_i \ ,$$

N_o = Single sided power spectral density of the input noise,

and

B_i = Single-sided low pass bandwidth of the input noise (essentially the bandwidth of the inphase and quadrature phase channel filters in Fig. 2)

Eq. (26) is obtained under the assumption that the phase error ϕ is very small; thus, the loop can be linearized for the analysis.

Although there is significant difference between the values of the last two columns of Table I, we can make some observations in regard to the trend of the loop behavior when operated in the Costas, phase-lock or hybrid loop mode. When the modulation index is 1, the transmitted power is totally in the carrier. The loop operation is equivalent to a second-order phase-lock loop. Similarly, when the modulation index is 0.2, the transmitted power in the carrier is small and the loop operation is nearer to that of a Costas loop. When the modulation index is 0.5, the transmitted power is

TABLE I

TABULATION OF LOOP PHASE ERROR UNDER VARIOUS CONDITIONS

m	SNR,dB	σ_{ϕ},rad	σ_H, rad
1	25	0.89	.055
	19	0.716	.127
	17	0.97	.14
0.5	25	1.13	.075
	19	1.20	.159
	17	1.36	.224
0.2	25	1.77	.1

Summary of parameters and variables:

m = modulation index

ρ = 0.3 (defined by (25))

SNR = Signal-to-noise ratio, noise measured in a loop bandwidth (defined by (27))

σ_{ϕ} = Experimentally measured phase error standard deviation

σ_H = Theoretical phase error standard deviation (defined by (27))

distributed in the ratio of 1 to 3 between carrier and modulation components, and the loop is operating in a hybrid loop mode. When β is very small (of the order of 10^{-3}) and the SNR is high, the phase error standard deviation is maximum when the loop is operated in Costas loop mode, which was the case in the experiment. Under the same conditions of β and SNR, the phase error standard deviation of the hybrid loop has an intermediate value between that of the Costas and phase-lock loop.

The disagreement in the values of the last two columns of Table I can be attributed to the inaccuracy of the hybrid loop model employed and to experimental measurement error. In regard to model inaccuracy, Stewart assumed a first-order loop to derive the expression for σ_H^2 given in (27). Charles and Lindsey have shown that the analysis for first order loop will also hold good for a second order loop without much loss of accuracy. The jitter from various sources contributes to the phase error in addition to the noise added to the signal and was not included by Stewart in his analysis. These additional jitter sources consist of the source jitter, the VCO jitter and finally the Exclusive-OR phase detector jitter. The phase jitter in the input signal may be due to the source itself or may be introduced during the frequency translation process. Although the VCO phase jitter was minimized by using a regulated power supply, it was not

completely eliminated. The exclusive-OR phase detector jitter might be due to the nature of its two inputs.

The measurement errors include such errors as calibration errors of the phase detector and probability density analyzer, inaccuracy in determining signal and noise levels at the loop input, and inaccuracies in loop parameters.

Another factor influencing the error was the type of noise generator used. In the calculation it was assumed that the added noise to the input signal was white. This was not true in the experiment. The power spectral density of the additive noise was not flat beyond 600-700 kHz. Also, the bandpass filter following the noise generator did not have an ideal flat response, as was assumed in the calculation.

It is interesting to compare the ratios of the experimental and computed phase-error standard deviations at the lowest SNR employed (17dB). At this SNR it is probable that most of the phase error was due to the added noise. At an SNR of 17dB, these ratios are,

$$\frac{\sigma_H|_{m=1}}{\sigma_H|_{m=0.5}} = 0.625 \quad \text{and} \quad \frac{\sigma_\phi|_{m=1}}{\sigma_\phi|_{m=0.5}} = 0.715$$

respectively. This is a relative comparison of the theoretical and experimental phase error standard deviations rather than the absolute comparison given in Table I. It

is seen that the results compare more favorably on this basis.

CONCLUSIONS

An experimental model of hybrid phase-lock loop was built and was tested experimentally. There is disagreement between the theoretically computed values of phase error standard deviation and the values obtained experimentally. The difference in the values of the phase error standard deviations can be attributed to various errors of the experiment and also to the assumptions in the analysis. Attempts are being made to improve the hybrid loop built and to minimize the measurement errors.

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VITA

Srinivasa H.R. Raghavan was born on September 17, 1944 in Bangalore, India and received his primary and secondary education there. He received his Bachelor of Engineering Degree in Electrical Engineering and Master of Technology degree in Electronic Instrumentation in 1967 and 1969, respectively, from the Osmania University, India. From January 1969 to January 1971, he was a senior research fellow of the Council of Scientific and Industrial Research, in the Instrumentation Division of the National Aeronautical Laboratory, Bangalore, India.

He has been enrolled in the Graduate School of the University of Missouri-Rolla since January 1971.

Mr. Raghavan is a member of IEEE and the Instrument Society, Bangalore.

APPENDIX A

EXPERIMENTAL HYBRID LOOP COMPONENTS

a. Voltage Controlled Oscillator and 90^{o} Phase Shifter

The circuit diagram for this module is shown in Fig. 11. In order to minimize the dependence of VCO frequency upon power supply voltage a one stage positive voltage regulator is used. The negative feedback principle is used; namely, an error voltage generated by zener comparison of the output of the regulator is amplified and fed back as a correction signal. A 100μfd capacitor is used at the output of the regulator to reduce high frequency noise and transients. The zener used in the regulator has a value of 6.2 volts.

The voltage controlled oscillator consists of an astable multivibrator whose frequency is controlled by changing the charging current on the two cross-coupling capacitors by the input voltage. Potentiometers p_1 and p_2 are used to control the sensitivity of the VCO (voltage to frequency conversion rate) and the waveform symmetry. The VCO collectors are clamped to the 5 volts zener level by a pair of diodes to improve the frequency stability by establishing a firm logic level.

The outputs from the two collectors of the astable multivibrator are fed to two bistable multivibrators.

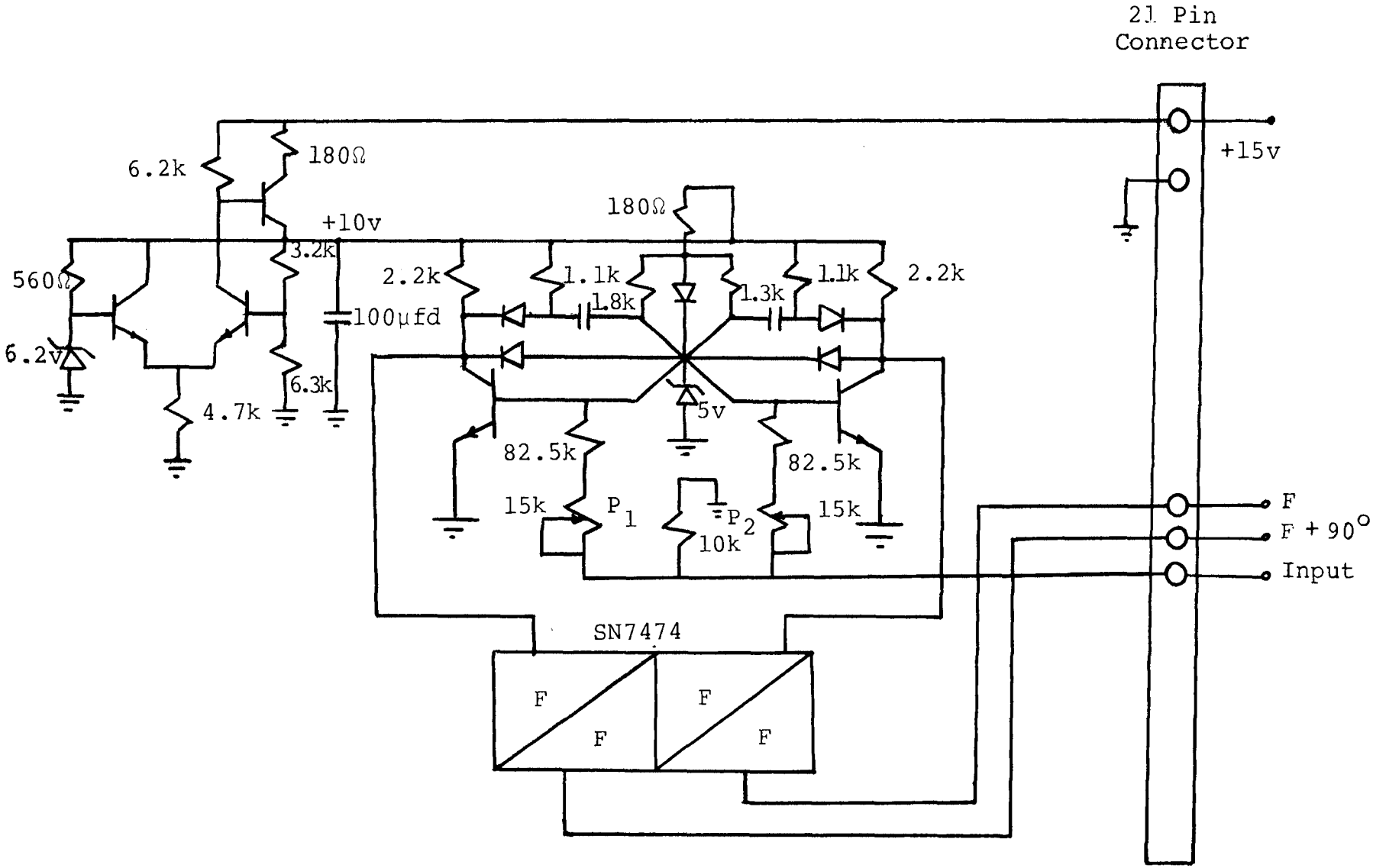

Figure 11. Voltage Controlled Oscillator

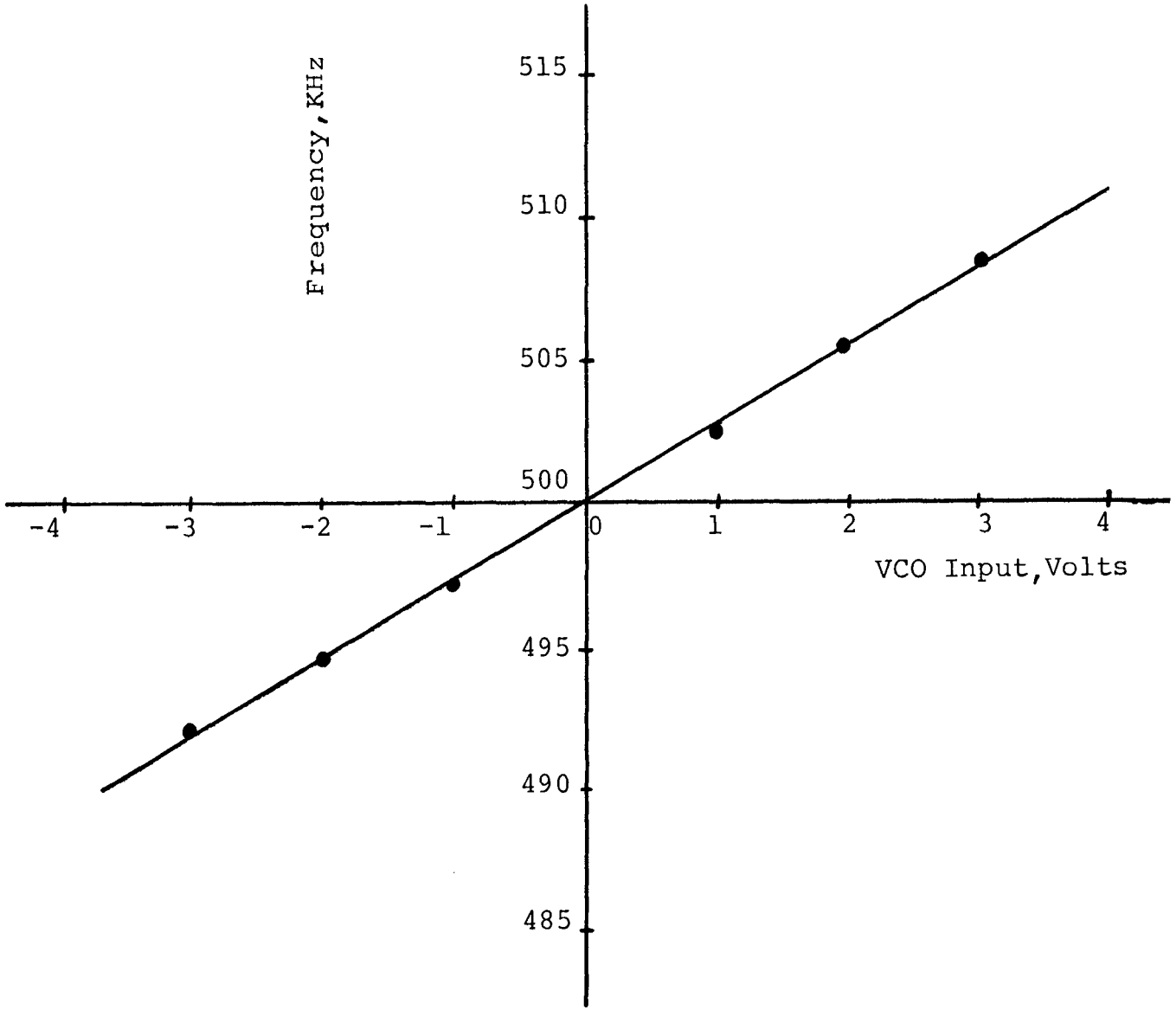

Figure 12. VCO Characteristic

Here IC chip-SN7474 which has two flip-flops triggered by positive going edges of the input waveform is used. As the inputs to the two flip-flops are 180^{o} out of phase and as the flip-flops are triggered by the positive rising edge of the inputs, phase quadrature between the outputs of the two flip-flops is established. These signals are used as the reference inputs to the phase detectors of the hybrid loop.

b. Phase Detector

Multipliers M1 and M2 (Intronics Multipliers, Type M410) together with the outerloop filters G(p) form the phase detectors for the Costas loop and M1 in conjunction with F(p) form the phase detector for phase-lock loop (see Figures 13 and 14 for wiring diagrams). Filters G(p) are band pass filters with upper cut-off frequency at 16 kHz and lower cut-off frequency at 0.4 Hz. These phase detectors have a linear characteristic from zero to 180^{o} ($90^{o} \pm 90^{o}$) and have a gain constant of 1/10.

c. Adder, Loop Filter and Inverter

Three Intronic (Type A101) operational amplifiers (see Fig. 15) are used for adder, loop filter and inverter. Band switches B_1 and B_2 are provided to select loop bandwidth of 8.5Hz, 85Hz, 850Hz, and 8.5kHz. Potentiometers P_1 and P_2 are provided to adjust the phase-lock

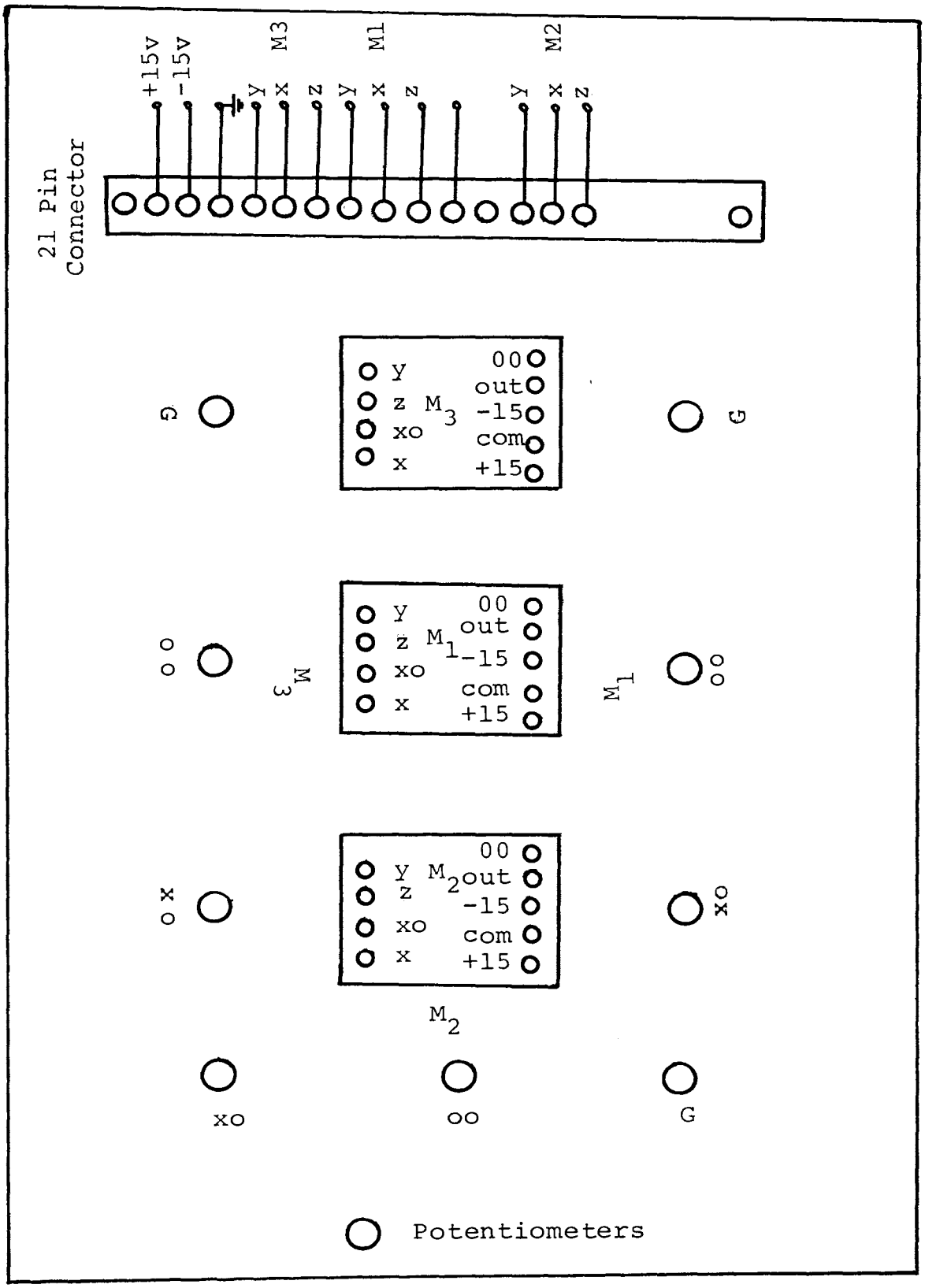

Figure 13. Phase Detectors

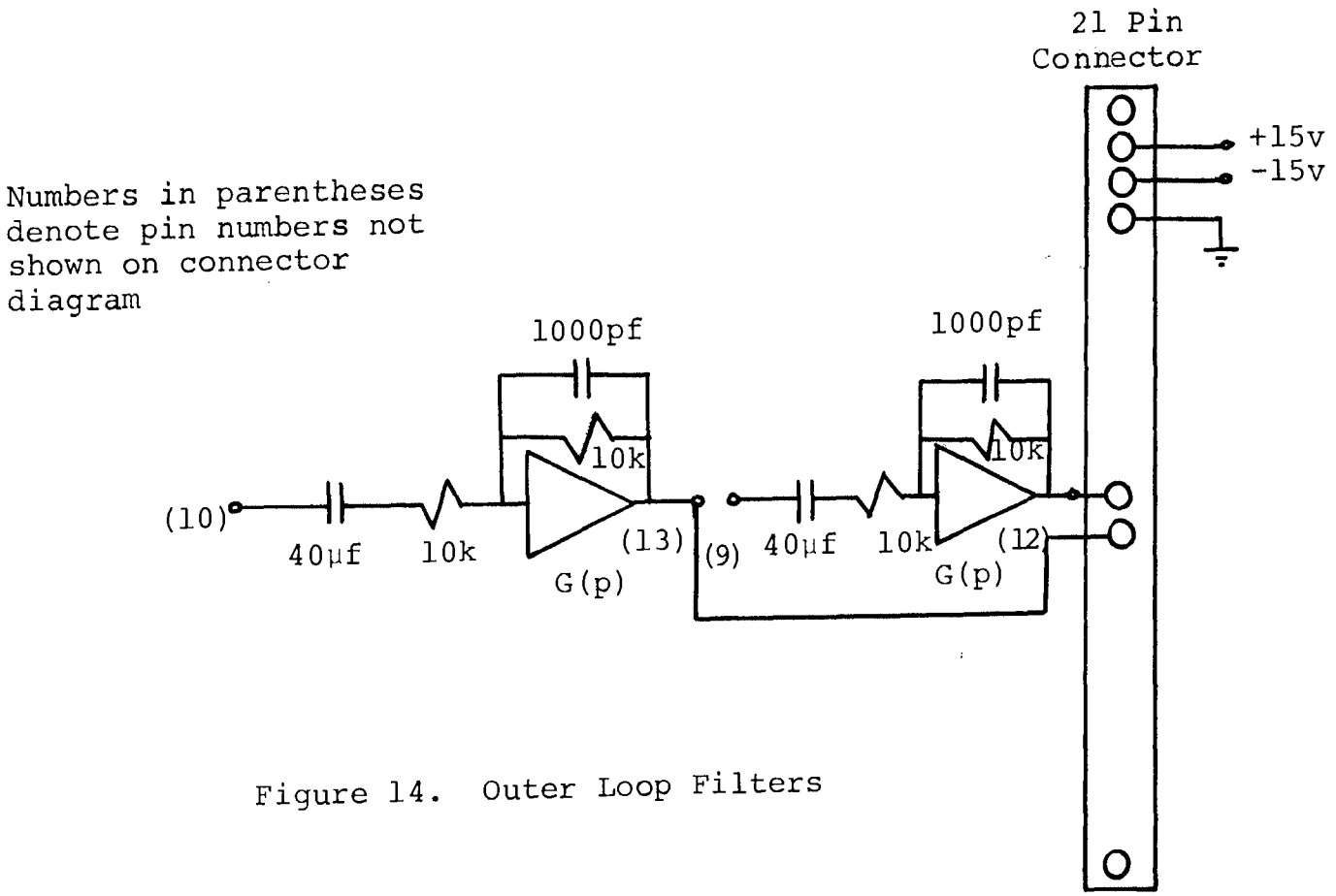

Figure 14. Outer Loop Filters

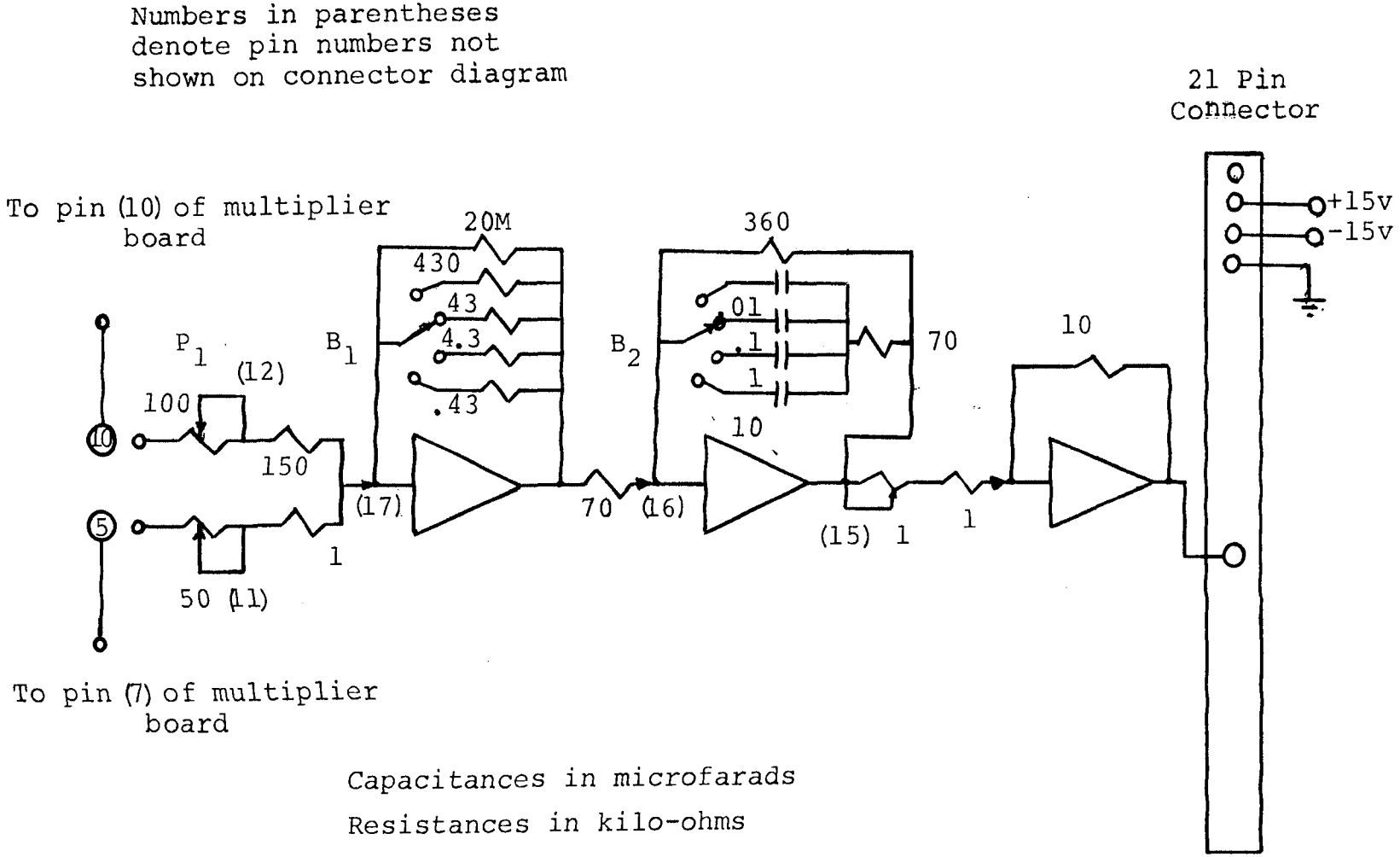

Figure 15. Adder, Loop Filter and Inverter

loop gain a_1 and Costas loop gain a_2 to the required value. With different settings of these two potentiometers, we obtain different values of ρ, which is proportional to the ratio of a_2 to a_1. The loop filter used here has a transfer function of the form

$$F(p) = \frac{p+a}{p+\varepsilon}$$

where a is the filter time constant and ε is the filter imperfection factor. In Table II the values of loop bandwidth, and damping factor ξ for various positions of B_1, B_2, P_1 and P_2 are shown.

APPENDIX B

DESIGN EXAMPLE

A damping factor of 0.707 and loop band-width of 850Hz are chosen in the following design example.

(i) Let $\varepsilon/G_o = 0.1$

then,

$$B_L = \frac{G_o + a}{4(1+\varepsilon/G_o)}$$

$$= \frac{G_o+a}{4.4}$$

(ii) Calculation of a/G_o

$$\sqrt{2a/G_o} = 1 + \varepsilon/G_o = 1.1$$

Therefore, $a/G_o = 0.605$

(iii) Calculation of G_o

$$G_o = \frac{4\sqrt{2a/G_o}}{1+a/G_o} \; B_L$$

$$= \frac{4 \times 1.1}{1.605}$$

$$= 2740$$

(iv) Determination of loop filter time constants.

$$a = 0.605\ G_o = 1660$$

$$\varepsilon = 0.1\ G_o = 274$$

Now, $F(p) = K_3 \frac{p+a}{p+\varepsilon}$

where, $K_3 = R_3/R_1 \cdot R_2/R_2+R_3$

$$a = 1/R_2C \quad \text{and} \quad \varepsilon = \frac{1}{(R_2+R_3)C} \ .$$

Let $C = 0.01\mu fd$

Then, $R_2 = 1/aC$

$$= \frac{10^7}{1660} = 60k$$

$$R_2 + R_3 = \frac{10^7}{274}$$

$$= 365k$$

$$R_3 = 305k$$

$$R_1 = 60k$$

so that k_3 is nearly unity.

(v) Computation of gains a_1 and a_2

$$G_o = k_v k_3\ a_1 k_o k_1 A\ [m+\rho(1-m^2)]$$

Let $m = 1/2$

$\rho = 0.66$

$k_o = 1/10$

(approximately for optimum operation as obtained from Stewart [5])

$$k_1 A = 3$$

$$m+\rho(1-m^2)=1 \qquad \text{(approximate relation for optimized operation)}$$

Therefore,

$$a_1 = \frac{2740 \times 0.83}{2.2\text{x}10^4\text{x}1/10\text{x}3}$$

$$= 0.357$$

$$a_2 = \frac{0.66 \times 0.357}{1/100 \times 3}$$

$$= 7.6$$

Similarly the values for other loop bandwidths are calculated and they are tabulated in Table 2.

TABLE II

SUMMARY OF LOOP COMPONENT VALUES

ε	C	a	Total Gain	R		a_1	a_2	G_o	B_L	ξ
2300	0.001μF	14300	43	450	MAX	.003	.45	23.2	35Hz	2
					MIN	.0018	.009	14.0	21.6Hz	2.6
				4.5k	MAX	.03	4.5	232	330Hz	0.695
					MIN	.018	.09	140	310Hz	0.86
				45k	MAX	.3	4	2320	2.08kHz	0.4
					MIN	.18	.9	1400	1.58kHz	0.415
				450k	MAX	3	450	23200	8.5kHz	.702
					MIN	1.8	9	14000	6.1kHz	.575
230	0.01μF	1430	4.3	450	MAX	.003	.45	2.32	3.5Hz	2
					MIN	.0018	.009	1.40	2.16Hz	2.6
				4.5k	MAX	.03	4.5	23.2	33Hz	0.695
					MIN	.018	.09	14.0	31Hz	0.86
				45k	MAX	0.3	45	232	208Hz	0.4
					MIN	0.18	.9	140	158Hz	0.415
				450k	MAX	3	450	2320	850Hz	.702
					MIN	1.8	9	1400	610Hz	.575
23	0.1μF	143	4.3	450	MAX	.003	.45	2.32		
					MIN	.0018	.009	1.4		
				4.5k	MAX	.03	4.5	23.2	8.5Hz	.4
					MIN	.018	.09	14.0	6.1Hz	.415
				45k	MAX	.3	45	232	85Hz	.702
					MIN	.18	.9	140	61Hz	.575
				450k	MAX	3	450	2320	616Hz	2.04
					MIN	1.8	9	1400	386Hz	1.58
2.3	1μF	14.3	4.3	450	MAX	.003	.45	2.32		
					MIN	.0018	.009	1.4		
				4.5k	MAX	.03	4.5	23.2	8.5Hz	.702
					MIN	.018	.09	14.0	6.1Hz	.575
				45k	MAX	.3	45	232	58Hz	2
					MIN	.18	0.9	140	35Hz	5
				450k	MAX	3	450	2320		
					MIN	1.8	9	1400		

$0.05 \leq \rho \leq 2.5$

APPENDIX C
PHASE ERROR PROBABILITY DENSITY MEASUREMENT

A block schematic of the set up used to measure the phase error density is given in Figure 16. Noise from the noise generator is passed through the band pass filter with equivalent noise bandwidth B; the output of the BPF is added to the received signal which then is the input to the hybrid loop under test. The unmodulated reference from the source is hard limited in two stages of amplification, and then used as a reference input to the phase detector. The voltage controlled oscillator output, whose phase is to be compared with that of the reference, is the second input to the phase detector.

The phase detector itself consists of two flip-flops and four nand gates. Flip-flops are used for further wave shaping of the VCO output and the reference signal as well as to double the range of the phase detector. The four nand gates are connected to form an exclusive-OR gate which functions as the phase detector. The squarer and the phase detector used are shown in Figure 17.

The high frequency components of the phase detector output are removed by a low-pass filter which is sufficiently wideband to pass the phase error undistorted and then given to the probability density analyzer. The output of the probability density analyzer is recorded with the help of

an XY Plotter and the resulting phase-error probability plots are shown in Figures 4-10. Figures 4-10 were obtained with the loop bandwidth set at 85Hz, input signal level at 0.6v rms, PLL gain a_1 at 0.3, Costas loop gain a_2 at 11 (resulting ρ is 0.3) and the total gain at 4.3. The corresponding settings with respect to Fig. 2 were, band-switches B_1 and B_2 at position 2, potentiometer P_1 at 0, potentiometer P_2 at 3.10 and P_3 at 9.50.

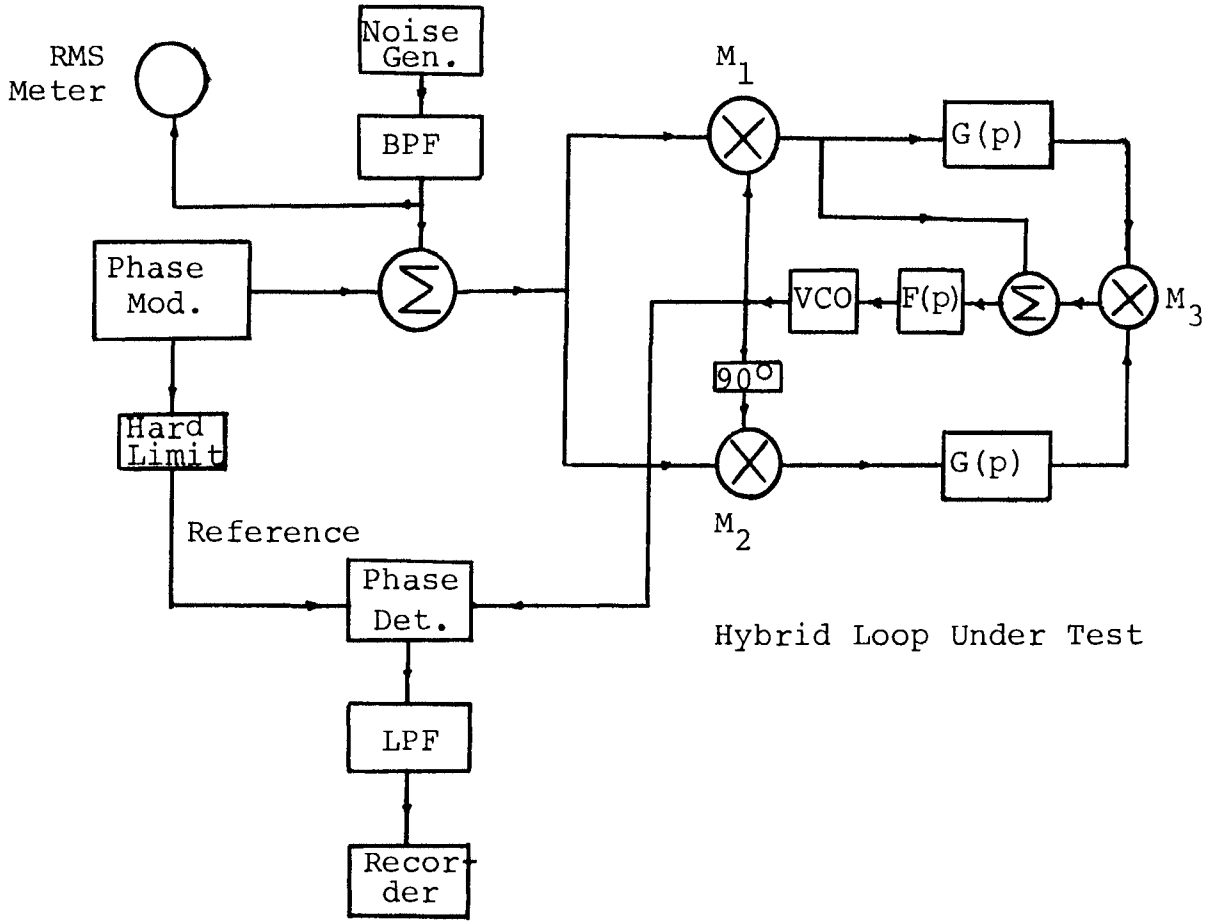

Figure 16. Experimental Set Up for Measurement of Phase Error Probability Density

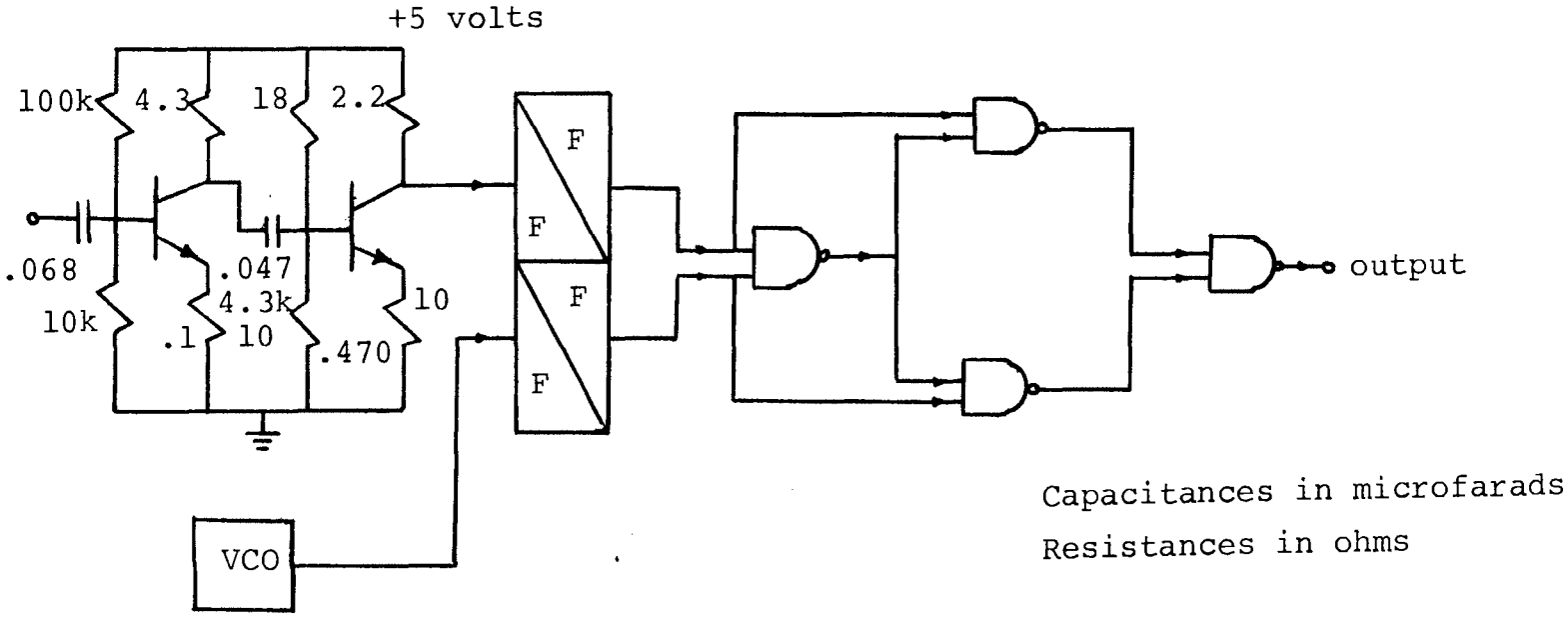

Figure 17. Exclusive-OR Phase Detector

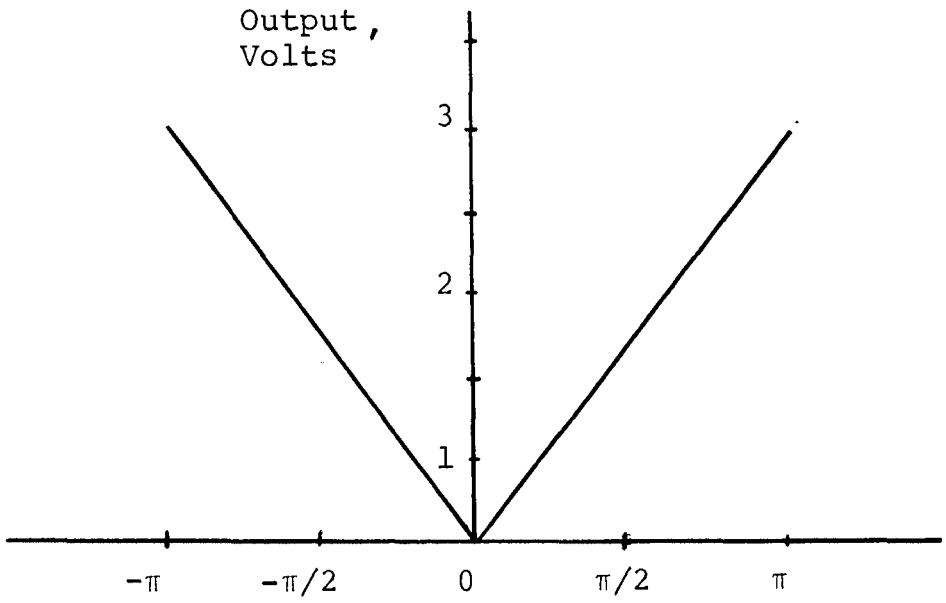

Figure 18. Exclusive-OR Phase Detector Characteristic