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A computer approach to transistor circuit design

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A Computer Approach to Transistor Circuit Design

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A

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ABSTRACT

The design of amplifiers is usually approached through experimental study. This thesis proposes a mathematical approach, using a digital computer to predict the performance of an active transistor circuit (a frequency equalizer circuit to compensate for the RIAA[1] recording frequency characteristics) prior to the actual construction of the physical system. The simple but powerful computer analysis method will be based upon the nodal equations of the complete circuit. The primary aim is to design a circuit which would give a desired frequency-gain characteristic. The complete set of simultaneous complex nodal equations describing the circuit operation is then written. Based on these equations, the IBM 1620 digital computer is programmed to pick up the transistor "y" parameters and solve the complex elements of the matrix at each frequency. The gain, phase shift, input and output impedances are then determined. The theoretical results are compared with results obtained in the laboratory.

Background material relevant to the problem is reviewed. Suggestions for additional developement and improvement of the circuit are proposed.

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LIST OF SYMBOLS

$\bar{A}$ – amplification (complex notation).

B, b – base electrode.

C, c – collector electrode.

E, e – emitter electrode.

$f_{\alpha b}$ – small-signal short-circuit forward current transfer ratio cutoff frequency (common base).

$f_{\alpha e}$ – small-signal short-circuit forward current transfer ratio cutoff frequency (common emitter).

h_{FB} – static value of the forward current transfer ratio (common base).

h_{fb} – small-signal short-circuit forward current transfer ratio (common base).

h_{FE} – static value of the forward current transfer ratio (common emitter).

h_{fe} – small-signal short-circuit forward current transfer ratio (common emitter).

h_{ib} – small-signal value of the short-circuit input impedance (common base).

h_{ie} – small-signal value of the short-circuit input impedance (common emitter).

h_{ob} – small-signal value of the open-circuit output admittance (common base).

h_{oe} – small-signal value of the open-circuit output admittance (common emitter).

h_{rb} – small-signal value of the open-circuit reverse voltage transfer ratio (common base).

h_{re} – small-signal value of the open-circuit reverse voltage transfer ratio (common emitter).

I_B – base current (dc).

I_c – collector current (dc).

I_E – emitter current. (dc)

I_{CBO} - collector cutoff current (dc) emitter open.

P_{dc} - total power input (dc) to all electrodes.

R_E - external emitter resistance.

R_c - external collector load resistance.

V_{BE} - base to emitter voltage (dc).

V_{cc} - collector supply voltage (dc).

V_{CE} - collector to emitter voltage (dc).

V_{EE} - emitter supply voltage (dc).

y_{ie} - small-signal input admittance for a.c. short-circuited output.

y_{re} - small-signal reverse transfer admittance for a.c. short-circuited input.

y_{fe} - small-signal forward transfer admittance for a.c. short-circuited output.

y_{oe} - small-signal output admittance for a.c. short-circuited input.

$\bar{\beta}$ - feedback factor (complex notation).

ABBREVIATIONS

db - decibels.

cps - cycles per second.

kc - kilocycles per second.

Mc - megacycles per second.

RIAA - Recording Industries Association of America.

EIA - Electronic Industries Association.

CHAPTER I

(A) INTRODUCTION

The use of the digital computer in solving engineering problems is becoming widely accepted. The advantages of this electronic device, however, are being exploited more effectively by engineers outside the electronics field. One explanation for the relative lag in the application of the digital computer to electronic circuit design is the fact that a large amount of data can be obtained easily, quickly and inexpensively through experimental study. The computer is very useful where time and expense are involved, and where it is not feasible to simulate a scaled model for experimental study.

The future trend of electronic circuits is towards microminature, modular and integrated circuits. In this field, it is essential that the performance of the circuit be predictable prior to the construction of the physical system because of the high cost of fabrication. With this in mind, this thesis proposes a computer approach to an electronic circuit design. It is not the intention here to design a circuit that would meet the exact specifications of the RIAA playback curve to very close tolerances. The investigation here serves two purposes:

(i) To illustrate the design calculations involved and the ready facility of the digital computer to perform innumerable arithmetic operations at high speed and without mistakes;

(ii) To investigate the accuracy of our transistor model and the validity of the basic assumptions made in the formulation of the equivalent circuit.

The design is viewed from a practical standpoint, with emphasis on economy, simplicity and the availability of components.

(B) REVIEW OF LITERATURE

The few applications of digital computers to electronic circuit design found in literature[2,3] refer mainly to network synthesis and switching circuits and seldom in audio work. Brinkerhoff[4] was perhaps the first to use the computer for transistor circuit calculations. In a paper presented to the International I.R.E. Convention in 1960, he showed how the digital computer can be effectively employed to solve the equations of a transistorized output stage.

In June, 1964, Purnhagen and Lubelfeld[5] approached the problem of laser design using a computer. Based on a mathematical model, the equations which relate the subefficiencies to physically measurable parameters were derived. Their results were in general agreement with known theoretical and experimental properties of the pulsed four-level laser.

Lately, Drew and Atwood[6] successfully analysed an integrated circuit with simulated parasitic elements with the use of a computer. They offered some good suggestions on the general approach to the simulation problem.

This concludes the review of literature for the moment. In the interest of preserving coherence, more background information will be provided during the development of the different phases of the design.

(C) DESIGN CONSIDERATIONS

For various reasons which will not be discussed in detail, a non-linear recording velocity versus frequency characteristic is employed in disc recording. To ensure flat overall frequency response, this recording characteristic has to be compensated by a special unit known as a frequency equalizer in the reproducing system. Thus a frequency equalizer has to perform two different functions: First, it has to amplify to a suitable level the very small voltages delivered by the cartridge of a record player; second, it has to provide the correct playback frequency response to compensate for the recording characteristic. Since the RIAA recording characteristic is standard in disc recording, the equalizer is designed to feature the RIAA playback curve. However, it must be pointed out that the RIAA playback curve is not the only standard used in disc recording. There are numerous other recording companies which do not use this frequency characteristic in disc recording although their playback curves do not deviate appreciably from the RIAA standard.

The equalizer uses a standard circuit and features two amplifying stages using identical transistors. The required

voltage gain of 30 db at 1000 cps could easily be realized by a single transistor stage. However, to meet the additional requirements concerning frequency response, distortion and impedance levels, two stages are needed. To obtain high voltage gain, all stages are operated in the common-emitter configuration, although the transistor cutoff frequency is relatively low in this configuration. For reasons of stability as well as good low frequency response, the two stages are directly coupled. Operating points are stabilized against changes in transistor parameters, supply voltage and temperature by means of local and series negative feedback. The desired frequency response is achieved by means of a frequency dependent feedback loop. The use of large degrees of negative feedback further provides for high stability of performance characteristics, low distortion and proper impedance levels.

Most high quality cartridges have an internal resistance from 500 to 1000 ohms and an output voltage of the order of 5 to 10 mv. at a stylus velocity of 5.5 cm/sec. The input impedance of the equalizer should be as high as possible to avoid loading the cartridge of the record player.

Noise generated in a transistor amplifier normally consists of hum introduced by inadequate filtering of the supply voltage, thermal noise generated in the ohmic resistances and transistor noise. Thermal noise in resistors cannot be avoided but it can be minimized by the use of high stability carbon resistors or metal film resistors. Negative feedback

is not effective in reducing transistor noise. By using low-noise transistors specially designed for use in audio preamplifiers, and operating them at suitable operating points, the transistor noise level can be kept to a minimum.

The specifications which the frequency equalizer is expected to meet are:

(1) A voltage gain of 30 db at the reference frequency of 1000 cps.

(2) A frequency response to follow the RIAA playback curve with maximum tolerable deviations of $\pm$ 3 db at frequencies below 50 cps and $\pm$ 1 db within the rest of the frequency range.

CHAPTER II

SYNTHESIS OF THE FREQUENCY SENSITIVE NETWORK

The voltage gain of an amplifier with negative feedback is given by:

$$A_{vf} = \frac{\bar{A}}{1 + \bar{\beta}\bar{A}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1a)$$

where

$\bar{A}$ = voltage gain of the amplifier without feedback.

$\bar{\beta}$ = fraction of output voltage fed back into the input.

for $\bar{\beta}\bar{A} \gg 1$,

$$\bar{A}_{vf} = \frac{1}{\bar{\beta}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1b)$$

Equation (1b) signifies that for large values of $\bar{A}$, the overall voltage transmittance is independent of the amplification of the internal amplifier and is dependent on the transmission characteristics of the feedback network. Use is made of this property to design the frequency dependent feedback network.

The required frequency response of the equalizer is achieved by means of a negative feedback loop. Since a passive linear feedback network, incapable of inverting phase is to be used, the necessary 180^{o} phase shift is obtained by taking the feedback signal from the collector of stage 2 and feeding it back to the emitter lead of stage 1 as shown in Fig. 1.

To derive an expression for the voltage amplification of this circuit, it is assumed that the base current of the first stage is negligible compared to the collector current. The equations are:

$$v_i = v' + (i_c + i_f) R_{E1} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

$$v_o = (i_c + i_f) R_{E1} + i_f \bar{Z}_f \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

$$v_o = A_{v2}\left[A_{v1} v' - (i_c + i_f) R_{E1} \right] \quad \ldots\ldots\ldots\ldots \quad (4)$$

$$v_o = A_{v2}\, i_c\, R_{i2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

The solution of equations (2), (3), (4) and (5) for the ratio of the terminal voltages gives

$$A_{vf} = \frac{v_o}{v_i} = \frac{A_{v1} A_{v2}}{R_{E1}\left[A_{v1} A_{v2} R_{i2} + A_{v2} R_{i2} + (A_{v1} + 1)\bar{Z}_f\right] + R_{i2}(R_{E1} + \bar{Z}_f)} \quad \ldots\ldots\ldots\ldots \quad (6a)$$

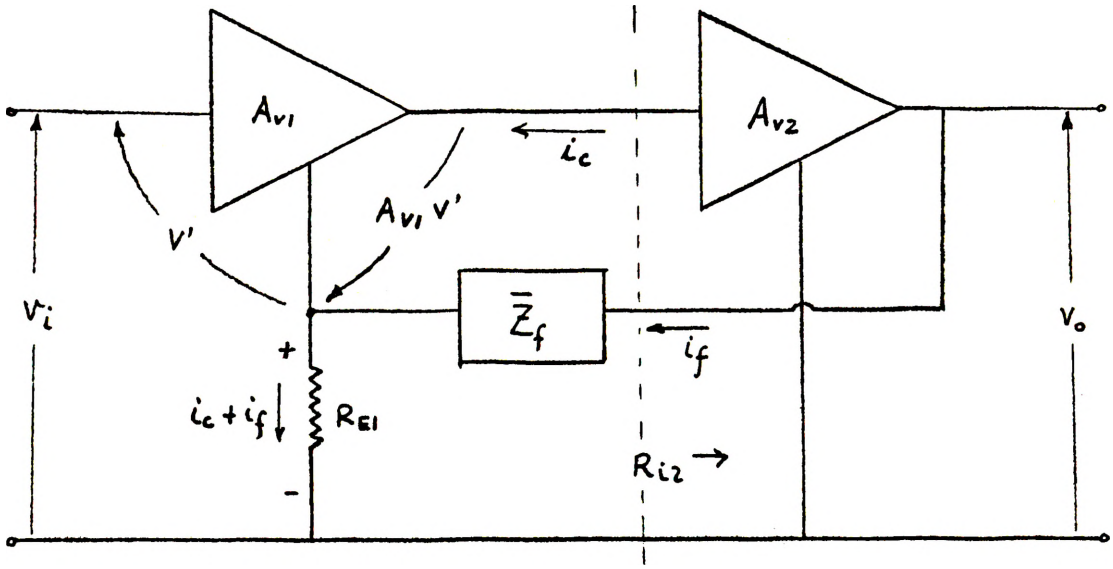


Fig. 1. Frequency sensitive feedback arrangement.

Dividing equation (6a) by $R_{i2}(R_{E1} + \bar{Z}_f)$ gives

$$A_{vf} = \frac{A_{v1} A_{v2}}{A_{v1} A_{v2} \frac{R_{E1}}{R_{E1} + \bar{Z}_f} + \frac{A_{v2} R_{E1}}{R_{E1} + \bar{Z}_f} + \frac{(A_{v1} + 1)\bar{Z}_f}{R_{i2}(R_{E1} + \bar{Z}_f)} + 1} \quad \ldots\ldots\ldots\ldots\ldots \quad (6b)$$

Considering the relative orders of magnitude, equation (6b) reduces to

$$A_{vf} \approx \frac{A_{v1} A_{v2}}{1 + \frac{R_{E1}}{R_{E1} + \bar{Z}_f} A_{v1} A_{v2}} \quad \ldots\ldots\ldots\ldots\ldots \quad (7)$$

Comparing equation (7) with equation (1a), it is seen that

$$\bar{\beta} \approx \frac{R_{E1}}{R_{E1} + \bar{Z}_f}$$

$$\approx \frac{R_{E1}}{\bar{Z}_f} \quad , \quad \text{for} \quad \bar{Z}_f \gg R_{E1}$$

Hence for large values of $\bar{A}$, since R_{E1} is frequency independent, the desired RIAA frequency response can be realized by a suitable design of the feedback network.

Consider the frequency-gain characteristics of the RIAA playback curve as shown in Fig. 2. The curve requires a low frequency boost of 6 db per octave from 500 cps down to 50 cps and a high frequency roll off starting at 2120 cps. The RIAA curve is seen to be well approximated by curve 1 (dotted). This assymptotic approximation method has come to be known as "breakpoint approximation" and is due to Bode.[7] Given this curve, the problem is to find an expression for a network function as a quotient of polynomials in s which has a

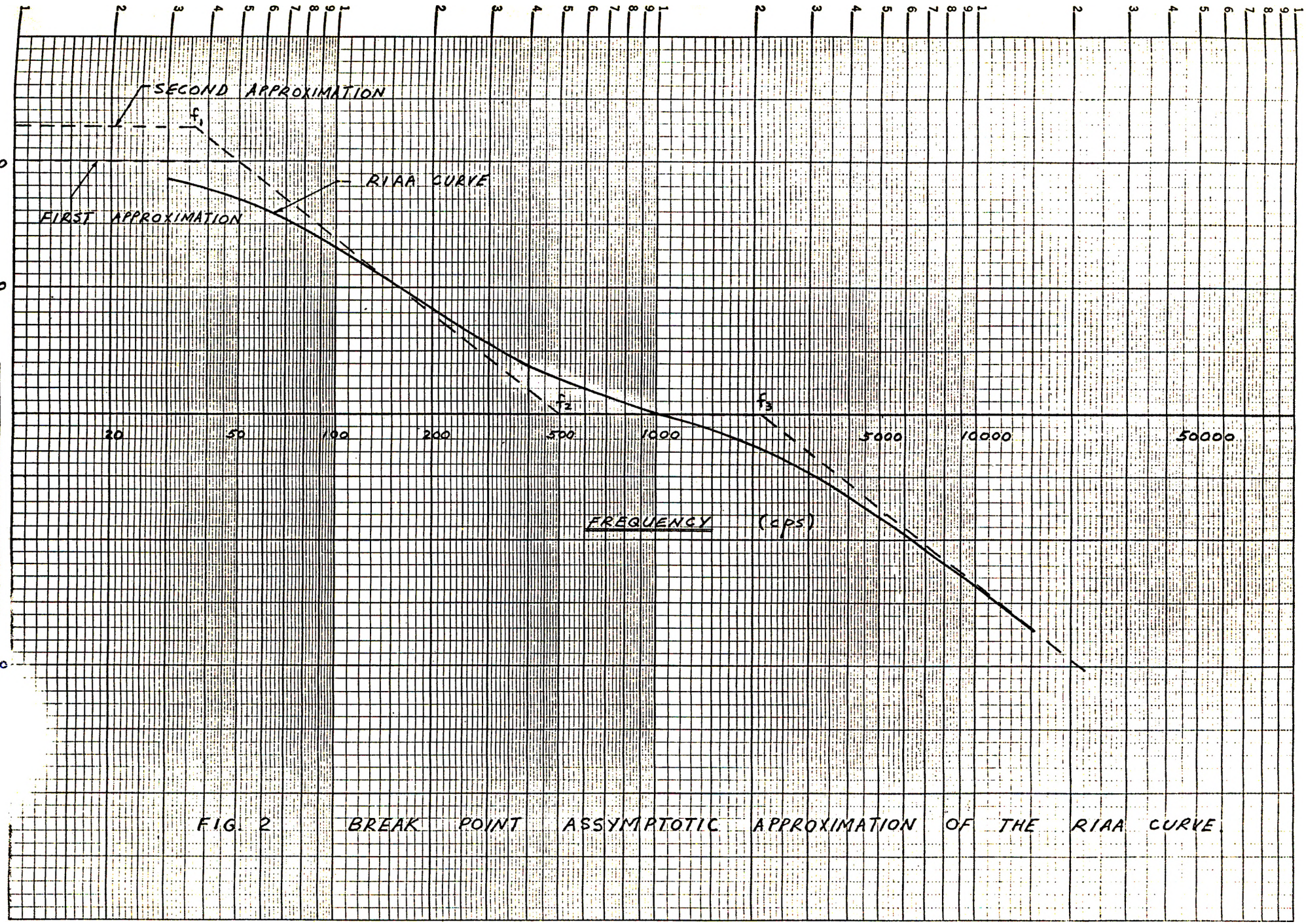


FIG. 2 BREAK POINT ASSYMPTOTIC APPROXIMATION OF THE RIAA CURVE.

magnitude approximating the curve to within an acceptable tolerance.

Since only 6 db per octave slopes are required, $Z_f(s)$ can be realized by a relatively simple RC network. The time constants of the RC network are determined by the 3 break frequencies:

$$T_1 = \frac{1}{2\pi f_1}$$

$$T_2 = \frac{1}{2\pi f_2}$$

$$T_3 = \frac{1}{2\pi f_3}$$

From consideration of the break points, T_1 and T_3 correspond to poles in the network function and T_2 corresponds to a zero. The log-log assymptotic dotted curve is easily seen to be represented by the expression:

$$Z_f(s) = \frac{K\ (T_2 s + 1)}{(T_1 s + 1)\ (T_3 s + 1)} \quad \ldots\ldots\ldots \quad (8a)$$

where K is a constant. The value of K controls the degree of feedback for a given value of emitter resistance R_{E1}. In this design, the degree of feedback is controlled by choosing a suitable value of R_{E1} and the value of K is chosen so that the components which form the network are readily obtainable commercially.

From equation (14a),

$$Z_f(s) = \frac{K\ T_1\ T_3\ (s + \frac{1}{T_2})}{T_2\ (s + \frac{1}{T_1})\ (s + \frac{1}{T_3})} \quad \ldots\ldots\ldots \quad (8b)$$

Using partial fractions,

$$Z_f(s) = \frac{K_1}{(s + \frac{1}{T_1})} + \frac{K_2}{(s + \frac{1}{T_3})}$$

$$= \frac{1}{(\frac{s}{K_1} + \frac{1}{T_1 K_1})} + \frac{1}{(\frac{s}{K_2} + \frac{1}{T_3 K_2})}$$

$$= \frac{1}{(\frac{s}{K_1} + \frac{2\pi f_1}{K_1})} + \frac{1}{(\frac{s}{K_2} + \frac{2\pi f_3}{K_2})} \quad \ldots \quad (8c)$$

Equation (8c) shows that the impedance function $Z_f(s)$ can be realized by an RC network as shown in Fig. 3.

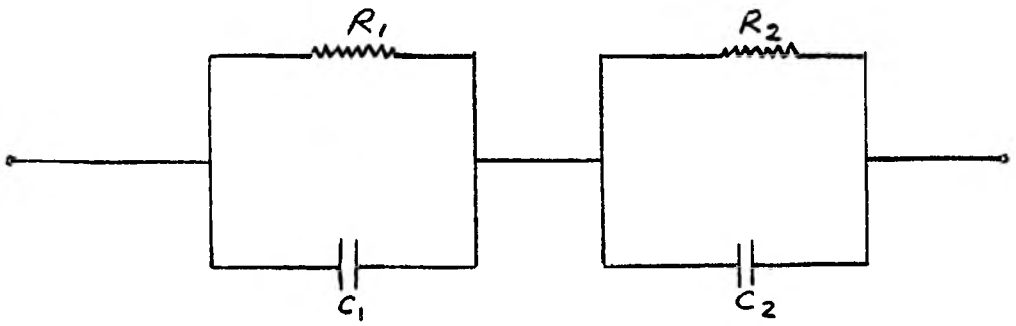


Fig. 3. The RC feedback network.

The values of the components are given by:

$$R_1 = \frac{K_1}{2\pi f_1} \quad \ldots \quad (9)$$

$$C_1 = \frac{1}{K_1} \quad \ldots \quad (10)$$

$$R_2 = \frac{K_2}{2\pi f_3} \quad \ldots \quad (11)$$

$$C_2 = \frac{1}{K_2} \quad \ldots \quad (12)$$

Referring again to Fig. 2, it appears that the first approximation is the best. This curve has break frequencies at 50 cps, 500 cps, and 2120 cps. However, with a network synthesized from this, the computer predicts that the response will be about 2.5 db down at 50 cps. This was subsequently verified in the laboratory.

To increase the response at low frequencies, curve 2 (dotted) is drawn with break frequencies at 36 cps, 500 cps, and 2120 cps.

Substituting $f_1 = 36$ cps, $f_2 = 500$ cps, and $f_3 = 2120$ cps into equation (14b) gives

$$Z_f(s) = \frac{K \quad 960 \quad (s + 1000\pi)}{(s + 72\pi) \quad (s + 4240\pi)}$$

$$K_1 = \frac{K \quad 960 \quad (s + 1000\pi)}{(s + 4240\pi)} \Bigg| \quad s = -72\pi$$

$$= \underline{\underline{214 \; K}}$$

$$K_2 = \frac{K \quad 960 \quad (s + 1000\pi)}{(s + 72\pi)} \Bigg| \quad s = -4240\pi$$

$$= \underline{\underline{746 \; K}}$$

Substituting for K_1 and K_2 into equations (9), (10), (11) and (12) gives

$$R_1 = \frac{K_1}{2\pi f_1} = \frac{K_1}{72\pi}$$

$$= \underline{\underline{0.945 \; K \quad \text{(ohms)}}}$$

$$C_1 = \frac{1}{K_1}$$

$$= \underline{\underline{\frac{4.67 \times 10^{-3}}{K} \quad \text{(farads)}}}$$

$$R_2 = \frac{K_2}{2\pi f_3} = \frac{K_2}{\pi 4240}$$

$$= \underline{5.6 \times 10^{-2} \; K \quad \text{(ohms)}}$$

$$C_2 = \frac{1}{K_2}$$

$$= \underline{\frac{1.34}{K} \times 10^{-3} \quad \text{(farads)}}$$

Let $K = 100 \times 10^3$, then

$R_1 = 94.5 \; K\Omega$

$C_1 = 0.0467 \; \mu F$

$R_2 = 5.6 \; K\Omega$

$C_2 = 0.0134 \; \mu F$

Choosing the nearest EIA standards,

$R_1 = 100 \; K\Omega$

$R_2 = 5.1 \; K\Omega$

$C_1 = 0.047 \; \mu F$

$C_2 = 0.015 \; \mu F$

CHAPTER III

SELECTION OF OPERATING POINTS AND CIRCUIT COMPONENTS

The selection of the operating point of a transistor audio-frequency amplifier stage has a great influence upon the useful collector-voltage swing, distortion and noise level. Any uncontrolled change in the operating point has to be avoided since it directly influences the performance characteristics of the stage. Once a suitable operating point has been selected, it has to be stabilized to be essentially independent of transistor parameter tolerances (especially of variations in the current transfer ratio), temperature and supply-voltage variations.

One of the most effective and convenient methods to achieve d.c. stabilization in a common-emitter stage is the insertion of a resistor in the emitter lead as shown in Fig. 4. The resulting negative d.c. series feedback stabilizes the operating point of the stage against changes in transistor parameters, temperature and supply voltage. For optimum stability, the emitter resistor should be made as large as possible. However, too high a value requires an impracticably high supply voltage. Normally, a compromise has to be made between stability requirements and supply voltage facilities.

In this design, both stages are operated in the common-emitter connection; they are directly coupled for optimum low frequency response and good d.c. stability. Operating

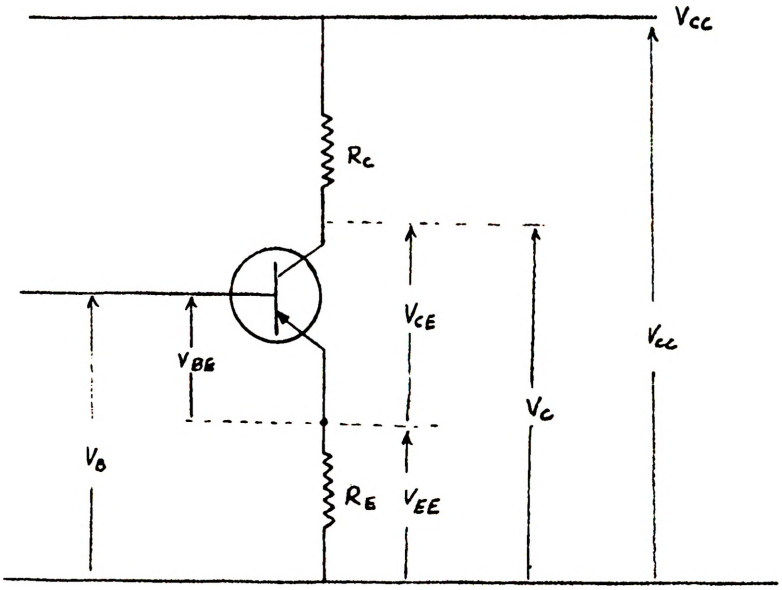


Fig. 4. Simplified circuit of a common emitter stage with series feedback.

point stability of the individual stages is achieved by emitter resistors, and a d.c. negative-feedback loop around the first two stages ensures high overall d.c. stability. The d.c. circuit of the amplifier is shown in Fig. 5.

The system used in the following calculations shall be explained briefly. In principle, any desired system of reference arrows may be used, the results of the calculations will be the same in any case. All reference arrows will be applied according to the sign convention used in four-terminal network theory. Current reference arrows will be counted positive for currents flowing into the network, and voltage reference arrows will be counted positive for voltages referred to the common or ground terminal. Actual d.c.

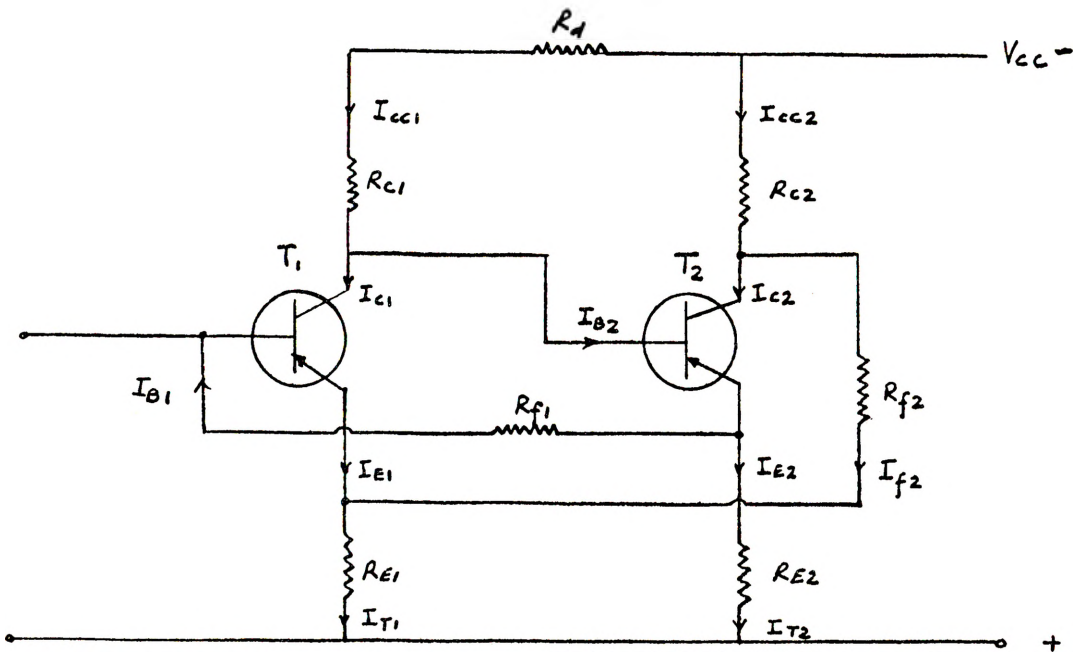


Fig. 5. D.C. circuit of the two-stage amplifier.

currents are counted positive in the direction of conventional current flow, and d.c. voltages are counted positive from positive to negative terminals.

When this system is applied to PNP-transistor circuit analysis, a number of values become negative. In the following calculations, the subscripts B, E and C refer to the respective transistor electrodes. The subscripts 1 and 2 refer to the individual amplifier stages.

Since direct coupling is employed, the base current of each stage affects the preceeding stage. The amplifier will therefore be designed starting with the last stage.

Stage Two

Since the amplifier is to be designed to give an undis-

torted output of about 225 mV at 1 kc, a rough calculation shows that at 20 cps., the relative gain is +20 db, which means that the collector voltage swing is of the order of 2.3 V. The operating point is selected where it is not too close to the saturation region.

Maximum ratings of the 2N414 transistor are:

V_{CE} = -15V (V_{BE} = 0.1V)

V_{CB} = -30V (emitter open)

V_{EB} = -15V (collector open)

I_C (steady) = 200 mA

P_c = 200 mW

Temperature (ambient) = 85°C.

To achieve maximum voltage gain, the collector resistor of this stage will be made as large as possible. The selected operating point is:

I_C = -1.0 mA

V_{CE} = -5.0 V

V_{cc} = -16.0 V (supply voltage available).

A suitable load resistor is 7.5 KΩ.

$$I_{cc_2} = I_{f2} + I_{c2}$$

$$V_{c2} \approx V_{cc_1} - I_{c_2} R_{c_2}$$

$$\approx -16.0 + 1.0 \times 10^{-3} \times 7.5 \times 10^{3}$$

$$\approx -8.5 \text{ V}$$

Since $R_{f2} \gg R_{E1}$

$$I_{f2} = \frac{V_{c2}}{R_{f2}} = \frac{-8.5 \text{ V}}{105 \times 10^{3} \Omega} = -0.081 \text{ ma.}$$

$$I_{cc_2} = I_{c_2} + I_{f_2}$$
$$(-1.0 - 0.081)\ \text{ma.}$$
$$= -1.081\ \text{ma.}$$

$$V_{c_2} = V_{cc_2} - I_{cc_2} R_{c_2}$$
$$= -16.0 + 1.081 \times 10^{-3} \times 7.5 \times 10^{3}$$
$$= -7.9\ \text{V}$$

$$V_{CE} = -5.0\ \text{V (selected)}$$

$$V_{E_2} = V_{c_2} - V_{CE_2} = -7.9 + 5.0 = -2.9\ \text{V}$$

$$I_c = \beta I_B + (\beta + 1)\ I_{CBO} \quad \ldots\ldots\ldots\ldots \quad (13)$$

$$\beta_2 = h_{FE}\Big|_{I_{C_2} = 1\ \text{ma.}}$$
$$= 60\ \text{(average)}$$

$$(\beta_2 + 1)\ I_{CBO} = 61\ (-2.0 \times 10^{-6}) = -0.122\ \text{ma.}$$

$$I_{B_2} = \frac{I_{c_2} - (\beta_2 + 1)\ I_{CBO}}{\beta_2}$$
$$= \left(\frac{-1.0 + .122}{60}\right)\ \text{ma.}$$
$$= -0.0146\ \text{ma.}$$

$$I_{E_2} = I_{c_2} + I_{B_2}$$
$$= (-1.0 - 0.046)\ \text{ma.}$$
$$= -1.0146\ \text{ma.}$$

From stage 1, it will be found that $I_{B_1} = -0.0105$ ma.

$$I_{T_2} = (-1.0146 + 0.0105)\ \text{ma.}$$
$$= -1.0041\ \text{ma.}$$

$$R_{E_2} = \frac{V_{E_2}}{I_{T_2}} = \frac{-2.9\ \text{V}}{-1.004\ \text{ma.}}$$
$$= \underline{\underline{2.89\ \text{K}\Omega}}$$

Choose $R_{E_2} = 3\text{K}\Omega$, the nearest EIA standard.

$$V_{EE2} = I_{T2} R_{E2}$$
$$= -1.004 \times 10^{-3} \times 3 \times 10^{3}$$
$$= \underline{\underline{-3.012 \text{ V.}}}$$

From the characteristic curves of all medium powered Ge transistors, $V_{BE} = +0.1$ V.

$$V_{B2} = (-3.012 - 0.1) V$$
$$= \underline{\underline{-3.112 \text{ V.}}}$$

$$P_C = \left| I_{C2} \times V_{CE} \right| = 1 \times 10^{-3} \times 5 = 5 \text{ mv.}$$
$$P_{dc} = \left| I_{CC2} \times V_{CC2} \right| = 1.081 \times 10^{-3} \times 16.0 = 17.3 \text{ mw.}$$

Stage One

Since the two stages are directly coupled,

$$V_{B2} = V_{C1} = -3.112 \text{ V}$$

To achieve the desired high signal to noise ratio, the first stage has to be designed for optimum low noise level. Since it has to handle only very small signals, the selection of the operating point is not limited by considerations concerning collector voltage swings. The source resistance is 800Ω. At the reference frequency of 1 kc, a suitable value of collector current is 0.5 mA. The selected operating-point is:

$$I_C = -0.5 \text{ ma.}$$
$$V_{CE} = -3 \text{ V.}$$
$$V_{CC} = -14.5 \text{ V}$$
$$R_{C1} = \frac{V_{CC1} - V_{C1}}{I_{C1} + I_{B2}}$$
$$= \frac{-14.5 \text{ V} + 3.112 \text{ V}}{(0.5 - 0.0146) \text{ ma}}$$

$$= \frac{11.39\ V}{0.5146\ ma.} \approx \underline{22\ K\Omega}$$

$$V_{C1} = V_{CC1} - I_{C1} \times R_{C2}$$

$$= -14.5 + 0.5146 \times 10^{-3} \times 22 \times 10^{3}$$

$$= -3.16\ V.$$

$$V_{CE1} = -3.0\ V \text{ (selected)}$$

$$V_{EE1} = V_{C1} - V_{CE1}$$

$$= -3.16\ V + 3.0\ V$$

$$= -0.16\ V$$

$$I_{B1} = \frac{I_{C1} - (\beta_1 + 1)\ I_{CBO}}{\beta_1}$$

$$\beta_1 = h_{FE} \Big|_{I_{C1} = 0.5\ ma}$$

$$\approx 40$$

$$I_{B1} = \frac{-0.5 + 0.082}{40}$$

$$= -0.0105\ ma.$$

$$I_{T1} = I_{C1} + I_{B1} + I_{f2}$$

$$= (-0.5 - 0.0105 - 0.081)\ ma$$

$$= -0.5915\ ma$$

$$R_{E1} = \frac{V_{EE1}}{I_{T1}} = \frac{-0.16\ V}{-0.5915\ ma.}$$

$$\underline{270\ \Omega}$$

From the graph of output voltage verses R_{E1}, (appendix B) it is seen that for $R_{E1} = 270\Omega$, the output voltage is 165 mV. at 1 kc. We require an output voltage of about 225 mV. Hence we choose $R_{E1} = 200\Omega$.

$$V_{EE1} = I_{T1} R_{E1}$$

$$= -0.5915 \times 10^{-3} \times 200$$

$$= -.118 \text{ V.}$$

$$V_{BE1} = +0.1 \text{ V}$$

$$V_{B1} = V_{EB1} + V_{EE1}$$

$$= -0.218 \text{ V.}$$

$$I_{B1} = -0.0105 \text{ ma.}$$

$$R_{f1} = \frac{V_{EE2} - V_{B1}}{I_{B1}}$$

$$= \frac{-3.072 \text{ V} + 0.218 \text{ V}}{-0.0105 \text{ ma.}}$$

$$= \frac{-2.79 \text{ V}}{-0.0105 \text{ ma.}}$$

$$\underline{\underline{266 \text{ K}\Omega}}$$

Choose R_{f1} = 270 KΩ, the nearest E. I. A. standard.

The low frequency response of the equalizer is limited by the values of coupling and emitter bypass capacitors. To ensure good low frequency response, the lower cutoff frequency should be as low as possible. The choice of the values for C_{S1}, C_{E2} and the decoupling capacitors are not critical. Since the input impedance of the amplifier is high, a convenient value of C_{S1} is 10μF. To ensure good low frequency response down to 20 cps., C_{E2} is chosen to be 100μF. To achieve a low hum level and to avoid low frequency instability, the decoupling capacitors have been chosen to be 100μF. The complete circuit of the frequency equalizer is shown in Fig. 10.

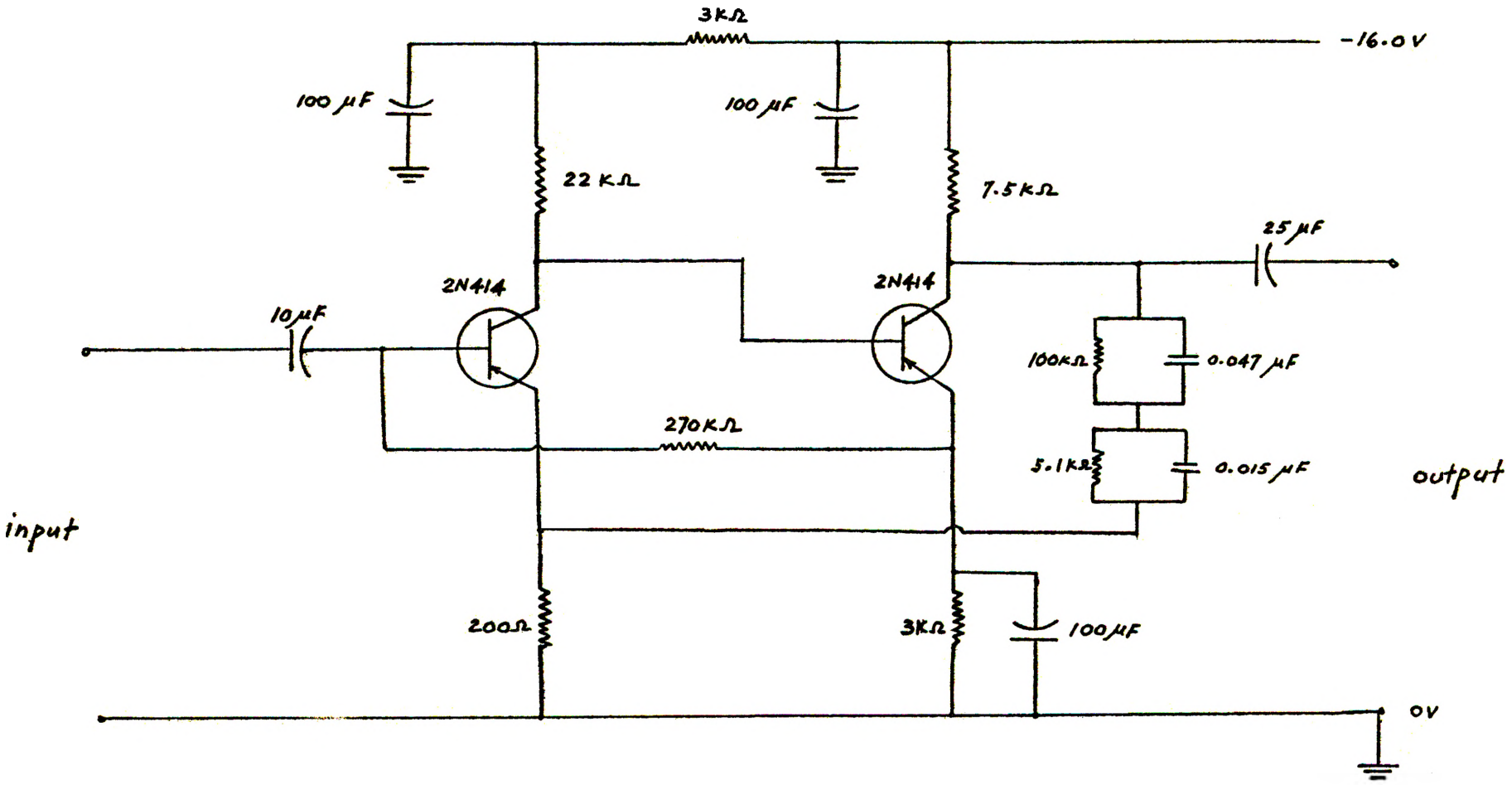


Fig. 16. Complete frequency equalizer circuit.

(B) D.C. BIAS AND STABILITY

The problem of designing bias circuits for transistor amplifiers has received the attention of many investigators.[8,9] Numerous reports have been made pertaining to the thermal displacement of the transistor operating point.

In this design, the first two stages of the circuit have a feedback bias arrangement with R_{f1} feeding bias current to the base of T_1 which is directly proportional to the current of T_2. This stabilizes the operating point for variation of both h_{FE} and the ambient temperature. Fig. 7 shows the feedback bias arrangement.

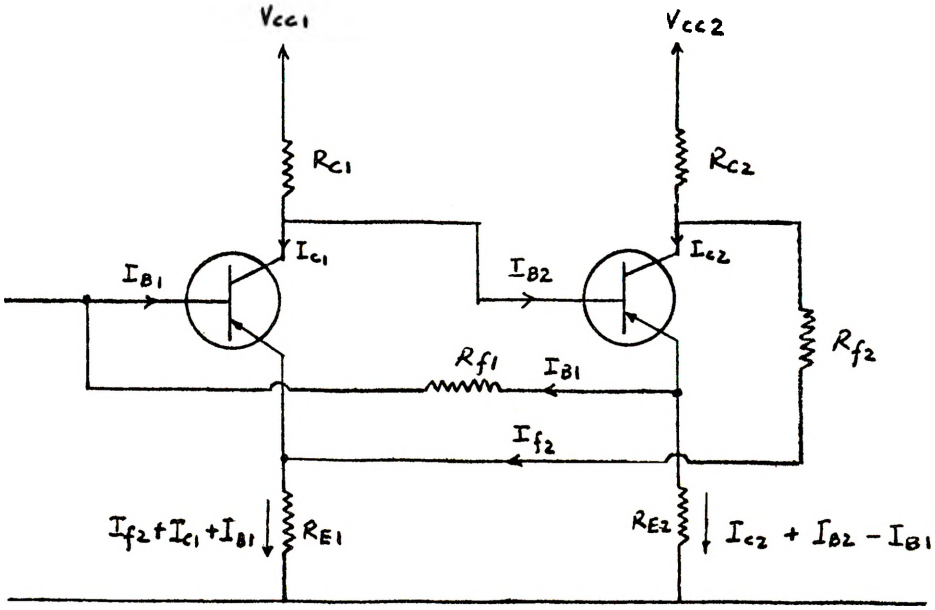


Fig. 7. Feedback bias arrangement.

In finding an analytical expression for the stability factors of the two stages, it is assumed that at a given

temperature, the reverse saturation current I_{cbo} is the same since the two transistors are identical. It is also assumed that the increment of this current with temperature is the same.

Neglecting the emitter junction voltage, the following equations apply:

$$V_{cc1} = R_{c1}(I_{c1} + I_{B2}) + R_{f1} I_{B1} + R_{E1}(I_{f2} + I_{c1} + I_{B1}) \quad (14a)$$

$$V_{cc1} = R_{c1}(I_{c1} + I_{B2}) + R_{E2}(I_{c2} + I_{B2} - I_{B1}) \quad (15a)$$

$$V_{cc2} = R_{c2}(I_{c2} + I_{f2}) + R_{f2} I_{f2} + R_{E1}(I_{f2} + I_{c1} + I_{B1}) \quad (16a)$$

Using equations (14a), (15a), (16a) and (13), the expressions for the stability factors are obtained by differentiating the collector currents with respect to I_{cBo}. As shown in Appendix B, the stability factors are:

$$S_1 = \frac{dI_{c1}}{dI_{cBo}} = 11.13$$

and

$$S_2 = \frac{dI_{c2}}{dI_{cBo}} = -64.9$$

The values are in good agreement[10,11] with values to be expected of such a circuit. The negative sign for S_2 indicates that the collector current of stage 2 decreases as I_{cBo} (or temperature) increases. S_2 is considerably larger than S_1 because of the gain factor.

CHAPTER IV

ANALYSIS OF THE CIRCUIT

(A) THE NODE EQUATIONS

The first step is to draw an equivalent circuit to provide a model for the mathematical analysis. At this point, a decision has to be made as to how exact an equivalent circuit is to be used. In hand calculations, many approximations are usually made to simplify calculations. On the digital computer, however, once the program is prepared, an exact solution can be obtained almost as rapidly as an approximate one. Factors which have negligible effect on the performance are of course eliminated to simplify programming.

In the analysis to follow, the small signal parameters of the transistor are assumed to be constant and frequency independent throughout the audio frequency range. The effects of stray wiring capacitance will also be assumed negligible. The y-parameter model will be used as it is most convenient for voltage amplification analysis. The complete equivalent circuit is shown in Fig. 8.

Since there is no standard program for the computer to solve simultaneous equations with complex coefficients, each of the five nodal equations had to be separated into the real and imaginary parts. The five nodal equations thus break up into a set of 10 simultaneous equations.

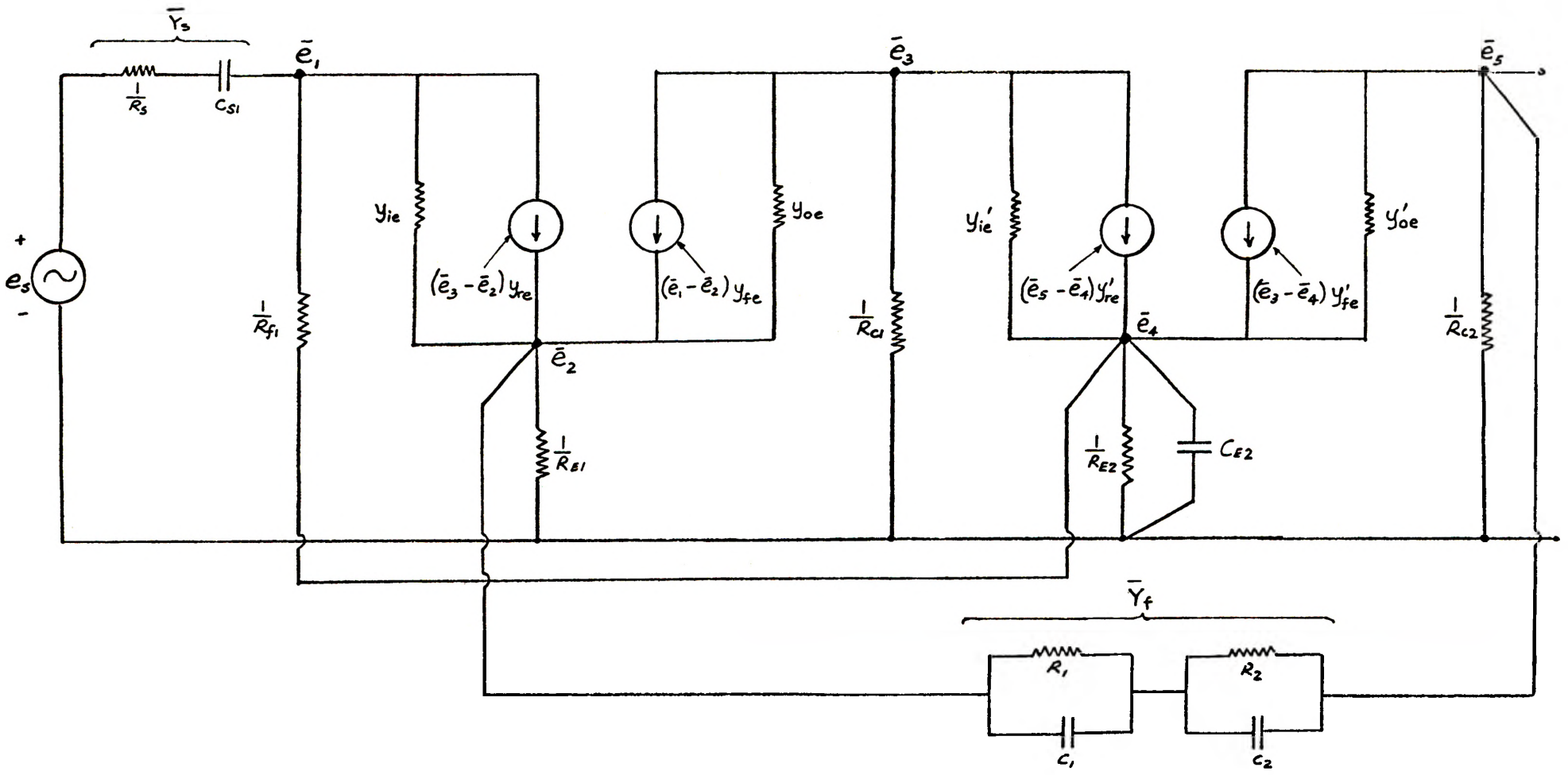


Fig. 18. Complete Equivalent Circuit.

THE NODAL EQUATIONS

$$\bar{e}_1\left[\bar{Y}_s + \frac{1}{R_{f1}} + Y_{ie}\right] - \bar{e}_2\left[Y_{re} + Y_{ie}\right] + \bar{e}_3\left[Y_{re}\right] - \bar{e}_4\left[\frac{1}{R_{f1}}\right] = \bar{e}_s\left[\bar{Y}_s\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (17)$$

$$-\bar{e}_1\left[Y_{ie} + Y_{fe}\right] + \bar{e}_2\left[\frac{1}{R_{E1}} + Y_{ie} + Y_{oe} + Y_{re} + Y_{fe} + \bar{Y}_f\right] - \bar{e}_3\left[Y_{re} + Y_{oe}\right] - \bar{e}_5\left[\bar{Y}_f\right] = 0 \quad \ldots\ldots\ldots\ldots \quad (18)$$

$$\bar{e}_1\left[Y_{fe}\right] - \bar{e}_2\left[Y_{fe} + Y_{oe}\right] + \bar{e}_3\left[\frac{1}{R_{C1}} + Y_{oe} + Y'_{ie}\right] - \bar{e}_4\left[Y'_{re} + Y'_{ie}\right] + \bar{e}_5\left[Y'_{re}\right] = 0 \quad \ldots\ldots\ldots\ldots \quad (19)$$

$$-\bar{e}_1\left[\frac{1}{R_{f1}}\right] - \bar{e}_3\left[Y'_{ie} + Y'_{fe}\right] + \bar{e}_4\left[\frac{1}{R_{E2}} + j\omega C_{E2} + \frac{1}{R_{f1}} + Y'_{ie} + Y'_{oe} + Y'_{fe} + Y'_{re}\right] - \bar{e}_5\left[Y'_{oe} + Y'_{re}\right] = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (20)$$

$$-\bar{e}_2\left[\bar{Y}_f\right] + \bar{e}_3\left[Y'_{fe}\right] - \bar{e}_4\left[Y'_{fe} + Y'_{oe}\right] + \bar{e}_5\left[\frac{1}{R_{C2}} + \bar{Y}_f + Y'_{oe}\right] = 0 \quad \ldots\ldots\ldots\ldots \quad (21)$$

$$
\begin{bmatrix} .875 \times 10^{-5} \\ 1.74 \times 10^{-7} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} =
\begin{bmatrix}
1.761 \times 10^{-3} & -.2485 \times 10^{-4} & -.508 \times 10^{-3} & 0 & -.1618 \times 10^{-6} & 0 & -0.37 \times 10^{-5} & 0 & 0 & 0 \\
.2485 \times 10^{-4} & 1.761 \times 10^{-3} & 0 & -.508 \times 10^{-3} & 0 & -.1618 \times 10^{-6} & 0 & -.37 \times 10^{-5} & 0 & 0 \\
-2.00 \times 10^{-2} & 0 & 24.29 \times 10^{-3} & -.1174 \times 10^{-3} & -11.62 \times 10^{-6} & 0 & 0 & 0 & -.1155 \times 10^{-3} & .1174 \times 10^{-3} \\
0 & -20.0 \times 10^{-3} & .1174 \times 10^{-3} & 24.29 \times 10^{-3} & 0 & -11.62 \times 10^{-6} & 0 & 0 & -.1174 \times 10^{-3} & -.1155 \times 10^{-3} \\
19.49 \times 10^{-3} & 0 & -19.5 \times 10^{-3} & 0 & .7653 \times 10^{-3} & 0 & -.708 \times 10^{-3} & 0 & -.2543 \times 10^{-6} & 0 \\
0 & 19.49 \times 10^{-3} & 0 & -19.5 \times 10^{-3} & 0 & .7653 \times 10^{-3} & 0 & -.708 \times 10^{-3} & 0 & -.2543 \times 10^{-6} \\
-.37 \times 10^{-5} & 0 & 0 & 0 & -40.0 \times 10^{-3} & 0 & 40.36 \times 10^{-3} & -.1571 & -21.0 \times 10^{-6} & 0 \\
0 & -.37 \times 10^{-5} & 0 & 0 & 0 & -40.0 \times 10^{-3} & .1571 & 40.36 \times 10^{-3} & 0 & -21.0 \times 10^{-6} \\
0 & 0 & -.1155 \times 10^{-3} & .1174 \times 10^{-3} & 39.29 \times 10^{-3} & 0 & -39.31 \times 10^{-3} & 0 & .27 \times 10^{-3} & -.1174 \times 10^{-3} \\
0 & 0 & -.1174 \times 10^{-3} & -.1155 \times 10^{-3} & 0 & 39.29 \times 10^{-3} & 0 & -39.31 \times 10^{-3} & .1174 \times 10^{-3} & .27 \times 10^{-3}
\end{bmatrix}
\begin{bmatrix} e_{1R} \\ e_{1I} \\ e_{2R} \\ e_{2I} \\ e_{3R} \\ e_{3I} \\ e_{4R} \\ e_{4I} \\ e_{5R} \\ e_{5I} \end{bmatrix}
$$

Fig. 19. Matrix (10 x 10) of nodal coefficients.

This allows the real and the imaginary parts of the nodal voltages to be found simultaneously. The (10 x 10) matrix of the nodal equations which describe the performance of the circuit at 1 kc. is shown in Fig. 9. The input voltage $\bar{e}_s$ is assumed to be 7.0 mv and R_s equal to 800 ohms.

THE INPUT AND OUTPUT IMPEDANCES

One of the important effects of feedback is its influence on the impedance that the amplifier presents to any external circuit connected to it. For an amplifier with negative voltage feedback the input impedance is increased while the output impedance is decreased.

The input impedance of the equalizer is effectively the reactance of the input coupling capacitor in series with the impedance $\bar{Z}_{i1}$ which is the driving point impedance between node 1 and ground. $\bar{Z}_{i1}$ is determined by taking the ratio of $\bar{e}_1$ and the sum of the node currents leaving the node. Thus

$$\bar{Z}_{i1} = \frac{\bar{e}_1}{\sum i_1}$$

$$= \frac{\bar{e}_1}{(\bar{e}_1 - \bar{e}_4)\frac{1}{R_{f1}} + (\bar{e}_1 - \bar{e}_2)\, Y_{ie} + (\bar{e}_3 - \bar{e}_2)\, Y_{re}}$$

and

$$\bar{Z}_i = \bar{Z}_{i1} - j\,\frac{1}{\omega C_{s1}} \quad \ldots\ldots\ldots\ldots \quad (22)$$

The output impedance of the amplifier is effectively the reactance of the output coupling capacitor in series with the

impedance $\bar{Z}_{05}$ which is the driving point impedance between node 5 and ground. $\bar{Z}_{05}$ is determined by applying a test voltage at node 5 and taking the ratio of the node voltage and currents leaving the node. Thus

$$\bar{Z}_{05} = \frac{\bar{e}_5}{\sum i_5}$$

$$= \frac{\bar{e}_5}{(\bar{e}_3 - \bar{e}_4)\, y'_{fe} + (\bar{e}_5 - \bar{e}_4)\, y'_{oe} + \bar{e}_5 \left(\frac{1}{R_{c_2}}\right) + (\bar{e}_5 - \bar{e}_2)\, \bar{Y}_f}$$

and

$$\bar{Z}_o = \bar{Z}_{05} - j \frac{1}{\omega C_{c_2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (23)$$

The circuit for the determination of $\bar{Z}_{05}$ is shown in Fig. 10.

THE NYQUIST TEST FOR STABILITY

The benefits derived from the use of negative feedback are great but they are achieved at the expense of gain and the possibility of self-oscillation because the forward and feedback elements are frequency sensitive. Consider equation (1a)

$$\bar{A}_{vf} = \frac{\bar{A}}{1 + \bar{\beta}\,\bar{A}}$$

when $\bar{\beta}\,\bar{A} = -1$, $\bar{A}_{vf} \to \infty$, a condition intolerable in amplifiers and represents an output limited only by the saturation and cutoff regions of the transistors.

To test for the stability of the circuit, $\bar{\beta}\,\bar{A}$ is plotted in polar coordinates. According to the Nyquist criterion,[12] oscillation will occur if the locus of $\bar{\beta}\,\bar{A}$ encloses the

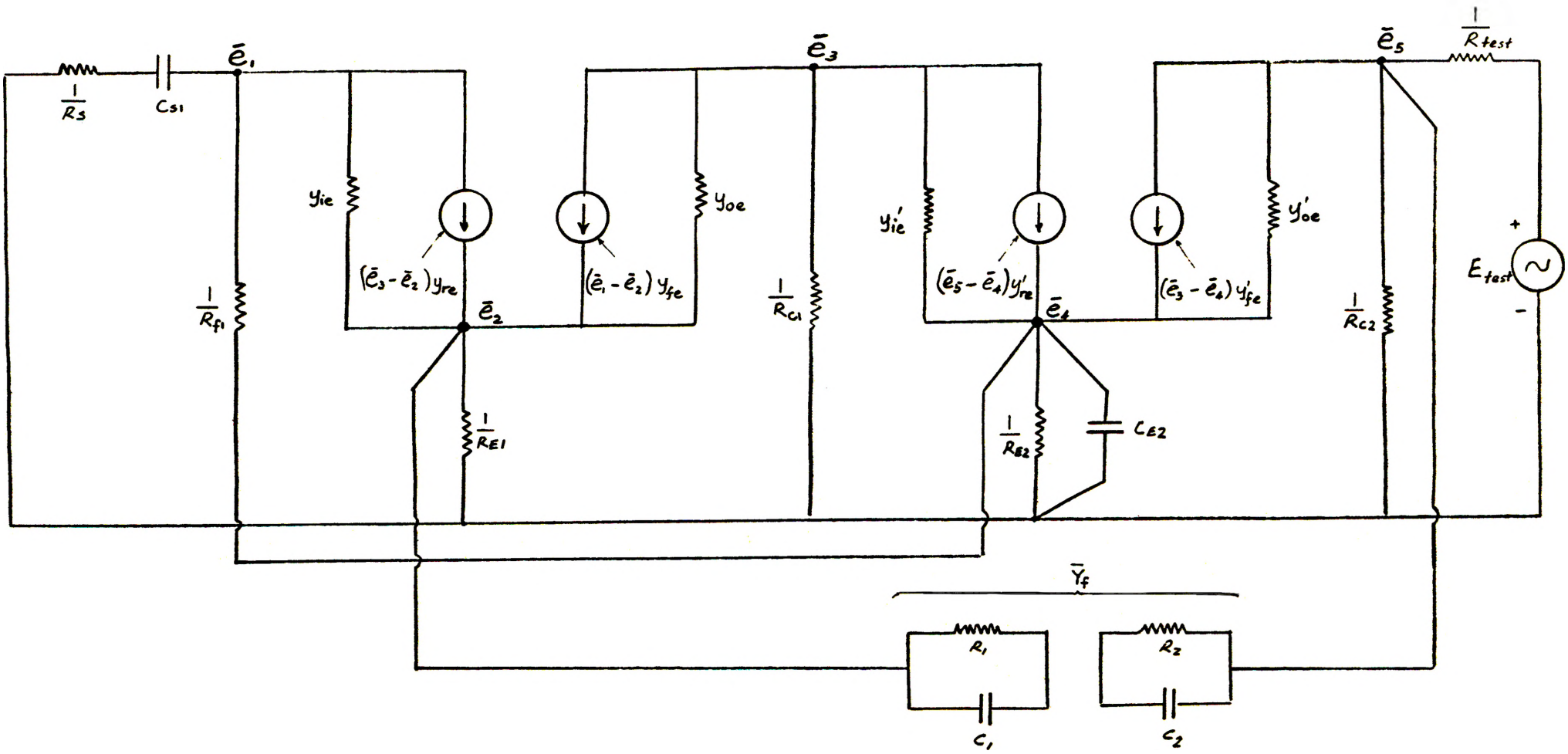


Fig. 10. Circuit for the determination of $\bar{Z}_{os}$.

critical point (-1, 0).

The overall frequency characteristics of the amplifier with the frequency dependent feedback loop open is approximated by assuming that the amplifier has uniform gain over the mid-band as shown in Fig. 11.

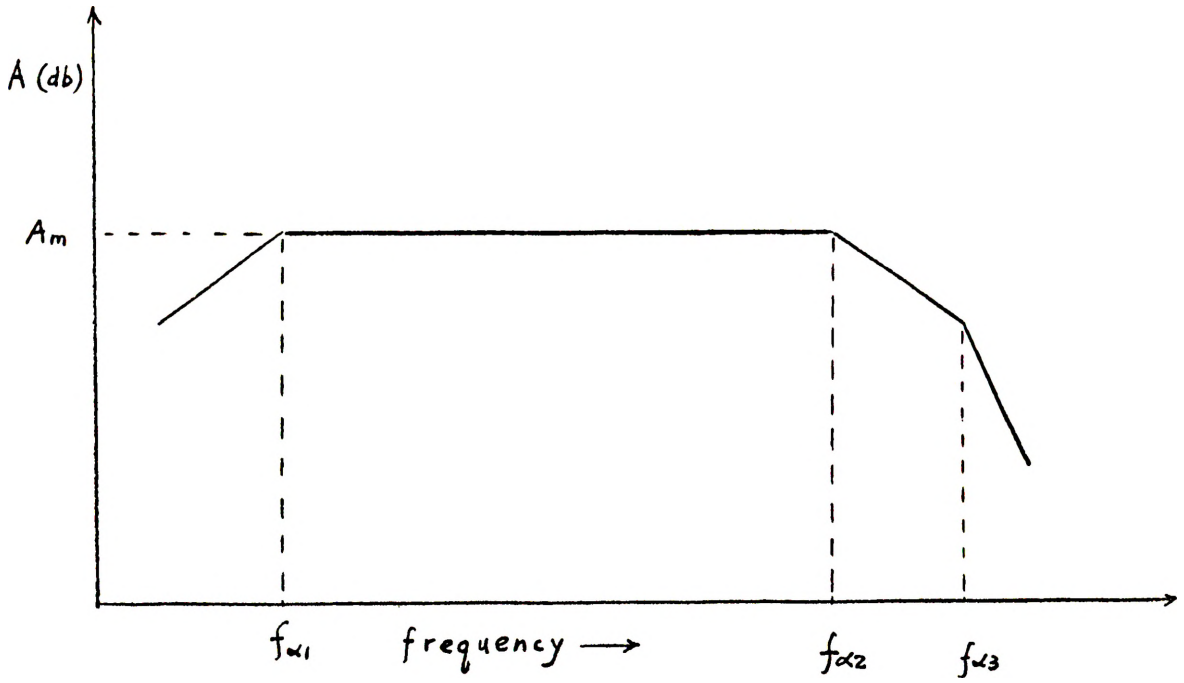


Fig. 11. Approximation of the overall frequency characteristics.

$f_{\alpha 1}$ is the low frequency half power point and is determined by using the computer to calculate the amplifier's response at low frequencies. $f_{\alpha 2}$ and $f_{\alpha 3}$ are the high frequency half power points of stages 1 and 2 respectively and they are related to the circuit parameters by:

$$f_{\alpha e} = (1 + h_{fb})\, f_{\alpha b} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (24)$$

The mid-band voltage gain is taken to be the gain at 1 kc and is denoted by A_m. The overall transfer function is thus given by:

$$\bar{A} = \frac{Am}{(1-j\frac{f_{\alpha 1}}{f})\,(1 + j\frac{f}{f_{\alpha 2}})\,(1 + j\frac{f}{f_{\alpha 3}})}$$

$$= \frac{Am\left[\left(1-\frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right) + f_{\alpha 1}\left(\frac{f_{\alpha 2}+f_{\alpha 3}}{f_{\alpha 2}f_{\alpha 3}}\right)\right] + j\left[f\frac{(f_{\alpha 2}+f_{\alpha 3})}{f_{\alpha 2}f_{\alpha 3}} - \frac{f_{\alpha 1}}{f}\left(1-\frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right)\right]}{\left[\left(1-\frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right) + f_{\alpha 1}\frac{(f_{\alpha 2}+f_{\alpha 3})}{f_{\alpha 2}f_{\alpha 3}}\right]^2 + \left[f\frac{(f_{\alpha 2}+f_{\alpha 3})}{f_{\alpha 2}f_{\alpha 3}} - \frac{f_{\alpha 1}}{f}\left(1-\frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right)\right]^2}$$

$$= \frac{Am\,(P_1 + jP_2)}{P_3 + P_4}$$

where

$$P_1 = \left(1 - \frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right) + f_{\alpha 1}\left(\frac{f_{\alpha 2} + f_{\alpha 3}}{f_{\alpha 2}f_{\alpha 3}}\right)$$

$$P_2 = \frac{f\,(f_{\alpha 2} + f_{\alpha 3})}{f_{\alpha 2}f_{\alpha 3}} - \frac{f_{\alpha 1}}{f}\left(1 - \frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right)$$

$$P_3 = \left[\left(1 - \frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right) + f_{\alpha 1}\left(\frac{f_{\alpha 2} + f_{\alpha 3}}{f_{\alpha 2}f_{\alpha 3}}\right)\right]^2$$

$$P_4 = \left[\frac{f\,(f_{\alpha 2} + f_{\alpha 3})}{f_{\alpha 2}f_{\alpha 3}} - \frac{f_{\alpha 1}}{f}\left(1 - \frac{f^2}{f_{\alpha 2}f_{\alpha 3}}\right)\right]^2$$

Letting $\bar{\beta} = \beta_R + j\beta_I$,

$$\bar{\beta}\bar{A} = \frac{Am\,(P_1\beta_R + P_2\beta_I) + j\,(P_1\beta_I - P_2\beta_R)}{P_3 + P_4} \quad \ldots\ldots \quad (25)$$

Using equation (24), the half power frequencies $f_{\alpha 2}$ and $f_{\alpha 3}$ were found to be 119 kc and 178 kc respectively. The low frequency half power point was computed to be 20 cps.

The computer was programmed to calculate the real and imaginary components of equation (25) over a wide range of frequencies from 10 cps to 10^8 cps. The polar plot is shown in Fig. 12. It is seen that the locus of $\overline{\beta}\ \overline{A}$ does not encircle the critical point (-1, 0). The loop amplitude and phase characteristics are also plotted as shown in Fig. 13a and Fig. 13b. It is seen that the gain magnitude drops to unity (0 db) before the phase shift is 180° at both ends of the frequency spectrum. This indicates that the amplifier is stable.

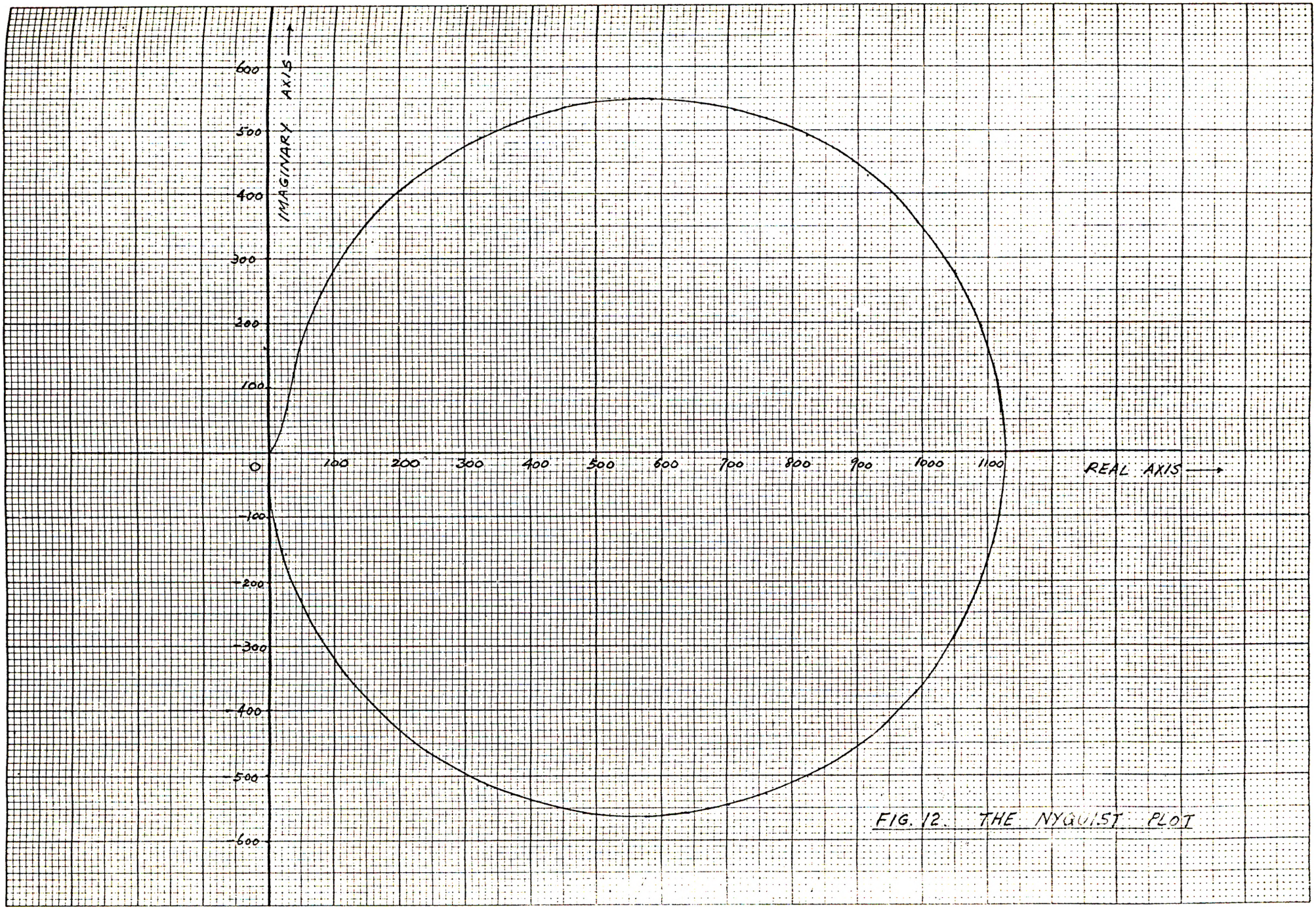


FIG. 12. THE NYQUIST PLOT

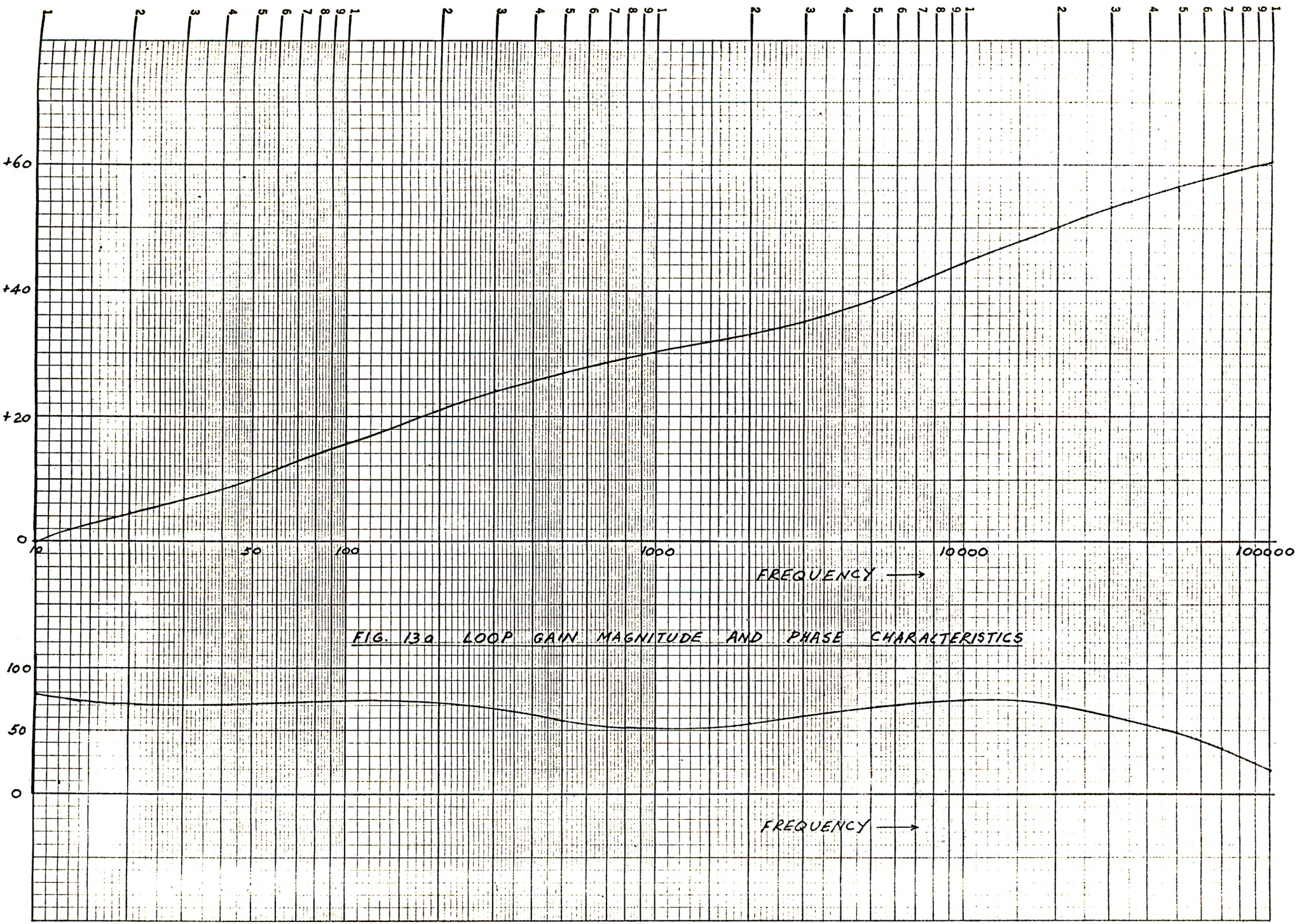


FIG. 13a LOOP GAIN MAGNITUDE AND PHASE CHARACTERISTICS

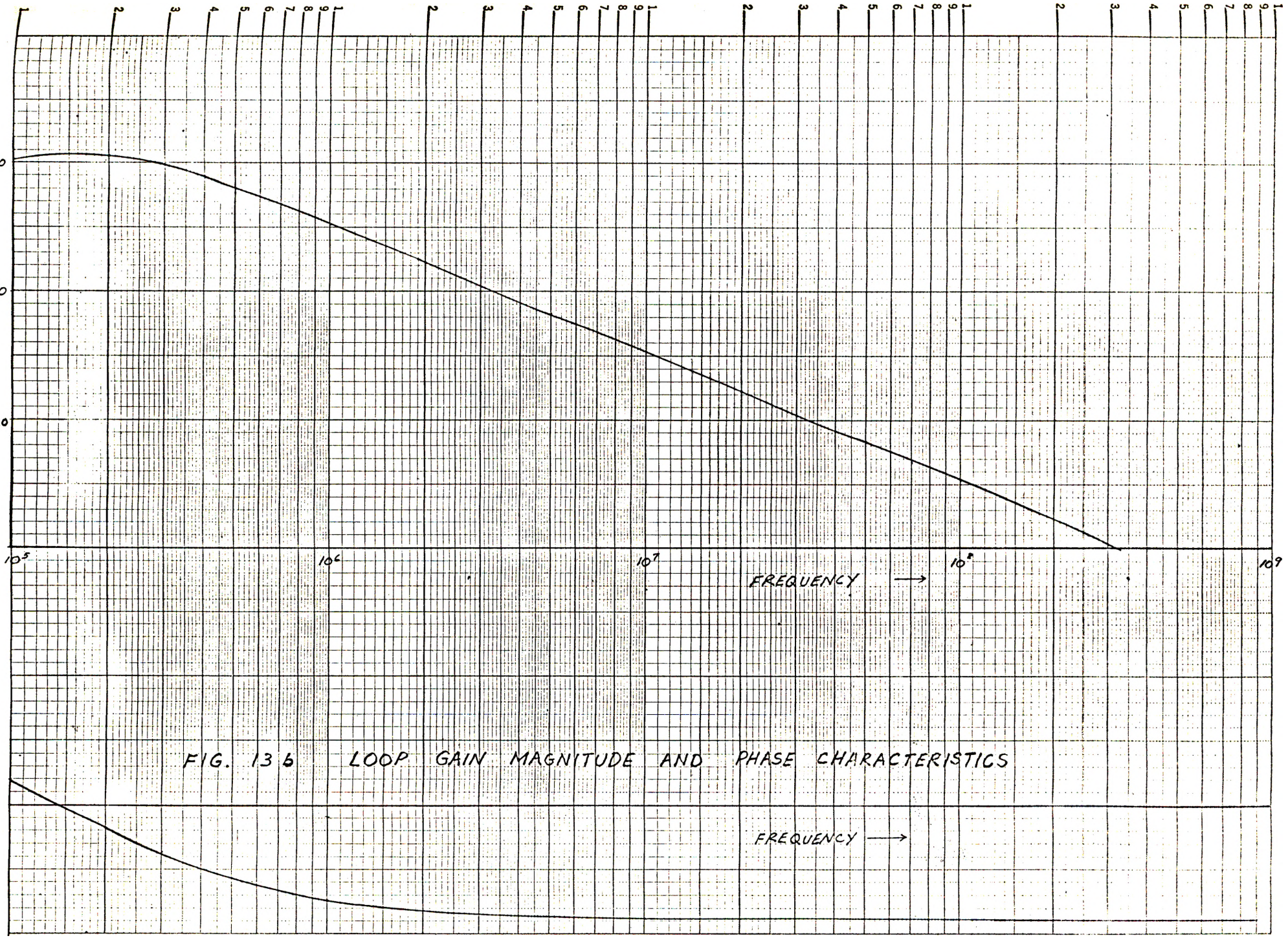


FIG. 13 b LOOP GAIN MAGNITUDE AND PHASE CHARACTERISTICS

CHAPTER V

EXPERIMENTAL DETERMINATION OF THE CIRCUIT PERFORMANCE

OPERATING POINTS

A VTVM with an input resistance of 11 megohms was used for all d.c. measurements. Since it is not possible to take current measurements in a transistor circuit without upsetting normal operating conditions of the circuit, all direct current values of interest had been determined from voltage and resistance measurements.

FREQUENCY RESPONSE MEASUREMENTS

The equipment was connected as shown in Fig. 14.

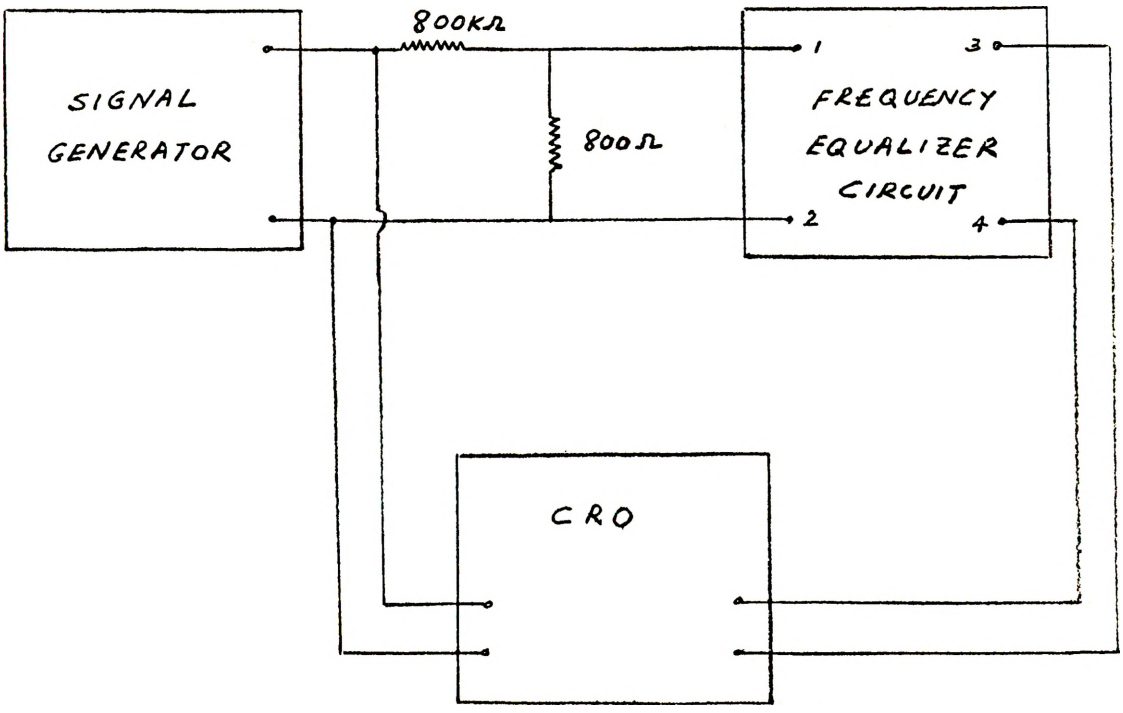


Fig. 14. Frequency response and phase shift measurement.

The oscillator which provided a constant amplitude signal was connected in series with a 1000:1 voltage dividing network. The output of the amplifier was connected to one of the inputs of the CRO. The signal frequency was varied from 20 cps to 15 kc. Measurements of the input and output voltages were taken. The phase shift of the amplifier at each frequency was obtained by measuring the time delay of the two signals traced on the screen. The results are shown in table 2.

INPUT AND OUTPUT IMPEDANCE MEASUREMENT

A Z-angle meter was used to determine the input and output impedance of the circuit. The equipment was connected as shown in Fig. 15.

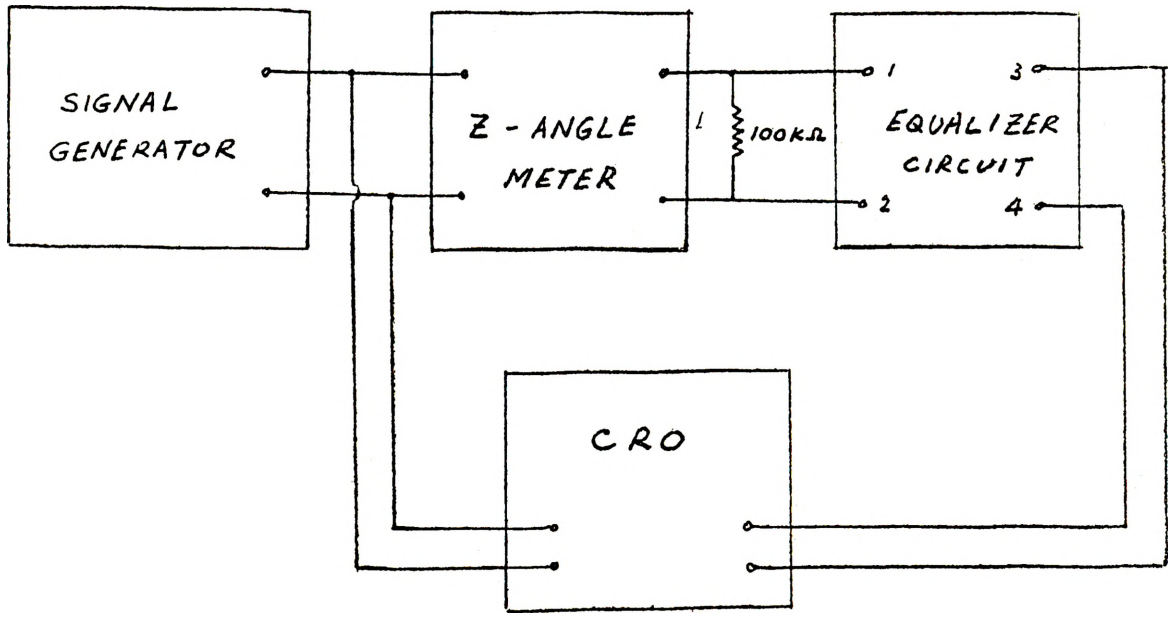


Fig. 15. Measurement of the input impedance.

Since the expected value of the input impedance slightly exceeds the range of the Z-angle meter, an accurately measured resistor of 100 KΩ was connected in parallel with the input impedance to be measured. The connecting leads were kept as short as possible to insure that extraneous signals were not introduced. The CRO was used to check that the equalizer circuit was working in the linear region when the measurements were taken.

The circuit to measure the output impedance is shown in Fig. 16.

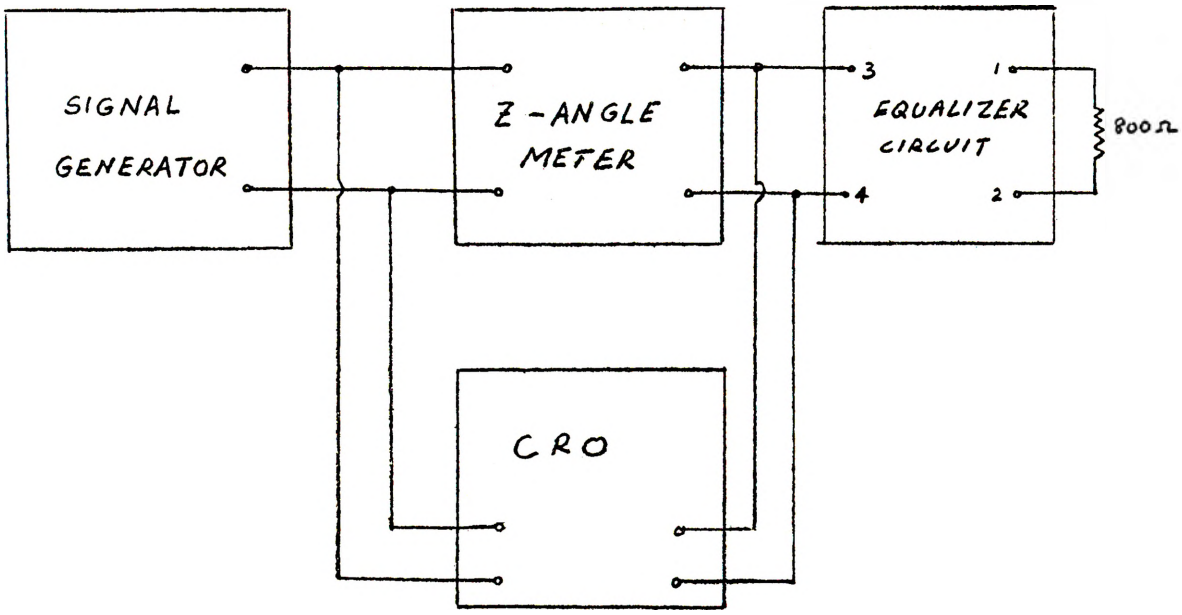


Fig. 16. Measurement of output impedance.

The input terminals were terminated by a resistance of 800 ohms which was the assumed resistance of the source. The results of the measurements are shown in table 4.

CHAPTER VI

CONCLUSIONS

(A) COMPARISON OF THE EXPERIMENTAL RESULTS TO THE ANALYTICAL RESULTS

Table 1 shows the d.c. measurements of the circuit as compared to the analytically calculated values. It is seen that the static operating points actually achieved closely approximate the intended values.

Table 2 shows the frequency response and phase shift of the circuit. The relative frequency response of the circuit as compared with the desired RIAA frequency characteristic is shown in table 3. The values are seen to be in very close agreement for frequencies above 500 cps. Maximum deviation of the frequency-gain characteristic is +1.3 db. at 30 cps which is well within the specification limit of the design. The photographs of the waveforms at 1 kc and 10 kc (shown in Appendix C) show no trace of waveform distortion or of any spurious response. The circuit can, therefore, be expected to give a good performance under normal working conditions.

The plot of phase shift versus frequency shows appreciable deviation between the experimental values and the theoretically expected values. The discrepancy may be accounted for by the fact that it is not possible to take very accurate measurements on the oscilloscope when the order of magnitude is small. Assuming that the time delay

between the two waveforms can be measured to an accuracy of say ± 0.2 of a small division, then taking a typical reading of 5 small divisions as an example, we see that an error of ± 10% can be expected in the measurement of the phase shift.

The experimental and theoretical values of the input and output impedance at 1 kc are in reasonably good agreement. However, transistors have a wide range of parameter variations and a deviation of ± 30% or more can generally be expected.

	Intended values	Measured values
Stage 1		
V_{cc1}	-14.5 V	-14.55 V
V_{cE1}	- 3.0 V	- 2.95 V
I_{c1}	- 0.5 ma	- 0.516 ma
Stage 2		
V_{cc2}	-16.0 V	-16.0 V
V_{cE2}	- 5.0 V	- 5.3 V
I_{c2}	- 1.0 ma	- 0.976 ma

Table 1. Operating points.

Frequency (cps)	Output voltage (volts)		Phase shift (degrees)	
	Theoretical	Experimental	Theoretical	Experimental
20	2.36	2.60	16.0	18.8
30	2.15	2.30	26.5	31.0
50	1.74	1.85	40.5	44.2
70	1.42	1.53	48.8	50.4
100	1.09	1.15	55.4	57.3
200	0.615	.65	60.3	60.0
300	0.446	.46	58.3	59.5
500	0.319	.32	53.2	52.7
700	0.270	.28	50.1	51.4
1000	0.232	.235	48.8	48.8
2000	0.172	.175	54.7	52.8
3000	0.134	.135	61.0	61.8
5000	0.090	.090	68.1	69.7
7000	0.067	.070	71.1	73.1
10000	0.048	.050	72.5	74.0
15000	0.033	.033	71.5	73.9

Table 2. Frequency response and phase shift.

Frequency	RIAA values (db)	Computer calculated values (db)	Measured values (db)
30	+18.61	+19.30	+19.9
50	+16.96	+17.46	+17.8
70	+15.31	+15.72	+16.0
100	+13.11	+13.42	+13.8
200	+ 8.22	+ 8.43	+ 8.9
300	+ 5.53	+ 5.63	+ 5.9
700	+ 1.23	+ 1.29	+ 1.2
1000	0.00	0.00	0.0
2000	- 2.61	- 2.62	- 2.5
3000	- 4.76	- 4.78	- 4.8
5000	- 8.23	- 8.24	- 8.3
7000	-10.85	-10.83	-10.5
10000	-13.75	-13.70	-13.4
15000	-17.17	-17.05	-17.2

Table 3. Relative frequency response.

	Theoretical		Experimental	
	$\|Z\|$	Phase angle	$\|Z\|$	Phase angle
Input Impedance	114.3 KΩ	+14.4°	116 KΩ	+10°
Output Impedance	180.9 Ω	-51.5°	192 Ω	-49°

Table 4. Input and output impedance.

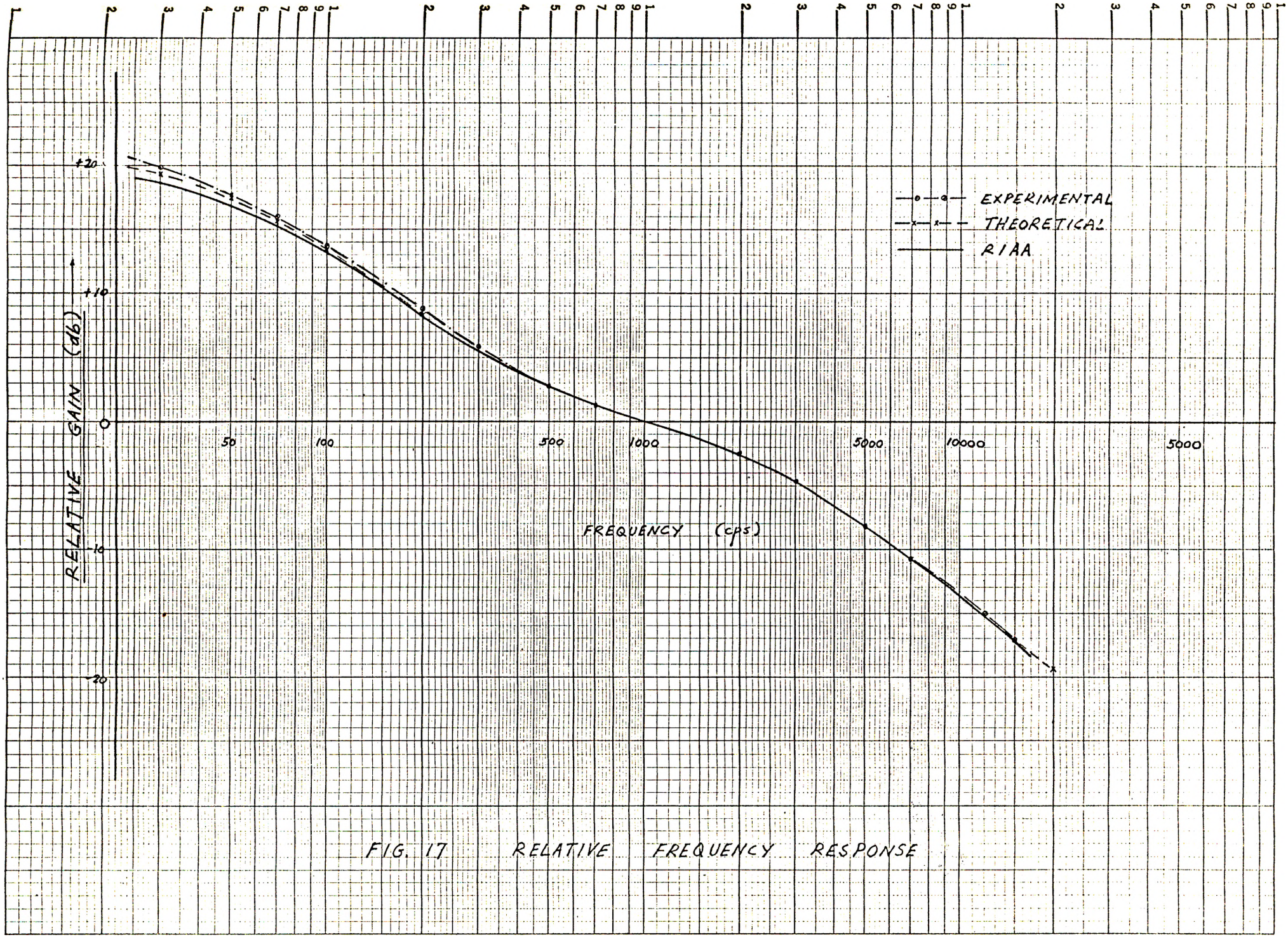


FIG. 17 RELATIVE FREQUENCY RESPONSE

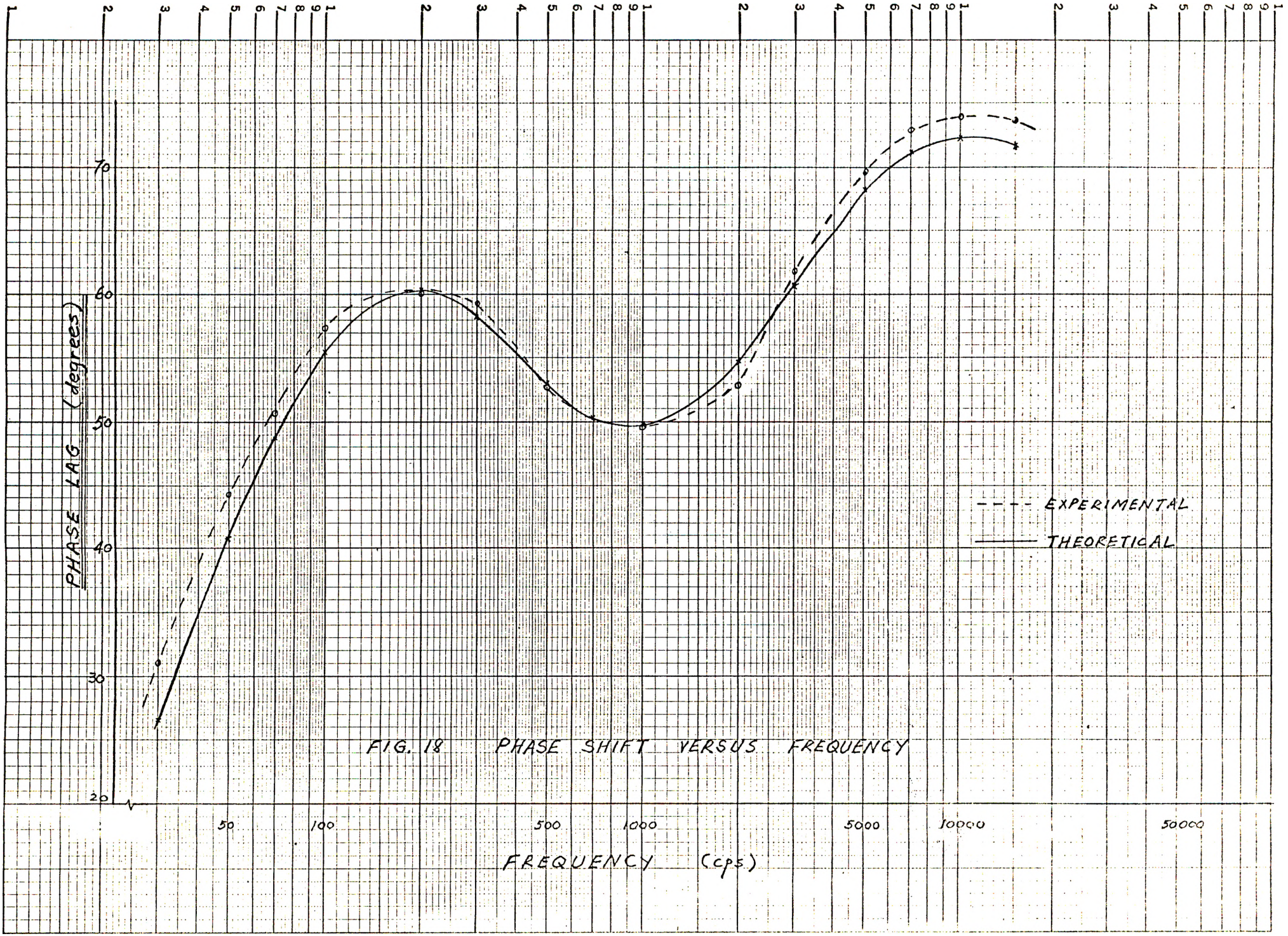


FIG. 18 PHASE SHIFT VERSUS FREQUENCY

(B) SUGGESTIONS FOR AN EXTENSION OF THE RESEARCH

The results of the work to this point indicates that within the audio frequency range, the circuit is well approximated by the y-parameter equivalent circuit. The basic assumptions that the parameters are constant and frequency independent within this range of frequency are therefore justifiable. Although frequency has been the only parameter thus far varied, the program can easily be extended to include the effects of the collector and emitter capacitances. Further, tabulated values of the expected variations in transistor parameters as a function of frequency or temperature can be individually introduced into the circuit equations in the same manner that the y-parameter values were handled.

In this work, the standard design technique has been accelerated with the use of the digital computer. The total computer time necessary for the design of this amplifier is only about half an hour. The investigation indicates, however, the immense possibilities of the computer. It provides the designer with a tool which ensures an accurate and correct design on the first try. It makes possible a unified approach to circuit analysis, and to any other system which can be described by a set of simultaneous linear complex equations. More sophisticated programs are highly possible where the input consists of performance specifications and the computer is programmed to scan the circuit parameters and

search out all the possible combinations which will meet the required specifications.

APPENDIX A

PARAMETER CALCULATIONS

The common-base h-parameter values for the 2N414 transistor are obtained from the manufacturer's data sheet and corrected for the operating conditions.

STAGE 2

Parameter	Parameter value from data sheet	Correction at I = 1 ma., V = -5.0 V factor	value
h_{ib} (ohms)	25	1	25
h_{rb}	0.5×10^{-3}	1.05	0.525×10^{-3}
$1 + h_{fb}$	0.017	1.04	0.0177
h_{ob} (mhos)	0.62×10^{-6}	1.01	0.626×10^{-6}

$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}} = 60$$

$$60 + 60\, h_{fb} = -h_{fb}$$

$$h_{fb} = \frac{-60}{61} = \underline{\underline{-0.983}}$$

Using the standard transformation equations from design texts,[13,14]

$$h_{ie} = \frac{h_{ib}}{1 + h_{fb}} = \frac{25}{0.0177} = \underline{\underline{1410 \text{ ohms}}}.$$

$$h_{re} = \frac{h_{ib}\, h_{ob} - h_{rb}\, h_{fb} - h_{rb}}{1 + h_{fb}}$$

$$= \frac{25 \times 0.626 \times 10^{-6} - 0.525 \times 10^{-3} \times (-0.982) - 0.525 \times 10^{-3}}{0.177}$$

$$= \underline{\underline{0.3592 \times 10^{-3}}}$$

$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}} = \frac{+(0.9823)}{0.0177} = \underline{55.49}$$

$$h_{oe} = \frac{h_{ob}}{1 + h_{fb}} = \frac{0.626 \times 10^{-6}}{0.0177} = \underline{0.3537 \times 10^{-4} \text{ mhos}}$$

$$y'_{ie} = \frac{1}{h_{ie}} = \frac{1}{1410} = \underline{0.708 \times 10^{-3} \text{ mhos}}$$

$$y'_{re} = \frac{-h_{re}}{h_{ie}} = \frac{-0.3592 \times 10^{-3}}{1410} = \underline{-0.2543 \times 10^{-6} \text{ mhos}}$$

$$y'_{fe} = \frac{h_{fe}}{h_{ie}} = \frac{55.49}{1410} = \underline{0.3929 \times 10^{-1} \text{ mhos}}$$

$$y'_{oe} = \frac{h_{ie} h_{oe} - h_{re} h_{fe}}{h_{ie}}$$

$$= \frac{(1410)(0.3537 \times 10^{-4}) - (0.3592 \times 10^{-3})(55.49)}{1410}$$

$$= \underline{0.2125 \times 10^{-4} \text{ mhos}}$$

STAGE 1

Parameter	Correction at V_{ce} = -6.0V, I_c = -0.5 ma. factor	Correction at V_{ce} = -6.0V, I_c = -0.5 ma. value	Correction at V_{ce} = -3.0V, I_c = -0.5 mA. factor	Correction at V_{ce} = -3.0V, I_c = -0.5 mA. value
h_{ib} (ohms)	2	50	1	50
h_{rb}	0.93	0.465×10^{-3}	1.25	0.581×10^{-3}
$1 + h_{fb}$	1.30	0.0221	1.15	0.0254
h_{ob} (mhos)	0.7	0.435×10^{-6}	1.05	0.457×10^{-6}

$$h_{ie} = \frac{50}{0.0254} = 1969 \text{ ohms}$$

$$h_{re} = \frac{50 \times 0.457 \times 10^{-6} + 0.581 \times 10^{-3}\ (0.975) - 0.581 \times 10^{-3}}{0.0254}$$

$$= \underline{\underline{0.3186 \times 10^{-3}}}$$

$$h_{fe} = \frac{0.9746}{0.0254} = \underline{\underline{38.37}}$$

$$h_{oe} = \frac{0.457 \times 10^{-6}}{0.0254} = \underline{\underline{0.1799 \times 10^{-4}\ \text{mhos}}}$$

$$Y_{ie} = \frac{1}{1969} = \underline{\underline{0.508 \times 10^{-3}\ \text{mhos}}}$$

$$Y_{re} = \frac{-0.3186 \times 10^{-3}}{1969} = \underline{\underline{-0.1619 \times 10^{-6}\ \text{mhos}}}$$

$$Y_{fe} = \frac{38.37}{1969} = \underline{\underline{0.1949 \times 10^{-1}\ \text{mhos}}}$$

$$Y_{oe} = \frac{(1916)\ (0.1799 \times 10^{-4}) - (38.37)\ (0.3186)}{1969}$$

$$= \underline{\underline{0.1178 \times 10^{-4}\ \text{mhos}}}$$

RAYTHEON TYPE 2N414 *P-N-P* GERMANIUM JUNCTION TRANSISTOR

The 2N414 is a medium gain PNP fusion alloy junction transistor especially intended for high frequency amplifier applications up to 8 megacycles. This transistor features rigid processing control to insure reliability and stability of electrical characteristics. Reliable hermetic sealing is assured by use of a welded package.

MECHANICAL DATA

Case: Metal
Base: Metal with glass eyelets. 0.017″ silver plated flexible leads.
Length: 1.5″ min. Spacing: 90° on 0.200″ circle diameter.
Terminal Connections:
Lead 1 Emitter
Lead 2 Base
Lead 3 Collector
Mounting Position: Any

ELECTRICAL DATA

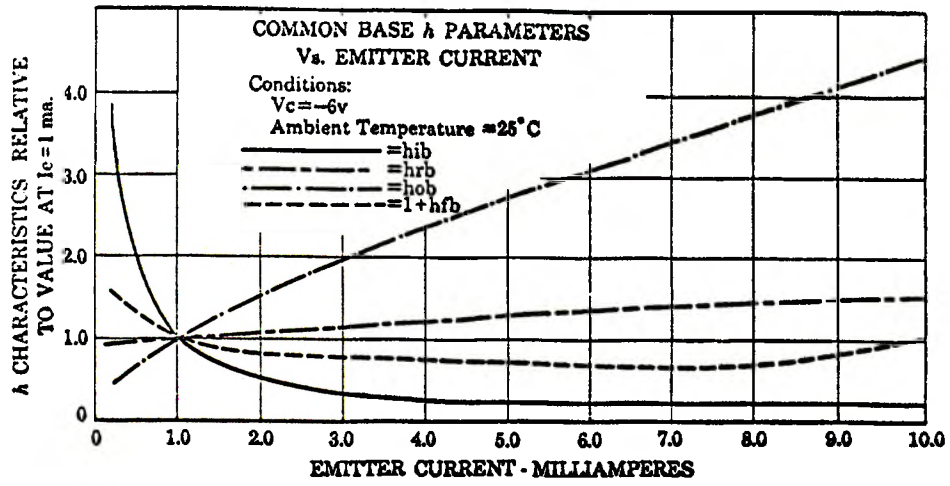
Absolute Maximum Ratings:

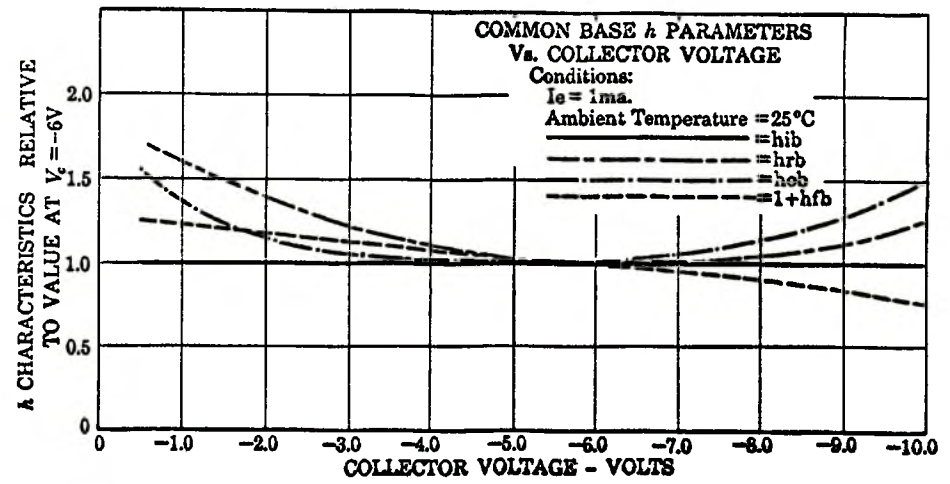
Collector to Base Voltage (Emitter Open)	−30 volts
Emitter to Base Voltage (Collector Open)	−20 volts
Collector to Emitter Voltage (Base Open)	−15 volts
Collector to Emitter Voltage (V_{BE} = +0.1 volt)	−20 volts
DC Collector Current	−200 ma
Peak Collector Current	−400 ma
Dissipation Coefficient (in air) Ka*	0.4 °C/mw
Dissipation Coefficient (in sink) Ks*	0.18 °C/mw
Junction Temperature (Operating or Storage)	−65 to +85 °C
Lead Temperature (at $\frac{1}{16}$″ ± $\frac{1}{32}$″ from case)	240 °C for 10 seconds

Characteristics: @25° C (V_{CB} = −6 V, I_E = 1 ma, f = 1 Kc, except as noted)

Parameter	*Sym.*	*Conditions*	*Design Values* *Min.*	*Avg.*	*Max.*	*Units*
Collector Cutoff Current	I_{CO}	V_{CB} = −12 V	....	−2.0	−5.0	μa
Emitter Cutoff Current	I_{EO}	V_{EB} = −12 V	....	−2.0	−5.0	μa
Input Impedance	hib		....	25	....	ohms
Base Current Gain	hfe	V_{CE} = −6 V	....	60	....	....
Voltage Feedback Ratio	hrb		....	0.5	....	$\times 10^{-3}$
Output Admittance	hob		....	0.62	....	μmhos
Alpha Cutoff Frequency	fαb		....	7	....	Mc
Collector Capacitance	Cob	f = 2 Mc	....	12	....	μμf
Extrinsic Base Resistance	rb″	f = 2 Mc	....	55	....	ohms
Noise Figure	N.F.	V_{CE} = −6 V, f = 1.5 Mc	....	6	....	DB
Power Gain	Gp	V_{CE} = −6 V, f = 1.5 Mc	....	16	....	DB

* Maximum allowable total transistor power dissipation at any ambient temperature is given by the relation: P = (Max. $Tj - Ta)/K$ where Tj is junction temperature, Ta is ambient temperature and K is the dissipation coefficient.


COMMON BASE h PARAMETERS
Vs. EMITTER CURRENT
Conditions:
Vc=-6v
Ambient Temperature =25°C
=hib
=hrb
=hob
=1+hfb
h CHARACTERISTICS RELATIVE TO VALUE AT Ie=1 ma.
4.0
3.0
2.0
1.0
0
0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0
EMITTER CURRENT - MILLIAMPERES


COMMON BASE h PARAMETERS
Vs. COLLECTOR VOLTAGE
Conditions:
Ie = 1ma.
Ambient Temperature =25°C
=hib
=hrb
=hob
=1+hfb
h CHARACTERISTICS RELATIVE TO VALUE AT Vc=-6V
2.0
1.5
1.0
0.5
0
0 -1.0 -2.0 -3.0 -4.0 -5.0 -6.0 -7.0 -8.0 -9.0 -10.0
COLLECTOR VOLTAGE - VOLTS

APPENDIX B

COMPUTER RESULTS

The node voltages calculated by the computer at 1 kc for different values of emitter resistance R_{E1} are shown in table 5.

Input voltage = 7.0 mV.

Node Voltage (mV)	Value of Emitter Resistance (ohms)						
	100	150	200	250	300	400	500
e_{1R}	6.935	6.950	6.958	6.963	6.966	6.969	6.972
e_{1I}	0.0248	0.0169	0.0129	0.0104	0.0088	0.0067	0.0054
e_{2R}	6.816	6.868	6.895	6.911	6.922	6.936	6.943
e_{2I}	0.0813	0.0552	0.0417	0.0336	0.0281	0.0213	0.0171
e_{3R}	-2.775	-1.870	-1.412	-1.137	-0.952	-0.722	-0.5832
e_{3I}	1.482	1.003	0.758	0.609	0.509	0.384	0.308
e_{4R}	0.0718	0.0487	0.0368	0.0296	0.0247	0.0186	0.0149
e_{4I}	0.1713	0.1154	0.0871	0.0701	0.0586	0.0444	0.0359
e_{5R}	297.6	201.4	152.9	123.8	104.3	80.02	65.41
e_{5I}	-345.7	-233.1	-175.7	-140.9	-117.6	-88.47	-70.85

Table 5.

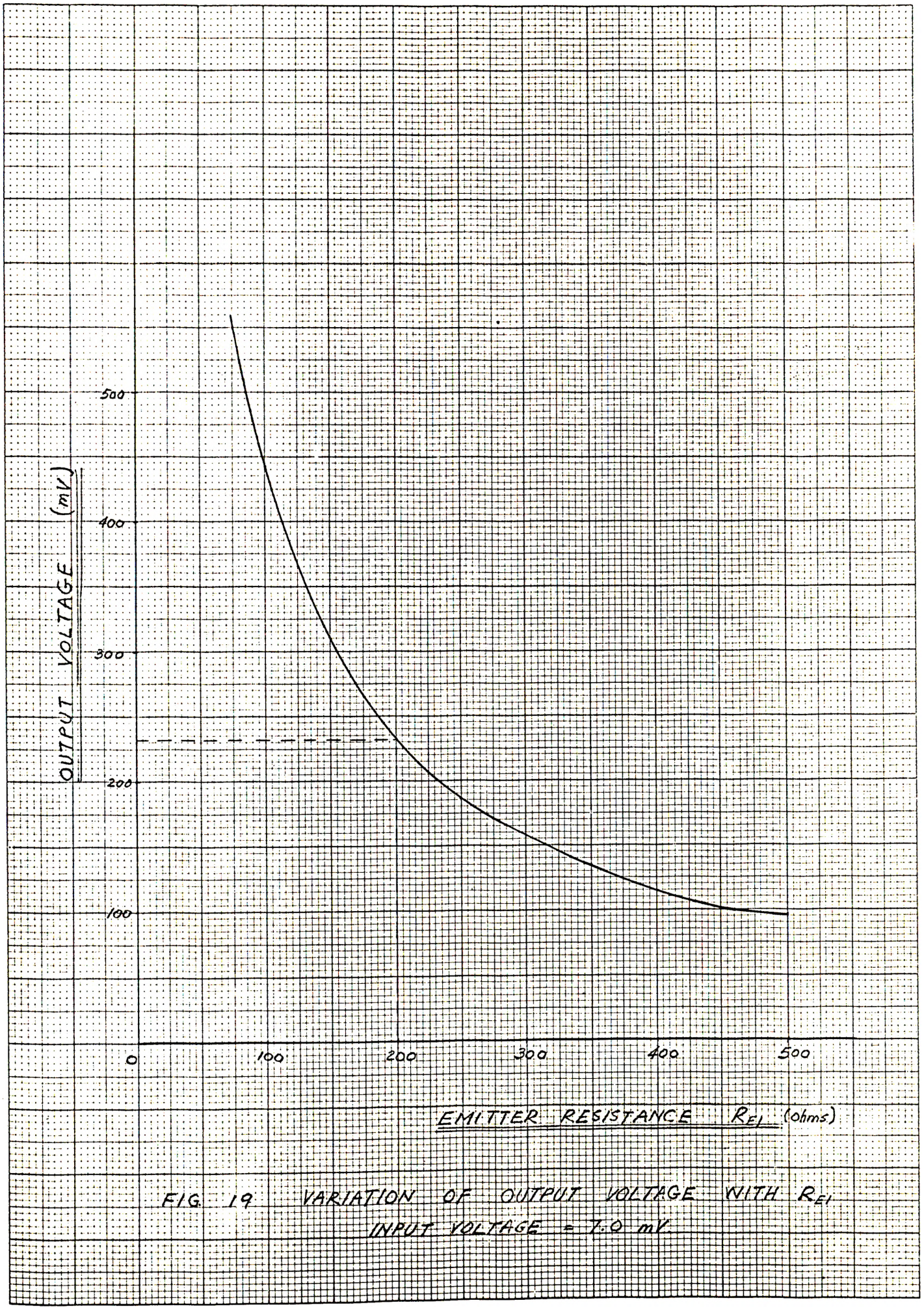


FIG. 19 VARIATION OF OUTPUT VOLTAGE WITH R_{E1}
INPUT VOLTAGE = 1.0 mV.

Table 6. Node voltages of the circuit for different frequencies.

e_s = 7.0 mV.

R_s = 800 ohms

Node Voltage (volts)	Signal frequency (cps) 20	30	50	70	100
e_{1R}	6.999E-3*	6.960E-3	6.933E-3	6.958E-3	6.953E-3
e_{1I}	3.115E-4	2.236E-4	1.468E-4	1.050E-4	8.036E-5
e_{2R}	6.608E-3	6.627E-3	6.693E-3	6.776E-3	6.819E-3
e_{2I}	4.938E-4	4.237E-4	3.499E-4	2.900E-4	2.324E-4
e_{3R}	-3.683E-3	-1.900E-3	-1.282E-3	-1.274E-3	-1.355E-3
e_{3I}	2.922E-2	1.907E-2	1.101E-2	7.715E-3	5.297E-3
e_{4R}	5.875E-3	6.333E-3	4.644E-3	3.177E-3	1.876E-3
e_{4I}	2.679E-2	1.545E-2	6.713E-3	3.626E-3	1.861E-3
e_{5R}	2.267E+0	1.923E+0	1.321E+0	9.359E-1	6.180E-1
e_{5I}	-6.516E-1	-9.587E-1	-1.130E+0	-1.017E+0	-9.004E-1

* 6.999E-3 = 6.999×10^{-3}

Table 6. (continued)

Node Voltage (volts)	Signal frequency (cps) 200	300	500	1000	2000
e_{1R}	6.948E-3	6.959E-3	6.967E-3	6.958E-3	6.961E-3
e_{1I}	4.377E-5	2.978E-5	1.949E-5	1.288E-5	9.982E-6
e_{2R}	6.863E-3	6.884E-3	6.898E-3	6.895E-3	6.907E-3
e_{2I}	1.326E-4	9.266E-5	6.182E-5	4.176E-5	3.302E-5
e_{3R}	-1.468E-3	-1.490E-3	-1.490E-3	-1.412E-3	-1.231E-3
e_{3I}	2.636E-3	1.797E-3	1.169E-3	7.583E-4	5.755E-4
e_{4R}	5.586E-4	2.648E-4	1.073E-4	3.680E-5	1.475E-5
e_{4I}	5.954E-4	3.468E-4	1.907E-4	8.711E-5	3.796E-5
e_{5R}	3.039E-1	2.329E-1	1.913E-1	1.529E-1	9.946E-2
e_{5I}	-5.346E-1	-3.797E-1	-2.563E-1	-1.756E-1	-1.407E-1

Table 6. (continued)

Node Voltage (volts)	Signal frequency (cps) 3000	5000	7000	10000	15000
e_{1R}	6.963E-3	6.966E-3	6.966E-3	6.967E-3	6.967E-3
e_{1I}	8.147E-6	5.749E-6	4.375E-6	3.146E-6	2.130E-6
e_{2R}	6.915E-3	6.922E-3	6.925E-3	6.927E-3	6.927E-3
e_{2I}	2.737E-5	1.943E-5	1.473E-5	1.064E-5	7.198E-6
e_{3R}	-1.104E-3	-9.885E-4	-9.446E-4	-9.182E-4	-8.996E-4
e_{3I}	4.721E-4	3.324E-4	2.508E-4	1.811E-4	1.226E-4
e_{4R}	8.219E-6	3.513E-6	1.900E-6	9.625E-7	4.338E-7
e_{4I}	2.288E-5	1.240E-5	8.499E-6	5.799E-6	3.794E-6
e_{5R}	6.493E-2	3.343E-2	2.153E-2	1.440E-2	1.032E-2
e_{5I}	-1.176E-1	-8.376E-2	-6.341E-2	-4.589E-2	-3.105E-2

Table 7. Node voltages of the circuit with frequency dependent feedback loop open.

e_S = 7.0 mV.

Node Voltage (volts)	Signal frequency (cps)	
	20	1000
e_{1R}	6.442E-3	6.550E-3
e_{1I}	1.577E-5	8.364E-4
e_{2R}	5.118E-3	5.210E-3
e_{2I}	1.334E-5	7.025E-4
e_{3R}	-3.195E-2	-5.657E-2
e_{3I}	1.671E-3	7.302E-2
e_{4R}	-1.219E-5	-2.688E-2
e_{4I}	1.862E-3	8.185E-2
e_{5R}	5.120E+0	7.101E+0
e_{5I}	3.075E-2	2.121E+0

Table 8. Node voltages of the circuit with test generator applied to the output node and the input generator replaced by its internal resistance. Assumption: test generator voltage = 235 mV, test generator resistance = 600 ohms.

Node Voltage (volts)	Signal frequency (cps)
	1000
e_{1R}	1.514E-4
e_{1I}	-2.059E-6
e_{2R}	5.219E-4
e_{2I}	4.792E-6
e_{3R}	9.468E-3
e_{3I}	-4.011E-4
e_{4R}	1.146E-5
e_{4I}	-6.034E-4
e_{5R}	4.363E-2
e_{5I}	-5.258E-2

The loop amplitude and phase characteristics are shown in table 9.

TABLE 9

frequency (cps)	Real part	Imaginary part	$\lvert\bar{\beta}\,\bar{A}\rvert$ (db)	Phase angle (degrees)
0.1000 E+2	0.1859 E+0	0.9626 E+0	-0.1724 E+0	0.7894 E+2
0.2000 E+2	0.4775 E+0	0.1658 E+1	0.4739 E+1	0.7381 E+2
0.3000 E+2	0.6908 E+0	0.2229 E+1	0.7362 E+1	0.7266 E+2
0.4000 E+2	0.8459 E+0	0.2777 E+1	0.9257 E+1	0.7294 E+2
0.5000 E+2	0.9772 E+0	0.3327 E+1	0.1080 E+2	0.7351 E+2
0.1000 E+3	0.1683 E+1	0.6096 E+1	0.1602 E+2	0.7444 E+2
0.5000 E+3	0.1227 E+2	0.1974 E+2	0.2732 E+2	0.5804 E+2
0.1000 E+4	0.1986 E+2	0.2537 E+2	0.3016 E+2	0.5187 E+2
0.2000 E+4	0.2419 E+2	0.3680 E+2	0.3288 E+2	0.5659 E+2
0.3000 E+4	0.2612 E+2	0.5037 E+2	0.3508 E+2	0.6249 E+2
0.5000 E+4	0.3005 E+2	0.7943 E+2	0.3858 E+2	0.6916 E+2
0.1000 E+5	0.4636 E+2	0.1534 E+3	0.4409 E+2	0.7306 E+2
0.2000 E+5	0.1085 E+3	0.2915 E+3	0.4986 E+2	0.6947 E+2
0.3000 E+5	0.2040 E+3	0.4055 E+3	0.5314 E+2	0.6320 E+2
0.4000 E+5	0.3226 E+3	0.4878 E+3	0.5534 E+2	0.5642 E+2
0.5000 E+5	0.4533 E+3	0.5351 E+3	0.5692 E+2	0.4964 E+2
0.6000 E+5	0.5854 E+3	0.5482 E+3	0.5808 E+2	0.4305 E+2
0.7000 E+5	0.7103 E+3	0.5311 E+3	0.5896 E+2	0.3673 E+2
0.8000 E+5	0.8218 E+3	0.4893 E+3	0.5961 E+2	0.3072 E+2
0.9000 E+5	0.9163 E+3	0.4289 E+3	0.6010 E+2	0.2504 E+2
0.1000 E+6	0.9922 E+3	0.3559 E+3	0.6046 E+2	0.1970 E+2
0.1100 E+6	0.1050 E+4	0.2757 E+3	0.6071 E+2	0.1470 E+2
0.1200 E+6	0.1090 E+4	0.1926 E+3	0.6088 E+2	0.1001 E+2
0.1300 E+6	0.1114 E+4	0.1100 E+3	0.6098 E+2	0.5629 E+1
0.1400 E+6	0.1125 E+4	0.3022 E+2	0.6103 E+2	0.1536 E+1
0.1500 E+6	0.1125 E+4	-0.4502 E+2	0.6103 E+2	-0.2288 E+1
0.1600 E+6	0.1115 E+4	-0.1147 E+3	0.6099 E+2	-0.5862 E+1
0.1700 E+6	0.1099 E+4	-0.1783 E+3	0.6093 E+2	-0.9203 E+1
0.1800 E+6	0.1077 E+4	-0.2357 E+3	0.6084 E+2	-0.1233 E+2
0.1900 E+6	0.1050 E+4	-0.2869 E+3	0.6074 E+2	-0.1525 E+2
0.2000 E+6	0.1021 E+4	-0.3322 E+3	0.6062 E+2	-0.1800 E+2
0.2100 E+6	0.9894 E+4	-0.3720 E+3	0.6048 E+2	-0.2057 E+2
0.2400 E+6	0.8900 E+3	-0.4621 E+3	0.6002 E+2	-0.2739 E+2
0.2600 E+6	0.8242 E+3	-0.5022 E+3	0.5969 E+2	-0.3130 E+2
0.3000 E+6	0.7025 E+3	-0.5485 E+3	0.5900 E+2	-0.3792 E+2
0.3500 E+6	0.5750 E+3	-0.5655 E+3	0.5813 E+2	-0.4454 E+2
0.4000 E+6	0.4739 E+3	-0.5582 E+3	0.5729 E+2	-0.4958 E+2
0.5000 E+6	0.3321 E+3	-0.5153 E+3	0.5575 E+2	-0.5710 E+2
0.6000 E+6	0.2428 E+3	-0.4646 E+3	0.5439 E+2	-0.6230 E+2
0.9000 E+6	0.1154 E+3	-0.3425 E+3	0.5116 E+2	-0.7126 E+2
0.1100 E+7	0.7866 E+2	-0.2878 E+3	0.4980 E+2	-0.7459 E+2
0.1400 E+7	0.4926 E+2	-0.2309 E+3	0.4746 E+2	-0.7783 E+2
0.2200 E+7	0.2022 E+2	-0.1500 E+3	0.4360 E+2	-0.8218 E+2
0.2800 E+7	0.1253 E+2	-0.1184 E+3	0.4152 E+2	-0.8382 E+2

Table 9 (continued)

frequency (cps)	Real part	Imaginary part	$/ \bar{\beta}\ \bar{A} /$ (db)	Phase angle (degrees)
0.3500 E+7	0.8036 E+1	-0.9504 E+2	0.3959 E+2	-0.8052 E+2
0.4000 E+7	0.6158 E+1	-0.8327 E+2	0.3843 E+2	-0.8563 E+2
0.1000 E+8	0.9876 E+1	-0.3342 E+2	0.3048 E+2	-0.8816 E+2
0.2000 E+8	0.2470 E+0	-0.1672 E+2	0.2447 E+2	-0.8900 E+2
0.5000 E+8	0.3952 E-1	-0.6689 E+1	0.1651 E+2	-0.8951 E+2
0.1000 E+9	0.9881 E-2	-0.3345 E+1	0.1049 E+2	-0.8968 E+2
0.2000 E+9	0.2470 E-2	-0.1672 E+1	0.4466 E+1	-0.8977 E+2
0.3000 E+9	0.1098 E-2	-0.1115 E+1	0.9443 E+0	-0.8979 E+2
0.3300 E+9	0.9073 E-3	-0.1013 E+1	0.1164 E+0	-0.8980 E+2
0.4000 E+9	0.6176 E-3	-0.8361 E+0	-0.1554 E+1	-0.8981 E+2

STABILITY FACTORS

From equation (13),

$$I_B = \frac{I_C - (\beta + 1)\, I_{CBo}}{\beta}$$

Substituting for I_B into equations (14a), (15a) and (16a) gives

$$V_{cc1} = A_{11} I_{c1} + A_{12} I_{c2} - A_{13} I_{cBo} + R_{E1} I_{f2} \quad \ldots\ldots \text{(14b)}$$

where

$$A_{11} = R_{c1} + \frac{R_{f1}}{\beta_1} + R_{E1} + \frac{R_{E1}}{\beta_1}$$

$$A_{12} = \frac{R_{c1}}{\beta_2}$$

$$A_{13} = \frac{(\beta_2 + 1)}{\beta_2} R_{c1} + \frac{(\beta_1 + 1)}{\beta_1} R_{f1} + \frac{(\beta_1 + 1)}{\beta_1} R_{E1}$$

$$V_{cc1} = A_{21} I_{c1} + A_{22} I_{c2} - A_{23} I_{cBo} \quad \ldots\ldots \text{(15b)}$$

where

$$A_{21} = R_{c1} - \frac{R_{E2}}{\beta_1}$$

$$A_{22} = \frac{R_{c1}}{\beta_2} + R_{E2} + \frac{R_{E2}}{\beta_2}$$

$$A_{23} = \frac{R_{c1}(\beta_2 + 1)}{\beta_2} + \frac{R_{E2}(\beta_2 + 1)}{\beta_2} - \frac{(\beta_1 + 1)}{\beta_1} R_{E2}$$

$$V_{cc2} = A_{31} I_{c1} + A_{32} I_{c2} - A_{33} I_{cBo} + A_{34} I_{f2} \quad \ldots\ldots \text{(16b)}$$

where

$$A_{31} = R_{E1} + \frac{R_{E1}}{\beta_1}$$

$$A_{32} = R_{c2}$$

$$A_{33} = \frac{(\beta_1 + 1)\, R_{E1}}{\beta_1}$$

$$A_{34} = (R_{c2} + R_{f2} + R_{E1})$$

From equation (16b),

$$I_{f2} = \frac{V_{cc2} - A_{31} I_{c1} - R_{c2} I_{c2} + A_{33} I_{cBO}}{A_{34}}$$

Substituting for I_{f2} into equation (14b) gives

$$V_{cc1} = B_{11} I_{c1} + B_{12} I_{c2} + B_{13} I_{CBo} + \frac{R_{E1}}{A_{34}} V_{cc1} \quad \ldots\ldots \quad (14c)$$

where

$$B_{11} = A_{11} - \frac{R_{E1} A_{31}}{A_{34}}$$

$$B_{12} = A_{12} - \frac{R_{E1} R_{c2}}{A_{34}}$$

$$B_{13} = \frac{R_{E1} A_{33}}{A_{34}} - A_{13}$$

From equation (15b),

$$I_{c2} = \frac{V_{cc1} - A_{21} I_{c1} + A_{23} I_{cBo}}{A_{22}}$$

Substituting for I_{c2} into equation (14c) and differentiating I_{c1} with respect to I_{cBo} gives

$$S_1 = \frac{d I_{c1}}{I_{cBo}} = \frac{B_{13} + \frac{B_{12} A_{23}}{A_{22}}}{\frac{B_{12} A_{21}}{A_{22}} - B_{11}}$$

From equation (15b),

$$I_{c1} = \frac{V_{cc1} - A_{22} I_{c2} + A_{23} I_{cBo}}{A_{21}}$$

Substituting for I_{c1} into equation (14c) and differentiating I_{c2} with respect to I_{CBo} gives

$$S_2 = \frac{dI_{c2}}{I_{CBo}} = \frac{-B_{13} - \frac{B_{11} A_{22}}{A_{21}}}{B_{12} - \frac{B_{11} A_{22}}{A_{21}}}$$

The values of R_{E1}, R_{E2}, R_{c1}, R_{c2}, R_{f1}, R_{f2}, β_1 and β_2 were substituted into the expressions for S_1 and S_2. The computed values are:

$$S_1 = \frac{dI_{c1}}{dI_{CBo}} = 11.1$$

$$S_2 = \frac{dI_{c2}}{dI_{CBo}} = -64.9$$

APPENDIX C

EXPERIMENTAL DATA

List of Equipment used.

Tektronix Type 516 Cathode Ray Oscilloscope
Z-Angle Meter Type 310-B
H/P Audio Oscillator Model 200 AB
Electro Filtered Power Supply
RCA VTVM Model Wv-98A

D.C. Measurements

$V_{cc2} = -16.0$ V
$V_{cc2} - V_{c1} = -7.8$ V
$V_{cB2} = -5.3$ V
$V_{EE2} = -2.9$ V
$V_{cc1} = -14.55$ V
$V_{cc1} - V_{c1} = -11.6$ V
$V_{cE1} = -2.95$ V
$V_{EE1} = -0.11$ V

Input and Output Impedance Measurement

Test frequency = 1000 cps.
Voltage at unknown terminals = 40 mv.
No indication of distortion at output.

$Z_c = Z_i \,//\, 100$ K

$\lvert Z_c \rvert$	θ_c	$\lvert Z_i \rvert$	θ_i
53.8 KΩ	4.5°	116 KΩ	10°

Table 10. Input impedance measurements.

$\lvert Z_o \rvert$	θ_o
192 Ω	-49°

Table 11. Output impedance measurements.

Frequency Response and Phase Shift Measurement

Input Voltage = 7.0 mV

Frequency (cps)	Output Voltage (volts)	Gain (db)	Phase Shift (degrees)
20	2.6	52.8	18.8
30	2.3	50.4	31.0
50	1.85	48.3	44.2
70	1.53	46.5	50.4
100	1.15	44.3	57.3
200	0.650	39.4	60.0
300	0.460	36.4	59.5
500	0.320	33.2	52.7
700	0.280	31.7	51.4
1000	0.235	30.5	48.8
2000	0.175	28.0	52.8
3000	0.135	25.7	61.8
5000	0.090	22.2	69.7
7000	0.070	20.0	73.1
10000	0.050	17.1	74.0
15000	0.033	13.3	73.9
20000	0.225	9.65	68.6

Table 12. Frequency response and phase shift measurements.

PHOTOGRAPHS OF WAVEFORMS

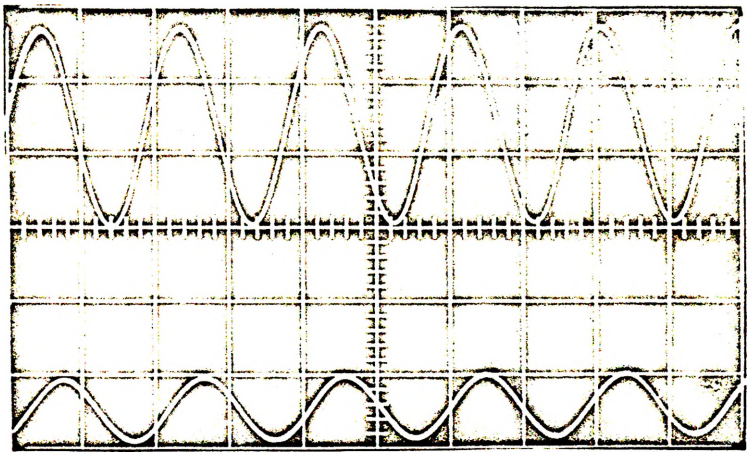


Fig. 20a. Waveforms at 1 kc.

A Input waveform, scale: 5 volts per division.

B Output waveform, scale: 0.5 volts per division.

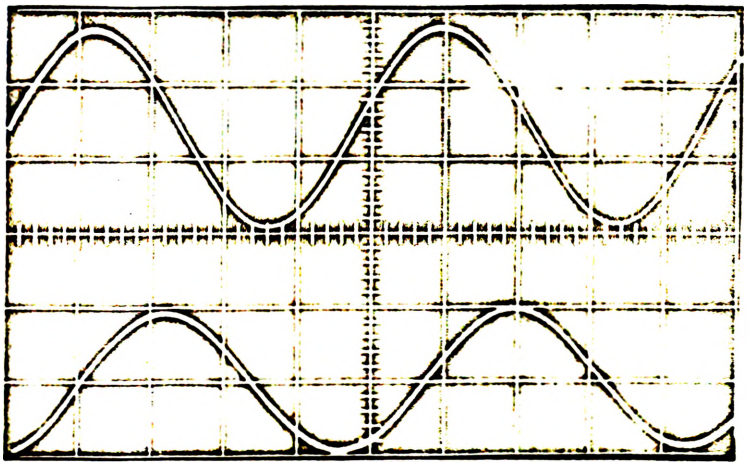


Fig. 20b. Waveforms at 10 kc.

A Input waveform, scale: 5 volts per division.

B Output waveform, scale: 0.05 volts per division.

BIBLIOGRAPHY

1. Tremaine, H. M., The Audio Cyclopedia, Bob-Merril Inc., New York, 1959, pp. 429-435.

2. Desoer, C. A., "Design of Lossy Ladder Filters by Digital Computer", IRE Transactions on Circuit Theory, Vol. CT-8, March, 1961, pp. 192-201.

3. Goldstick, G. H. and Kawahara, M., "Application of the NCR Data Processor to the Synthesis of a Digital Building Block", IRE National Convention Record, Part 4, March, 1959, pp. 204-217.

4. Brinkerhoff, D. E., "Calculation of the Gain-Frequency Characteristic of a Multi-Mesh Transistor Stage using a programmed Computer," IRE International Convention Record, Part 7, March, 1960, pp. 73-79.

5. Purnhagen, T. G. and Lubelfeld, J., "A Computer Approach to Laser Design", IEEE Transactions on Electron Devices, Vol. ED-11, May, 1964, pp. 219-228.

6. Drew, L. C. and Atwood, A. G., "Using the Computer for Integrated Circuit Analysis", Electronic Industries, July, 1964, pp. 52-57.

7. Bode, H., Analysis and Feedback Amplifier Design", Van Nostrand Inc., New York, 1945.

8. Ghandhi, S. K., "Bias Considerations in Transistor Circuit Design", IRE Transactions on Circuit Theory, Vol. CT-4, September, 1957, pp. 194-202.

9. Mulligan, H. H., Jr. and Shamis, S. S., "Transistor Amplifier Stages with Prescribed Gain and Static and Dynamic Sensitivity", AIEE Transactions on Communication and Electronics, Vol. 80, Part I, 1961, pp. 335-339.

10. Millman, J., Vacuum-Tube and Semiconductor Electronics, McGraw-Hill Inc., 1958, pp. 234-235.

11. Berkum, P. A. and Herick, D. J., "A Two-Stage D.C. coupled Transistor Video Amplifier", IRE Transactions on Broadcast and Television Receivers, Vol. BTR-7, November, 1961, pp. 72-79.

12. Ryder, J. D., Engineering Electronics, McGraw-Hill Inc., New York, 1958, pp. 196-203.

13. Fitchen, F. C., Transistor Circuit Analysis and Design, Van Nostrand Inc., New York, 1960.

14. Walston, J. A. and others, Transistor Circuit Design, McGraw-Hill Inc., New York, 1963, pp. 96-101.

15. Gibson, J. E. and Tuteur, F. B., Control System Components, McGraw-Hill Inc., 1958, pp. 13-109.

VITA

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