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Real time testing with a time scaled analog computer.

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Department:

REAL TIME TESTING WITH A TIME SCALED ANALOG COMPUTER

BY

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THESIS

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ABSTRACT

A present limitation to the testing of a physical subsystem within an analog simulation is that the analog computer must compute in real time. If it is necessary to time scale the simulation of the complete system, a physical subsystem of the complete system may not be tested within the simulation. Therefore, a means of changing the time scale of the analog signal is needed to test a physical subsystem within a time scaled analog computer simulation.

In this thesis a means of time conversion by sampling the analog signal at one rate, storing the samples, and reading the samples out at another rate is presented. A closed loop test procedure is presented which requires that the analog signal be converted to real time before applying to the physical subsystem under test, and the output of the subsystem is converted to computer time before being fed back into the analog simulation. The effect of errors in time conversion on the entire system is also considered.

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CHAPTER I

INTRODUCTION

A. Analog Simulations and Testing

An analog simulation is one of the most powerful tools available to an engineer for the testing of a design before and after system construction. Such simulations can include the overall dynamic characteristics of a system, or they can simulate the physical components themselves, part by part. A very valuable technique for analog simulations is the replacement of components and subsystems by the actual devices, and testing under conditions closely approximating actual operating conditions. This technique considerably reduces the time required to arrive at a satisfactory design, and is also economical because the entire system does not have to be constructed before testing.

For example, in the testing of a breadboard design of an autopilot, as described by Prince (13), the airplane, gyro, and airplane control system are simulated on the analog computer. Such a simulation is diagrammed in Figure 1. In this test the simulated response of the gyro to the simulated airplane motion is fed into the breadboard design of the autopilot, and the output of the autopilot is supplied to the simulation of the airplane control system. The simulated output of the control system is then fed back into the simulation of the airplane. By this simulation large amounts of data can be obtained quickly in a form that can be readily interpreted by an engineer, and the decision to conduct flight tests of the design can be based on the success of the simulator studies. Thus, much time and money can be saved by testing the design without construction of the complete system.

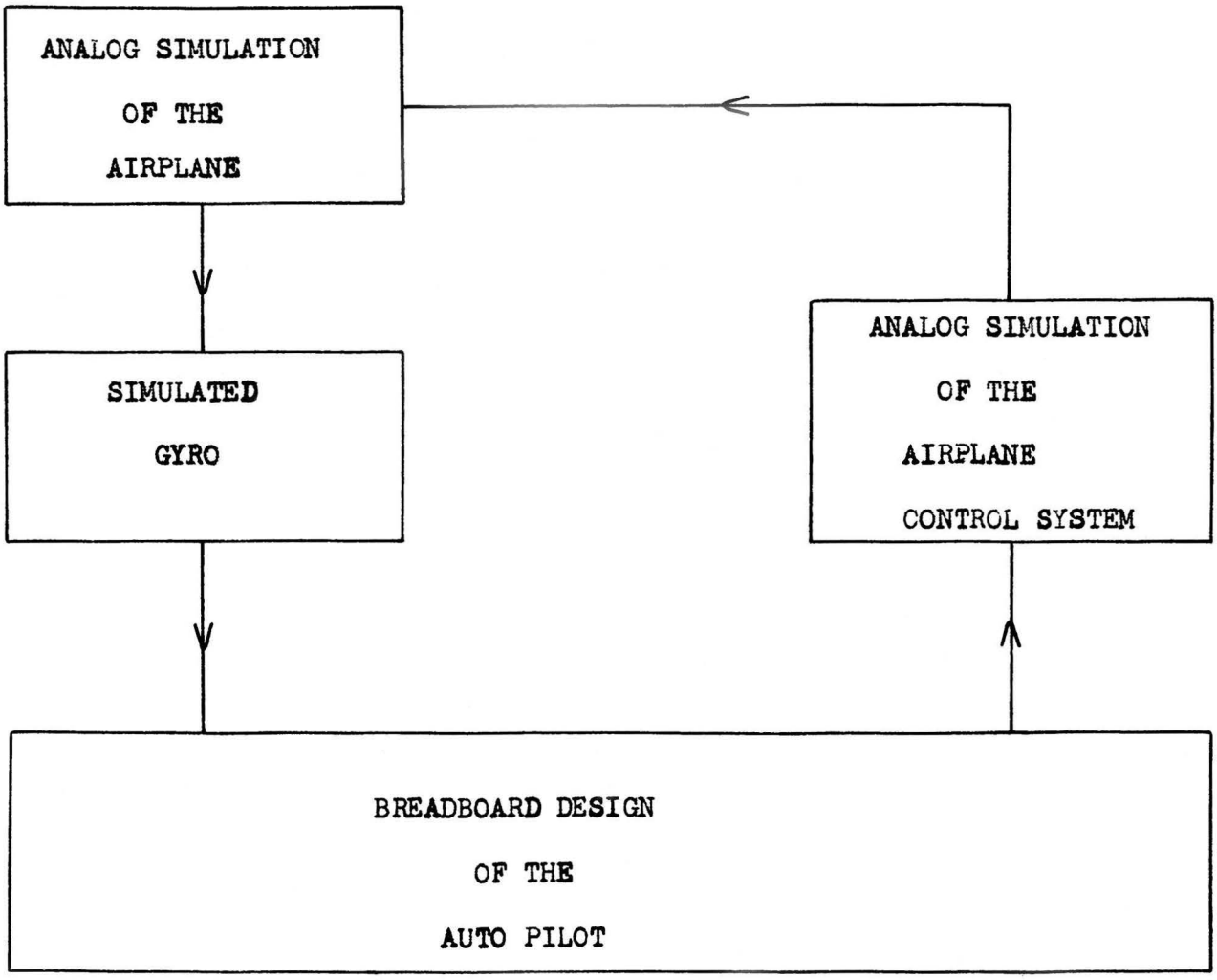

FIGURE 1

Simulation setup to evaluate the performance of a breadboard design of an autopilot

B. Limitations of Analog Testing

A definite limitation in testing a physical subsystem with an analog simulation is that the analog computer must operate in real time. This detracts greatly from the advantages of analog simulations because in a simulated model time may be scaled. When physical subsystems are tested in the simulated model, conditions must be employed that closely approximate environmental conditions. Thus, real time operation is required. In the simulation setup of Figure 1 the analog simulation of the airplane, gyro, and the airplane control system must compute in real time to test the breadboard design of the autopilot. In a time scaled analog simulation actions that are too fast to follow on the computer may be slowed down to operate on the computer, and actions that are too slow may be sped up to computer speeds.

C. Object of the Thesis

The object of this thesis is to present a method of testing a physical subsystem with an analog computer simulation computing slower than real time. Such a method is diagrammed in Figure 2.

In the simulation setup of Figure 2 a computation cycle is performed by the repetitive, slow speed, analog simulation and the output of the simulation is fed into a time compression circuit. The time compression circuit converts the slow computer time to real time. Then the real time signal is applied to the physical subsystem under test, and the output is converted to computer time by the time extension circuit. At the same time the output of the time extension circuit is fed back into the analog simulation and another computation cycle is started. By repeating the computation cycles the system will reach a solution. However, in some cases the system may diverge rather than converge,

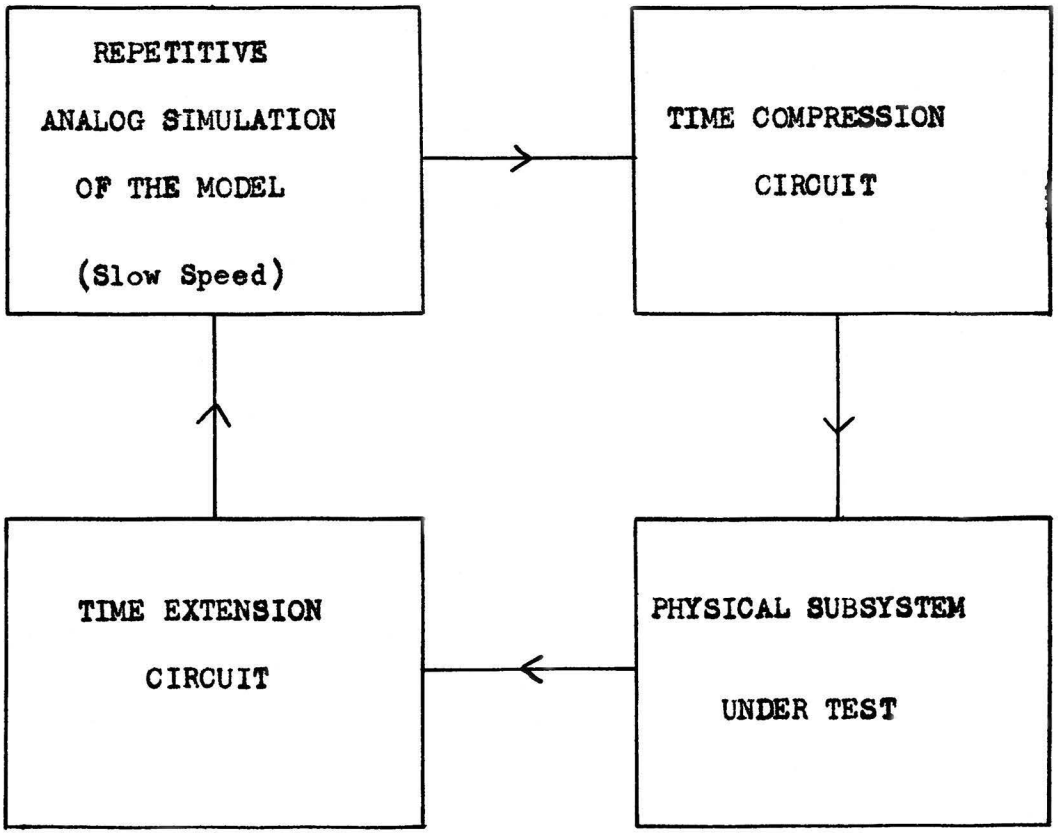

FIGURE 2

Simulation setup to test a physical subsystem with a slow speed analog simulation of the model

and no solution will be obtained. When a solution is reached, useful data for the physical subsystem are obtained.

This thesis presents a method for converting the time scale of a signal by sampling the analog signal at one rate, storing the samples in a memory, and reading the samples out at another rate. A closed-loop test procedure is presented in which the output of the simulation is time compressed before applying to the physical subsystem under test, and the output of the subsystem is time extended before being fedback into the analog simulation. The effect of errors in time conversion on the system performance is also presented.

CHAPTER II

REVIEW OF THE LITERATURE

Analog computer simulations are a powerful tool for the testing of complex systems. Such simulations reduce the problem of test measurement and recording to connection of ordinary laboratory instruments, and computers are designed to make the changing of simulated process effects easy and fast. Simulation testing is also advantageous because the real system need not be constructed for testing. This is economical and leads to better design because all ideas may be tested before construction. Also the time scale may be changed on analog computers. That is, if the simulation frequencies exceed the capabilities of the computer, then a time transformation must be made that slows the simulation down, or speeds it up, whichever is necessary (10) and (15).

By placing breadboard designs of portions of the system in place of their simulated counterparts, the system may be tested futher. Prince (13) points this important factor out in the testing of an autopilot. For this test the motion of the plane, response of the gyro, and the control system are all simulated on an analog computer to test the performance of an autopilot. This method of testing is advantageous in that it is economical and no personnel are endangered by the test. This article also points out that such tests are limited to real time operation of the analog computer.

To achieve more accuracy and higher speeds of operation analog computers have been combined with digital computers for testing (4) and (8). These hybrid computation techniques possess all of the advantages of analog techniques plus the added speed, accuracy, and memory of

digital methods. Truitt (17) has designed an analog-digital computer which is very effective in the prediction and control of missile flight paths.

The use of a high speed iterative analog computer in a control system was first proposed by Ziebolz and Paynter (19) and (20). Their means of control was to first predict the future variable, assuming no change of the disturbances during the computation cycle, and control the high speed model rather than the real plant. The control action is then sampled and the real time plant is controlled with a servo which reduces the control valve travel rate by a factor equal to the ratio of the two time scales.

A special purpose high speed iterative analog computer is commercially available, and its use for high accuracy real time prediction is described by Stern (16). In this process the high speed output of the computer is sampled, the samples are then stored in a memory and readout for a period much greater than the sample period. By this means, a real time version of the high speed output is obtained. The method of sampling the iterative signal and reading the sample out for a long period of time to achieve time extension is achieved by a sample and hold circuit (3), (5) and (9).

In a closed-loop test of a physical subsystem with a time scaled analog computer it is necessary to have both time extension and time compression. The time compression may be achieved by storing the information in an analog form, and reading the information out faster than it was read in (2) and(6). Another method of time compression is to sample the analog signal, convert the samples into a digital code, and compress the coded samples by circulating them through a delay line (14).

In this thesis the time compression method of circulating digital pulses through a delay line loop and a sample and hold circuit are combined with the proper control generators and analog to digital converters to test a physical subsystem with a time scaled analog computer.

CHAPTER III

TIME CONVERSION

A. Introduction

The frequency response of the individual analog elements limits the highest natural frequency which can be simulated with fidelity on an analog computer. When a simulation operates too fast (the operating frequency is above the cutoff frequency) it becomes necessary to slow the simulation down by time scaling. Time scaling may also increase the speed of computation for slow responding systems to the cutoff frequency of the computer. Thus, the output of an analog computer is bandlimited at the cutoff frequency of the computer, f_c.

If a physical subsystem is to be tested within a closed-loop, time scaled, analog simulation, the problem is to convert the output of the computer to real time before applying it to the subsystem under test, and to convert the output of the subsystem back to computer time before feeding it back into the computer. When the computer is operating in slow time it is necessary to first time compress the output of the computer, and then to time extend the signal before feedback into the computer. The steps necessary for time conversion of a bandlimited analog signal with a Fourier transform $F(f)^*$ are determined by sampling the analog signal and changing the frequency of the sampling pulses. If the analog signal is sampled at one rate, the samples stored in a memory device, and readout at a faster rate, the signal is time compressed and the frequency extended. If the samples are read out at

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*The symbolism for the Fourier transform is the same as used by Hancock (7).

a slower rate, the time scale of the signal is extended and the frequency compressed. The Fourier transform is related to the time domain function $f(t)$, by Equation 1.

$$F(f) = \int_{-\infty}^{\infty} f(t) \epsilon^{-j\omega t} dt \tag{1}$$

A time domain function and the corresponding Fourier transform are given in Figures 3 and 4 respectively.

B. Sampling Theory

The signal $f(t)$ is now sampled with a periodic pulse train, $S(t)$, with a unit magnitude. That is, the product of $f(t)$ and $S(t)$ is taken in the time domain. The resultant signal $f(t)\,S(t)$ will appear in the time domain as a periodic pulse train with amplitudes proportional to the amplitude of the signal $f(t)$. This product is illustrated in Figure 5 with the envelope of $f(t)$ superimposed.

The Fourier transform of the sampled signal $f(t)\,S(t)$ is $X(f)$, where

$$X(f) = \int_{-\infty}^{\infty} f(t)\, S(t)\, \epsilon^{-j\omega t} dt \tag{2}$$

From the derivation in Appendix A, $S(t)$ is expressed as a Fourier series of the form

$$S(t) = \sum_{n=-\infty}^{\infty} \frac{\Delta T}{T} \frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{n\omega_0 \frac{\Delta T}{2}} \epsilon^{jn\omega_0 t} \tag{3}$$

where

$$\omega_0 = 2\pi f_0 \tag{4}$$

$$f_0 = \frac{1}{T} \tag{5}$$

and ΔT is the pulse width.

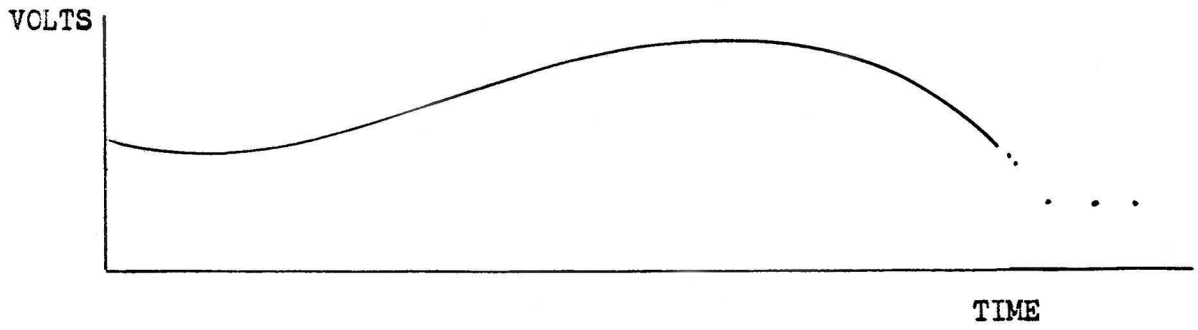


FIGURE 3

A bandlimited analog signal

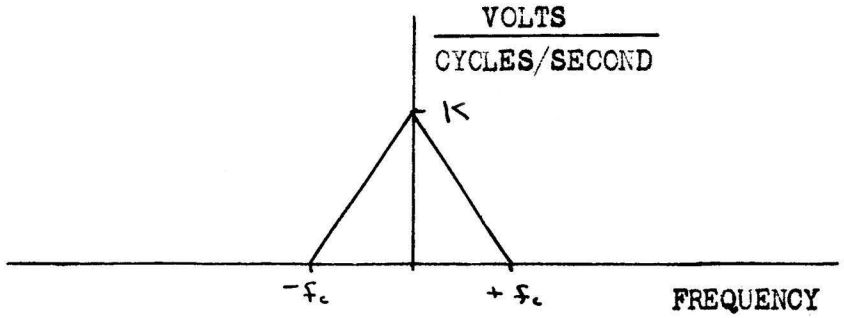


FIGURE 4

Frequency spectrum of the bandlimited analog signal

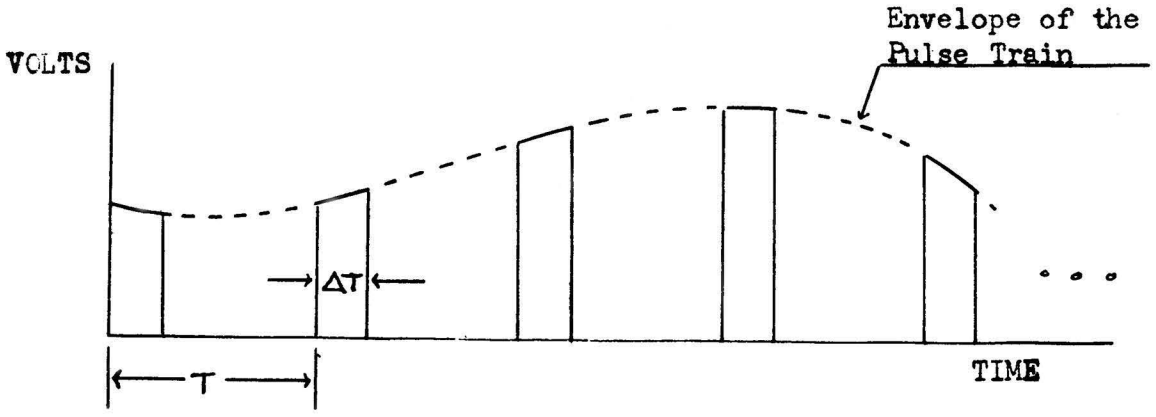


FIGURE 5

Sampled waveform

The sampled signal is then given by

$$x(t) = f(t)\,s(t) = \sum_{n=-\infty}^{\infty} f(t)\,\frac{\Delta T}{T}\,\frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{\left(n\omega_0 \frac{\Delta T}{2}\right)}\,\epsilon^{jn\omega_0 t} \tag{6}$$

and the corresponding Fourier transform becomes

$$X(f) = \int_{-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{\Delta T}{T}\,\frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{\left(n\omega_0 \frac{\Delta T}{2}\right)}\,\epsilon^{-j(-n\omega_0 + \omega)t}\,dt \tag{7}$$

Interchanging the order of the summation and integration leads to

$$X(f) = \frac{\Delta T}{T} \sum_{n=-\infty}^{\infty} \frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{\left(n\omega_0 \frac{\Delta T}{2}\right)} \int_{-\infty}^{\infty} f(t)\,\epsilon^{-j(\omega - n\omega_0)t}\,dt \tag{8}$$

Since $F(f)$ has been expressed as

$$F(f) = \int_{-\infty}^{\infty} f(t)\,\epsilon^{-j\omega t}\,dt \tag{9}$$

the last term of Equation 8 is simply $F(f)$ shifted to $n\omega_0$ or nf_0. This term is then expressed as $F(f - nf_0)$. Thus,

$$X(f) = \frac{\Delta T}{T} \sum_{n=-\infty}^{\infty} \frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{\left(n\omega_0 \frac{\Delta T}{2}\right)}\,F(f - nf_0) \tag{10}$$

A sketch of $X(f)$ versus frequency is given in Figure 6. The magnitude of each of the terms of Equation 10 is determined by the magnitude of the multiplier, $\frac{\sin\left(n\omega_0 \frac{\Delta T}{2}\right)}{\left(n\omega_0 \frac{\Delta T}{2}\right)}$.

From the preceding results, it is apparent that $F(f)$ and consequently $f(t)$ can be reconstructed from $X(f)$ by filtering about zero frequency with a bandwidth of f_c. A restriction on the sampling rate, f_0, is also obtained from Figure 6. The sampling rate must be such that the spectrum about nf_0 does not overlap the spectrum of $(n-1)f_0$. That is,

$$f_0 \geq 2f_c \tag{11}$$

The above derivation does not show how the time scale of a signal may be changed, but how a bandlimited signal may be represented by a train of pulses.

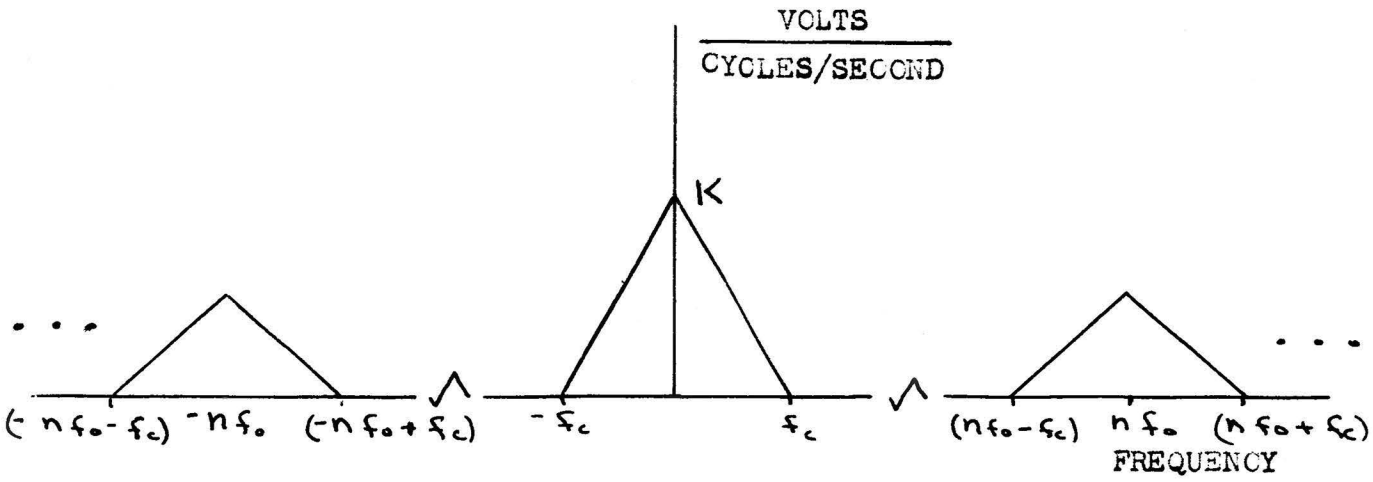


FIGURE 6

The frequency domain of the sampled waveform

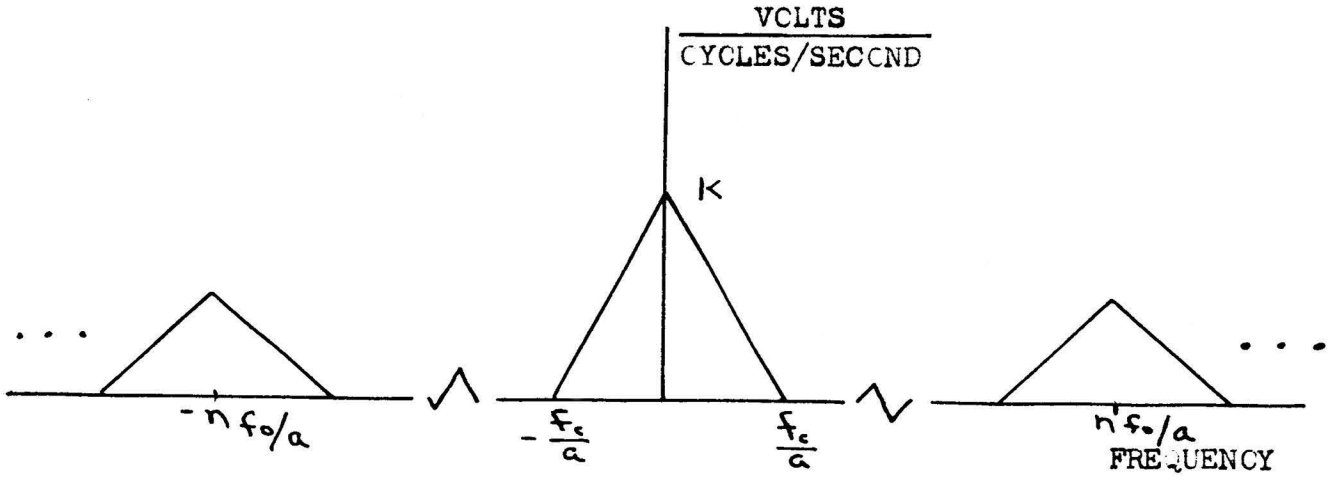


FIGURE 7

The frequency domain of the transformed waveform

C. Time Scale Changing

To change the time scale of the analog signal the frequency of the pulses is changed after the sampling has taken place. The frequency change is achieved by storing the samples in a memory and reading them out at a different rate. That is, the period, T, of the sampling pulse train is compressed or extended to form a new period T', where T' is related to T by

$$T' = a\,T \tag{12}$$

and a is known as the time conversion factor. By changing the period the frequency is also changed.

$$f_o' = \frac{f_o}{a} \tag{13}$$

$$\omega_o' = \frac{\omega_o}{a} \tag{14}$$

By replacing T by T' and ω_o by ω_o' in Equation 6, a new time domain function $x'(t)$ is obtained.

$$x'(t) = \sum_{n=-\infty}^{\infty} f(t)\,\frac{\Delta T}{T'}\,\frac{\sin\left(n\omega_o'\frac{\Delta T}{2}\right)}{\left(n\omega_o'\frac{\Delta T}{2}\right)}\,\epsilon^{j n\omega_o' t} \tag{15}$$

Replacing T' by aT and ω_o' by ω_o/a

$$x'(t) = \sum_{n=-\infty}^{\infty} f(t)\,\frac{\Delta T}{aT}\,\frac{\sin\left(\frac{n\omega_o}{a}\frac{\Delta T}{2}\right)}{\left(\frac{n\omega_o}{a}\frac{\Delta T}{2}\right)}\,\epsilon^{j\frac{n\omega_o}{a}t} \tag{16}$$

The corresponding Fourier transform for the new time domain function becomes

$$X'(f) = \frac{\Delta T}{aT}\sum_{n=-\infty}^{\infty}\frac{\sin\left(\frac{n\omega_o}{a}\frac{\Delta T}{2}\right)}{\left(\frac{n\omega_o}{a}\frac{\Delta T}{2}\right)}\int_{-\infty}^{\infty} f(t)\,\epsilon^{-j(\omega-\frac{n\omega_o}{a})t}\,dt \tag{17}$$

From the above equation it is noted that changing the period after sampling changes the scale of $X(f)$. That is,

$$X'(f) = X\left(\frac{f}{a}\right) \tag{18}$$

By use of a theorem of Fourier transformations,

$$F[f(at)] = \frac{1}{a} F\left(\frac{f}{a}\right) \tag{19}$$

Equation 17 transforms into the time domain as

$$\mathcal{F}^{-1}\left[X\left(\frac{f}{a}\right)\right] = a\,x(at) \tag{20}$$

The frequency spectrum of the new time domain function $a\,x(at)$ appears as in Figure 7.

By filtering about zero frequency with a bandwidth f_c/a a time domain signal $g(t)$ is formed. Since filtering about zero frequency on the original frequency spectrum, $X(f)$, reconstructs the original time domain signal, $f(t)$, filtering about zero frequency on the new frequency spectrum, $X(\frac{f}{a})$, forms a time domain function which is related to the original time doamin function by Equation 21.

$$g(t) = \frac{1}{a} f(at) \tag{21}$$

Thus, if a is greater than unity, the time domain of $f(t)$ is extended. Also, if a is less than unity, the time domain of is compressed

Therefore, to change the time scale of a bandlimited signal, the signal is first sampled and then the period of the train of pulses of the sampled function is changed. The amount the period is changed, a, must give a scale change sufficient to convert from computer time to real time.

CHAPTER IV

TIME COMPRESSION

A. Introduction

To compress the time scale of a signal the method developed in Chapter III is used. That is, the signal is sampled at one rate, and the spacing between the samples compressed.

The simplest means of compression would be to compress the samples directly retaining the amplitude of each sample. Because of possible losses in the storage necessary for compression this method is not feasible. To avoid the errors due to possible losses in storage a binary code is formed from the sampled data of the analog signal. It is this binary code which is compressed rather than the samples themselves.

B. Analog to Digital Conversion

The conversion to a binary code is accomplished by an analog to digital converter. An analog to digital converter is divided into two basic operations, quantizing and encoding. The function of the quantizer is to yield a fixed voltage output when the input voltage falls between two predetermined values. The encoder takes the output of the quantizer to form a binary code word corresponding to the voltage range for the two predetermined values. It is these code words which are compressed.

The binary code formed by the encoder is a set of digital pulses on parallel lines. The number of parallel lines depends upon the accuracy and range over which the converter must operate. A more detailed explanation of an analog to digital converter is given in

Appendix B. From this point on, since the compression technique for each path of the binary code is identical, the compression will be described for only one digit.

C. The Time Compressor

Time compression is not a continuous operation; that is, only a predetermined interval can be compressed, and the compressed output cannot be obtained until after the complete interval has occurred. Therefore, to compress a portion of a continuous bandlimited signal, it is necessary to gate the analog input such that bursts of the analog signal T_s seconds long separated by ΔT_s second intervals reach the time compression loop. The object of the time compression loop is to compress each T_s second long interval into an interval ΔT_s seconds long. The amount of time compression is then $T_s/\Delta T_s$. This compression ratio must be sufficient to convert computer time to real time.

The complete time compression loop is shown in Figure 8. The control generator gates the analog signal with a pulse T_s seconds ON and ΔT_s seconds OFF. The gated signal is then applied to the input terminals of the analog to digital converter. This converter samples the incoming signal at a rate f_o, where f_o is greater than twice the limiting frequency of the input, and forms the corresponding binary code. The first digital pulse, T_c seconds wide, passes into an OR gate and then into an AND gate. The OR gate allows pulses coming from the converter or pulses being fed back to enter the AND gate. In the AND gate the pulses are strobed by a high frequency clock pulse. The purpose of this clock pulse is to convert the digital pulses into equivalent high frequency signals that can pass through the delay line. The output of the AND gate is then fed into an amplifier where the

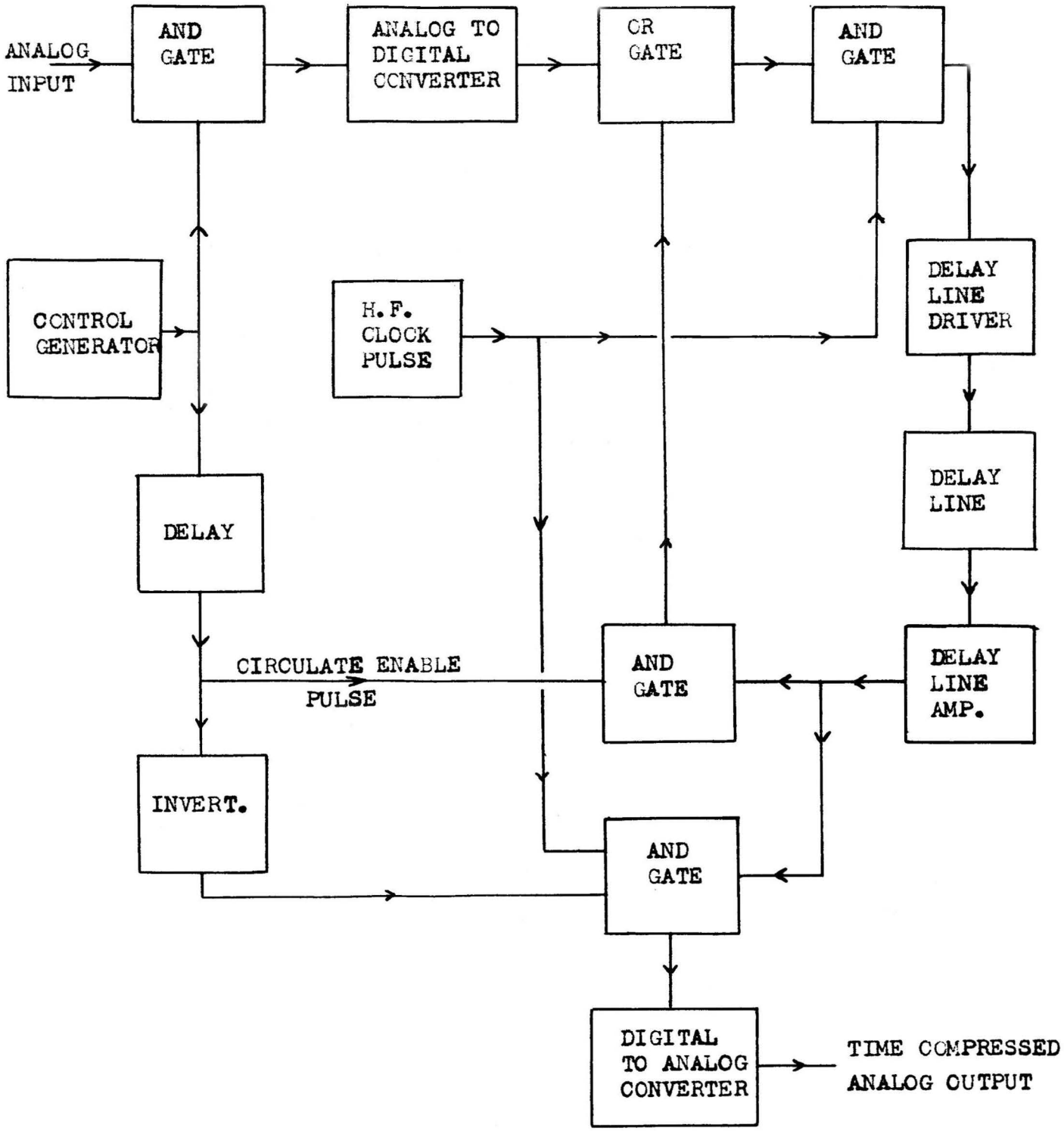


FIGURE 8

A time compressor using a delay line storage

modulated pulse is shaped to energize the delay line. At the output of the line the pulse is first amplified before being allowed to pass through the AND gate by the circulate enable pulse. After this the digital pulse is fed back into the delay line through the first OR gate.

The length of the delay line is selected so that the second digital pulse coming form the encoder is fed into the delay line T_D seconds after the first pulse is fed back into the line. The process of circulating the digital pulses through the line is continued until $\alpha - 1$ pulses are stacked together on the line. The amount of time compression, α , is the reciprocal of the time conversion factor, a . The time compression factor is related to the delay time by the expression

$$\alpha = \frac{T}{T_c + T_D} \tag{22}$$

Where T is the period of the sampling pulses and also the digital pulses. The delay line loop is opened by the absence of the circulate enable pulse which is applied to the AND gate, and the pulses are allowed to pass through the readout AND gate by the presence of the readout pulse. While in the readout AND gate the pulses are again strobed by the high frequency clock pulse before being passed into the digital to analog converter. The strobing at this point is to time and reshape the pulses. During the readout time of ΔT_s seconds the $\alpha'th$ pulse coming from the encoder passes into the delay line and into the readout gate without being circulated. This technique converts a set of α pulses for a burst T_s seconds long of the analog signal into an analog signal T_s/α or ΔT_s seconds long.

The process of time compression is illustrated in a more detailed manner by the pulse sequence diagrams of Figures 9 and 10. Figure 9 shows a set of α digital pulses with width T_c spaced T seconds apart. Superimposed above the α pulses is the circulate enable pulse which is T_s seconds long. These pulses are stacked together in the delay line as they circualte through the loop. Figure 10 shows the output of the delay line after $3T$ seconds or after pulse # 1 has made two loops. The pulses continue to circulate in the delay line until there are $\alpha - 1$ pulses stacked on the line or the first pulse appears at the output of the line for the α^{th} time. At this time the circulate enable pulse turns OFF and the readout enable pulse turns ON. The readout enable pulse is the inverse of the circulate enable pulse. Refering to Figure 8 it is seen that the circulate enable pulse and the readout enable pulse are obtained by delaying the control gating pulse a time equal to the delay of the analog to digital converter. The readout enable pulse allows the $\alpha - 1$ pulses on the line to be fed into the digital to analog converter through the read-out enable AND gate. The α^{th} digital pulse passes through the delay line and directly through the readout enable AND gate without being fed back into the delay line. This compresses the α samples of the analog signal T_s seconds long into a period ΔT_s seconds long.

D. Requirements of the Compressor

From the previous discussion and Figures 9 and 10 some new relationships for the time compression factor α are obtained. The spacing between the code pulses times the compression factor must equal the length of the burst to be compressed.

$$T_s = \alpha T \tag{23}$$

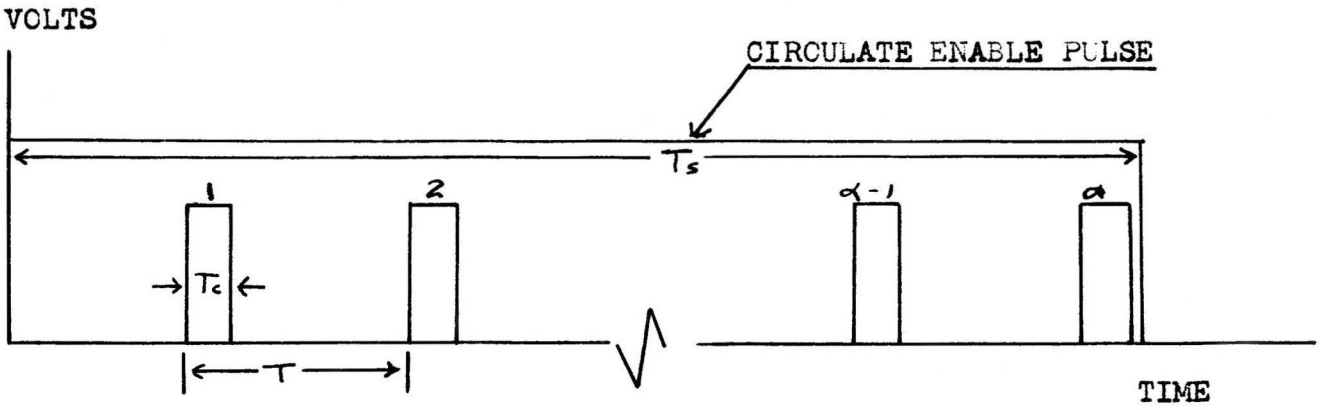


FIGURE 9

The digital pulse output for one channel of the analog to digital converter with the circulate enable pulse superimposed above

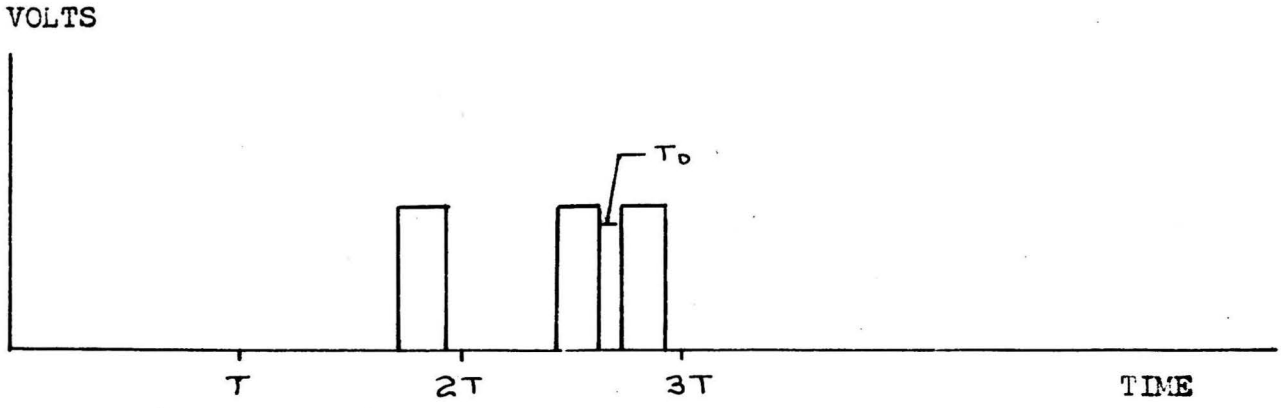


FIGURE 10

The output of the delay line for the first 3T seconds

Since the spacing of the code pulses is equal to the reciprocal of the sampling frequency, f_o , and also the smapling frequency must be greater than twice the bandlimiting frequency, f_c , Equation 24 follows directly from Equation 23.

$$T_s = \frac{\alpha}{f_o} \leq \frac{\alpha}{2 f_c} \tag{24}$$

Equation 24 gives a very useful relationship between the bandlimiting frequency, the compression ratio, and the length of the burst to be compressed. This equation is, however, misleading. It shows that the burst to be compressed can be increased without limit as α is increased for any given bandlimiting frequency, f_c . Equation 24 does not account for a change in the sampling frequency, f_o , with a change in the compression ratio. Since the compression process of the digital pulses compresses α pulses into an interval T seconds long, the compression factor times the period of the compressed pulses, $T_c + T_D$, must equal the period of the sampling pulses, T , or

$$T = \alpha (T_c + T_D) \tag{25}$$

For the best performance T_D approaches zero, and

$$T = \alpha T_c \tag{26}$$

or

$$f_o = \frac{1}{\alpha T_c} \geq 2 f_c \tag{27}$$

Equation 27 shows that the sampling frequency is inversely proportional to the compression factor. Substituting from Equation 26 into Equation 24 a limit is obtained for α .

$$\alpha \leq \frac{1}{2 f_c T_c} \tag{28}$$

The above equation is the required restriction on α which must be satisfied before any of the preceding equations involving the sampling

frequency and the interval to be compressed can be applied.

Time compressors may be rated by the following factors: their dynamic range, distortion, noise, bandwidth, and magnitude of input segment. When using an analog to digital converter the first three depend solely on the characteristics of the converter, since the time compression is achieved in a digital manner. By using a large number of quantum steps properly tapered, it is possible to obtain a compressor with a large dynamic range and a low noise level.

CHAPTER V

TIME EXTENSION

A. Introduction

To extend the time domain of an analog signal the method developed in Chapter III is employed, the analog signal is sampled, the samples are stored, and the frequency of the samples is then decreased. A means of time extension is to store the samples and read the samples out for a period much longer than the sample period. This process is illustrated in Figure 11 for a repetitive input. Part A of Figure 11 shows the repetitive input and the sampling pulses. The length of one cycle of the input is ΔT_s seconds, and the sampling frequency, f_o, is the reciprocal of the signal length plus the width of the sampling pulses, T_1.

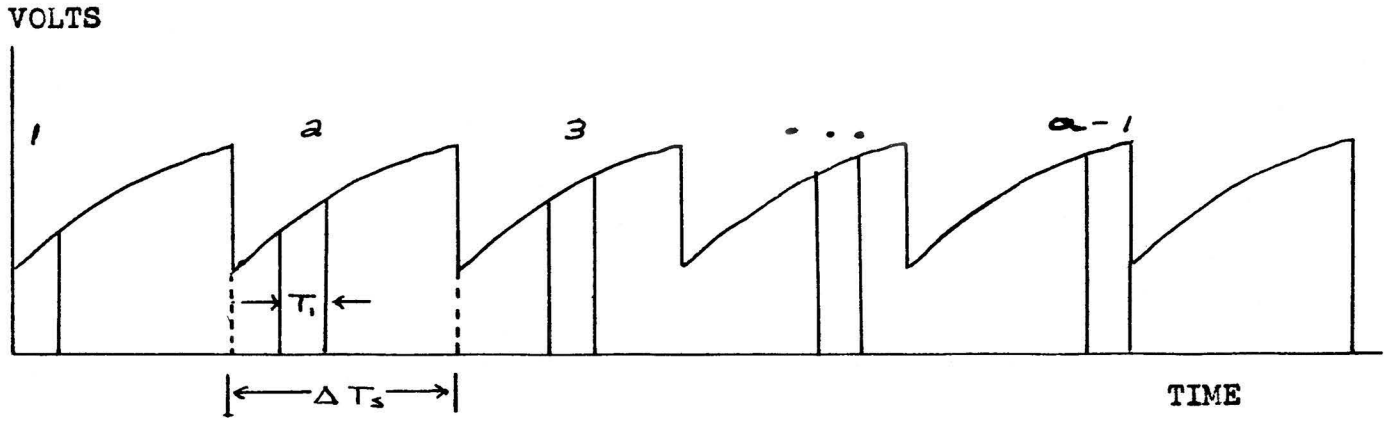
$$f_o = \frac{1}{\Delta T_s + T_1} \tag{29}$$

Part B of Figure 11 shows that a time extended version of one cycle of the input is obtained by holding and reading out each sample for ΔT_s seconds. The waveform of Part B is a step function, but with a good low pass filter the waveform becomes a time extension of one cycle of the original waveform.

From Figure 11 it is also noted that $a-1$ of the gate control pulses must equal the time of the original analog signal, or

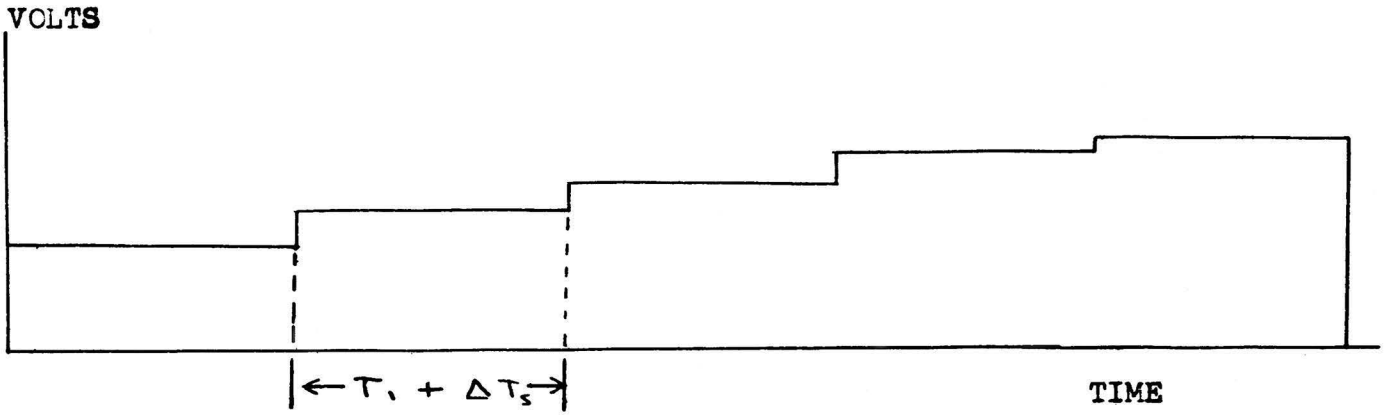
$$\Delta T_s = (a-1) T_1 \tag{30}$$

Since f_o must be greater than twice the bandlimiting frequency f_c, Equation 29 can be rewritten as in Equation 31.



PART A
FIGURE 11

A repetitive signal and the sample periods



PART B
FIGURE 11

The time extended output of one cycle

$$2 f_c \leq f_o = \frac{1}{\Delta T_s + \Delta T_s/(a-1)} \tag{31}$$

or

$$\Delta T_s \leq \frac{a-1}{2 a f_c} \tag{32}$$

Equation 32 gives the restriction on the length of the bandlimited analog signal to be extended, and Equations 29 and 30 give the requirements on the sample period and the sampling frequency. Each of the preceding equations must be satisfied for conversion from real time to computer time.

B. The Sample and Hold Circuit

A circuit which achieves this type of time extension is a sample and hold circuit. A sample and hold circuit is a circuit which samples an analog voltage at a well defined point in time, then provides a non-destructive readout of this voltage sample for a relative long period of time. Such a system consists mainly of a storage device, a system for reading the information into storage, and a system for reading the information out of storage without seriously disturbing it until readout is complete. A block diagram of a sample and hold circuit is shown in Figure 12.

The sample and hold circuit shown in Figure 12 operates by a pulse from the gate control opening the gate allowing the signal from the input amplifier to charge the storage capacitor. After sufficient time has elapsed to bring the charge on the storage capacitor very near its final value, the gate closes, thereby preventing futher change in charge on the storage capacitor. The output amplifier is provided to read the voltage on the storage capacitor without destroying the voltage present.

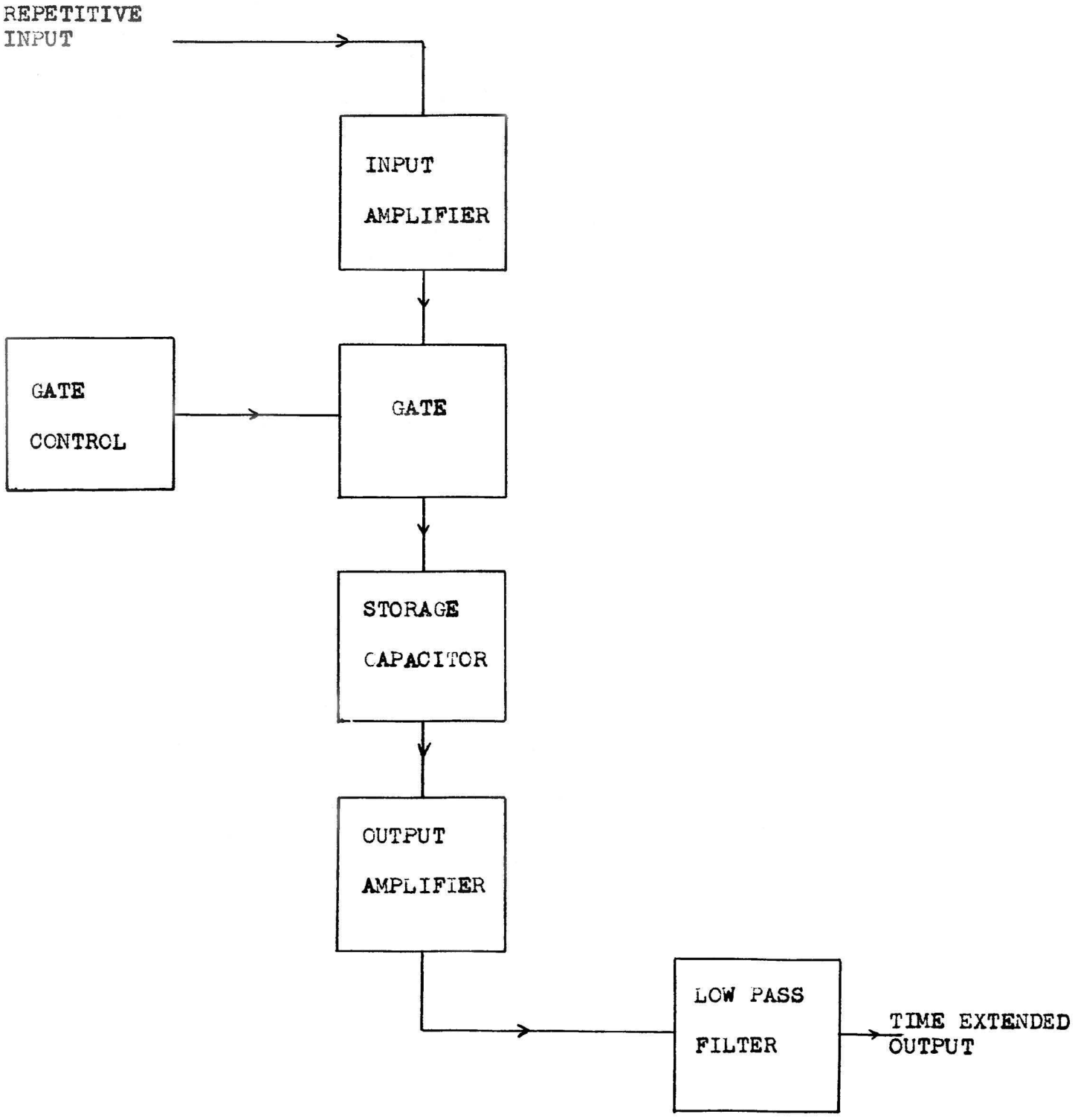


FIGURE 12

A sample and hold circuit

C. Repetitive Readout Memory Device

For the time extension to take place as described in the preceding paragraph, the analog voltage must be repetitive so that each sample is taken during a short interval, compared to the hold time, after the preceding sample. That is, an analog signal ΔT_s seconds long is fed into a memory device which provides a repetitive readout, and this output is sampled by a pulse train with a period $\Delta T_s + T_1$. Each sample, T_1 seconds long, is held and readout for ΔT_s seconds. This procedure gives a time extension of $\Delta T_s / T_1$. This time extension must be sufficient to convert real time to computer time.

The repetitive readout memory device which is necessary for the input to the sample and hold circuit consists of a delay line ΔT_s seconds long with positive feedback. For the repetitive memory device shown in Figure 13, gate #1 is opened and gate #2 is closed as the signal is read in. After the signal ΔT_s seconds long is passed through gate #1 gate #1 is closed and gate #2 is opened. With gate #2 opened the signal is readout at the readout point again, also as long as gate #2 is opened the signal continues to circulate through the delay line loop. The delay line amplifier has sufficient gain to restore the signal to its original amplitude at the readout point. Thus, the delay line loop illustrated in Figure 13 provides a repetitive readout of the original signal when the gates are opened at the proper times.

D. Limitations of the Sample and Hold Circuit

The limitations of a sample and hold circuit as noted by Eddins (5) are diagrammed in Figure 14. The input and output amplifiers have limited voltage handling capabilities which limit the dynamic range of the system. The D-C drift and gain drift cause errors which limit the

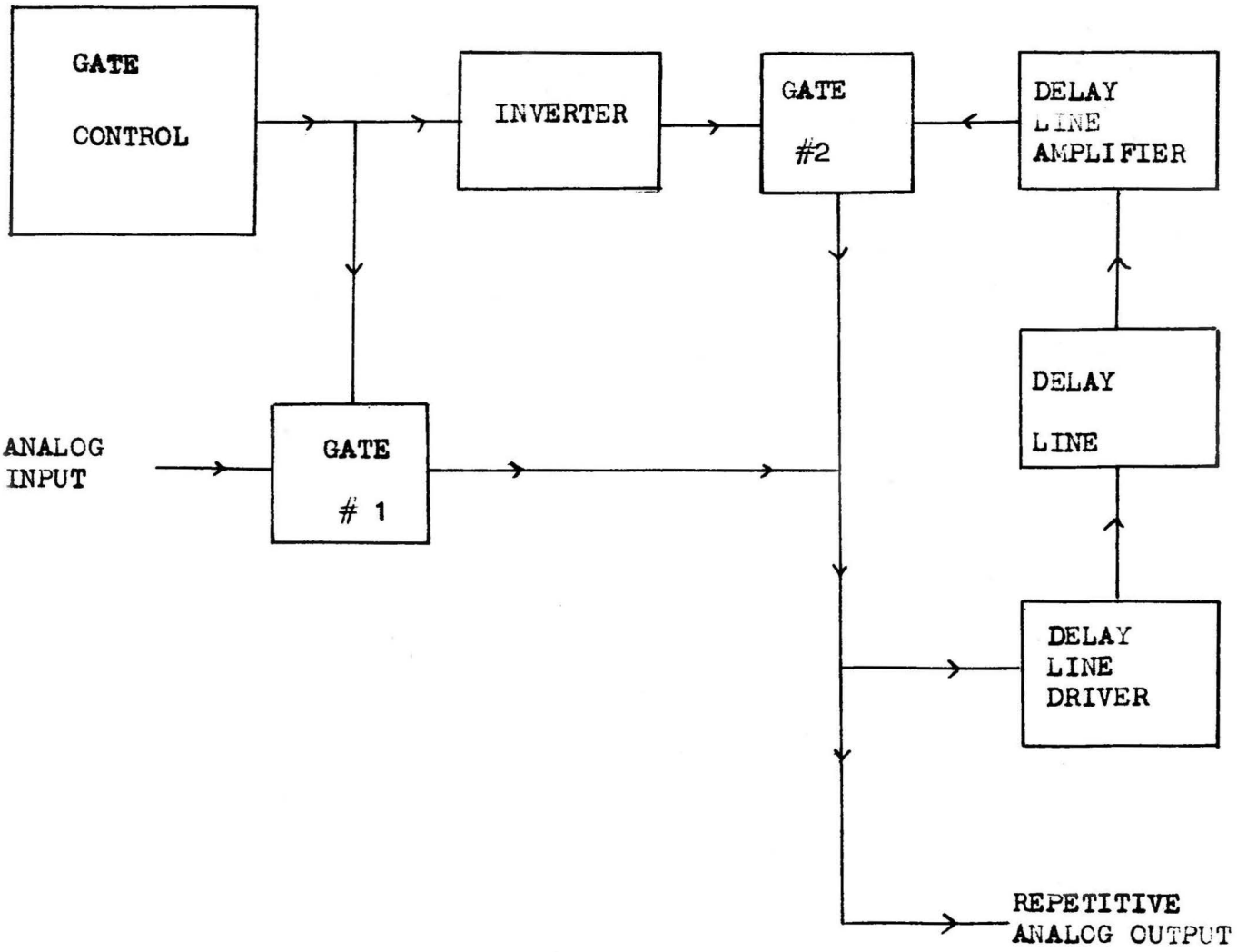


FIGURE 13

A repetitive readout memory device

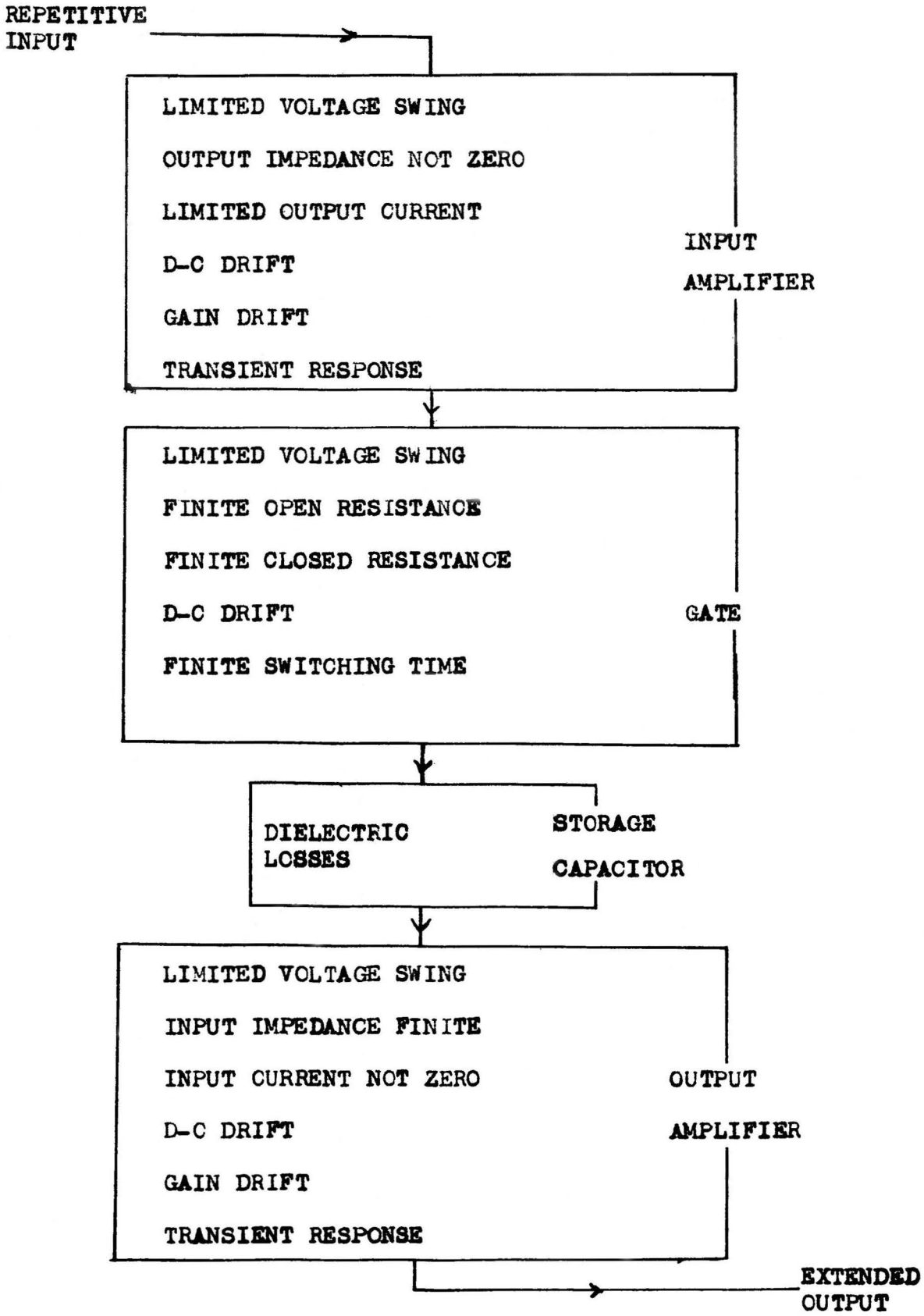


FIGURE 14

Limitations of a sample and hold circuit

resolution of the system. The finite response times limit the minimum sample time, and the leakage from the storage capacitor places restrictions on the maximum ratio of the sample period to the hold period.

The average leakage current, I_L, during the hold period through the closed gate and the output amplifier causes a charge loss on the storage capacitor. This loss causes the stored voltage to decrease by ΔV volts over the hold period, ΔT_s seconds. This voltage is given by

$$\Delta V = \frac{I_L \Delta T_s}{C} \tag{33}$$

For optimum performance ΔV must be very small compared to the system resolution. Since ΔT_s can be large, the problem is to have a low leakage current.

When the capacitor is charged the voltage must change from an initial value of E_0 volts to a final value of E_2 volts. The net change in charge is then given by

$$\Delta Q = C(E_2 - E_0) \tag{34}$$

If the charging time is T_1 seconds, and the charging current is i_c, the net change in charge is also given by

$$\Delta Q = \int_0^{T_1} i_c \, dt \tag{35}$$

Combining the last two equations

$$(E_2 - E_0) = \frac{1}{C} \int_0^{T_1} i_c \, dt \tag{36}$$

If the charging current is approximately constant during the charging period, T_1, the last equation becomes

$$(E_2 - E_0) = \frac{I_c T_1}{C} \tag{37}$$

Equation 38 follows directly by substituting from Equation 33 into Equation 37.

$$(E_2 - E_o) = \Delta V \frac{T_c I_c}{\Delta T_s I_L} \tag{38}$$

Equation 38 shows that the maximum voltage change during the charge period is determined by the system resolution, the ratio of the charge time to the hold time, and the ratio of the charge current to the leakage current.

The output impedance and stability of practical amplifiers may not be adequate for high resolution systems. If such is the case, negative feedback must be employed. This feedback could either be a loop around the entire system or around the input and output amplifiers. Whichever type of feedback is employed, the opening of the gate places a virtual short circuit upon the input amplifier causing it to go into current saturation, and charging the hold capacitor at a constant current, I_c. The change in voltage after time t is given by

$$E = \frac{I_c t}{C} \tag{39}$$

As E approaches a final value the amplifier comes out of current saturation. From this time until the gate closes, the capacitor charges toward its final value. If the change occurs at T_o, then the voltage at the closure of the gate is given by

$$E_1 = E_2 - \left(E_2 - E_o - \frac{I_c T_o}{C}\right) \epsilon^{-\frac{(T_1 - T_o)}{RC}} \tag{40}$$

Where E_o is the voltage on the capacitor when the gate opens, E_1 is the voltage on the capacitor when the gate closes, R is the sum of the dynamic resistances of the input amplifier and the gate, and E_2 is the final value toward which the capacitor is charging. The entire charging process as given by Eddins (5) is shown in figure 15.

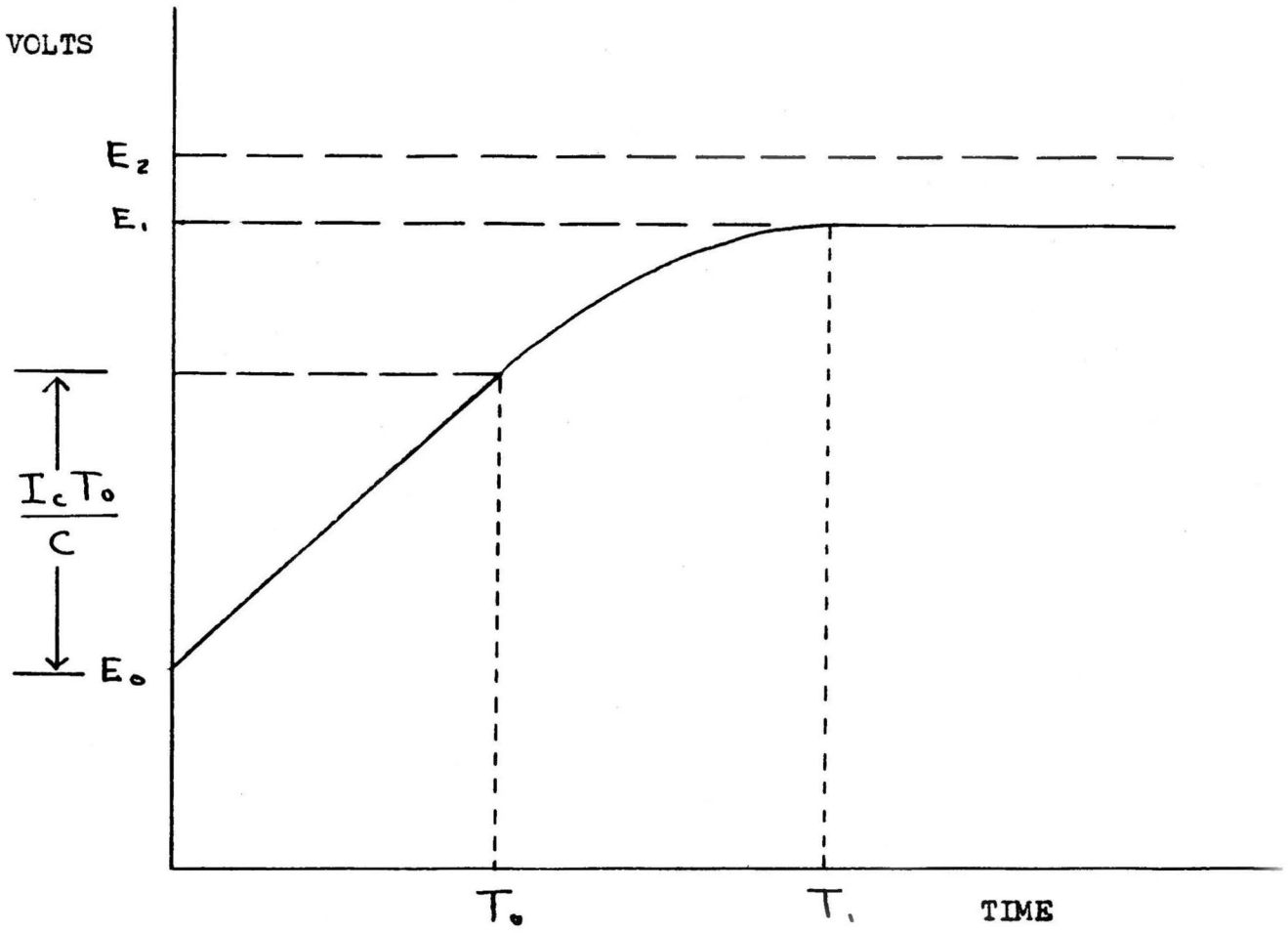


FIGURE 15

The charging of the storage capacitor

CHAPTER VI

A COMPLETE TEST SYSTEM

For testing with an analog computer operating in slow time it is necessary to time compress the output of the computer before applying the signal to the subsystem under test, and then to time extend the output of the subsystem before feeding the signal back into the analog computer. Because the time conversion is not a continuous operation the analog computer must compute for a predetermined interval, and the feedback signal must be timed properly to reach the computer as a new computation cycle is beginning. The diagram of Figure 16 is the complete block diagram for testing a subsystem in a closed-loop, slow-time , analog simulation. This diagram combines the analog computer, time compression loop, time extension circuit, and the necessary control generators.

When an analog computer is time scaled the computer time, τ , is related to real time, t , by

$$\tau = \alpha t \tag{41}$$

For a computer to compute in slow time α must be greater than unity. By the time conversion technique of Chapter III a time scale change is made as indicated by Equation 42.

$$a\tau = a\alpha t \tag{42}$$

Since it is desired that Equation 42 transform computer time into real time, the product of $a\alpha$ must equal unity. Thus, using the technique of Chapter IV, a is adjusted such that

$$a = \frac{1}{\alpha} \tag{43}$$

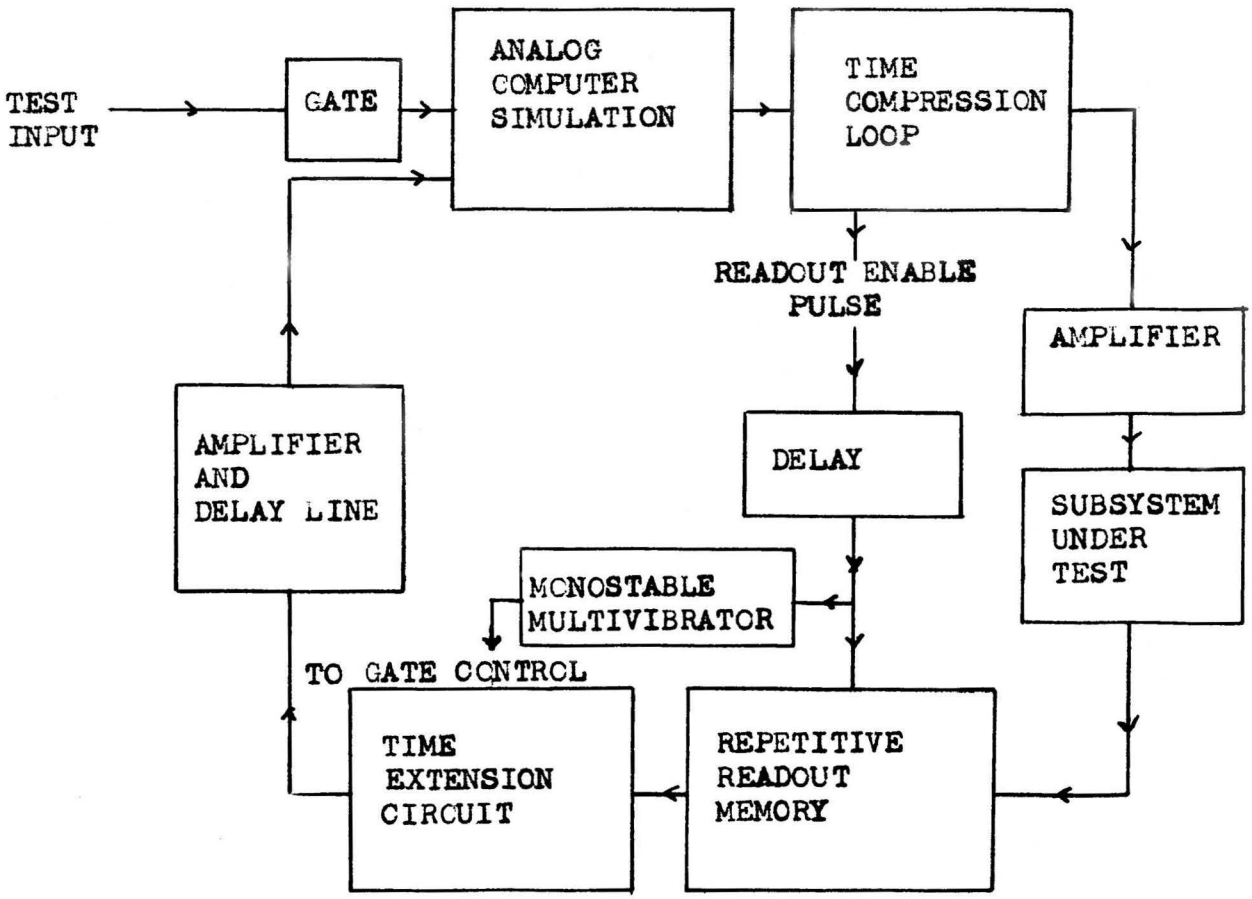


FIGURE 16

A complete time scaled analog computer test system

If this is done, computer time is transformed into real time. Also, the extension ratio of the sample and hold circuit must be equal to the time scale factor of the computer. This is because the time transformation of the sample and hold circuit must transform real time to computer time.

For the analog simulation and the time compression loop to operate in synchronism both are turned ON and OFF by the same control generator. This control generator has a period of T_s seconds ON and ΔT_s seconds OFF, and this output controls the time compression loop as described in Chapter IV.

Up to this point no mention has been made of the voltage or power level of the analog signal which is applied to the subsystem. The analog computer is assumed to have an output near its maximum output voltage level, which may be an amplitude scaled output. The analog to digital to analog conversion system is assumed to have a sufficient range to handle the analog signal, and the amplifiers within the loop provide sufficient amplitude to circulate the digital pulses through the loop, and have no effect on the magnitude of the output. Therefore, an amplifier must be supplied to provide the necessary signal level before applying the signal to the subsystem under test.

As the output of the digital to analog converter is fed through the amplifier and the subsystem, the readout enable pulse is delayed a time interval equal to the delay of the converter, and the amplifier. Then as the analog signal is coming out of the system, the delayed readout enable pulse opens gate #1 and closes gate #2 of the repetitive readout memory device. This sets the repetitive readout memory device into operation as described in Chapter V. Since the readout enable

pulse is the same length as the time compressed signal, this pulse also closes gate #1 and opens gate #2 at the proper time. The delayed readout enable pulse is also used to trigger a monostable multivibrator. The output of the multivibrator is then used to turn ON the gate control generator. The gate control generator has a frequency which allows the storage capacitor to charge and a proper hold time to give a time extension of a . The pulse duration of the monostable multivibrator is T_s , long enough to allow complete time extension.

After the signal is properly extended it is fed through another amplifier and delay line. This amplifier-delay line combination serves to delay the analog signal such that the signal is just reaching the analog computer as the control generator starts another computation cycle, and to provide the proper amplitude to the feedback signal. The second cycle operates in the same fashion as the first cycle, except that the output of the computer is different due to the feedback from the subsystem. This cyclic computation and testing process is repeated until a solution is achieved and data on the subsystem under test are obtained. A proper solution will occur when the output for each cycle is the same.

CHAPTER VII

ERRORS DUE TO TIME CONVERSION

In the time scale changing and testing of a subsystem the analog signal in computer time is compressed by a factor of $\frac{1}{\alpha}$ before applying the signal to the subsystem. The output of the subsystem is then extended by a factor of α and fed back into the analog computer. This complete process is illustrated by the block diagram in Figure 17. In this diagram and all preceding discussions the compressions and extensions were assumed exactly $\frac{1}{\alpha}$ and α respectively. However, there is a possibility of error in these time conversions because of the precise delays and accurately timed pulse generators that are required. If an error is present, the effect of the error on the system must be determined.

If the error in α is $\Delta\alpha$ the amount of time compression is given by

$$\frac{1}{\alpha + \Delta\alpha_1} \tag{43}$$

where

$$\alpha \gg \Delta\alpha_1 \tag{44}$$

and the amount of time extension is given by

$$\frac{\alpha}{1 + \Delta\alpha_2/\alpha} \tag{45}$$

where

$$\alpha \gg \Delta\alpha_2 \tag{46}$$

Denoting all values of the signal that have an error in α present with a subscript ℓ, the value at point 2 of Figure 17 is given by

$$C'_\ell \left(\frac{t}{1 + \Delta\alpha_1/\alpha} \right) \tag{47}$$

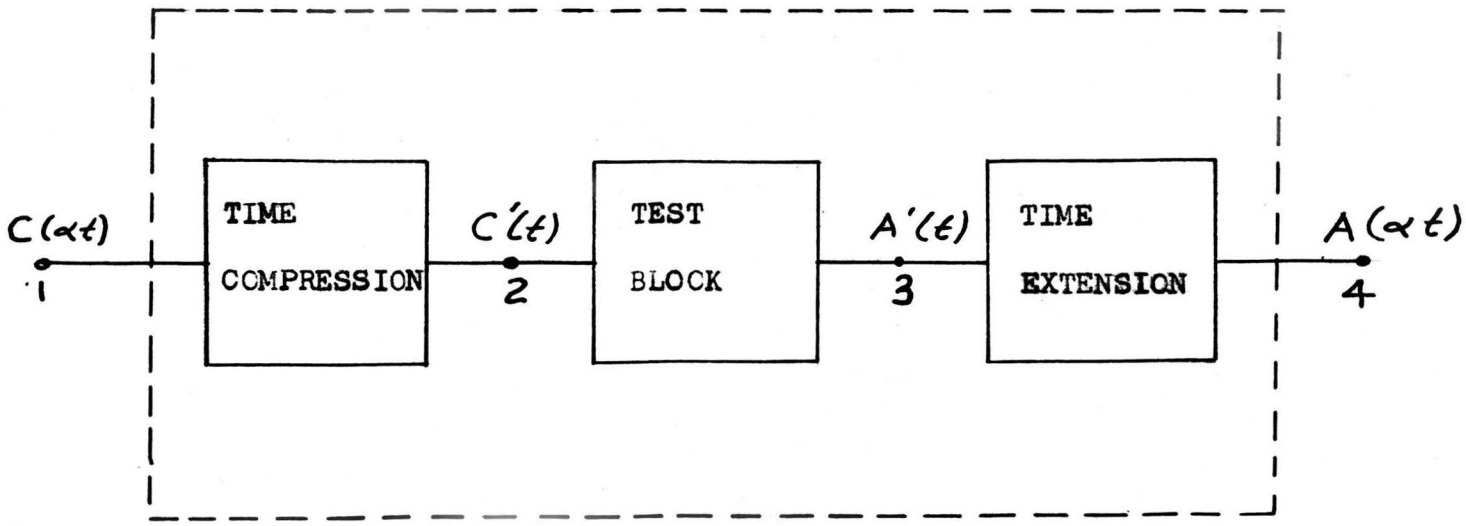


FIGURE 17

The portion of the test system external to the analog computer

The corresponding values for points 3 and 4 are

$$A'_2\left(\frac{t}{1+\Delta\alpha_1/\alpha}\right) \tag{48}$$

and

$$A_2\left(\frac{\alpha t}{(1+\Delta\alpha_1/\alpha)(1+\Delta\alpha_2/\alpha)}\right) \tag{49}$$

The above expressions show that the input to the subsystem and the feedback signal are both in time scale error due to the errors in α . If these errors are small enough not to effect the time or frequency response of the system under test, they are acceptable.

To determine the effect of the time conversion errors on the test system the Laplace transform of the portion exterior to the analog computer is studied. Since

$$\mathcal{L}[f(t)] = F(s) \tag{50}$$

and

$$\mathcal{L}[f(at)] = \frac{1}{a}F\left(\frac{s}{a}\right) \tag{51}$$

the desired transform of the input is given by

$$\mathcal{L}[A(\alpha t)] = \frac{1}{\alpha}\bar{A}\left(\frac{s}{\alpha}\right) \tag{52}$$

the transform due to errors becomes

$$\frac{(1+\Delta\alpha_1/\alpha)(1+\Delta\alpha_2/\alpha)}{\alpha}\bar{A}_2\left[\frac{(1+\Delta\alpha_1/\alpha)(1+\Delta\alpha_2/\alpha)}{\alpha}s\right] \tag{53}$$

considering the term

$$(1+\Delta\alpha_1/\alpha)(1+\Delta\alpha_2/\alpha) = 1+\frac{1}{\alpha}(\Delta\alpha_1+\Delta\alpha_2)+\frac{1}{\alpha}(\Delta\alpha_1\Delta\alpha_2) \tag{54}$$

and since

$$\frac{1}{\alpha}(\Delta\alpha_1\Delta\alpha_2) \approx 0 \tag{55}$$

Equation 54 now becomes

$$\left(1 + \frac{\Delta\alpha_1}{\alpha}\right)\left(1 + \frac{\Delta\alpha_2}{\alpha}\right) \approx 1 + \frac{1}{\alpha}\left(\Delta\alpha_1 + \Delta\alpha_2\right) \quad (56)$$

Using the above approximation the Laplace transform of the output due to errors in α becomes

$$\frac{1 + \frac{1}{\alpha}(\Delta\alpha_1 + \Delta\alpha_2)}{\alpha}\, \bar{A}_2\left(\frac{1 + \frac{1}{\alpha}(\Delta\alpha_1 + \Delta\alpha_2)}{\alpha}\, s\right) \quad (57)$$

The desired transfer function is given by

$$\frac{\bar{A}\left(\frac{s}{\alpha}\right)}{\bar{C}\left(\frac{s}{\alpha}\right)} \quad (58)$$

and the transfer function due to time conversion errors is given by

$$\frac{\frac{1 + \frac{1}{\alpha}(\Delta\alpha_1 + \Delta\alpha_2)}{\alpha}\, \bar{A}_2\left(\frac{1 + \frac{1}{\alpha}(\Delta\alpha_1 + \Delta\alpha_2)}{\alpha}\, s\right)}{\bar{C}\left(\frac{s}{\alpha}\right)} \quad (59)$$

From the above two expressions it is noted that the errors in time conversion act only to shift the poles and zeros of the test block and to change the gain of the test block. The change in gain can be compensated for by additional amplification, and the effect of the shift in poles and zeros is determined by considering the poles and zeros of the complete system. That is, the amount of shift or error in the poles and zeros of the subsystem which can exist and yield favorable test results is compared with the shift due to errors in time conversion. Also if $\Delta\alpha_1$ and $\Delta\alpha_2$ are equal and of opposite sign, the overall effect on the complete system is approximately zero.

CHAPTER VIII

CONCLUSION

From the preceding chapters it is noted that the testing of a subsystem with an analog simulation is not limited to real time computation. Repetitive bursts of analog computation in slow time can test a subsystem in real time, if time compression and extension methods are used. Using these techniques a completely new field of analog testing comes into view.

With the time compression methods of Chapter IV the length of the burst ot be compressed, the sampling frequency of the compressor, and the width of the digital pulses required can all be calculated knowing the bandlimiting frequency and the time scale factor. The sample period and hold period can also be found knowing the bandlimiting frequency and the time scale factor for the time extension circuit. It is also noted that the amount of time conversion is limited only by the width of the digital pulses and the sample period. Thus, the size of the time scale factor is limited only by the design of the analog to digital converter and the sample and hold circuit.

Although this new method opens a completely new field of analog testing, the design and cost of the special equipment are no easy or small matters. For added flexibility the equipment must be designed such that: (1) the analog to digital converter has a very narrow digital pulse and the sampling frequency is variable; (2) the delay line is variable; (3) the smaple period of the sample and hold circuit is adjustable to very small values and the hold period is variable; (4) the ON and OFF times of the control generator are variable.

If the design employs these items, the equipment will have a variable time conversion, and the effect of errors in time conversion can be determined by the method of chapter VII. All gates and logic circuits must have a fast turn ON and turn OFF time to handle the required pulses, and the delay of these circuits must be known to properly time the circuit.

The use and need of testing with a time scaled analog computer will be the determining factors in the construction of the time conversion test equipment.

APPENDIX A

The Sampling Function

A periodic sampling function $S(t)$ is specified for one period as follows:

$$S(t) = 1.0 \qquad 0 \le t \le \Delta T/2 < T \tag{1A}$$

$$S(t) = 0 \qquad \Delta T/2 < t < T - \Delta T/2 \tag{2A}$$

$$S(t) = 1.0 \qquad T - \Delta T/2 < t \le T \tag{3A}$$

It is known that $S(t)$ may be represented in the frequency domain by frequencies n/T where $-\infty < n < \infty$. The magnitude of each of these frequency components may be evaluated by first determining C_n; Thus,

$$C_n = \int_{-\Delta T/2}^{\Delta T/2} \epsilon^{-j n \omega_0 t}\, dt \tag{4A}$$

$$C_n = \frac{1}{j n \omega_0}\left[\epsilon^{j n \omega_0 \frac{\Delta T}{2}} - \epsilon^{-j n \omega_0 \frac{\Delta T}{2}}\right] \tag{5A}$$

$$C_n = \Delta T\left[\frac{Sin\left(n \omega_0 \frac{\Delta T}{2}\right)}{\left(n \omega_0 \frac{\Delta T}{2}\right)}\right] \tag{6A}$$

The complete form of the Fourier Series for $S(t)$ can now be written as follows.

$$S(t) = \frac{\Delta T}{T} \sum_{n=-\infty}^{\infty} \frac{Sin\left(n \omega_0 \frac{\Delta T}{2}\right)}{\left(n \omega_0 \frac{\Delta T}{2}\right)} \epsilon^{j n \omega_0 t} \tag{7A}$$

APPENDIX B

Analog to Digital Converter

In time scaled analog testing an analog to digital converter is used in the time compression loop. This analog to digital converter forms a binary code for each voltage sample taken and places each binary digit on a separate parallel line. The overall operation as outlined in Chapter IV is performed by the circuit of Figure 18.

For the purpose of illustration the formation of a three-digit binary code is described. For good fidelity 6 or 7 digits are necessary. A three digit system forms a different binary code word for each of 8 voltage levels. An example of a binary code with a range from zero to 40 volts is given in Table I.

To form the binary code given in Table I the quantizer must first determine what level the given sample is in; this is accomplished by various means of voltage comparison with ramp voltages, staircase voltage, or separately timed pulses. The quantizer then puts out a pulse on one of 7 channels corresponding to the respective voltage level. There is no channel for the zero level because no digits are required for this level. The encoder then forms the required binary code for the given level. The simplest means of achieving this is to place the pulse of the quantizer on each of the required channels. This process is diagrammed in Figure 19.

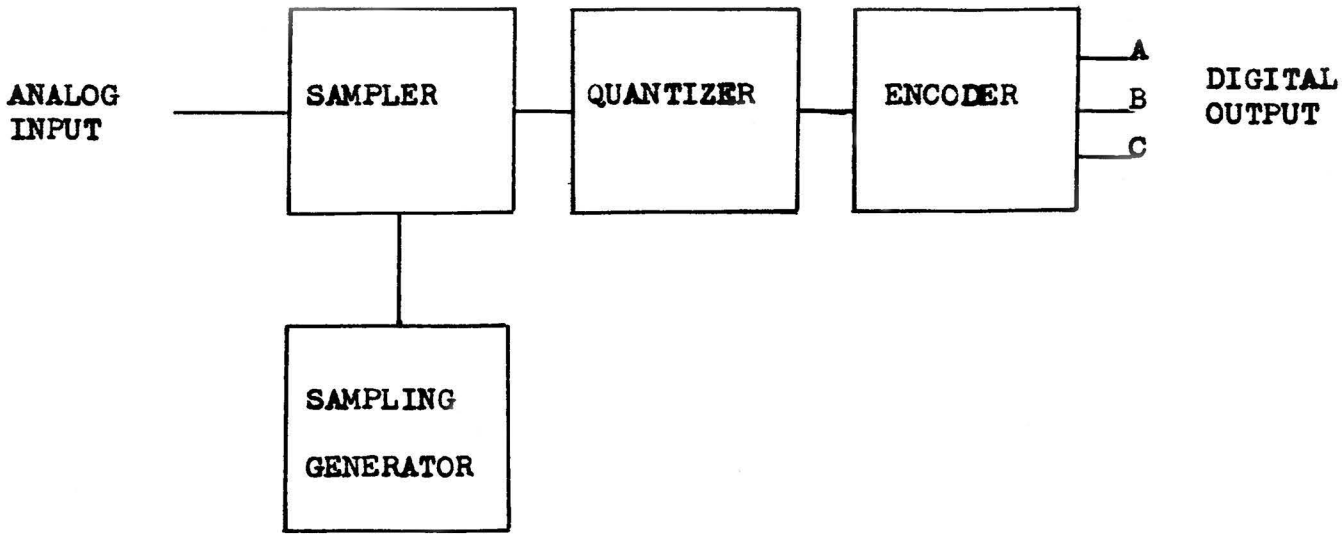


FIGURE 18

An analog to digital converter

LEVEL	MID-LEVEL VOLTS	LEVEL LIMITS VOLTS	OUTPUTS		
			A	B	C
		0			
0	2.5		0	0	0
		5			
1	7.5		1	0	0
		10			
2	12.5		1	1	0
		15			
3	17.5		0	1	0
		20			
4	22.5		0	1	1
		25			
5	27.5		1	1	1
		30			
6	32.5		1	0	1
		35			
7	37.5		0	0	1
		40			

TABLE I

Voltage levels of the quantizer and the digital codes

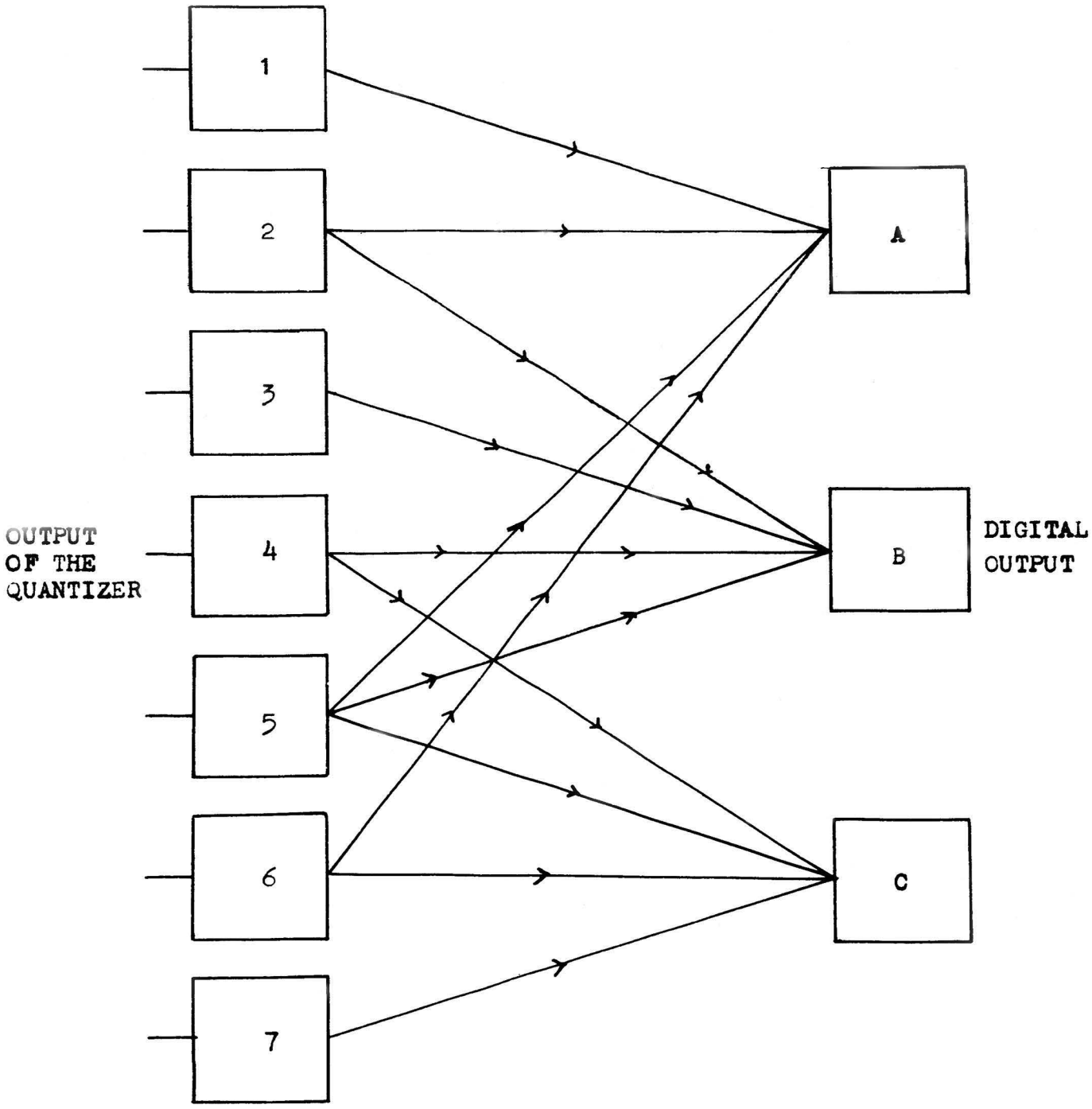


FIGURE 19

A three digit encoder

Digital to Analog Converter

The purpose of the digital to analog converter is to convert the incoming digital pulses into the relative voltage level represented by the particular pulse combination. In this system the digital pulses defining each voltage level or sample occur simultaneously on three parallel lines. Each line drives a flip-flop which is turned ON by the presence of a digital signal pulse on the line. Midway in time between the signal pulses, a reset pulse is fed to the flip-flop on another line in order to turn OFF the flip-flop. A diagram for one digit is illustrated in Figure 20.

The normal and complementary outputs of each flip-flop are then matrixed together in a series of AND gates, according to the desired code, as shown in the block diagram of Figure 21. At any instant of time only one gate is open and only one level of voltage passes through the OR gate common to all the AND gates. The output of this OR gate is then filtered to obtain the time compressed analog voltage.

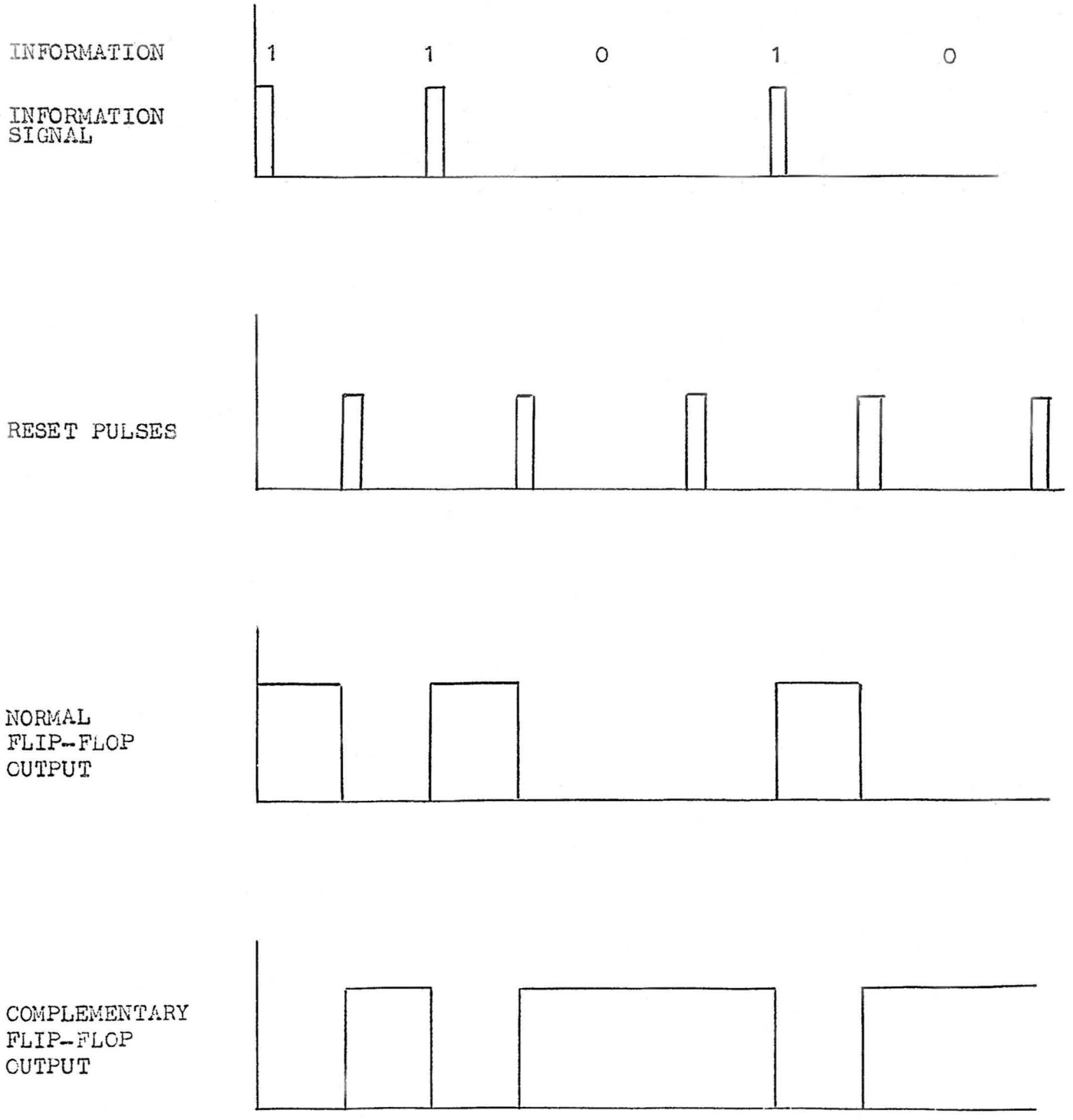


FIGURE 20

Pulse to flip-flop conversion for the digital to analog converter

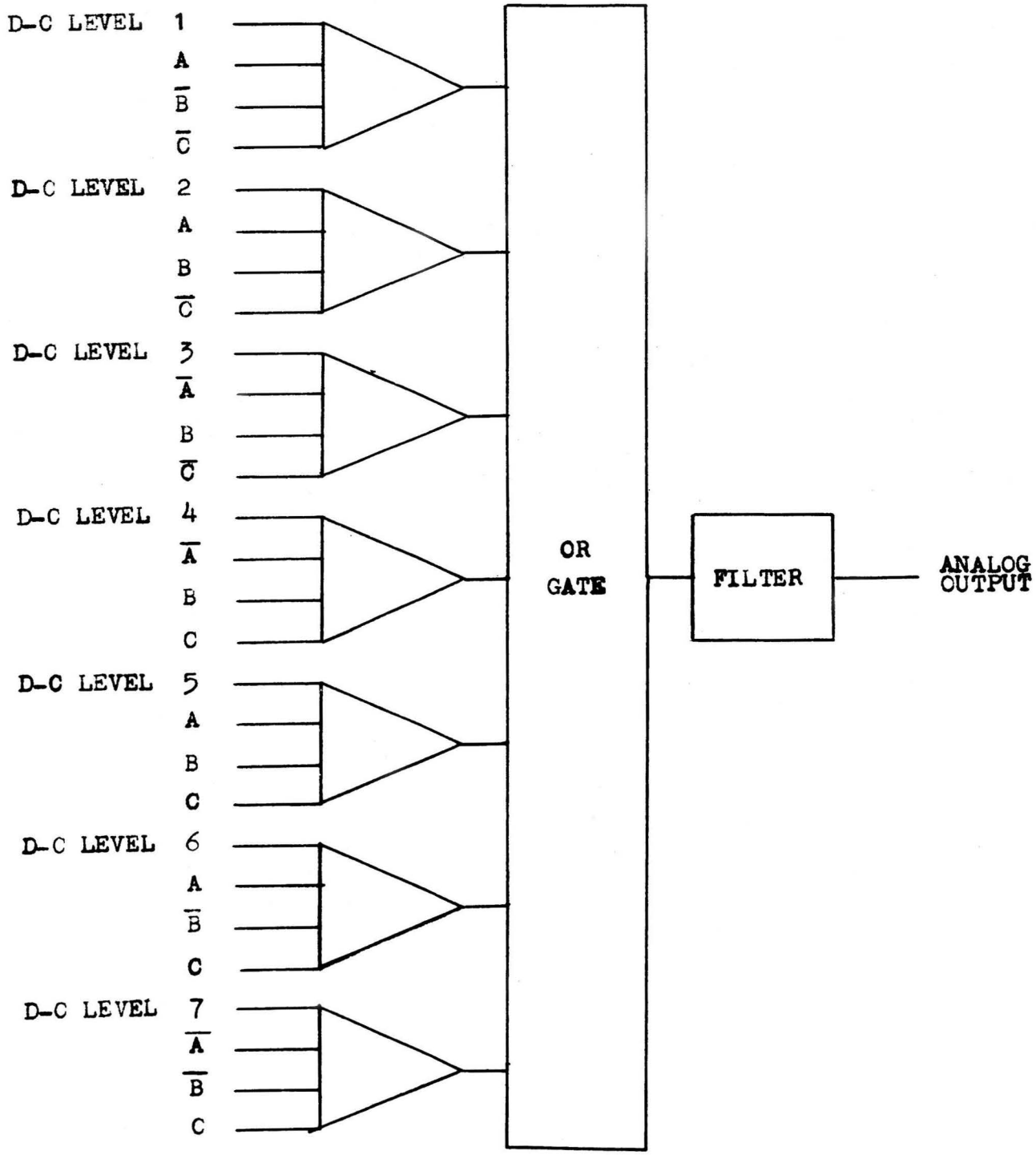


FIGURE 21

A three digit matrix decoder

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The organizations in which he is a member include the Institute of Electrical and Electronics Engineers, Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi, and Sigma Xi.