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Sputter deposition of thin-film capacitors onto low temperature co-fired ceramic substrates

Jack Murray

Department:

SPUTTER DEPOSITION OF THIN-FILM CAPACITORS ONTO LOW TEMPERATURE CO-FIRED CERAMIC SUBSTRATES

by

JACK EDWIN MURRAY

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Wayne Huebner, Advisor
Matthew J. O'Keefe, Co-Advisor
Robert W. Schwartz

PUBLICATION THESIS OPTION

This thesis has been prepared with three papers for publication. A general introduction is given on pages 1-15. The first paper was accepted for publication in the Proceedings of the 2011 International Symposium on Microelectronics and is located on pages 16-29. The second paper was submitted to Materials Letters and is located on pages 30-38. The third paper will be submitted to Thin Solid Films and is located on pages 39-55.

ABSTRACT

Single layer thin film capacitor structures were fabricated on the surface of low temperature co-fired ceramic (LTCC) substrates using sputter deposition. The capacitor structures had areas between ~10^4 μm^2 to ~10^6 μm^2 and featured ~200 nm Al or Pt electrodes with 150-1500 nm Al_2O_3 dielectric layers. Impedance analysis and current-voltage testing were carried out to determine the effect of electrode material and dielectric thickness upon capacitor performance. Capacitance values for devices with Al electrodes ranged from ~10 to ~700 pF, depending on capacitor area and dielectric thickness, and the fit to expected values was better than devices with Pt or mixed (one Al, one Pt) electrodes. Dielectric loss increased with increasing Al_2O_3 thickness, most likely due to cracking in thick (>1 μm) sputtered films. All measured loss values for the sputter deposited Al_2O_3 (tanδ~0.02) were greater than bulk Al_2O_3 (tanδ ~0.001). Transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) were utilized to examine selected capacitor structures. Electron beam induced crystallization of amorphous Al_2O_3 was observed during the selected area diffraction (SAD) patterns. TEM examination and impedance analysis both confirm that functional capacitors with Al electrodes and 300 – 1000 nm thick Al_2O_3 dielectric layers can be fabricated on LTCC substrates using sputter deposition.

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1. INTRODUCTION

1.1. LOW TEMPERATURE CO-FIRED CERAMIC SUBSTRATES

Low temperature co-fired ceramics (LTCCs) are made up of multiple layers of tape cast ceramics, often with additions of low melting point (<900 °C) glass. Uses for LTCC technology include microfluidic [1] and microelectronic [2-6] applications. For microelectronic applications LTCC technology is used as an alternative to traditional printed circuit board technology, where passive circuit elements can be integrated between layers with connecting layers of conductive materials. An example of an LTCC system is shown in Figure 1.1. The circuit elements and systems illustrated in Figure 1.1 include hermetically-sealed surface-mounted chips, integrated capacitors, and metallic interconnects.

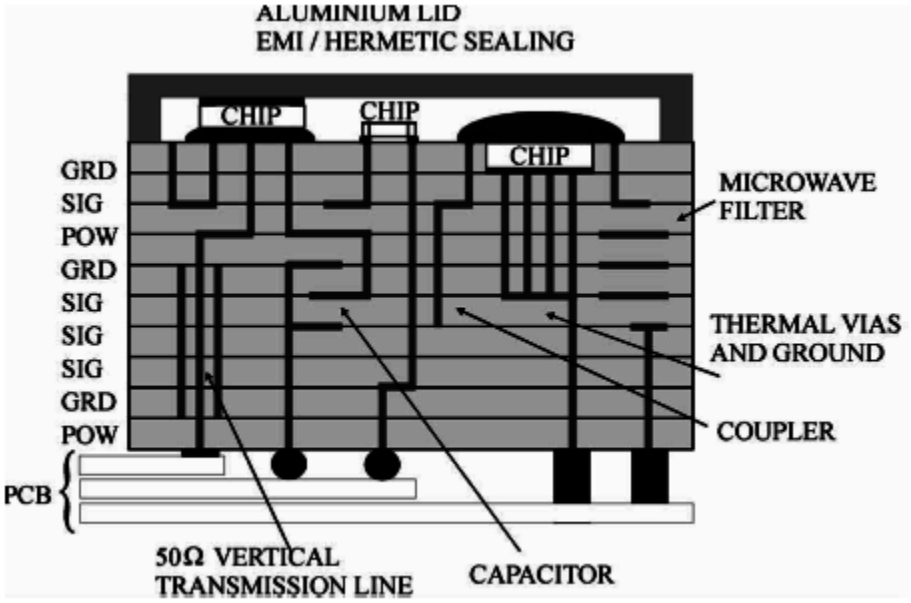

Figure 1.1. Example LTCC multilayer structure with embedded electronic devices. [3] The entire LTCC system is mounted on a printed circuit board (PCB).

A variety of compositions exist for LTCC materials [7], but most are made up of a ceramic, such as Al_2O_3 or cordierite, with fluxing oxides and low melting temperature glasses. The firing temperature must be less than the melting point of any conductive materials used in the full LTCC system, which is usually ~950 °C. Any of the substrate materials used in LTCC applications must possess satisfactory electrical properties for high frequency (100 MHz to 300 GHz) operation, including low loss and a non-dispersive permittivity. The conductive materials in LTCC systems consist of pastes of metallic conductors that are fired with the ceramic substrate. Common metals in LTCC systems are Cu, Ag, and Au, or their alloys [8] due to their high melting point (1085, 961, and 1064°C respectively [9]) and low resistivity (1.7, 1.6, and 2.3×10^{-8} Ω m respectively [10]). Pastes are formed by dispersing metal powder into organic binders. Full sintering of the paste leaves behind a connected system of metal particles or a non-porous metal layer, depending on the paste composition.

After an LTCC system is laminated, the resulting stack (ceramic layers and conductive paste) is fired in one step. Care must be taken to pick materials with similar thermal expansion coefficients and sintering kinetics, as well as low chemical reactivity. Deformation during co-firing, resulting in warped packages, is not uncommon and much of the research effort in LTCC technology is focused on alleviating this concern. Methods have been developed to measure the camber or warpage of LTCC systems during firing [11], which help with understanding the different sintering kinetics of conductive paste and ceramic constituents. The surface roughness of LTCC substrates is ~1 μm [8] which is much higher than atomically smooth Si substrates used in other areas of microelectronics. Recent efforts have also focused on eliminating glass from LTCC compositions due to the poor performance of most glasses at high frequencies, as well as possible reactions with metal phases [4, 5].

1.2. SPUTTER DEPOSITION

Sputter deposition is a physical vapor deposition (PVD) technique where a solid target material is deposited as a solid onto a substrate under high vacuum. Sputtering is considered a physical, rather than chemical, process because the material does not typically undergo any chemical composition changes during deposition. During

sputtering, incident atoms, usually ions, strike the surface of the target material. If the incident atoms have sufficient energy they will cause the ejection of target atoms after colliding with the surface. The process is illustrated in Figure 1.2. Most sputter systems supply the incident ions in the form of a plasma and attract the ions with voltage applied to the target which is located at the cathode. The substrate and chamber are grounded, to ensure safe operation. Atoms are ejected from the surface of the target and deposited throughout the vacuum chamber in a line of site direction [12].

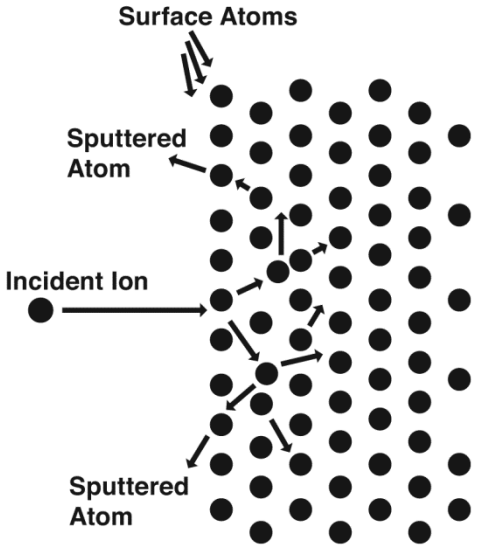

Figure 1.2. Schematic of physical sputtering process at the sputtering target. [13]

The steps in the sputter deposition process are evacuation of the vacuum chamber, backfill with working gas, ignite the plasma, clean the target, and finally deposit material. Sputtering must take place in ultra high vacuum conditions to ensure that the mean free path of sputtered atoms is sufficient to travel from the target to the substrate [14]. The working gas, usually Ar or Ne, is ionized to create the plasma. Higher sputter yield is realized with higher mass gases, so Ar is the most widely used working gas [14]. The

working gas is ionized by applying a large voltage to it. A DC or RF power supply applies the voltage to the cathode, depending on the material to be deposited. A wide variety of materials can be sputtered, including metals, insulators and semiconductors. Typically DC sputtering is used to deposit metals and RF (13.56 MHz) sputtering is used to deposit insulators.

1.3. Al_2O_3 DIELECTRIC

Several characteristics of aluminum oxide (Al_2O_3) are important to understand to allow for effective use in dielectric applications. The crystal structure of Al_2O_3 plays a part in many of its properties and varies depending on processing characteristics, such as temperature and deposition technique. Other structural characteristics include the defects and stoichiometry deviations that result from various processing techniques. Also useful is an understanding of the electrical properties of Al_2O_3, including dielectric constant, band gap, resistivity, and dielectric breakdown strength, and their variation depending on structure and processing. Various electrical phenomena occur at different thicknesses of Al_2O_3 films and must be accounted for when their use is desired for a specific application. This section highlights these characteristics.

In normal bulk conditions Al_2O_3 is a crystalline material (α-Al_2O_3) with a trigonal crystal structure and a space group of $\bar{3}2/m$ [15]. Figure 1.3 shows the crystal structure of α-Al_2O_3 in a hexagonal arrangement, with the trigonal unit cell outlined in dashed lines. Many polymorphs of Al_2O_3 exist at different temperatures and are formed from different processing conditions [16]. When thin films of Al_2O_3 are deposited, they are often arranged in amorphous or nanocrystalline structures.

The electrical properties of Al_2O_3 are sufficient for use as a dielectric or insulating material in a variety of applications. Pure α-Al_2O_3 exhibits a non-dispersive dielectric constant, K, of 10 [18]. Only the electronic and ionic polaraization mechanisms are active, contributing ~30% and 70% of the overall K. Relative to other ceramic capacitor materials, such as TiO_2 or $BaTiO_3$, Al_2O_3 is considered a low-K material [19] but in Si microelectronic applications where Al_2O_3 would replace SiO_2 or Si_3N_4 it is considered a high-K dielectric [20]. The band gap of Al_2O_3 is 6.31 eV [17] which makes it an electrical insulator. In fact, 99.9% pure Al_2O_3 features exceptional electrical resistivity

($1x10^{13}$ Ω m) which degrades when impurities are present [19]. Thin films of Al_2O_3 feature high dielectric breakdown strengths, often in the range of several MV/cm [31, 33, 34].

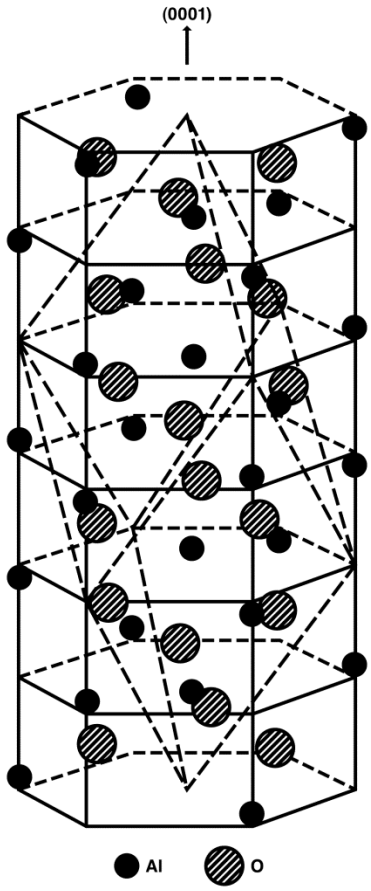

Figure 1.3. Crystal structure of Al_2O_3 in a hexagonal arrangement with trigonal unit cell highlighted with dashed lines. [17]

Two main thickness regimes of Al_2O_3 thin films have been studied since the late 1960's. The thinnest films are tens of nm thick. In early examples these films were fabricated by evaporation from solid Al_2O_3 sources [21, 22], or were oxidized from Al by

thermal or anodic methods [23, 24]. Later, Al_2O_3 films of similar thicknesses were deposited by RF magnetron sputtering [25, 26] or pulsed laser deposition (PLD) [27]. Current research into replacements for SiO_2 and Si_3N_4 in metal-insulator-metal (MIM) capacitors for Si microelectronics also involves Al_2O_3 films tens of nanometers thick, discussed further below. Thicker Al_2O_3 films, with thicknesses in the hundreds of nm, have been deposited by anodic oxidation of Al [28] or evaporation [29], but the vast majority have been synthesized by sputter deposition [30-34].

Films of Al_2O_3 with thicknesses around 10 nm exhibit unique characteristics that are not measured (or observed) at greater thicknesses. Antula [21] examined an apparent positive ionic space charge in Al_2O_3 films between 6 and 34 nm thick. Films were deposited by the evaporation of Al in an O_2 atmosphere, yielding Al_2O_3. After deposition the films were aged in atmospheric pressure at temperatures from 150-200°C and times between 2 and 6 hours. Current-voltage testing indicated an ionic space charge in the Al_2O_3 that disappeared after aging. Birey [22] examined the dielectric properties of Al_2O_3 films between 6 and 1000 nm in thickness. The Al_2O_3 films were again deposited by the evaporation of Al in an O_2 atmosphere. The resultant dielectric loss was exceptionally high for the capacitors, with values between 10 and 60%. The anomalous results from both of these studies can be attributed to the use of reactive evaporation as the deposition method. Pinholes, low density and high residual film stress are common defects of reactive evaporated films due to the limited control over processing parameters [35]. The positive ionic space charge [21] can be attributed to the migration of Al ions into the porous Al_2O_3 layer and high dielectric loss [22] is most likely due to defects in the Al_2O_3 film from processing.

Voltage-controlled negative resistance (VCNR) was detected in thermally and anodically oxidized Al_2O_3 films less than 10 nm thick by Dittmer [24]. Similar results were found by Rahman et al. [25] in sputter deposited Al_2O_3 films around 10 nm in thickness. VCNR occurs when the applied voltage leads to a current response opposite what is implied by Ohm's Law, negative current slope with increasing voltage, for example. In both cases, the Al_2O_3 films were part of a sandwich structure with an Al bottom electrode and a Au top electrode. In the first case [24], multilayer Al_2O_3 films fabricated using multiple deposition methods had properties such as porosity that differed

between successive layers. VCNR was thought to occur because of Al rich regions in the Al_2O_3 films as well as Au precipitates in porous Al_2O_3. The complex electronic structure resulting from the non-stoichiometric films obscures the actual mechanism for VCNR. Further confusing the issue are the results from Rahman et al. [25] which only observed VCNR in Al-Al_2O_3-Au structures below pressures of 0.1 Torr. The study featured sputter deposited Al_2O_3 films which are far less porous than the thermally and anodically oxidized films studied by Dittmer, which should lead to a more easily understood electronic structure. No explanation was offered for the pressure dependence of VCNR. Partial dielectric breakdown is now thought to be the cause of VCNR in Al-Al_2O_3-Au structures. Hickmott [36] proposed that conducting channels develop in the Al_2O_3 and these contribute to a positive charge region at the Al-Al_2O_3 interface. Voltages above a certain threshold overcome the positive charge and result in decreasing electric current.

Both reactive and direct sputter deposition of Al_2O_3 films with thicknesses in the hundreds of nanometers have been utilized for microelectronic applications. Yip et al. [34] investigated the effect of different top electrodes on the dielectric strength of Al-Al_2O_3-x capacitor structures where x was either Al, Au, Ni, Cu, or Ag. In all electrical testing the bottom Al electrode was the cathode. Devices with an Al top electrode featured the highest dielectric strength (4.5 MV/cm) with decreasing strength for each of the other top electrode materials. Electric field enhanced diffusion of the electrode materials into the RF sputter deposited Al_2O_3 layer is thought to cause the differing dielectric strengths of the devices. Also, the addition of an Al layer between the dielectric and the top electrode increased the dielectric strength by acting as a diffusion barrier. Although it is supposed that there are open sites and defects in amorphous Al_2O_3 structures that allow for easier diffusion, there is no estimate of the reduction in diffusion energy required. Furthermore, dielectric strength was tested at room temperature while diffusion rates were listed at 1473 K with no estimate of the increased diffusion energy provided by the applied electric field.

Several studies have been carried out to investigate the effect of oxygen addition and sputtering pressure during the RF sputtering of Al_2O_3. Segda et al. [31] found that Al_2O_3 films with the stoichiometry closest to ideal were deposited by RF sputtering in a pure Ar atmosphere. The addition of O_2 led to oxygen-rich films with atomic ratios of up

to $Al_2O_{3.50}$, as measured by X-ray fluorescence. Greater sputter pressure (1.0 Pa, as opposed to 0.1 Pa) led to less Ar incorporation in the Al_2O_3 films due to the reduced mean free path of the Ar atoms with higher pressure. Increasing sputter power was found to reduce the molar fraction of Ar in the resulting Al_2O_3 films. Similar results were found by Voigt et al. [33] who determined that the Al_2O_3 films with the highest breakdown fields (~2.5 MV/cm) were deposited by RF sputter deposition in a pure Ar environment. A further requirement for satisfactory films is the "conditioning" of the Al_2O_3 target by sputtering in a mixed Ar/O_2 atmosphere prior to deposition.

1.4. THIN FILM MIM CAPACITORS

A thin film capacitor is made up of electrode and dielectric layers usually less than several micrometers thick. When the capacitor is arranged in a stack with a bottom electrode layer, a single dielectric layer, and a top electrode layer (or layers) it is known as a metal-insulator-metal (MIM) capacitor. Capacitors arranged in the MIM layout are used for energy storage [37], dynamic random access memory (DRAM) [38-40], and radio frequency (RF) and mixed signal integrated circuits [41-50]. Commonly the dielectric thickness ranges from several nanometers to several hundreds of nanometers, depending on the application. A representative MIM capacitor structure is shown in Figure 1.4, with TiN and W electrodes, Al_2O_3 dielectric layer and via structures visible. MIM capacitors are fabricated using a variety of chemical vapor deposition techniques such as plasma enhanced chemical vapor deposition (PECVD) [41] and atomic layer deposition (ALD) [37-40, 42, 46, 48, 49, 51-53]. Physical vapor deposition techniques such as pulsed laser deposition (PLD) [43] and sputter deposition [45, 50, 54] are also used to fabricate MIM capacitors.

The most common dielectric materials used in current MIM capacitors are oxides and nitrides of Si [41-47], which are cost effective and straightforward to fabricate on Si surfaces. A drawback of using these materials is their low dielectric constant (3.0 for SiO_2 and 7.5 for Si_3N_4). Constant miniaturization of devices has led to a desire for thinner dielectric layers. To facilitate higher capacitance with thinner dielectric layers, high-K dielectric materials have been researched for use in MIM capacitors.

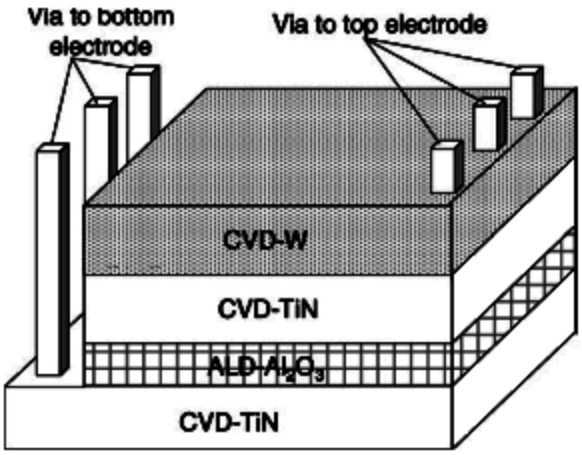

Figure 1.4. Example MIM capacitor layout with W and TiN electrodes and alumina Al_2O_3 dielectric layers. [46]

Lee et al. [38] used ALD to deposit 50 nm W bottom electrodes and 11 nm ZrO_2 dielectric layers for use in MIM capacitors. Top Pt electrodes were e-beam evaporated onto the surface and the resulting structures were characterized by TEM and electrical testing. A thin (~1 nm) interfacial oxide, made up of WO_x with a small amount of Zr, was detected. The K value of the dielectric stack was calculated to be 22-25, which includes the ZrO_2 and the interfacial layer. Kim et al. [51] used ALD to deposit ZrO_2 dielectric layers with thicknesses of 6, 8, and 10 nm at temperatures from 225 to 275 °C. All of the dielectric layers were annealed at 400 °C after deposition to increase the crystallinity of the ZrO_2 films. TiN electrodes were used to created MIM structures. A K value of ~43 was obtained for the 8 nm ZrO_2 layer deposited at 275 °C. In both studies, crystalline films of ZrO_2 were deposited with one study obtaining a higher K than the commonly accepted value of 25.

Al_2O_3 is also a common high-K material under investigation for MIM capacitor use. Bajolet et al. [46] studied the effect of electrode post-treatment on MIM capacitors. CVD was used to deposit TiN electrodes and ALD was used to deposit a 20 nm Al_2O_3 dielectric layer. When TiN is deposited by CVD the resulting films contain enough carbon to degrade the conductivity so post treatment in a N_2/H_2 plasma is required to reduce the carbon content. However, post treatment of the top electrode led to nitrogen diffusion into the Al_2O_3 layer, and a resultant degradation of dielectric properties,

including higher dielectric loss and higher leakage current. Meng et al. [40] used ALD exclusively to deposit similar capacitor structures, with TiN electrodes and a 5 nm Al_2O_3 dielectric layer. Since ALD was used to deposit the electrodes, no plasma post treatment was required. TEM analysis did not show an interfacial layer between the TiN electrodes and the Al_2O_3 dielectric layer. The lack of an interfacial layer was confirmed by capacitance calculations, assuming a dielectric constant of 9 for the Al_2O_3 dielectric. The calculations could be improved by assuming a dielectric constant of 10 for the Al_2O_3 dielectric. Both studies indicate the suitability of constructing MIM capacitors with ALD Al_2O_3 dielectric films and TiN electrodes.

Another high-K dielectric material for use in MIM capacitor applications is HfO_2. Hu et al. [43] used PLD to deposit HfO_2 onto a Ta electrode at 200 °C. Al was used as a top electrode. The dielectric constant of the HfO_2 in the MIM capacitor arrangement was 18 across a frequency range of 500 Hz to 1 MHz. A drawback with using pure HfO_2 as a dielectric material in MIM capacitors is its low crystallization temperature, which degrades the leakage current and dielectric breakdown characteristics by creating disorder at grain boundaries in addition to a volume change [42]. Zhu et al [42] got around this problem by depositing four different stack or laminate structures with alternating layers of ALD HfO_2 and Al_2O_3. The MIM structures featured TiN electrodes and dielectric layers near 50 nm. Laminate structures with 1 nm Al_2O_3 layers around 10 nm HfO_2 layers stacked up to 56 nm in total thickness had the best leakage current and dielectric breakdown characteristics of all of the tested combinations.

1.5. RESEARCH DIRECTION

This work addresses the sputter deposition of thin film capacitor structures onto LTCC substrates and is divided into three sections. First, the fabrication and electrical testing of MIM capacitors with two different layouts was investigated. The capacitors were fabricated on the surface of LTCC substrates and featured 300 nm thick Al_2O_3 dielectric layers with 200 nm thick Al electrodes. Electrical testing was carried out at low (DC and <15 MHz) and high (<1 GHz) frequency to characterize the resulting devices. Successful sputter deposition fabrication of thin film capacitor structures onto the rough (~1 μm) surface of LTCC substrates was demonstrated.

Second, this work documents the electron beam induced crystallization of amorphous Al_2O_3 in a capacitor structure. Crystallization occurred when capturing selected area diffraction patterns in a transmission electron microscope (TEM). The crystallized Al_2O_3 region was visible in selected area diffraction patterns and subsequent TEM images. Crystal growth occurred upon further beam exposure, indicating the thermal nature of the crystallization process. This represents an opportunity to spatially modify and control the microstructure of Al_2O_3, thus affecting the properties over a nanometer scale range.

Third, this work investigates how the choice of electrode material affects thin film capacitor properties. Capacitors with Al, Pt, or both Al and Pt electrodes and Al_2O_3 dielectric layers of various thicknesses were fabricated by sputter deposition and subsequently underwent electrical testing. Devices with Pt electrodes exhibited higher dielectric loss and a larger deviation from expected capacitance values than devices with Al electrodes.

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PAPER

1. SPUTTER DEPOSITION OF THIN FILM MIM CAPACITORS FOR RF BYPASS AND FILTERING APPLICATIONS

Jack Murray, Wayne Huebner, Matthew J. O'Keefe, Kristina Wilder
Missouri University of Science and Technology
Rolla, MO

Ryan Eatinger, William Kuhn
Kansas State University
Manhattan, KS

Daniel S. Krueger, J. Ambrose Wolf
Honeywell Federal Manufacturing and Technologies
Kansas City, MO

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Keywords: LTCC, Sputter deposition, thin-film, capacitor

ABSTRACT

Thin film capacitors for RF bypass and filtering applications were sputter deposited onto low temperature co-fired ceramic (LTCC) substrates. The capacitors were configured in a metal-insulator-metal (MIM) design featuring 200 nm thick Al electrodes and a 300 nm thick Al_2O_3 dielectric layer, with dimensions varied between ~150x150 μm and ~750x750 μm. DC current-voltage measurements ($E \leq 5$ MV/cm) coupled with impedance analysis (≤15 MHz) was used to characterize the resulting devices. More than 90% of the devices functioned as capacitors with high DC resistance (>20 MΩ) and low loss ($\tan \delta < 0.1$). A second set of capacitors were made under the same experimental conditions with device geometries optimized for high frequency (≥200 MHz) applications. These capacitors featured temperature coefficient of capacitance (TCC) values between 500 and 1000 ppm/°C as well as low loss and high self-resonant frequency performance (ESR <0.6 Ω at self-resonance of 5.7 GHz for 82 pF).

Capacitance and loss values were comparable between the capacitor structures of similar areas at the different frequency regimes.

1.1. INTRODUCTION

Physical vapor deposition techniques, such as sputter deposition, offer many advantages over other techniques for thin film deposition, namely chemical vapor deposition or plating. These advantages include the ability to deposit a wide variety of materials, thickness uniformity of deposited films, and good film adhesion [1]. Due to the physical nature of the process (solid source to solid substrate), there are none of the potentially toxic by-products that are associated with other processes. Sputter deposition is also a robust process that can use a wide variety of substrate materials.

Low temperature co-fired ceramic (LTCC) substrates consist of multilayer, tape cast, ceramic and glass dielectric materials with metal interconnects and vias. Passive devices can be used on the surface of an LTCC substrate, or be integrated within internal layers and fired in one step [2, 3]. One firing step is only possible if the densification temperature of the LTCC material is less than the melting point of the metal interconnects. A variety of different compositions are under investigation for LTCC applications and many of them densify at temperatures less than the melting point of common metals such as Cu and Au [4]. Surface roughness is much greater for LTCC substrates than Si wafers (~1 μm for LTCC compared to ~1 nm for Si) but sputtering is known for conformal deposition of thin films [1]. Whether on the surface or integrated internally on a substrate, thin film capacitors offer a size advantage over surface mounted devices. In this paper two different designs of MIM capacitor structures were sputter deposited onto LTCC substrates. Both designs utilized the same materials with the same layer thicknesses but different physical layouts. Electrical testing was carried out in different frequency regimes to characterize the capacitors.

1.2. EXPERIMENTAL

All capacitors were deposited on fired 11x11 cm LTCC substrates. Each substrate was cleaned by immersion and agitation in acetone, methanol, and de-ionized water for 3 minutes. Capacitors were sputter deposited through physical masks in three

separate layers, a 200 nm thick Al bottom electrode, a 300 nm thick Al_2O_3 dielectric layer and a 200 nm thick Al top electrode. Sputter deposition was carried out with a Denton Discovery 18 system at Missouri S&T. Aluminum electrode layers were deposited from a 99.99% pure metallic target at a power of 300 W using a DC power supply. The Al_2O_3 dielectric layer was deposited from a 99.9% pure ceramic target at a power of 200 W using a RF power supply. Layer thicknesses were measured using a Tencor Alpha Step 200 profilometer. All depositions were carried out in an atmosphere of 99.999% pure Ar at a working pressure of 8 mtorr. No substrate heating was used during deposition.

Masks were fabricated at Towne Technologies, Inc using a bilayer Cu/Ni configuration. The first set of masks featured metal electrodes with widths of approximately 150, 380, 530 and 750 μm (Figure 1.1). Combining the electrode widths led to 48 capacitors with 9 different areas. The second set of masks featured shapes optimized for high frequency electrical testing. This design featured 150 capacitor structures, but not all of the devices were testable due to incomplete pattern transfer during deposition. The results from four different capacitor device sizes were measured and are reported herein.

After deposition optical micrographs were taken of each capacitor. Figure 1.2 shows example images from both device designs. The Al_2O_3 layer is faintly visible in the top image as a vertical stripe that darkens the LTCC substrate. In the bottom image the Al_2O_3 dielectric layer is visible as a slight discoloration on the vertical edges of the top Al layer. ImageJ software was used to measure the width of each electrode and the capacitor area was calculated.

The DC resistance, R, was measured for each capacitor with a Keithly 2002 digital multimeter. These resistance measurements were used as a first indication of capacitor performance. A R= 20 MΩ was arbitrarily chosen as a dividing line between potential capacitors and non-functioning devices. Current-voltage measurements were carried out with a HP 4140B pA Meter. Capacitors were tested from -100V to 100V in an alternating fashion (10V, -10V, 20V, etc). Results are reported as current density, J (A/cm^2), vs. electric field, E (MV/cm). The testing voltages correspond to electric field values between -3.3 and 3.3 MV/cm. Capacitance and tan δ were measured at 10 kHz with a HP 4194A Impedance analyzer.

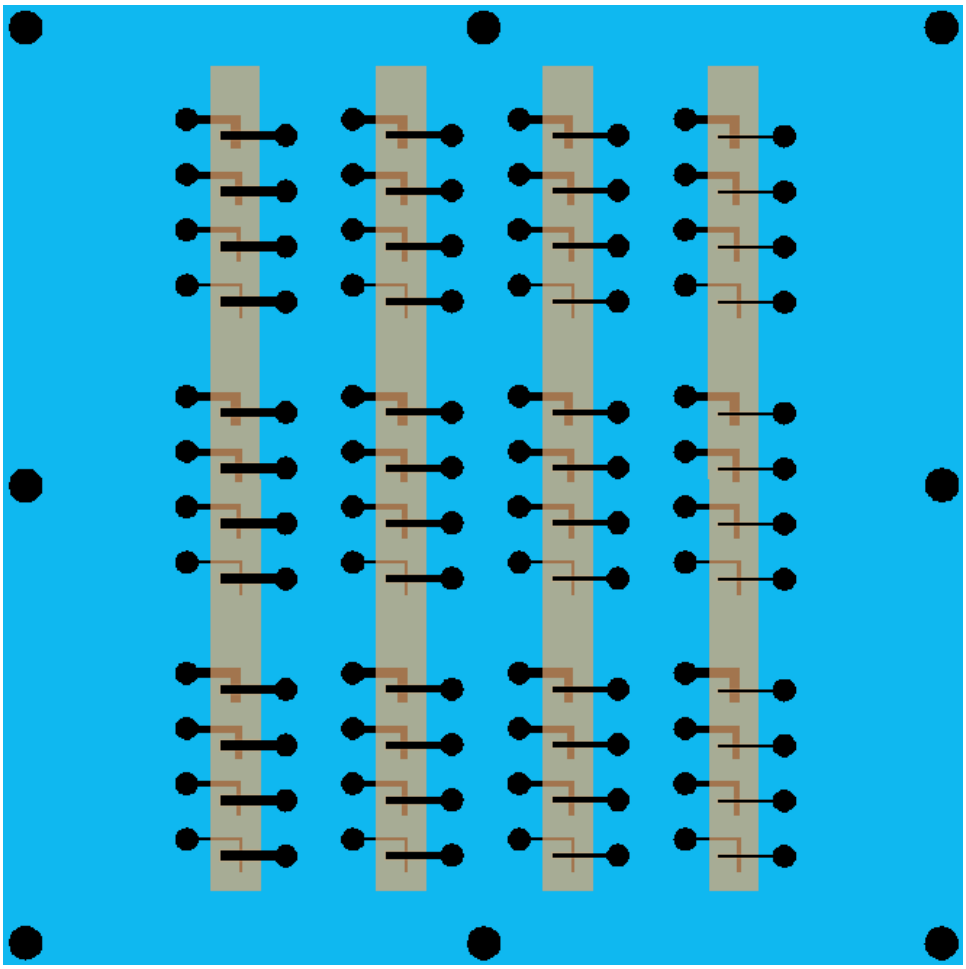

Figure 1.1. Design of LTCC substrates featuring thin film capacitors made for low frequency testing. The first metal layer is shown in black, the second layer (dielectric) is tan, and the third layer (metal 2) is black.

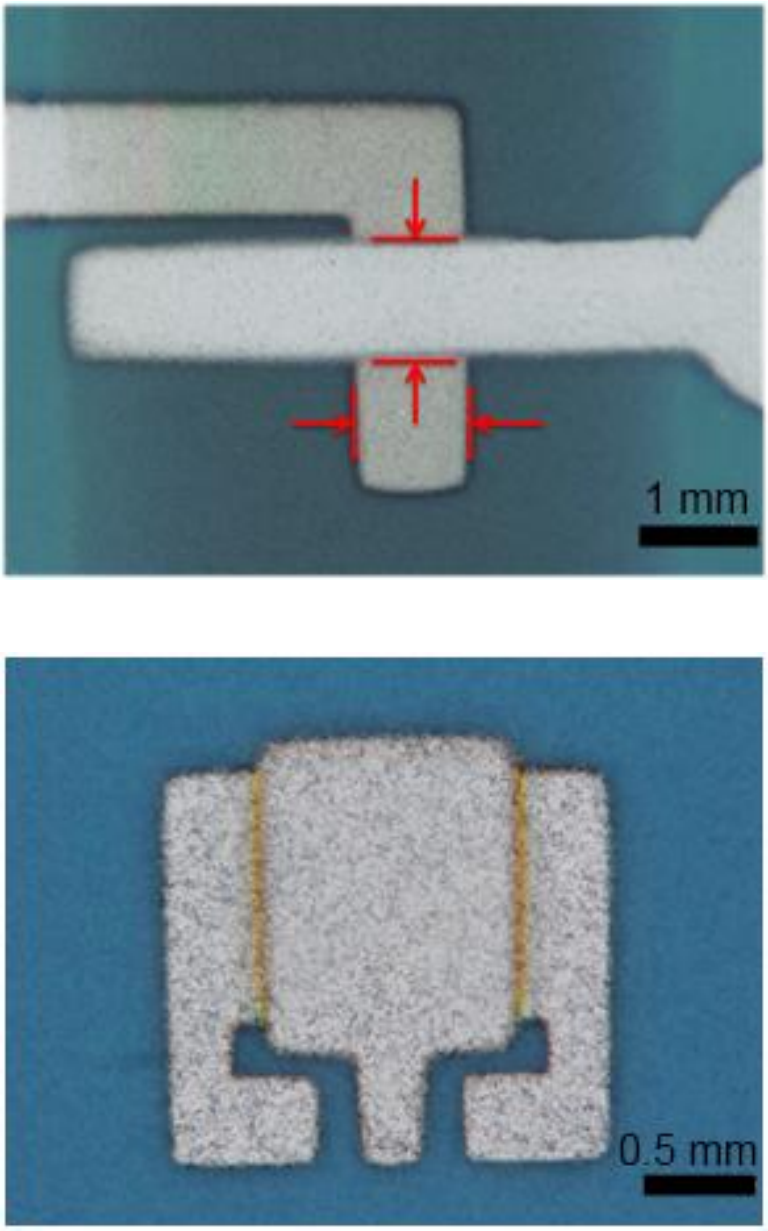

Figure 1.2. Optical micrograph of individual capacitors. The red dimensions indicate where measurements were taken using ImageJ. The top image is of a capacitor that was tested at low frequency. The bottom image is an example of the capacitors that were tested with a high frequency 3-point probe setup.

1.3. RESULTS AND DISCUSSION

One capacitor design was made for testing at DC and low (≤15 MHz) frequencies (see Figure 1.2 top), and another design was made for testing at high (≤1 GHz) frequencies (Figure 1.2 bottom). Impedance analysis was carried out on both device designs along with current-voltage testing on the low frequency samples.

The actual sizes of the capacitors were larger than the size of the mask openings due to lifting of the physical masks during deposition. Therefore, all of the devices were measured optically in order to determine actual capacitor dimensions. The mean percent error between the measured areas and the design areas was 55% with a standard deviation of 44%. The capacitors made for high frequency testing were also larger than expected. Due to the finer feature size of the high frequency capacitors, >90% of the devices were unusable due to poor pattern transfer.

1.3.1. Low Frequency and DC Testing. Initial testing of the fabricated devices indicated that 41 of the 48 potential capacitors had R ≥ 20 MΩ. This result was later verified by capacitance and loss measurements which indicated the same number of capacitors featured low loss and capacitance values matching the measured areas. Testing was not carried out to find the reason for device failure.

Figure 1.3 illustrates the J vs. E results for capacitors with areas of $5x10^{-3}$ cm^2 and $8x10^{-3}$ cm^2. Both capacitors exhibited nonlinear current response at E values greater than ±2 MV/cm and the larger capacitor broke down at E=2.3 MV/cm. The linear portion is indicative of Ohmic conduction, while the nonlinear portion could indicate a variety of conduction mechanisms, such as Schottky emission or space-charge-limited current. Current response was an order of magnitude greater for the larger capacitor, indicating lower resistance from Ohm's law:

$$\rho = \frac{E}{J} \tag{1}$$

where E is the electric field (V/cm), J is the current density (A/cm^2), and ρ is the resistivity (Ω cm). From the linear portion, the smaller capacitor featured a resistivity of

$1.8x10^{14}$ Ω-cm while the larger capacitor featured a resistivity of $1.9x10^{12}$ Ω-cm. These resistivity values are near the bulk value of 10^{13} Ω-cm and indicate that both capacitors are insulating to DC voltages.

Figure 1.4 shows the collected capacitance and loss data for all functioning capacitors. Capacitance values increased from 14 to 363 pF with area (Figure 1.4 top). All capacitors featured loss values less than 0.07 with 85% below 0.03 (Figure 1.4 bottom). The theoretical capacitance for each device area was calculated from the following equation:

$$C = \frac{\varepsilon_0 KA}{t} \tag{2}$$

where C is capacitance (F), ε_0 is the permittivity of free space (F/m), K is the dielectric constant, A is the capacitor area (m^2), and t is the dielectric thickness (m). Equation 2 was used to calculate the theoretical capacitance of each capacitor, using measured area and dielectric thickness. The K of the thin film Al_2O_3 was assumed to be equal to the bulk value of 10. The line in Figure 1.4 (top) shows the theoretical capacitance calculated by equation 2. Most of the capacitors lie along the theoretical capacitance vs. area line, indicating that the dielectric constant of thin film Al_2O_3 was very close to the bulk value. Rearranging equation 2 allows for the calculation of the dielectric constant. The 10 kHz capacitance values were used to calculate the dielectric constant for each functioning capacitor. The mean dielectric constant was 12.0 with a standard deviation of 3.4.

1.3.2. High Frequency Testing. High frequency measurements were carried out using a 6 GHz HP 8753E vector network analyzer (VNA) and 18 GHz ground-signal-ground GGB Industries probes. A GGB CS-9 calibration substrate was used to correct internal VNA errors and a de-embedding structure equivalent to that of the bottom capacitor in Figure 2.2. The dielectric was removed to measure and remove interconnect series-resistances and series-inductances from the measurements.

Capacitors with areas of $6.5x10^{-4}$ cm^2 and $1.0x10^{-2}$ cm^2 were measured. Raw measured results for the larger capacitor from 0.1 MHz to 6 GHz are shown in Figure 1.5a, and the de-embedded result with the series R and L removed is shown in Figure 1.5b. Note that the interconnect had an $R \geq 1\ \Omega$ due to the relatively thin metal films used, but for the capacitor itself the equivalent series resistance, ESR, is $< 0.5\ \Omega$.

De-embedded ESR and capacitance versus frequency are shown in Figures 1.6 and 1.7 respectively. Both capacitors featured a stable frequency range from ~1 MHz to over 500 MHz where the capacitance varied less than 5%. Variations seen outside this frequency range may be due to measurement limitations of the S-parameter equipment used, although the larger capacitor has a self-resonant frequency limitation seen at ~2 GHz.

The temperature coefficient of capacitance, TCC, was also measured for capacitors built using the high-frequency design with areas of $6.5x10^{-4}$, $2.6x10^{-3}$, $5.8x10^{-3}$, and $1.0x10^{-2}$ cm^2. The capacitance of each was measured at a frequency of 1 kHz and at temperatures of 25, 50, 75, and 100°C. Results, including the TCC and the change in capacitance over the 75°C temperature range are listed in Table 1.1. All of the capacitors feature less than 6.5% capacitance change over the 75°C temperature range. While the change in capacitance is higher than what is required for Electronic Industries Alliance (EIA) class I capacitors, all of the capacitors fall within the range of F type EIA class II capacitors.

1.4. CONCLUSIONS

Sputtering was used to deposit 2 different thin film capacitor designs onto LTCC substrates. The first design featured nonlinear current density vs. electric field response, as well as low (<0.06) tan δ values. These capacitors also featured capacitance values that suggested the thin film dielectric constant of Al_2O_3 was approximately 12, slightly higher than the bulk value of 10. Capacitance values from the second layout featured a stable frequency range from 1 to > 500 MHz where the capacitance varied less than 20 pF. The same capacitors also featured <6.5% variation in capacitance from 25 to 100°C. The high-frequency capacitor design featured self-resonant frequencies of up to 2 GHz for a 0.5 nF device, and low loss with ESR of approximately 0.5 Ohms in the GHz range.

De-embedding structure measurements suggest that even lower values of ESR may be achievable with thicker metal film depositions.

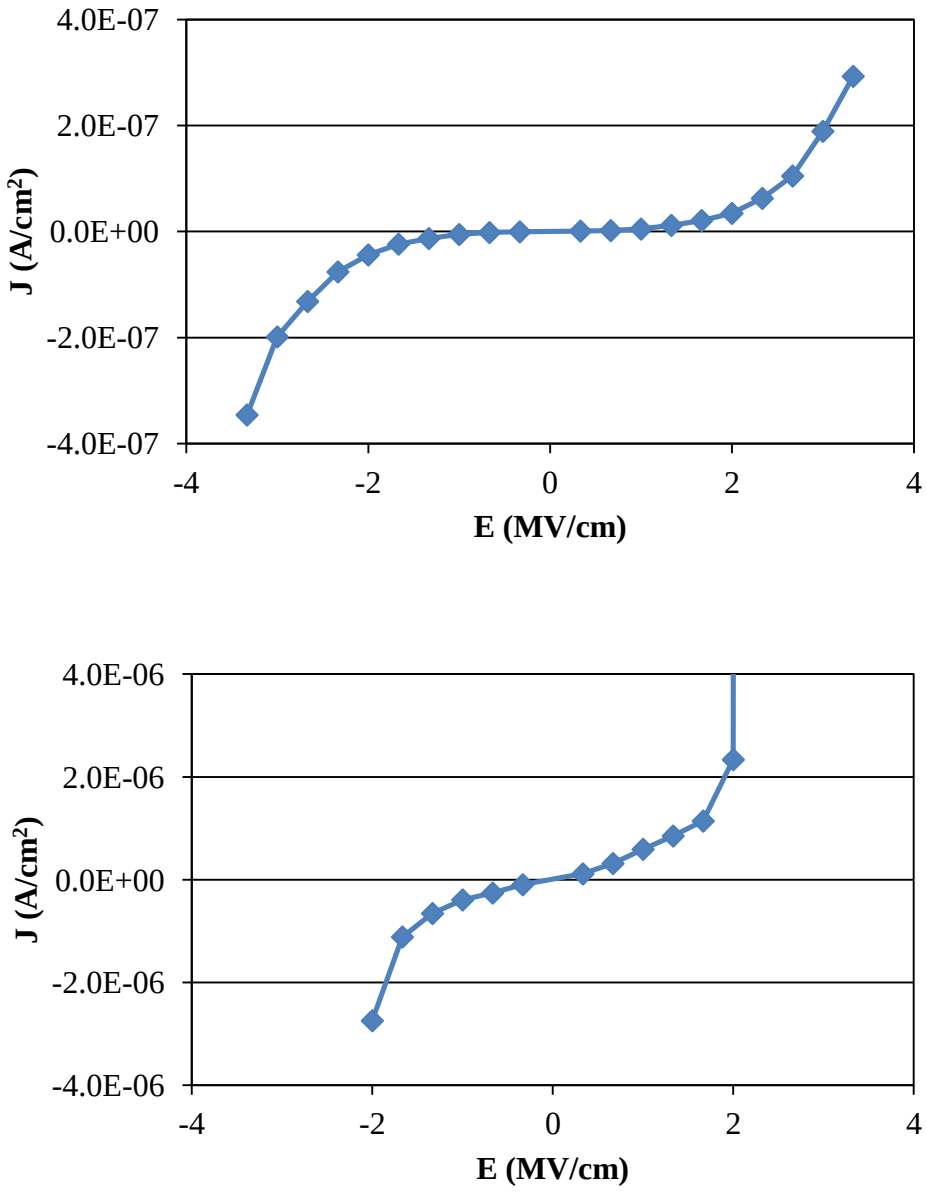

Figure 1.3. Electric field vs current density for capacitors with areas of $5x10^{-3}$ cm^2 (top) and $8x10^{-3}$ cm^2 (bottom).

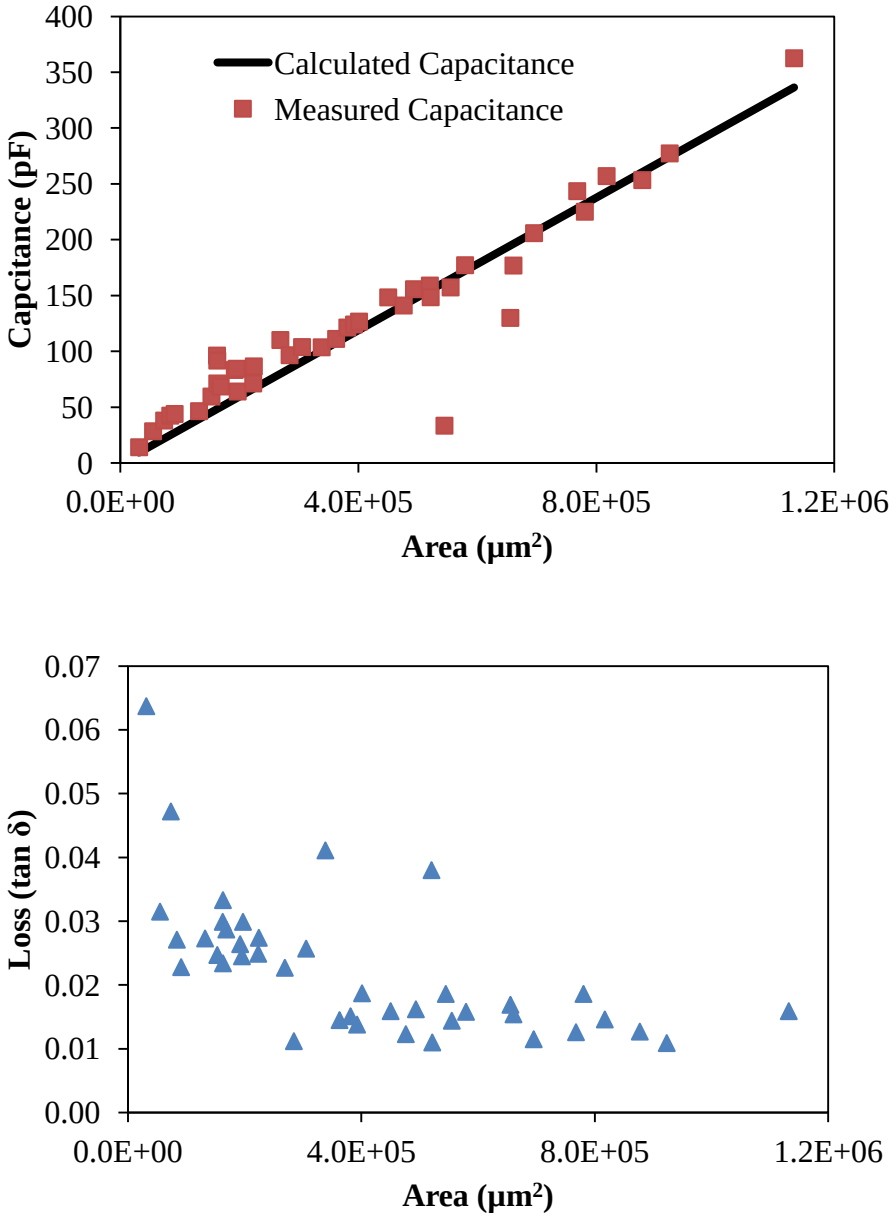

Figure 1.4. Capacitance vs. area (top) and loss vs. area (bottom) for the low frequency test devices.

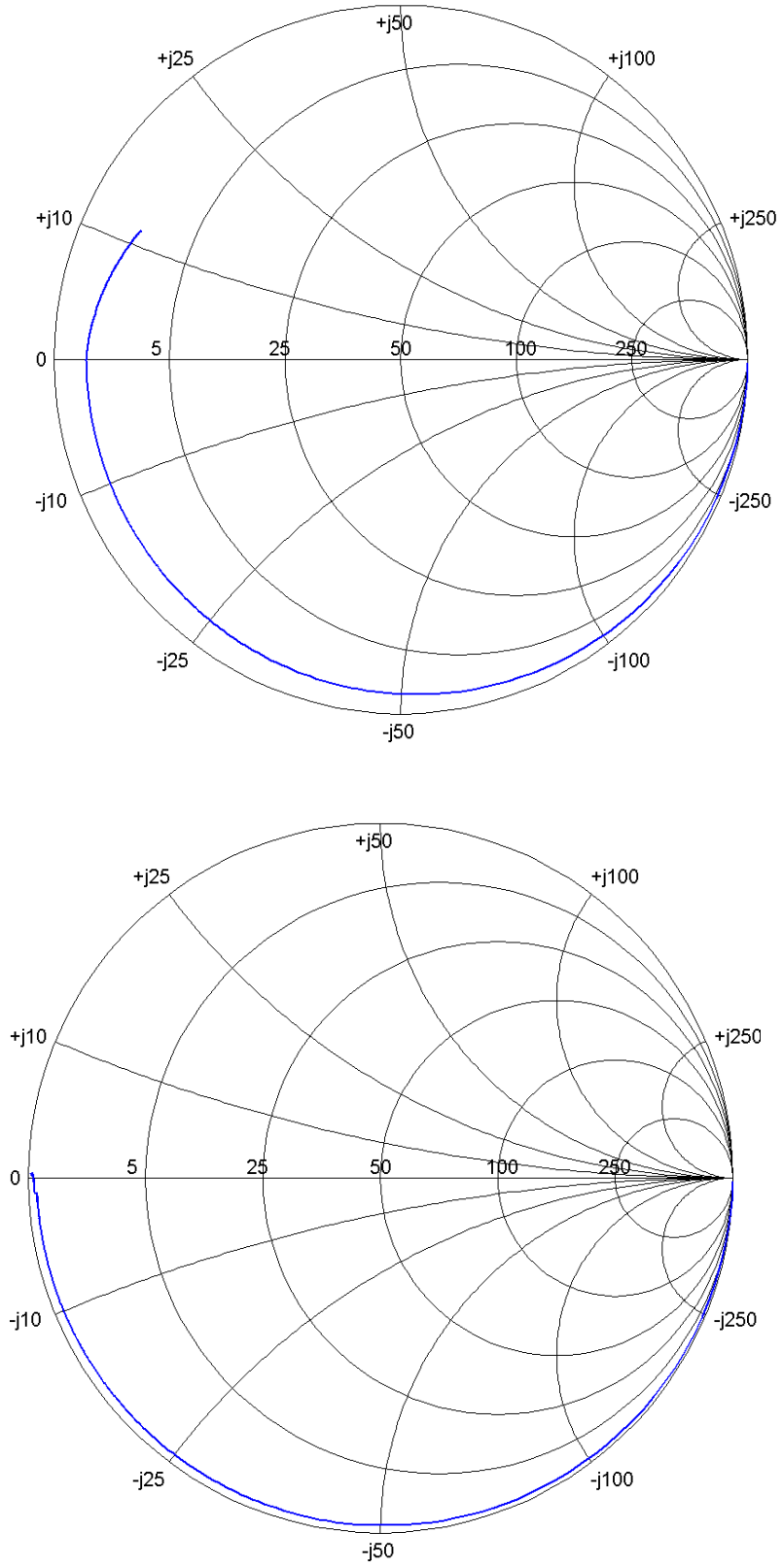

Figure 1.5. Top Smith chart is raw measurement (a). Lower chart (b) shows measured impedance after de-embedding of LR interconnect parasitics.

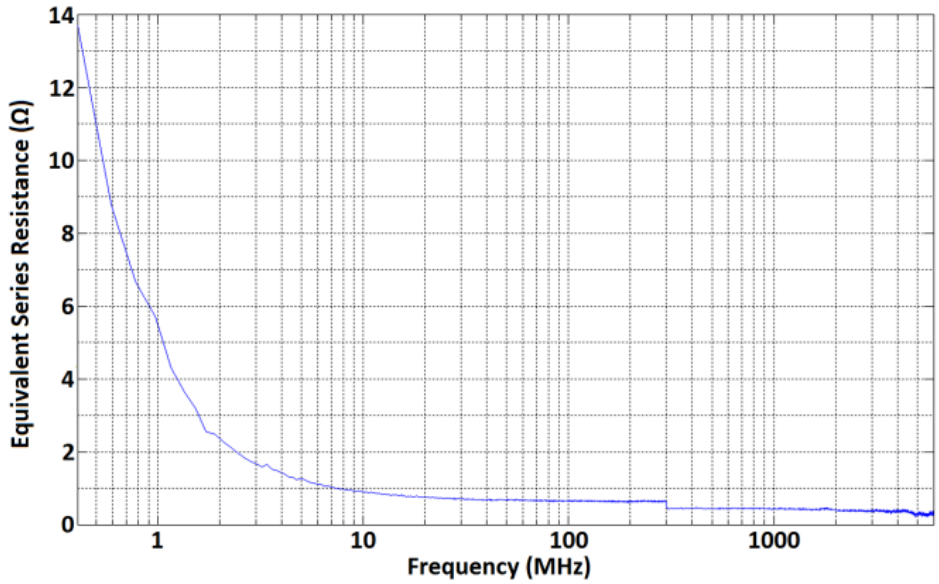

Figure 1.6. Equivalent series resistance (ESR) versus frequency for the $1.0x10^{-2}$ cm^2 capacitor.

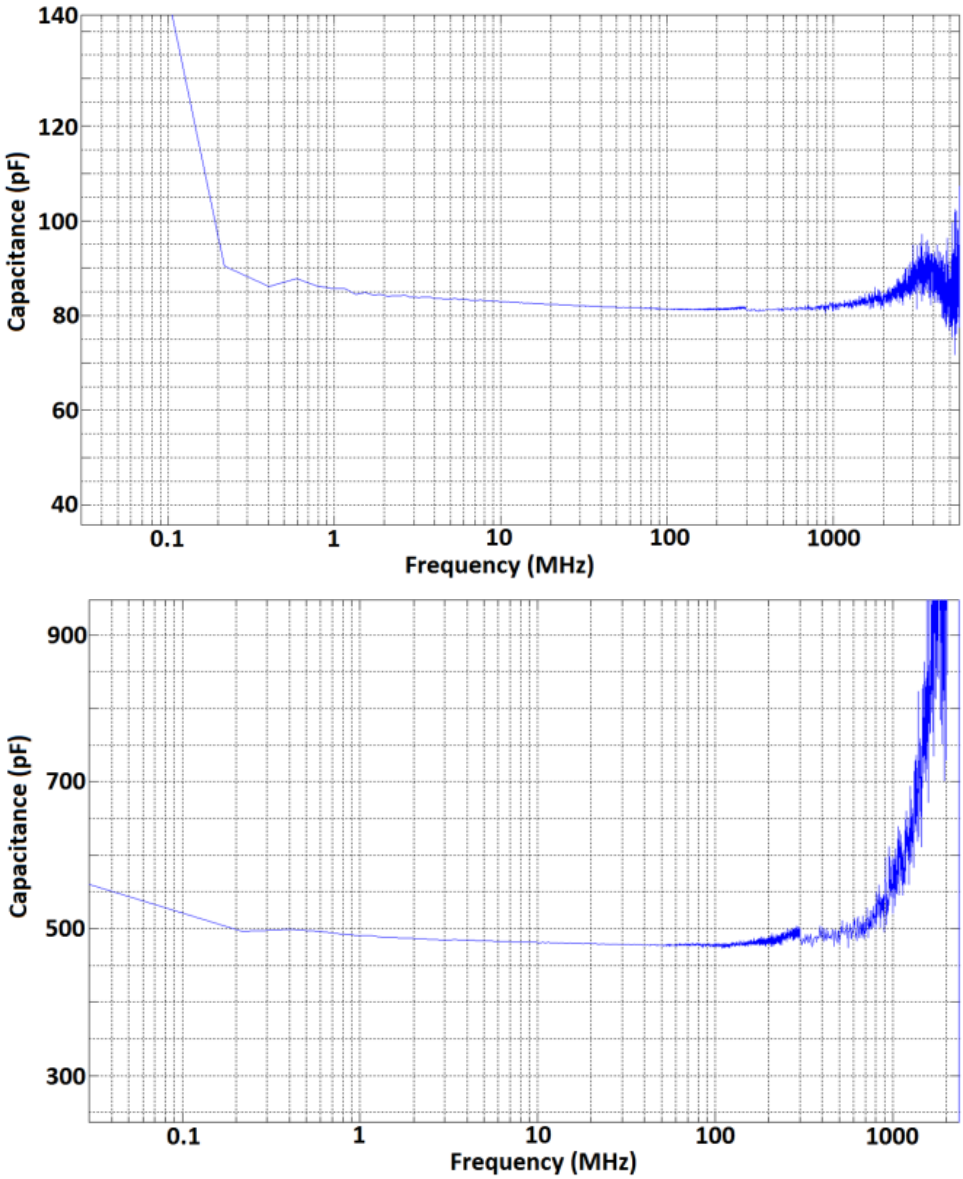

Figure 1.7. Capacitance vs. frequency for capacitors with areas of 6.5×10^{-4} cm^2 (top) and 1.0×10^{-2} cm^2 (bottom).

Table 1.1. Temperature coefficient of capacitance for 3-point probe capacitors.

Area	Temperature Coefficient	Capacitance change
cm^2	1/K	%
$6.5x10^{-4}$	$8.6x10^{-4}$	6.5
$2.6x10^{-3}$	$5.8x10^{-4}$	4.4
$5.8x10^{-3}$	$7.6x10^{-4}$	5.7
$1.0x10^{-2}$	$8.4x10^{-4}$	6.3

1.5. REFERENCES

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2. ELECTRON BEAM INDUCED CRYSTALLIZATION OF SPUTTER DEPOSITED AMORPHOUS ALUMINA THIN FILMS

Jack Murray, Kai Song, Wayne Huebner, and Matthew O'Keefe

Missouri University of Science and Technology
Department of Materials Science and Engineering
Rolla, MO 65409 USA

(Paper submitted to Materials Letters)

Keywords: crystallization, amorphous, alumina, thin-film, capacitor

ABSTRACT

Crystallization of amorphous alumina (Al_2O_3) in a thin film capacitor structure was induced by the electron beam of a transmission electron microscope (TEM). The crystallization was initially observed while collecting selected area diffraction (SAD) patterns after 2 minutes of beam exposure at an accelerating voltage of 200 keV and a beam current density of 13.0 A/cm^2. After 16 minutes of beam exposure, distinct ring patterns associated with crystal growth were evident in the SAD pattern. Bright field and dark field TEM images confirmed that crystallization occurred, with crystals growing up to ~50 nm in diameter.

2.1. INTRODUCTION

The crystalline form of alumina (α-Al_2O_3) is thermodynamically stable but amorphous alumina can be deposited by certain techniques in thin film form. Amorphous alumina has been deposited by a variety of techniques including pulsed laser deposition (PLD) [1] and sputter deposition [2-7]. Each of these deposition techniques is a form of physical vapor deposition (PVD), where the target material is vaporized and deposited onto the substrate with little to no change in chemical composition. Amorphous alumina is also deposited by anodization of aluminum [8], but the films are often porous and contain impurities from the anodization process.

Previous work has demonstrated the ability of an electron or ion beam to crystallize amorphous materials, including metal alloys [9-12], semiconductors [13], and insulators [3, 8, 13]. Electron or ion beam induced crystallization of amorphous alumina has been reported in the literature in only a few instances. One study involved the crystallization of amorphous anodic alumina coatings on Al under an electron beam in a TEM at an accelerating voltage of 100 kV [8]. This study does not mention the beam current necessary for crystallization and the anodic films contained impurities from the anodization solution. Another study documented the crystallization of sputter deposited amorphous alumina using 1 MeV Si^+ ions [3]. In this work electron beam-induced crystallization of a sputter deposited, amorphous Al_2O_3 film is reported. The results indicate that the process can be used to spatially manipulate the crystallinity, and thus the properties, of Al_2O_3 thin films over a selected area.

2.2. EXPERIMENTAL

Thin film capacitors with a Pt-Al_2O_3-Al layout were sputter deposited onto 11x11 cm fired low temperature co-fired ceramic (LTCC) substrates. The LTCC substrates were cleaned by immersion and agitation in acetone, methanol, and deionized (DI) water for 3 minutes each, with drying between each immersion step. Sputter deposition was carried out through 1.5 mm thick Mo shadow masks. Capacitor structures were constructed by depositing a Pt bottom electrode, followed by an Al_2O_3 dielectric layer, then a top Al electrode. Figure 2.1 shows a cross-section schematic of a metal-insulator-metal capacitor consisting of 0.1 μm Pt bottom electrode, 1 μm thick Al_2O_3 dielectric, and 0.2 μm Al top electrode.

Deposition was carried out using a Denton Discovery 18 magnetron sputter system. Metal (Al and Pt) electrode layers were deposited from 99.99% pure metal targets using a DC power supply at 300 W. The Al_2O_3 dielectric layer was deposited from a 99.9% pure ceramic target using a RF power supply at 200 W. No substrate heating was used during deposition and all films were deposited using 99.999% pure Ar as the sputtering gas, at a working pressure of 1.07 Pa. Base pressure before deposition was $\leq 10^{-6}$ Pa.

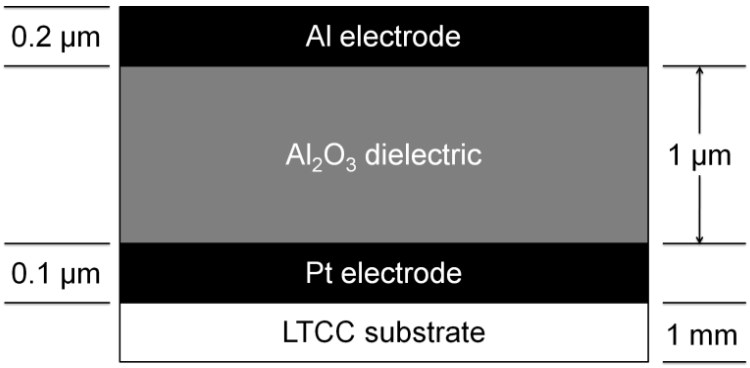

Figure 2.1. Schematic of the thin film capacitor layout used in this study, with approximate layer thicknesses.

TEM samples were prepared by focused ion beam (FIB) lift-out using a Helios Nano Lab 600 FIB. A cross section of a Pt-Al_2O_3-Al capacitor structure was milled using the FIB and lifted out using an omniprobe. TEM images and SAD patterns were collected using a Technai F20 TEM set at an accelerating voltage of 200 keV. SAD patterns were collected at beam currents of 18 nA and 135 nA, which correspond to current densities of 1.7 A/cm^2 and 13.0 A/cm^2. After the diffraction patterns were collected bright field TEM images were captured. Centered dark field images were also captured using a portion of the ring structure visible in the SAD patterns for the diffracted beam.

2.3. RESULTS AND DISCUSSION

Figure 2.2 shows selected area diffraction (SAD) patterns collected from the amorphous alumina region of the sample in the TEM at a current density of 1.7 A/cm^2. The first pattern was captured immediately after focusing and the second pattern was captured after 10 minutes of exposure to the electron beam. Both patterns are consistent with an amorphous material; no evidence of crystallization occurred for a current density of 1.7 A/cm^2 over the beam exposure times currently investigated.

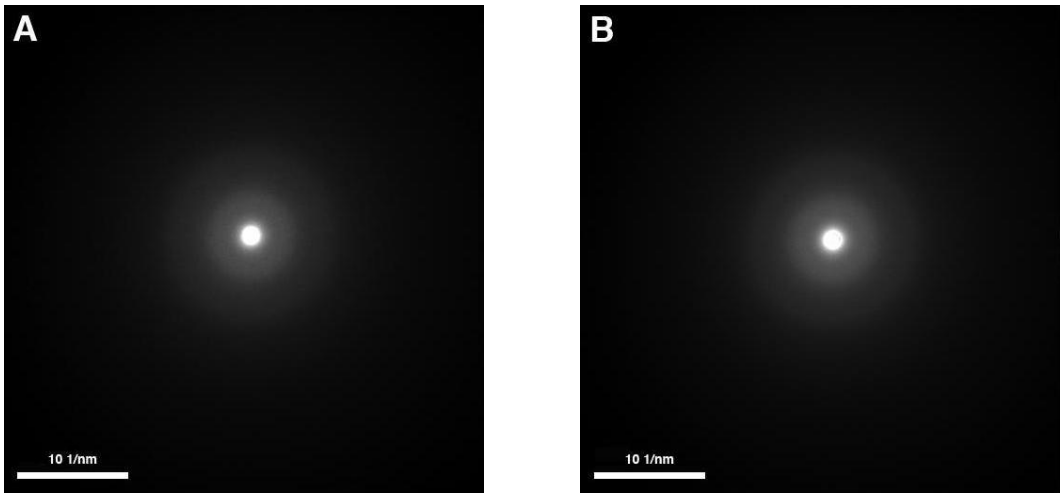

Figure 2.2. SAD patterns from Al_2O_3 thin film using a beam current of 1.7 A/cm^2: a) initially and b) after 10 minutes.

A second region of the amorphous alumina layer was then examined with a beam current of 13.0 A/cm^2. Figure 2.3 (a) shows the initial SAD pattern of the Al_2O_3 thin film, confirming the amorphous structure of the sputtered film. Crystallization began occurring after 2 minutes of electron beam irradiation (Figure 2.3 (b)). Increased beam time resulted in a sharpening of the polycrystalline rings in the subsequent patterns. Grain growth of the crystallized Al_2O_3 is shown by the formation of diffraction spots in the SAD pattern after 16 minutes of beam exposure, as shown in Figure 2.3 (c).

Polymorphs of Al_2O_3 are difficult to distinguish from each other using electron diffraction due to their similar d-spacings. The processing route from amorphous-Al_2O_3 to α-Al_2O_3 is believed to occur via the following sequence [14]:

$$\text{Amorphous} \rightarrow \gamma \rightarrow \delta \rightarrow \theta \rightarrow \alpha\text{-}Al_2O_3 \qquad (1)$$

Values for d-spacings for each of the outlined Al_2O_3 polymorphs were located in JCPDS diffraction files [15] and the existence of any one polymorph over the others could not be definitively confirmed. The crystals formed in this study appear to be a mix of several Al_2O_3 polymorphs, as calculated d-spacings matched at least one of the structures listed

above. This was in agreement with previous work that found that different Al_2O_3 polymorphs can be present in samples simultaneously [14].

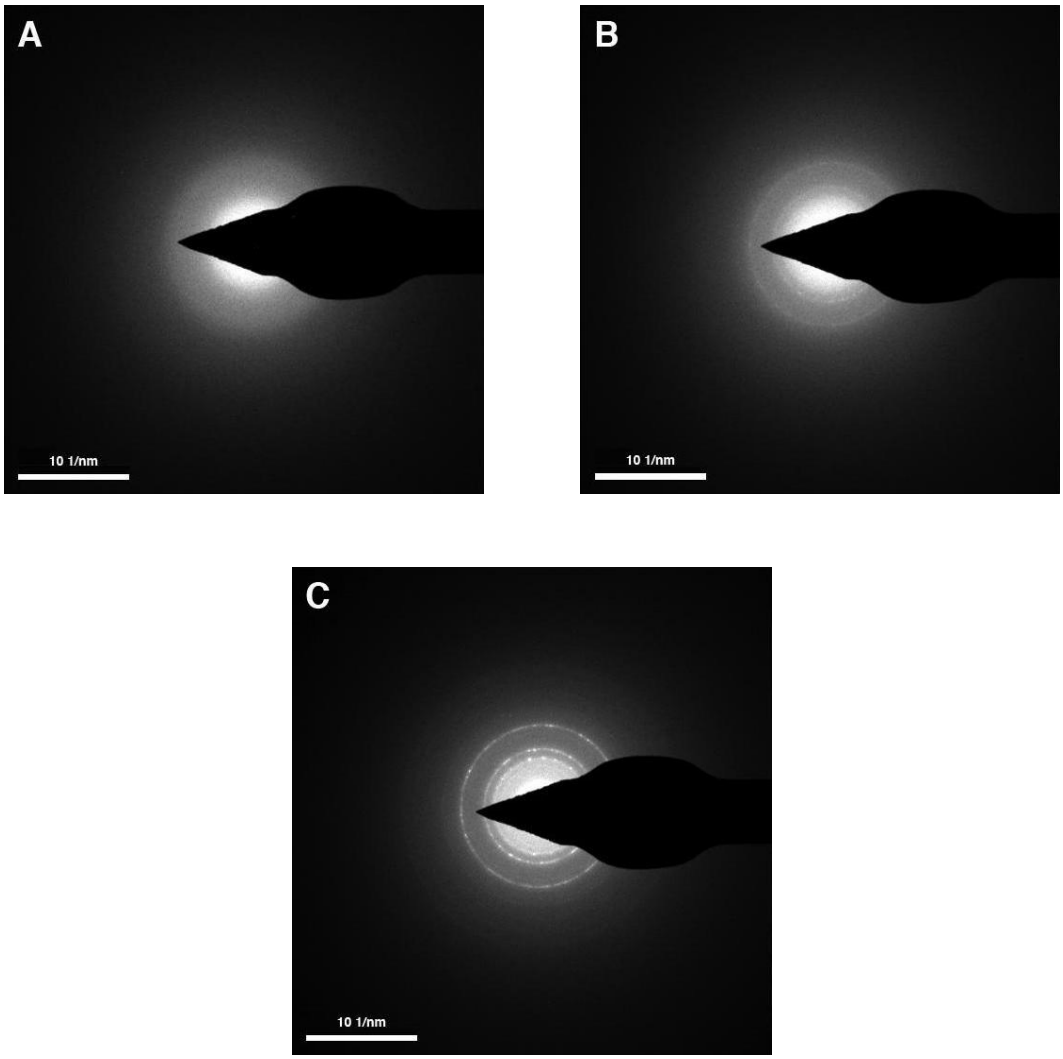

Figure 2.3. SAD patterns from Al_2O_3 thin film: a) 13.0 A/cm^2 initially, b) after 2 minutes, and c) after 16 minutes.

Figure 2.4 (a) shows the crystallized area in the amorphous Al_2O_3 layer that was exposed to the electron beam for 16 minutes. The bright-field TEM micrograph also shows the entire height of the thin-film capacitor structure, with the LTCC substrate, Pt electrode, Al_2O_3 dielectric and the Al electrode all visible. Holes in the sample are also visible to the right of the crystallized area from attempts at obtaining convergent beam electron diffraction (CBED) patterns. Collection of CBED patterns were unsuccessful; the patterns would change from amorphous to crystalline in a matter of seconds and then the beam would punch through the sample. A dark-field TEM micrograph of the crystallized alumina, after 16 minutes of electron beam exposure is shown in Figure 2.4 (b). The largest crystals oriented in the direction of the diffracted beam are ~ 50 nm in diameter.

Note that in Figure 2.4 (a) that there is a decrease in crystallization toward the top of the Al_2O_3 layer, near the Al top electrode. In contrast, the bottom of the area exposed to the electron beam is highly crystallized. The difference in crystallization between the two regions, both of which were exposed to the electron beam, is thought to occur because of the difference between the thermal conductivity, κ, of Al and Al_2O_3. In thin film form, the thermal conductivity of Al has been measured at 200 W m^{-1} K^{-1} [16]. In contrast, the thermal conductivity of thin film Al_2O_3 deposited by anodic oxidation measured 0.5 W m^{-1} K^{-1} [17]. The large thermal conductivity disparity seems to indicate that the Al dissipates thermal energy away from the Al_2O_3, minimizing crystallization in the region near the Al. This, along with the detection of crystal growth in the diffraction patterns indicates that the crystallization process is thermal in nature, instead of an athermal, energy dissipation process described elsewhere [9].

2.4. CONCLUSIONS

Sputter deposited thin film capacitor structures were fabricated and examined by transmission electron microscopy. Selected area diffraction patterns indicated that the amorphous alumina dielectric layer crystallized at current densities of 13.0 A/cm^2, but no crystallization occurred at 1.7 A/cm^2 beam current density. Crystallization began to occur after two minutes of beam exposure. Grain growth took place with longer beam exposure times and the largest crystals visible in TEM micrographs were ~ 50 nm in

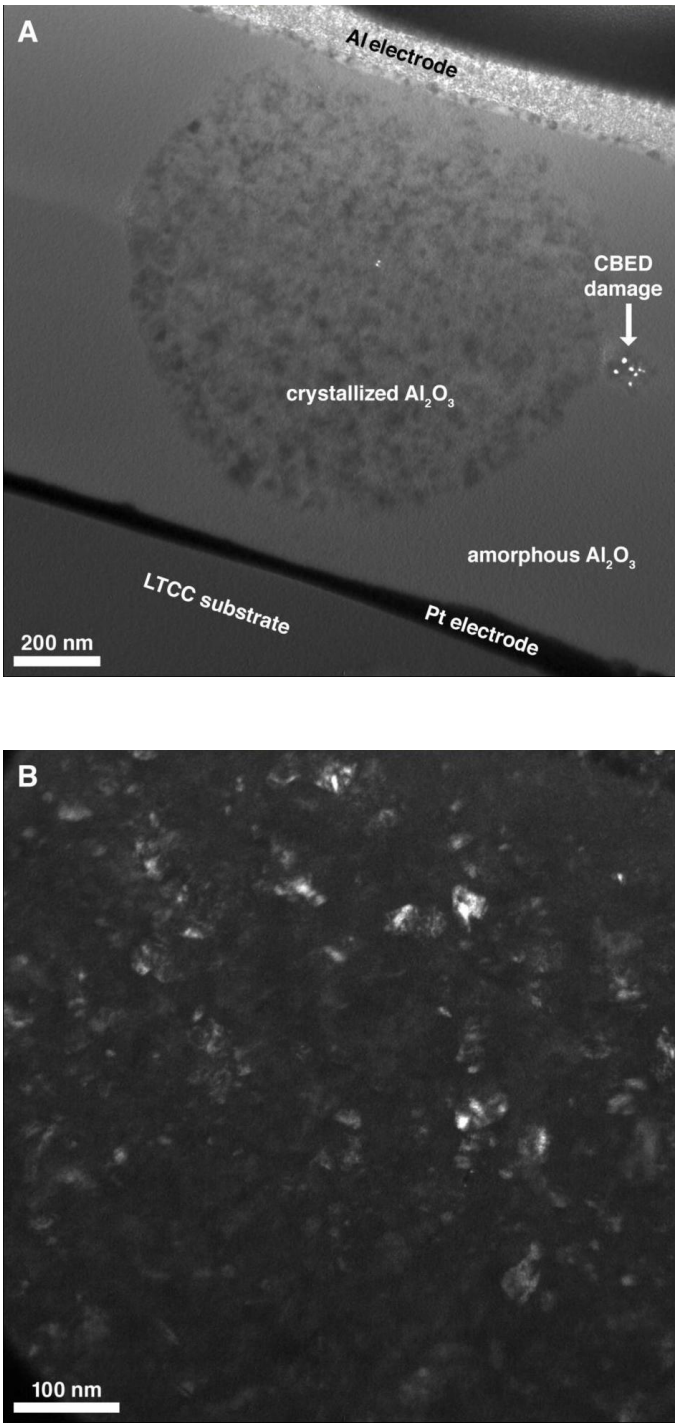

Figure 2.4. TEM micrographs illustrating crystallized Al_2O_3: a) bright-field overview of crystallized area and b) dark-field detail of crystallized area after 16 minutes of electron beam exposure.

diameter after 16 minutes of electron beam exposure. 10 minutes of beam exposure at a current density of 1.7 A/cm^2 did not lead to crystallization. These results show that an electron beam can be used to selectively crystallize amorphous thin films in precise areas. As such, spatial variation of anisotropic properties can be achieved commensurate with the symmetry of the crystallized region.

Acknowledgements

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3. EFFECT OF ELECTRODE MATERIAL AND DIELECTRIC THICKNESS ON THE PERFORMANCE OF SPUTTER DEPOSITED NANO CAPACITORS

Jack Murray, Kai Song, Wayne Huebner, and Matthew O'Keefe

Missouri University of Science and Technology
Department of Materials Science and Engineering
Rolla, MO 65409 USA

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ABSTRACT

Thin film capacitors with Al or Pt electrodes and Al_2O_3 dielectric layers were deposited on low temperature co-fired ceramic (LTCC) substrates by magnetron sputtering. The capacitors featured a single dielectric layer with thicknesses ranging from 150 to 1500 nm and device areas from ~10^4 μm^2 to ~10^6 μm^2. Impedance analysis and current-voltage testing were carried out to determine the effect of electrode material and dielectric thickness upon capacitor performance. Capacitance for devices with Al electrodes ranged from ~10 to ~700 pF, depending on capacitor area and dielectric thickness, and the fit to expected values was better than devices with Pt or mixed (one Al, one Pt) electrodes. Dielectric loss increased with increasing Al_2O_3 thickness, but loss of ~0.02 was higher than bulk Al_2O_3 ~0.001 for all capacitors. Transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) were utilized to examine selected capacitor structures. TEM examination and impedance analysis both confirm that functioning capacitors with Al electrodes and 300 – 1000 nm thick Al_2O_3 dielectric layers can be fabricated on LTCC substrates using sputter deposition.

3.1. INTRODUCTION

Low temperature co-fired ceramic (LTCC) substrates are made up of multilayer, tape cast ceramic and glass materials with conductive ink patterns that are fired together in one step. Devices, such as capacitors, can be embedded between layers of the

substrate or deposited onto the surface. LTCCs are being investigated for use in wireless communications as well as microelectronics packaging [1]. The surface roughness of LTCC substrates, ~ micrometers, is significantly higher than atomically smooth Si wafers, making it difficult to deposit functioning capacitor structures with thicknesses on the order of hundreds of nanometers.

Thin film capacitor structures in the metal-insulator-metal (MIM) configuration are being developed for use as filters in RF circuits [2, 3] or as a component in field effect transistors [4, 5]. In many cases, the dielectric materials used in MIM capacitor structures are SiO_2 or Si_3N_4 [3], with dielectric constant (K) values of 3 and 7.5, respectively. Recent efforts in MIM capacitor research involve the use of materials with higher K. Due to properties such as K~10, high electrical breakdown strength, and thermal stability up to 1000°C, Al_2O_3 is an attractive material for microelectronic applications. As such, thin films of Al_2O_3 have been deposited as a high-K material for use in transistors [6-11].

Platinum is widely used as an electrode material in microelectronic applications due to its low resistivity value (10.7×10^{-8} Ω m) and chemically inert characteristics. Although Pt is usually considered to be non reactive in most situations, reactions occur under certain conditions. Pt will react with Bi, a component of certain ferroelectric materials, under reducing atmospheres. The resulting alloy degrades capacitor properties [12]. Dissimilar metal electrodes can negatively affect the properties of capacitors, such as conduction [13] and leakage current [14]. These issues arise from work function differences between the metals [13] and diffusion of metal atoms into the dielectric [14]. When using different electrode materials in a thin film capacitor, care must be taken to account for these possible issues.

In this study thin film capacitors were deposited onto LTCC substrates with Al or Pt electrodes and Al_2O_3 dielectric layers of various thicknesses. The resulting devices were examined by transmission electron microscopy (TEM). Capacitance and loss, as well as current-voltage testing were carried out to determine the electrical response of the capacitor structures.

3.2. EXPERIMENTAL PROCEDURE

Sputter deposition was carried out with a Denton Discovery 18 system. Electrode layers were deposited from 99.99% pure metallic targets at a power of 300 W using a DC power supply. Dielectric layers were deposited from a 99.9% pure Al_2O_3 target at a power of 200 W using a RF power supply. All sputter deposition runs were carried out in an atmosphere of 99.999% pure Ar at a working pressure of 8 mtorr. Electrode layers were deposited to approximately 200 nm in thickness while the dielectric thickness was varied for each substrate, with thicknesses of approximately 150, 300, 450, 600, 1000, and 1500 nm. Layer thicknesses were measured using a Tencor Alpha Step 200 profilometer on glass microscope slides that were deposited on at the same time as capacitor layers. No substrate heating was used during deposition.

Capacitor layers were deposited through metallic shadow masks onto 11x11 cm fired LTCC substrates. The substrates were cleaned by immersion and agitation in acetone, methanol, and de-ionized water for three minutes before deposition. Deposition was carried out through three laser machined molybdenum metal masks. Each capacitor was fabricated in three steps, first the bottom Al or Pt electrode, then the Al_2O_3 dielectric, then the top Al or Pt electrode. The metal electrode masks featured openings with widths of approximately 150, 380, 530, and 750 μm and the dielectric mask featured four vertical openings, illustrated in Figure 3.1A. A total of 48 capacitors with 9 different areas were deposited on each substrate. The bottom electrodes are shown in black and feature a 90 degree bend. The Al_2O_3 dielectric layer is shown in gray and the top electrodes are black and cross over the bottom electrodes. Each area where the electrodes cross over is an individual capacitor structure. Figure 3.1B shows a cross sectional image of the thin film, metal-insulator-metal capacitors with the approximate layer thicknesses.

The experimental design was to investigate Al and Pt electrode materials and Al_2O_3 dielectric thicknesses. One set of substrates featured capacitors in an Al-Al_2O_3-Al (bottom electrode-dielectric-top electrode) configuration with dielectric thicknesses of approximately 150, 300, 450, 600, 1000, and 1500 nm. Two of the substrates feature capacitors in a Pt-Al_2O_3-Pt configuration with dielectric thicknesses of approximately 450 and 600 nm. Another two substrates featured capacitors with Pt-Al_2O_3-Al and Al-Al_2O_3-Pt layouts with dielectric thicknesses of approximately 1000 nm.

Cross-sectional samples were prepared for TEM examination by ion-milling in a Helios Nano Lab 600 FIB/SEM. The samples consisted of two capacitors with 1 μm Al_2O_3 dielectric layers, with Al electrodes on one sample and Pt bottom and Al top electrodes on the other sample. TEM examination was carried out in a Tecnai F20 STEM. In addition to TEM and STEM images, EDS line scans were carried out to verify the chemical composition of the films. Resistance measurements were carried out with a Keithly Model 2002 digital multimeter. A resistance value of 2 MΩ was chosen as a screening value between functioning and faulty capacitors. Capacitance and loss were measured with a HP 4194A Impedance analyzer. Measurements were carried out at 10 kHz. Current-voltage measurements were carried out with a HP 4140B pA Meter. Capacitors were tested from -100V to 100V in an alternating fashion (10V, -10V, 20V, etc). Results are reported as current density, J (A/m^2), vs. electric field, E (MV/m). The testing voltages correspond to electric field magnitudes below 3.3 MV/cm, depending on dielectric thickness.

3.3. RESULTS AND DISCUSSION

All of the devices were measured optically in order to determine actual sizes of electrode overlap area and those measurements were used to calculate capacitance values. Due to lifting of the shadow masks during deposition, up to a 50% deviation in the size of capacitors was observed. The significant spread in measured capacitor areas resulted in a continuous range of capacitor areas instead of the specific areas from the mask design.

3.3.1. TEM Examination. A focused ion beam (FIB) cross section of a selected capacitor was examined by transmission electron microscopy (TEM). Figure 3.2A is a bright field TEM overview of a Al-Al_2O_3-Al capacitor with a 1000 nm dielectric layer on an LTCC substrate. On the left side of the image is the LTCC substrate, which has visible grains on the order of 1 μm in size. The capacitor structure is visible on the right side of the image. Note that the sputter deposited films are continuous and completely covered the protruding grain from the substrate. All of the cross sections examined during the course of this study exhibited a conformal structure. Figure 3.2B is a bright field scanning transmission electron microscopy (STEM) image of a section of the

capacitor structure. The polycrystalline grain structure of the Al electrodes is visible, and the lack of visible grains indicates the amorphous structure of the Al_2O_3 dielectric layer. Convergent beam electron diffraction (CBED) patterns confirmed the amorphous structure of the dielectric layer. The holes that are visible in the middle of the dielectric layer are from the electron beam punching through the sample during CBED pattern collection. A CBED pattern of the amorphous Al_2O_3 dielectric is included as an inset in Figure 3.2B.

Standardless energy dispersive spectroscopy (EDS) was carried out to determine the chemical composition of the capacitor structures. Results from EDS line scans of one sample are shown in Figure 3.3. The scan went from the LTCC substrate through the entire capacitor structure, as illustrated in Figure 3.3A. An atomic map was made from the EDS data and is shown in Figure 3.3B. The Al electrodes had no appreciable O and an abrupt interface. The middle region of the line scan, which is expected to be made up of Al_2O_3, contains ~55 weight % Al and ~45 wt. % O. This corresponds to the ratio of Al to O of stoichiometric Al_2O_3. An Al rich section of the Al_2O_3 dielectric was detected next to each of the Al electrodes.

3.3.2. Electrical Testing. Resistance measurements were used to act as an initial screening measure between well behaved, functioning capacitors and highly conductive, faulty devices. More than 90% of the capacitors with Al electrodes with dielectric thicknesses between 300 and 1000 nm featured resistance values >20 MΩ. The substrates with the thinnest (150 nm) and thickest (1500 nm) Al_2O_3 dielectric layers featured less functioning capacitors. The smallest number of functioning capacitors (~70%) was found for capacitors with Pt electrodes, regardless of the thickness of the Al_2O_3 dielectric layer.

Capacitors featuring Al electrodes were deposited onto LTCC panels in the layout shown in Figure 3.1A with a variety of Al_2O_3 dielectric thicknesses. The capacitance and loss of each capacitor was measured and plotted against the corresponding capacitor area, shown in Figure 3.4. The theoretical capacitance was calculated for each capacitor from the following equation:

$$C = \frac{\varepsilon_0 AK}{t} \quad (1)$$

where C is capacitance (F), ε_0 is the permittivity of free space (F/m), K is the dielectric constant, A is the actual capacitor area (m^2) as measured optically, and t is the dielectric thickness (m). Based on the TEM and EDS data the dielectric constant of the thin film Al_2O_3 was assumed to be equal to the bulk value of 10. Calculated capacitance values for Al-Al_2O_3-Al structures are shown as the solid lines in Figure 3.4. Measured capacitance values are shown by solid triangles in Figure 3.4 and loss data is shown by open triangles.

From equation 1, the expected capacitance decreases as dielectric thickness increases. This is demonstrated by the line in Figures 3.4A-F. Measured capacitance values generally follow the expected value line in each plot, with some outliers and deviations. The fit of the measured capacitance values to the expected capacitance varies with thickness. A poorer fit to expected capacitance values was seen for the thinnest (Figure 3.4A) and thickest (Figure 3.4F) Al_2O_3 dielectric layers. In Figures 3.4D-F the measured capacitance values lie above the expected capacitance line, indicating either a slightly higher dielectric constant of thin film Al_2O_3 or local areas of thinner dielectric.

Departures from predicted capacitance values could either be due to inaccuracies in geometric measurements, or the assumption that the dielectric constant of the Al_2O_3 dielectric is constant and independent of deposited thickness. With respect to the area, optical images were used to determine the electrode dimensions. The thickness of the dielectric is assumed to be identical to that of the deposited thickness, which was measured by profilometry. Another possibility is that the electrodes form Ohmic contacts with the dielectric, resulting in an accumulated space charge within the dielectric and a thinner effective dielectric. This would result in greater measured capacitance values. Fringe fields at the edges of the electrodes would add to the measured capacitance. Modeling the field distribution as a function on dielectric thickness and dielectric constant was beyond the scope of this study, but this effect would increase with smaller dielectric thickness and greater electrode area, thereby increasing the measured capacitance.

Assuming the dielectric constant of the Al_2O_3 is independent of thickness depends upon the assumption that the degree of crystallinity and molar volume are constant. All TEM measurements indicated the deposited dielectric is amorphous. The fact that most of the dielectric measurements indicate using a crystalline K=10 is accurate suggest the molar volume of the amorphous state is close to that of the crystalline state. The total polarizability, P, of a linear dielectric is given by

$$P = \sum_i N_i \alpha_i \tag{2}$$

where N_i, is the concentration of the i^{th} ion and α_i is the atomic polarizability. Hence the dielectric properties depend primarily upon the presence of the Al^{3+} and the O^{2-} ions, and not as much on their crystalline arrangements. Thickness effects on the dielectric constant could then only be related to changes in stoichiometry (Al:O ratio) or the density of the deposited dielectric. These were not measured during the course of this study. If there were a crack in the Al_2O_3 dielectric layer and the top electrode were deposited conformally on top, there would be a thinner area in the dielectric which would lead to higher capacitance than calculated from Equation 1. Cracks are likely to form in thicker (~1000 nm) sputter deposited films, due to film stresses develop from the inhibition of atomic rearrangement after deposition.

Capacitor structures with Pt electrodes were also fabricated and tested. Figure 3.5 presents capacitance and loss data for MIM capacitors with Pt electrodes and Al_2O_3 dielectric. Although the capacitors in Figures 3.5A and 3.5B feature relatively low loss values (< 0.1), comparable to devices with Al electrodes, the capacitance values are very inconsistent and vary widely. Expected capacitance values were calculated from Equation 1 with the same assumption of the dielectric constant of Al_2O_3 and measured device geometry, but measured capacitance was higher than expected for ~90% of the capacitors in each set of devices. Capacitance and loss data for devices with dissimilar electrode materials are presented in Figures 3.5C and 3.5D. Both sets of capacitor structures include capacitance data that is spread away from the expected capacitance value trendline. Again, more than 90% of the measured capacitance values in Figure 4.5C

are higher than expected from Equation 1. Clearly the capacitor structures with Pt electrodes perform differently than capacitors with Al electrodes.

All of the capacitors in this study feature significantly higher dielectric loss than capacitors with bulk Al_2O_3 as the dielectric material. The increase in dielectric loss can possibly be attributed to the lack of long range order or microcracks in the amorphous Al_2O_3 films. Other studies point out that the lowest dielectric loss for a material is found when it is in perfect crystal form. Adding disorder or defects to the structure increases the dielectric loss measured in the material [15]. Another possible cause of the increased dielectric loss for the capacitors in this study is water infiltration into the Al_2O_3 dielectric layer [16]. This was tested by heating capacitors above 100°C while measuring dielectric loss. A slight decrease in loss was seen at elevated temperatures followed by an increase again at room temperature. All capacitors were measured under ambient conditions with no effort made to control the relative humidity. Adsorbed moisture on the surface could increase the dielectric loss. The capacitors in Figures 3.4F, 3.5C and 3.5D feature higher average dielectric loss values than any of the other capacitors tested in this study, possibly owing to the thickness of the Al_2O_3 layers and the increased cracking associated with thick sputter deposited films.

Current voltage measurements were carried out on selected capacitors with capacitance data shown in Figures 3.4E, 3.5C and 3.5D. The results are featured in Figures 3.6A-C and reported as current density, J (A/m^2), vs. electric field, E (MV/m). Figure 3.6A features a sweep from -100V to 100V for a capacitor with an area of $2.3x10^{-3}$ cm^2 and is representative of capacitors with both electrodes made from the same metal. Note that the slope of the line at any point in Figure 3.6A is the resistivity, ρ (Ω m), of the Al_2O_3 dielectric layer. The resistivity value from Figure 3.6A is $1.5x10^{11}$ Ω m which is comparable with the resistivity of bulk Al_2O_3 ($1x10^{13}$ Ω m) [17]. A highly insulating value is a good indication of capacitor performance; in this case the device had a capacitance of 32 pF and loss of 0.05. The plots featured in Figures 3.6B and 3.6C each include two sweeps from -100 to 100 V with the polarity of the top electrode being the difference between them. During the sweep with the top electrode positive (indicated by the closed circles in the plots), the voltage from the test apparatus readout was applied to the top electrode. During the other sweep the top electrode was negative (indicated by

the closed triangles in the plots), which means the opposite voltage from the test apparatus readout was applied to the top electrode. Polarity was switched by physically moving the leads to the test equipment between runs. Current density responds asymmetrically for applied field between each sweep in Figures 3.6B and 3.6C. Differences in charge injection mechanisms between the Al and Pt electrodes are the likely causes of the observed asymmetry. From the portion of each sweep with greater slope, it appears that Pt injects electrons into the Al_2O_3 when it is the cathode. The linear portion of each sweep indicates that there is a barrier to charge injection from the Al electrode.

Both the capacitance and loss (Figures 3.4 and 3.5), as well as I-V data (Figure 3.6) indicate a fundamental difference between capacitor structures with Al and Pt electrodes. This most likely arises due to the work function difference between Al (~4.25 eV) and Pt (5.64 eV). If band diagrams of each metal-insulator interface are constructed, then a number of situations can arise, including the Ohmic contact. An Ohmic contact results in electrons being injected into the insulator conduction band, resulting in an intrinsic field in the insulator. In Figure 3.6B and 3.6C an asymmetric response from switching the polarity indicates that Pt injects electrons into the Al_2O_3 layer while Al does not. These results from indicate that Pt forms an Ohmic contact with Al_2O_3 while Al does not. When used as electrode materials in a metal 1-insulator-metal 2 arrangement, metals with different work functions will transfer charge from the metal with the lower work function to the metal with the higher work function. This also creates an intrinsic field in the dielectric that alters the electrical properties of the capacitor structure, shown again in Figures 3.6B and 3.6C. The electrons in the Al_2O_3 dielectric layer that are injected from Pt lead to an effective insulator thickness that is smaller than the actual layer thickness. This lower effective thickness can explain the measured capacitance values that are higher than calculated when using Pt electrodes, as shown in Figures 3.5A, 3.5B and 3.5C.

3.4. CONCLUSIONS

Sputter deposited thin film capacitors were fabricated and characterized through electrical testing and microstructural analysis. Capacitors with Pt electrodes featured

higher dielectric loss and larger variation from expected capacitance values than devices with Al electrodes, owing to the formation of an Ohmic contact with Al_2O_3. All of the capacitors featured higher dielectric loss than exhibited by bulk Al_2O_3, which is likely due to disorder in the sputter deposited films. Images and diffraction patterns captured by TEM confirmed the conformal coating of the sputter deposited films and the amorphous structure of the Al_2O_3 films.

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This work was performed with the support of Honeywell FM&T under contract EP39664. The guidance and support of Dr. Ambrose Wolf and Dan Krueger is gratefully acknowledged. The authors would also like to thank Dr. Elizabeth Kulp and Dr. Travis McKindra for FIB TEM sample preparation assistance.

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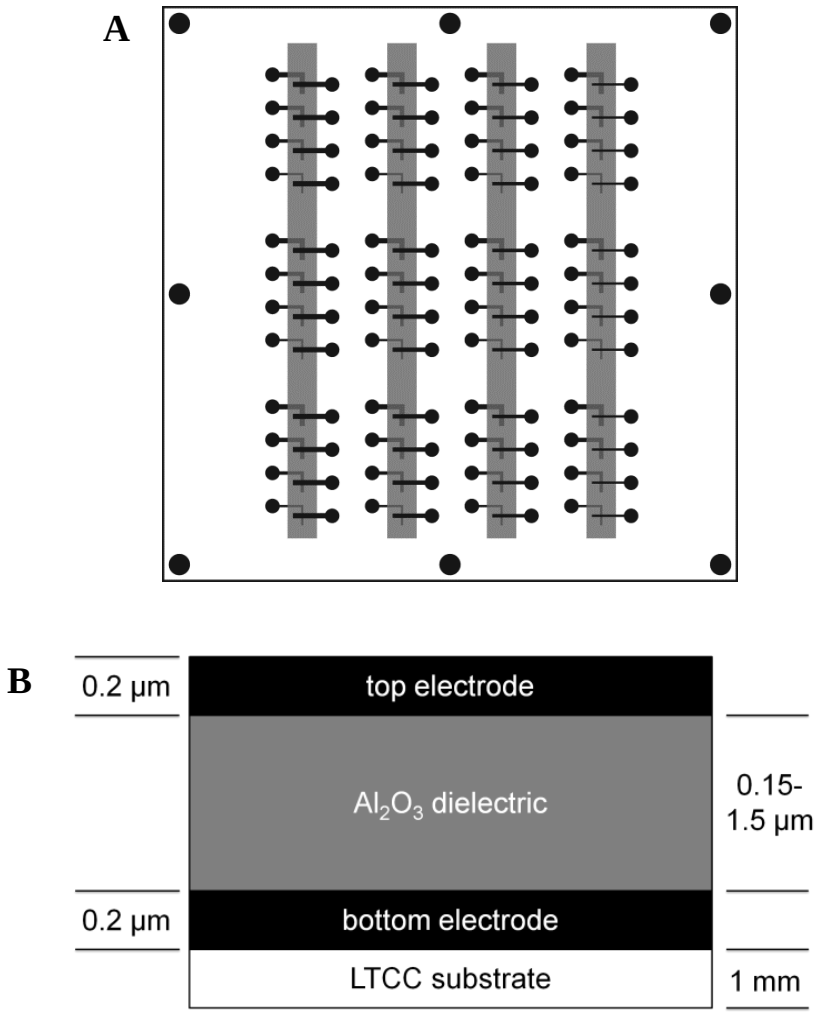

Figure 3.1. Diagrams of (a) capacitors on LTCC substrate, and (b) cross section of an example capacitor showing approximate layer thicknesses.

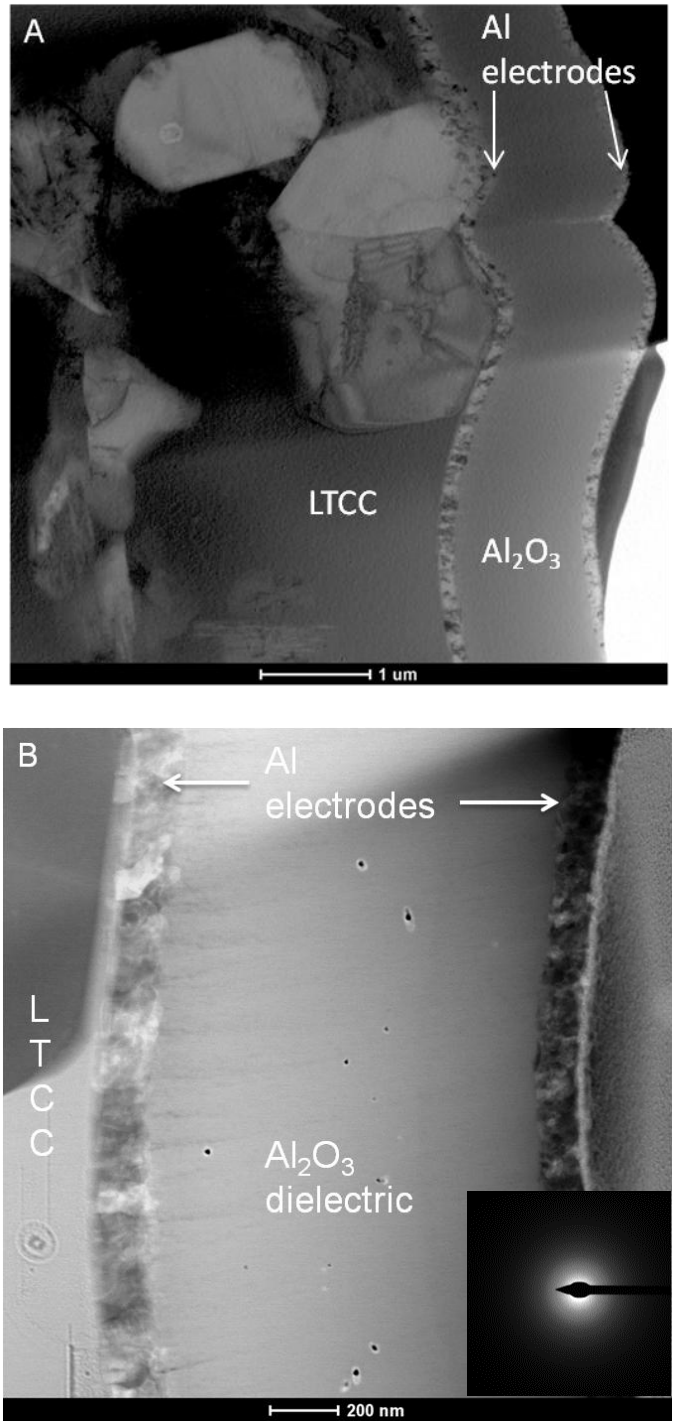

Figure 3.2. Al-Al_2O_3-Al capacitor, (a) TEM bright field overview and (b) STEM detail images with a CBED pattern from the amorphous Al_2O_3 region.

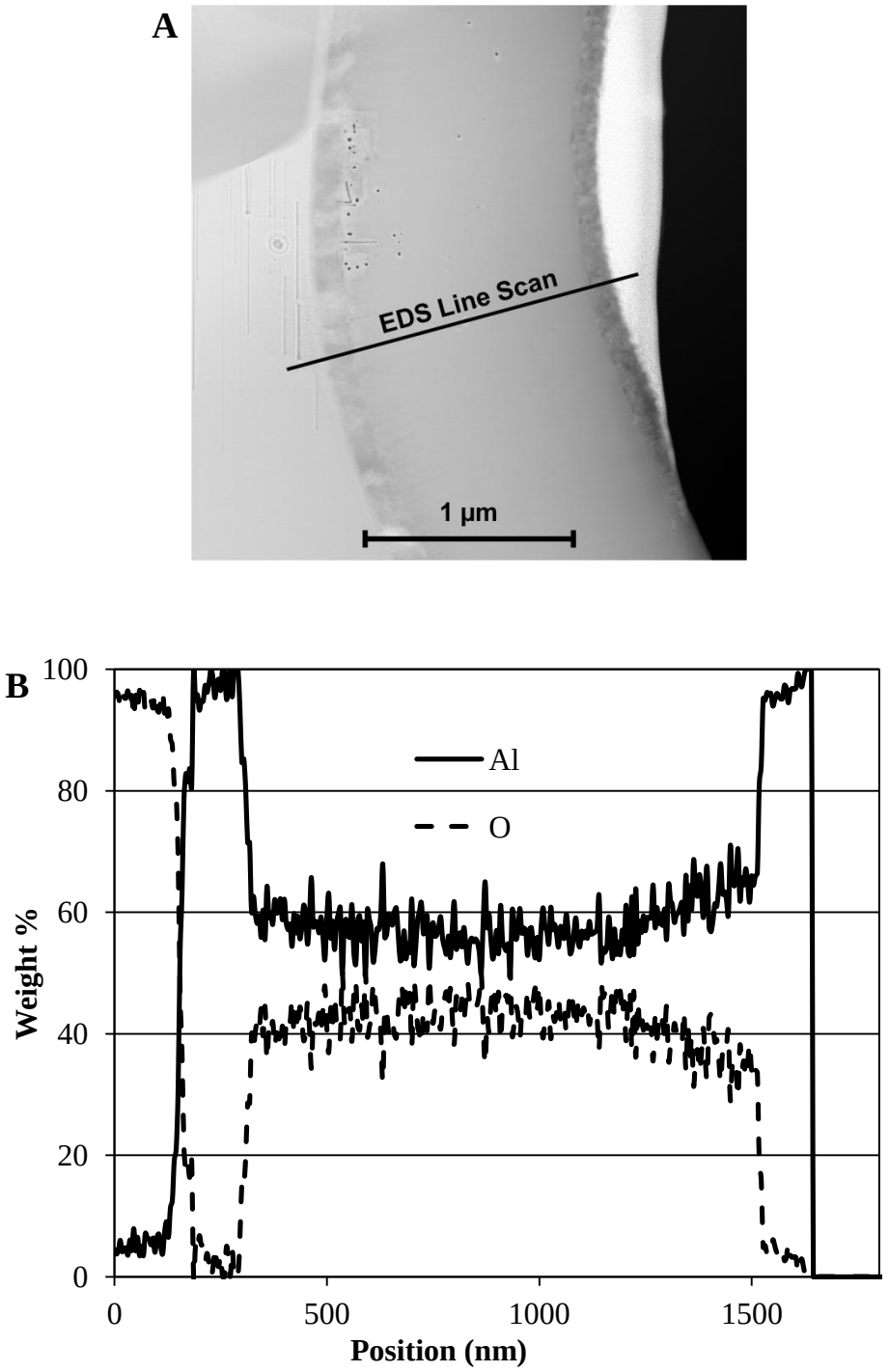

Figure 3.3. TEM image (a) illustrating the line scanned by EDS and the atomic map (b) of Al and O in the capacitor structure.

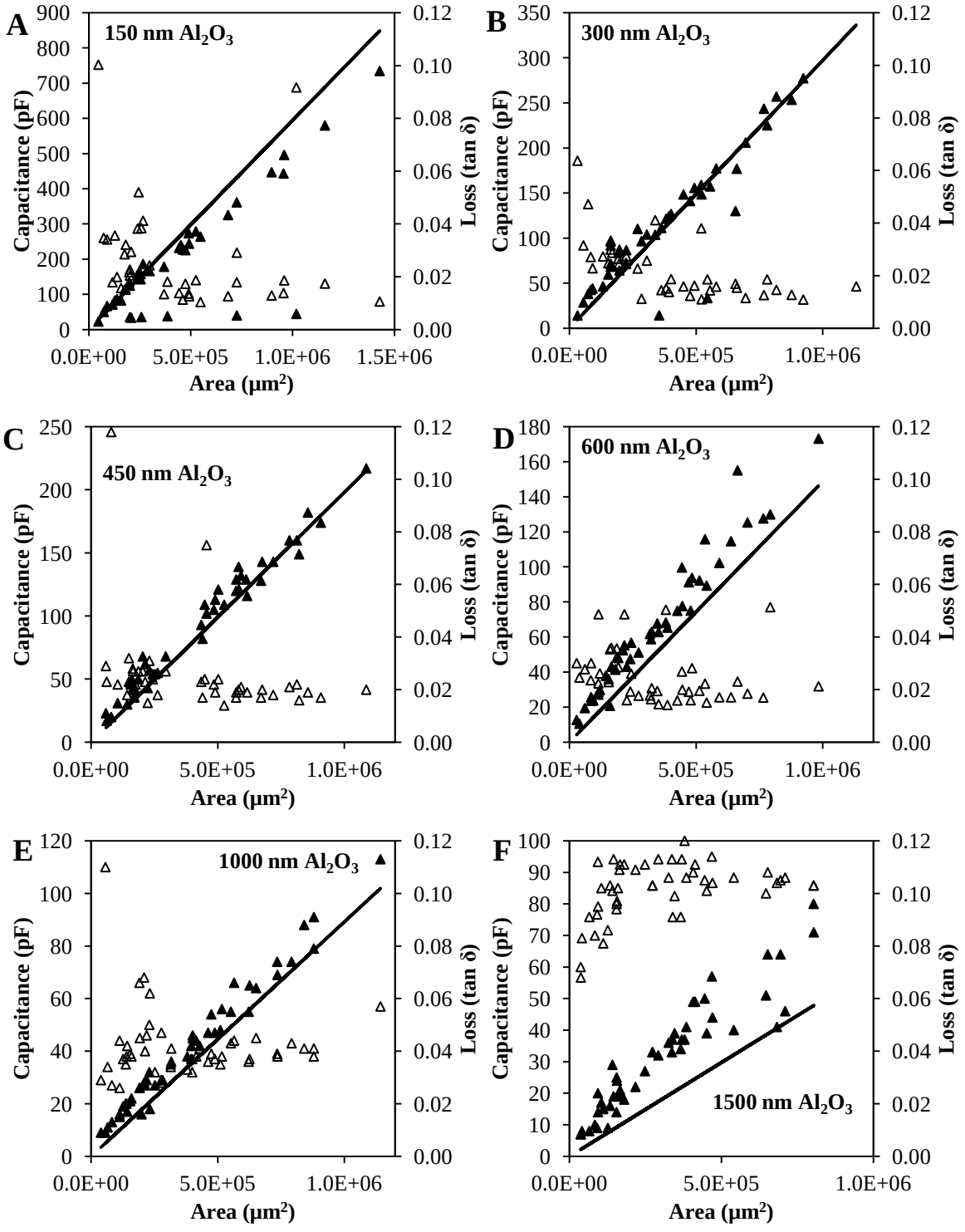

Figure 3.4. Capacitance and loss vs. area for Al-Al_2O_3-Al capacitors with Al_2O_3 dielectric thicknesses of (a) 150 nm, (b) 300 nm, (c) 450 nm, (d) 600 nm, (e) 1000 nm, and (f) 1500 nm. Closed triangles represent capacitance, open triangles represent loss and lines represent the calculated capacitance. Note the capacitance scale differences between each plot.

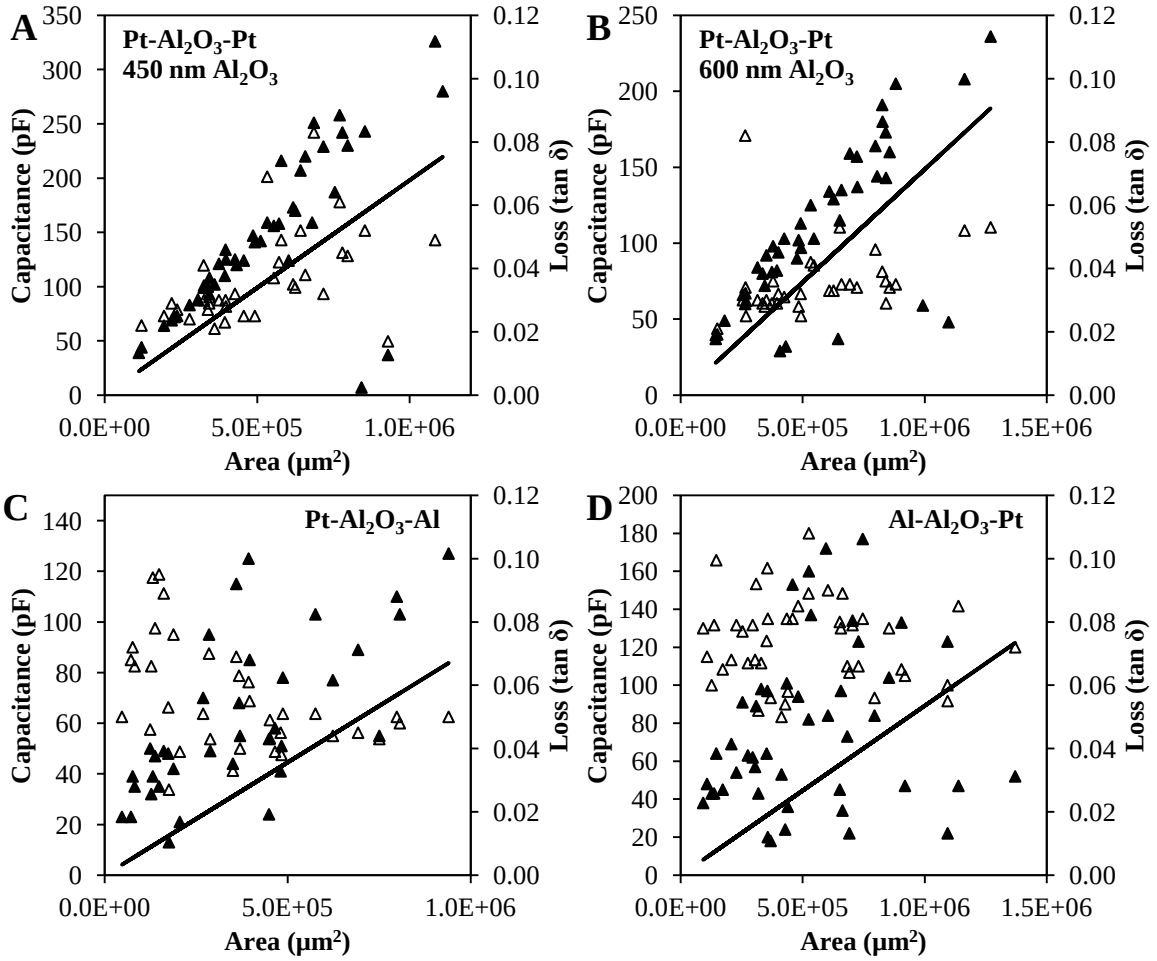

Figure 3.5. Capacitance and loss vs. area for Pt-Al_2O_3-Pt capacitors with Al_2O_3 dielectric thicknesses of (a) 450 nm and (b) 600 nm. Dissimilar metal electrodes were used with configurations of Pt-Al_2O_3-Al (c) and Al-Al_2O_3-Pt (d) and dielectric thicknesses of and 1000 nm. Closed triangles represent capacitance, open triangles represent loss and lines represent the calculated capacitance. Note the capacitance scale differences between each plot.

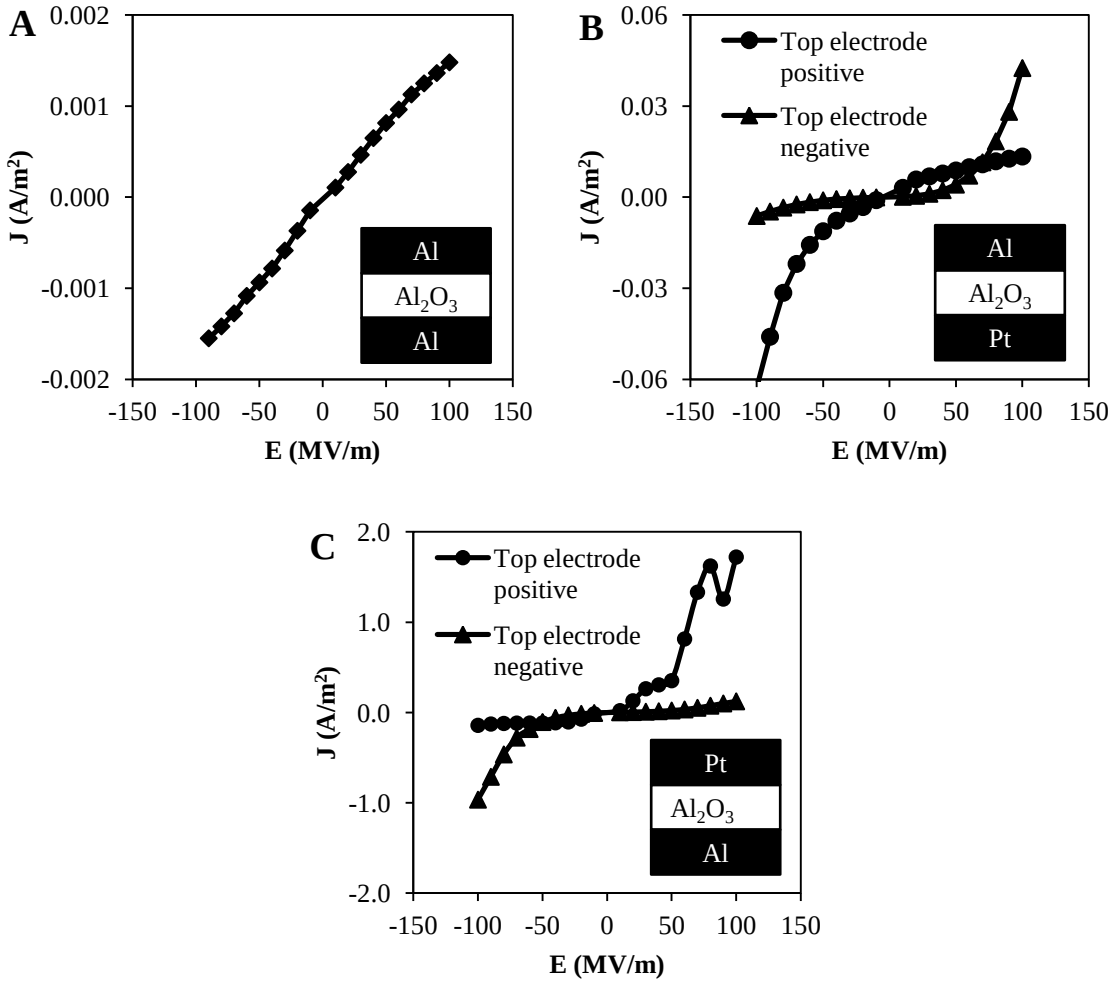

Figure 3.6. Electric field vs. current density for capacitors with 1 μm Al_2O_3 dielectric layer and (a) Al-Al_2O_3-Al layout, (b) Pt-Al_2O_3-Al layout and (c) Al-Al_2O_3-Pt layout.

2. CONCLUSION

Sputter deposition was used to fabricate thin film capacitor structures onto the surface of low temperature co-fired ceramic (LTCC) substrates. The capacitors featured a single dielectric layer and device areas between ~10^4 μm^2 to ~10^6 μm^2. Electrode layers (Al or Pt) were ~200 nm thick and Al_2O_3 dielectric thicknesses were between 150 and 1500 nm. Devices with Al electrodes featured capacitance values ranging from ~10 to ~700 pF, depending on the device geometry. The fit to expected capacitance values (calculated from geometric considerations) was greater for devices with Al electrodes than for devices with Pt as one or both of the electrodes. Dielectric loss was greater for the sputter deposited Al_2O_3 dielectric layers (tanδ~0.02) than for bulk Al_2O_3 (tanδ~0.001). The dielectric loss also increased with increasing Al_2O_3 layer thickness, most likely due to cracking in thick (>1 μm) sputtered films. Capacitor structures were examined by optical and transmission electron microscopy (TEM), along with energy dispersive spectroscopy (EDS) to characterize their microstructural characteristics. Electron beam induced crystallization of amorphous Al_2O_3 was observed during the collection of selected area diffraction (SAD) patterns on capacitors under TEM examination. From the electrical and microstructural results, sputter deposition is a useful method to deposit functional capacitors with Al electrodes and 300 – 1000 nm thick Al_2O_3 dielectric layers onto LTCC substrates.

VITA

Jack Edwin Murray was born on January 17, 1986 in Chesterfield, Missouri. After graduating from Fort Zumwalt North High School in O'Fallon, MO in 2004 he enrolled at the Missouri University of Science and Technology (then known as the University of Missouri-Rolla). He went on to earn his Bachelor of Science degree in December of 2009, majoring in ceramic engineering. In January of 2010 he began graduate school at Missouri S&T and earned his Master of Science degree in May of 2012, again majoring in ceramic engineering.