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Laminate dielectric and foil characterization for signal integrity on printed circuit board

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Department:

LAMINATE DIELECTRIC AND FOIL CHARACTERIZATION FOR SIGNAL INTEGRITY ON PRINTED CIRCUIT BOARD

by

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ABSTRACT

Accurate characterization of laminate dielectrics as substrates of printed circuit boards (PCB) over a wide frequency range (from tens megahertz to tens gigahertz) is important from a signal integrity (SI) point of view. Accurate knowledge of dielectric constants (DK) and dissipation factors (DF), or loss tangents, of laminate dielectrics, as well as loss in conductors, as functions of frequency over a wide frequency range, are needed to the designers of high-speed digital electronics.

An "in situ" wideband traveling-wave technique based on measuring S-parameters of the PCB test vehicles with auxiliary 'through-reflect-line" (TRL) calibration patterns has been developed. This technique has been extensively applied to the material characterization of PCBs up to 20 GHz. However, extension of the frequency range of testing PCBs up to 50 GHz requires solving numerous problems, related to a new PCB test vehicle design and improvement of the material parameter extraction algorithms to take into account various subtle effects arising as frequencies increase to 50 GHz. Extending the frequency range in the new 50-GHz test vehicles leads to potentially increasing uncertainties compared to the 20-GHz test vehicles. Different sources of errors and uncertainties for extracting DK and DF values are analyzed for both the present 20-GHz and the new perspective 50-GHz test vehicles. The limitations for the design of test vehicles are also discussed.

An alternative technique for measuring dielectric parameters of PCB laminate dielectrics is using split-post dielectric resonator (SPDR). This narrowband technique is applied to measurements of thin dielectric plates at frequencies 10 GHz, 15 GHz, and 20 GHz.

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TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS

Page

LIST OF TABLES

1. INTRODUCTION

An interest in the high-speed data rate transfer in printed circuit boards (PCBs) has raised the necessity to explore radio frequency and microwave parameters of the PCB materials – laminate dielectrics and conductors. The laminate dielectrics, used as substrates of striplines in multilayered PCBs, are characterized by the dielectric constant, DK, the real part of relative permittivity $\varepsilon_r' = \mathrm{Re}(\varepsilon_r)$ and dissipation factor DF, or loss tangent $\tan\delta = \varepsilon_r'' / \varepsilon_r' = \mathrm{Im}(\varepsilon_r) / \mathrm{Re}(\varepsilon_r)$.

The procedure to extract dielectric material parameters, as well as conductor loss in stripline structures inside PCBs, in this work is based on a traveling-wave method for TEM modes propagating along a stripline. This method includes measuring S-parameters of the specially designed test vehicles in the frequency domain using a vector network analyzer (VNA). These test vehicles have "through-reflect-line" (TRL) calibration patterns on them to eliminate port effects at the connectors of the lines. Currently, the test vehicles designed for operation over the frequency range from 50 MHz to 20 GHz have been used. However, data rates of high-speed digital designs using PCBs steadily increase with the progress in modern electronics, and hence there is a necessity for extending the frequency range of measuring material properties of PCBs. This requires not only improvement of the material parameter extraction algorithms, which would take into account various subtle effects arising as frequencies increase beyond twenty gigahertz, but also necessitates modifying a test vehicle design, or even developing substantially new designs of the test vehicles to satisfy requirements of operating at higher frequencies. The main goal of this work is to extend the frequency range of the PCB test vehicle operation up to 50 GHz.

Analysis of measurement errors and uncertainties both in the test vehicles design for measurements up to 20 GHz and in the new test vehicles operating up to 50 GHz is an important problem to be solved. Extending the frequency range to operate at frequencies up to 50 GHz, the new 50-GHz test vehicles should be designed. The extension of the frequency range may result in increased uncertainties compared to the 20-GHz test vehicles. To avoid problems, or at least minimize artifacts in the new design, the errors, uncertainties, and limitations are investigated and analyzed in Section I of this work. Section II is devoted to the new 50-GHz test vehicle design, including optimization of ground-via transitions at the connectors. There are several errors, described in Section I, which have been taken into account at the design of the new test vehicle.

PCB dielectric material parameters extracted using the traveling-wave method based on measuring S-parameters in the frequency domain on test vehicles with TRL calibration patterns sometimes need comparison with measurements done using other measurement techniques. In Section III, the method of dielectric characterization Split Post Dielectric Resonator (SPDR) is presented. The SPDR technique allows for only narrowband DK and DF measurements, and in this work SPDR results are obtained using a set of three different SPDRs - designed for 10GHz, 15 GHz, and 20 GHz. Measurements using travelling-wave technique on a stripline and SPDRs may results in different values of DK and DF for the same laminate dielectric. This is mostly related to anisotropy of PCB dielectric, since the electric field vectors in the SPDR and in the stripline have different orientations with respect to the glass fiber bundles in a resin matrix. Still, the comparison of the dielectric properties extracted using the SPDR approach and the traveling wave technique may be informative.

2. TRAVELING WAVE METHOD FOR PRINTED CIRCUIT BOARD CHARACTERIZATION

The systematic and random errors arising from the measurements using TRL-calibrated test vehicles over the frequency range below 20 GHz are comparatively low and almost do not affect the quality of designs using such PCBs. But as the upper frequency limit of measurements is increased from 20 GHz to 50 GHz, errors and uncertainties, associated with the measurement technique, may become significant. For obtaining adequate values of DK and DF (PCB) at higher frequencies (above 20 GHz), error assessment is needed.

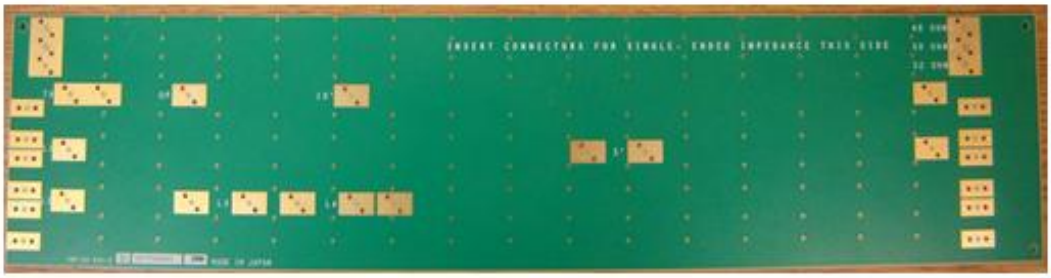
The objective of this section is the analysis of errors, uncertainties, and limitations associated with this method.

2.1. REVISIT OF MATERIAL PARAMETER EXTRACTION PROCEDURE USING A TRAVELING WAVE METHOD

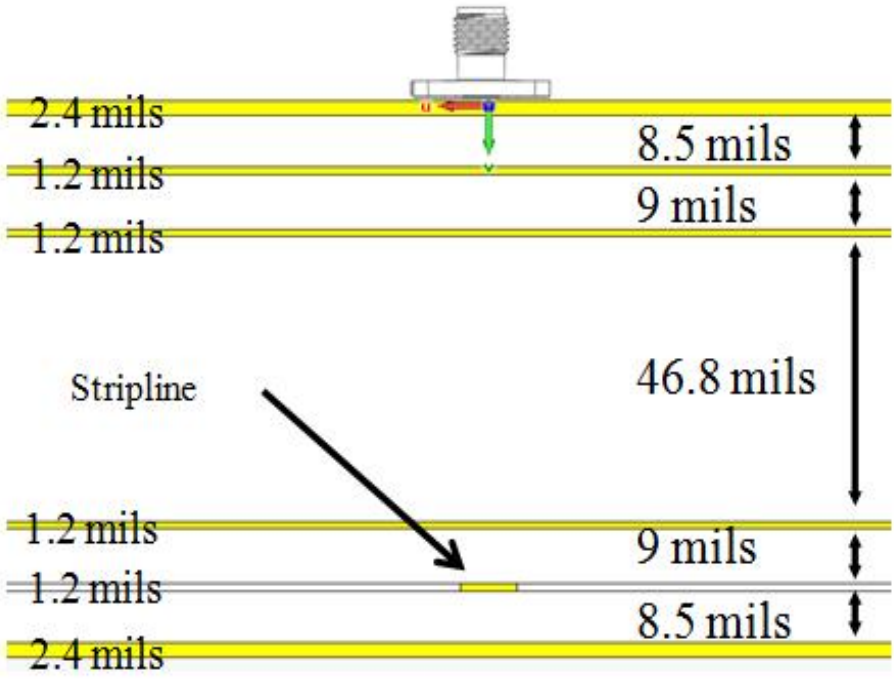
Dielectric material parameters (DK and DF) as functions of frequency over a wide frequency band are extracted herein using a technique based on a single-mode (TEM) propagation on low-loss transmission lines formed in PCBs. The scattering matrix parameters (S-parameters) of the specially designed test vehicles are measured in the frequency domain using a precision vector network analyzer (VNA). Currently, the frequency range of measurements is 50 MHz -20 GHz. Any test vehicle contains a comparatively long (16″) single-ended stripline on a 6-layer PCB, and also a number of single-ended auxiliary lines of different lengths for the “through-reflect-line” calibration,

which is called “a TRL calibration pattern” [4], [21]. The material parameter extraction procedure uses an algorithm, described in detail in [1]-[3].

The picture of the test vehicle and the test board stack-up are presented in Figure 2.1.



a)



b)

Figure 2.1 The picture of the test vehicle and stack-up
a) PCB outlook. b) PCB stack-up

The next steps after measuring S-parameters in the extraction procedure are converting them to ABCD transmission matrix parameters, and then calculating the complex propagation constant $\gamma = \alpha + j\beta$, where β is phase constant and α is total attenuation constant.

For any transmission line, the total attenuation constant consists of the sum of the conductor loss and dielectric loss, $\alpha = \alpha_T = \alpha_C + \alpha_D$. The problem of separation of conductor loss and dielectric loss is considered in papers [1], [3] and will be also reviewed below in Section 2.2

As soon as the dielectric loss, α_D, and the phase constant, β, are known, they can be used in DK and DF calculations.

The rigorous formulas for β and α_D may be applied.

$$\beta = \frac{\omega}{c}\sqrt[4]{\varepsilon_r^{'2} + \varepsilon_r^{''2}} \cdot \cos\left(\frac{\delta}{2}\right) \tag{2.1}$$

$$\alpha_D = \frac{\omega}{c}\sqrt[4]{\varepsilon_r^{'2} + \varepsilon_r^{''2}} \cdot \sin\left(\frac{\delta}{2}\right) \tag{2.2}$$

By solving the system of these two equations for $\varepsilon_r^{'}$ and $\varepsilon_r^{''}$, it is easy to obtain the dielectric constant $DK = \varepsilon_r^{'}$ and dissipation factor $DF = \tan\delta = \varepsilon_r^{''}/\varepsilon_r^{'}$ from

$$\varepsilon_r^{'} = x\sqrt{\frac{x}{x+y}} \tag{2.3}$$

$$\varepsilon_r^{''} = x\sqrt{\frac{y}{x+y}} \tag{2.4}$$

where $x = \frac{\beta^2 c^2}{\omega^2}$ and $y = \frac{4c^2\alpha_D^2}{\omega^2}$.

Formulas (2.1) - (2.4) are derived in Appendix A. The formulas (2.3) and (2.4) correlate $\varepsilon_r^{'}$ and $\varepsilon_r^{''}$ with the phase constant β and dielectric loss on the line α_D. However, β and α_D are not measured directly. They are obtained by calculations using the measured S-parameters. The expressions for $\varepsilon_r^{'}$ and $\varepsilon_r^{''}$, and $\tan\delta$ in terms of the measured unwrapped phase and magnitude of the S_{21} are

$$\varepsilon_r^{'} = \left(\frac{c}{2\pi}\right)^2 \left(\frac{[\varphi_{21}]_{unwrapped}}{l \cdot f}\right)^2 \tag{2.5}$$

$$\varepsilon_r^{'} = \frac{c}{\pi \cdot 8.686} \frac{\sqrt{\varepsilon_r^{'}}}{l \cdot f} \left(-|S_{21}{}^{dB}|_D\right) \tag{2.6}$$

$$\tan\delta = \frac{\left(-|S_{21}{}^{dB}|_D\right)}{4.343 \cdot [\varphi_{21}]_{unwrapped}} \tag{2.7}$$

where $[\varphi_{21}]_{unwrapped}$ is unwrapped phase of the measured S_{21} and $\left(-|S_{21}{}^{dB}|_D\right)$ is the magnitude of measured S_{21}, which corresponds to a dielectric part of loss α_D. Formulas (2.5) - (2.7) are derived in Appendix B

The advantage of the method specified in this work is that the calculations do not require solving complex electromagnetic problems with detailed analysis of scattering effects on conductor roughness. The extraction procedure is comparatively simple and could be applied for the experimental analysis of many different PCBs with fiber-glass-filled epoxy-resin-based substrates.

2.2. SOURCES OF TROUBLES AND ERROR ASSESMENT IN DK/DF EXTRACTION

The necessity of getting adequate ε_r' (DK) and $tan\delta$ (DF) on low-loss PCB over the frequency range up to 50 GHz is an important requirement for high-data-rate design. PCB material parameters in the current work have been extracted using the traveling wave technique, which was explained in Section 2.1. To estimate the systematic errors in measured DK and DF one can use the formulas presented in Appendix C. The derivation of these formulas is based on (2.5) - (2.7). TRL calibration is used to de-embed via and connector transitions. Most of the errors and uncertainties will be more significant after increasing the frequency range of measurements from 20 GHz to 50 GHz.

In Figure 2.2 sources of trouble are systematized.

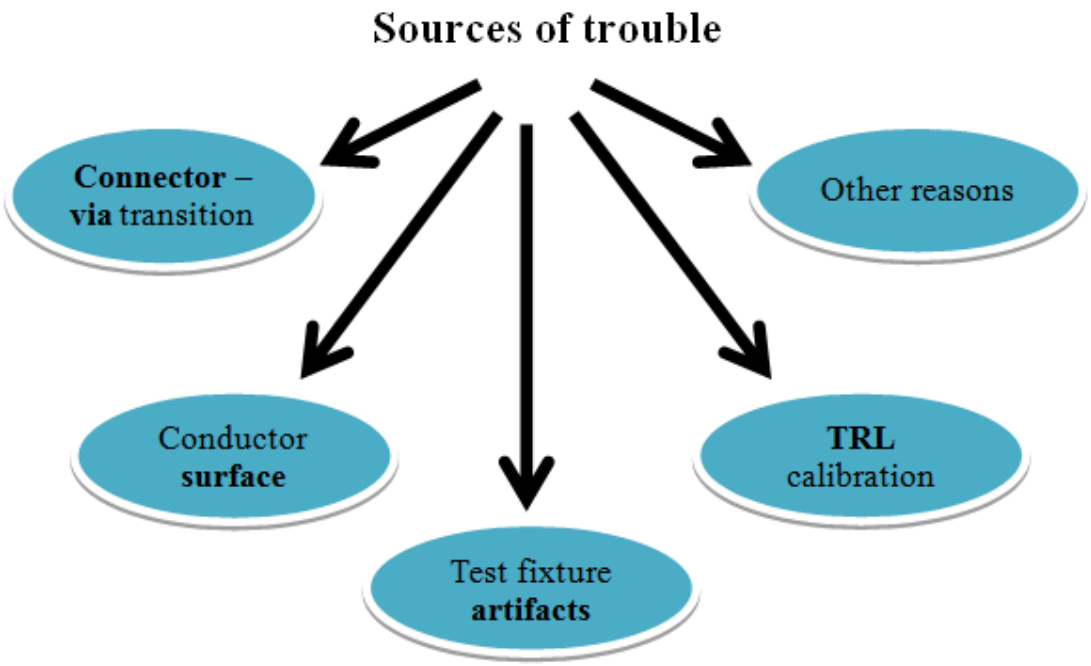


Figure 2.2 Sources of errors and uncertainties

2.2.1. Non-Ideal Effects Due To Via-Connector-Trace Transitions. Before the signal propagates through the PCB trace, it passes through the via-connector-trace structure, which may affect the measured S-parameters on the line, and eventually contribute to the errors in the extracted DK and DF of a dielectric under test. Even if the TRL calibration is applied, an improper via transition design may affect signal loss and mismatch and cause errors and unwanted limitations. Thus, via transition structure may limit frequency range of measurements, and may even cause the TRL calibration failure.

In the current measurement setup, 3.5-mm surface mounted SMA connectors have been used. The upper limit for the 3.5-mm SMA connector is 26.5 GHz. This is sufficient for the current measurement setup up to 20 GHz, but these connectors cannot be applied for the measurements up to 50 GHz. That means that the type and characteristics of a connector are the factors determining the frequency limitation. For a measurement setup with frequency range up to 50 GHz, 2.4-mm SMA connectors with frequency limit at 50 GHz should be chosen.

Even if the connectors applied to a PCB have proper characteristics over the entire frequency range, they still can be a source of uncertainty. An important assumption for the TRL calibration is that all the ports are of the identical geometry, which means the identity in the impedance of all the connectors. Non-uniformity of mounting connectors to a PCB and manufacturing tolerances can result in non-repeatability of time-domain response from the connectors. Figure 2.3 demonstrates an acceptable mounting of all the connectors, since impedance responses from all the connectors are quite similar. The deviation in impedance of these connectors is within 0.5 Ohm – 1 Ohm in the time span from 15.4 ns to 15.61 ns. In the case of unacceptable mounting, the impedance deviation

of all connectors will be higher than a few Ohms. Example of unacceptable mounting is plotted on Figure 2.4.

Non-uniformity of mounting can be caused by a mismatch between a via pad and the connector inner pin. For an ideal transition connector, a pin and a via pad should have the same sizes and need to be perfectly aligned. Unfortunately, in practice, it is difficult to satisfy those conditions for surface-mounted connectors. Misalignment and size mismatch reduce the area of contact. One of the other possible troubles is an air gap between a connector pin and a via pad. This could be a result of using a broken connector, which has its inner pin pushed inside, or this may be a via pad manufacturing error.

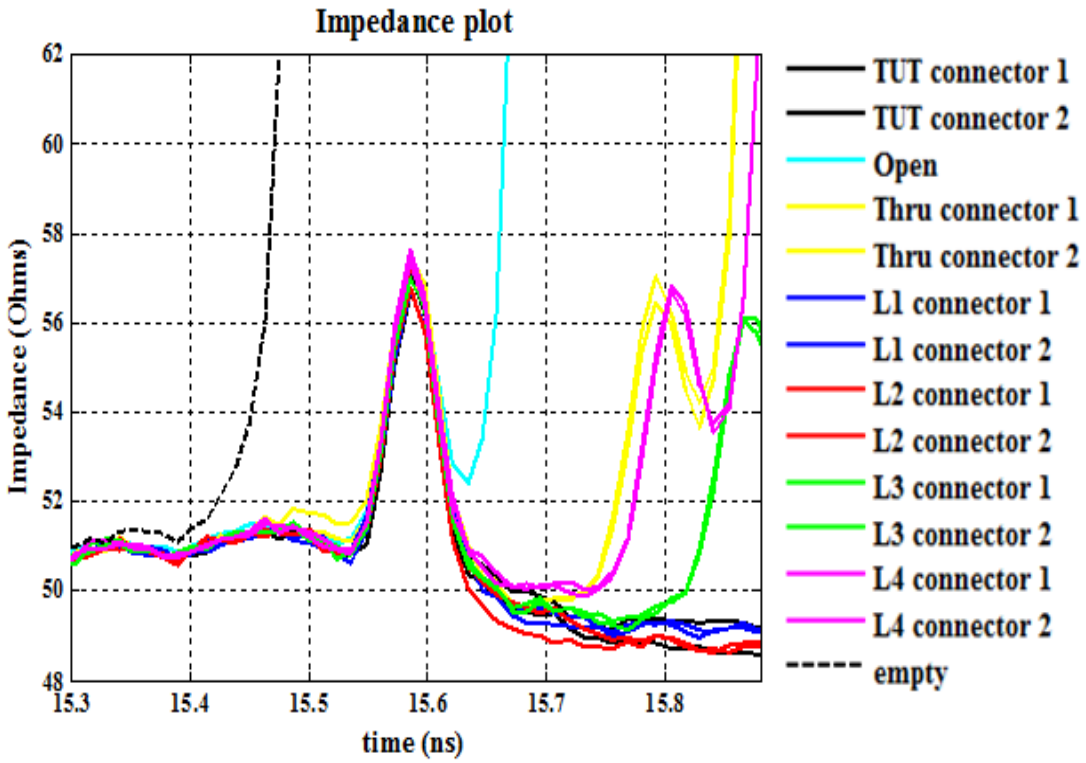


Figure 2.3 Acceptable connector mounting to PCB

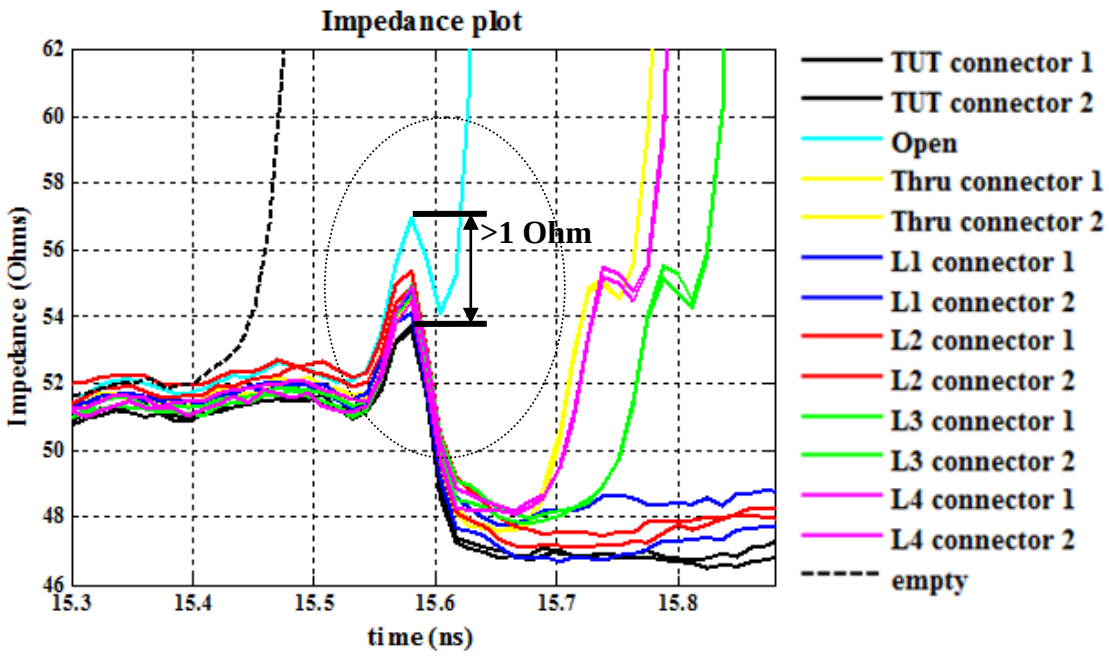


Figure 2.4 Non-acceptable connector mounting to PCB

Even if the signal successfully passes the transition between the connector pin and the via pad, there is still a possibility of having an unwanted resonance in the insertion loss in the high-frequency part of the frequency range of operation. This resonance could be caused by a via stub.

To demonstrate the resonant effect of the via stub, the simulated insertion loss curves for the 80.5 mil via with 10.9 mil stub and without any stub are presented in Figure 2.5. The difference between two curves around 45 GHz is significant.

It is a common practice to reduce the via stub length by back-drilling the stub as close as possible to the signal layer. In Figure 2.6-2.8, the comparison of the measured zero-length 'through' line for the same PCB, but in different scenarios, is presented (with a via stub vs. without via stub).

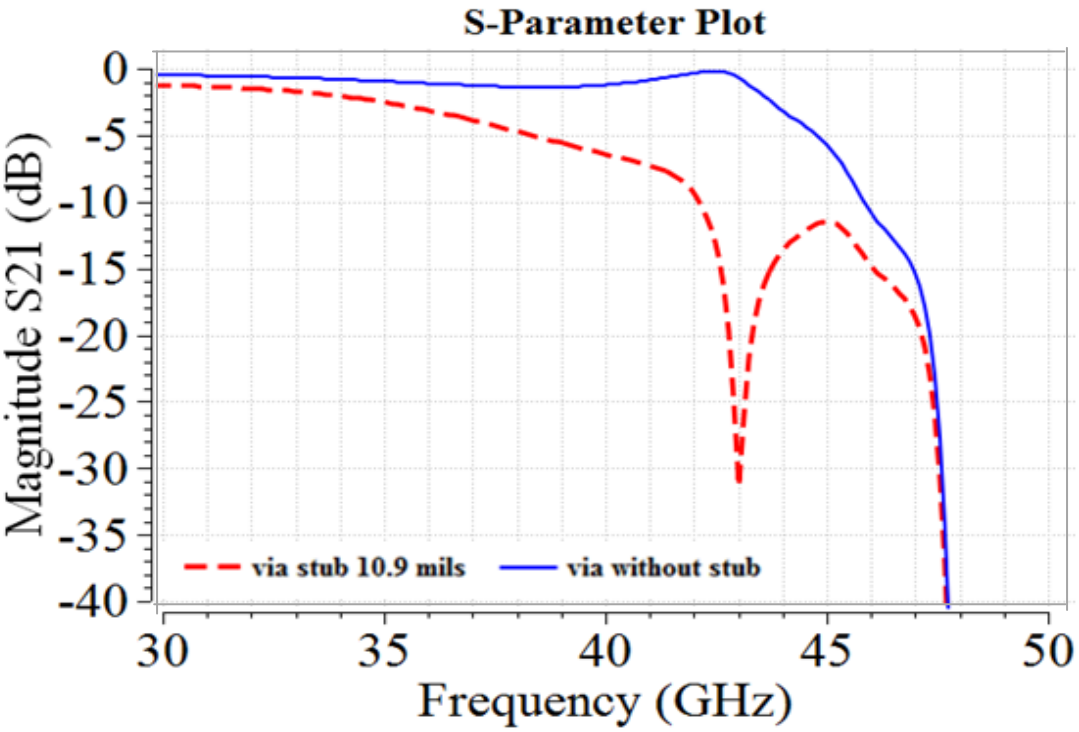


Figure 2.5 Modeling of the via with a stub and without any stub (MVTT tool)

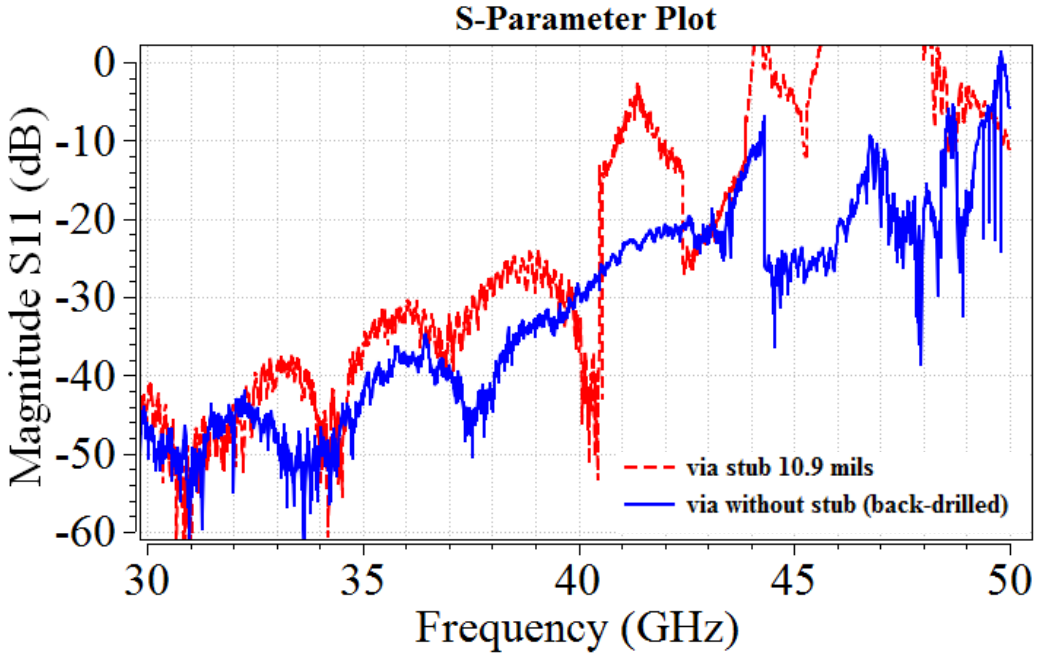


Figure 2.6 Comparison of the return loss for the PCB with 10.9mils via stub and PCB with back-drilled via (the same material and geometry of the test vehicles)

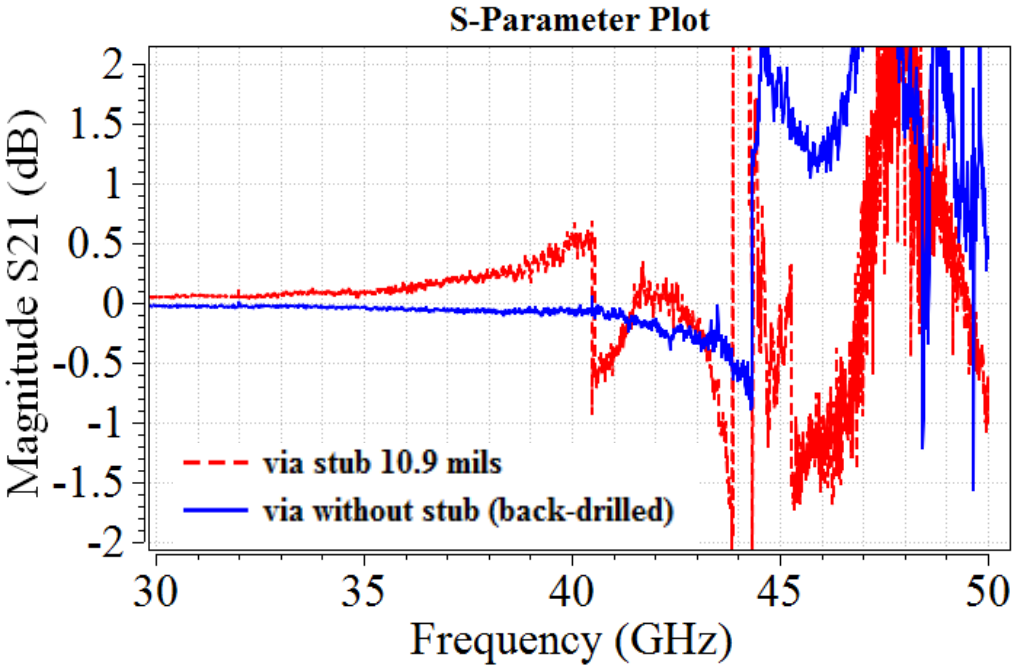


Figure 2.7 Comparison of the insertion loss for the PCB with 10.9mils via stub and PCB with back-drilled via (the same material and geometry of the test vehicles)

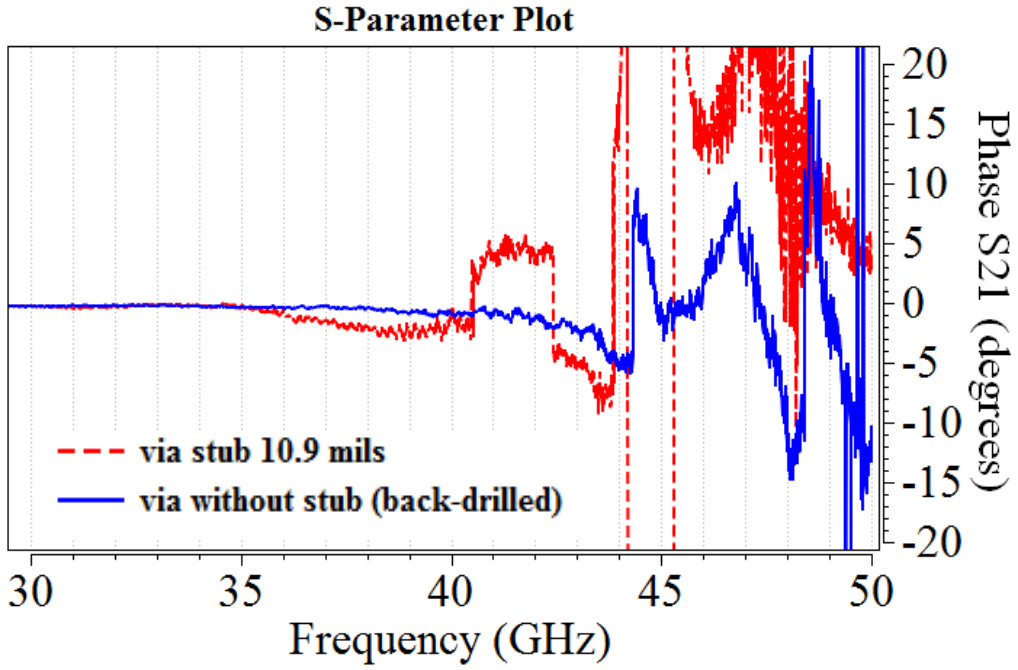


Figure 2.8 Comparison of the phase of the insertion loss for the PCB with 10.9mils via stub and PCB with back-drilled via (the same material and geometry of the test vehicles)

After applying the back-drilling technique, the return loss has improved at frequency above 40 GHz. Insertion loss and phase of insertion loss has been stabilized up to 40 GHz, and slightly improved above 40 GHz. Measurements have been made with the same setup settings. That allows to see improvement in results, after reducing the length of the via stub, what has been proven by above shown plots.

2.2.2. Non-Ideal Effects Due To TRL Calibration Pattern Design. Some of the uncertainties and effects related to imperfect via transitions mentioned above can be avoided applying 'through-reflect-line' (TRL) calibration, unless the via transition defects lead to the failure of the TRL calibration. The TRL calibration is the most effective method to remove the port effects from the measurements. However, the TRL calibration patterns have to be design properly according to certain rules.

All the test vehicles in this study have the same TRL calibration pattern, comprised of a number of auxiliary single-ended lines of different lengths on the same PCB under test. For the current test vehicle design, the TRL pattern contains a "through line" (TL), an "open line" (OL), and four lines with different lengths specified for different frequency ranges. The existing TRL patterns have been initially designed for the operation up to 50 GHz, but assuming that the laminate PCB dielectric has the DK value equal to 4.0, and this DK value is constant over the entire frequency range. However, it is well known from the experience, that the DK value of the laminate dielectrics is a frequency-dependent parameter, and the DK typically decreases as frequency increases. For different values of DK, the calculated lengths of the TRL calibration lines will be different. Table 2.1 represents the results of the TRL patterns calculations for different DK values (3.5, 4.0, and 4.5).

Table 2.1 Line length calculations for different DK values

TRL Line	Frequency range, GHz	ε' = 3.5	ε' = 4.0	ε' = 4.5
		Length of the line, mil	Length of the line, mil	Length of the line, mil
Line 1	0.0500	10122	9506.1	8996.2
	0.2812			
Line 2	0.2812	2285	2175.5	2084.9
	1.5811			
Line 3	1.5811	891.42	871.95	855.82
	8.8914			
Line 4	8.8914	643.60	640.14	637.27
	50			

The other assumption for the TRL calibration pattern design is that the impedance for all lines is the same. However, the manufacturing process does not always guarantee the same impedance over all the traces or even the translational invariance of impedance along any trace. This means the impedance difference on different lines may result in some uncertainty of measurements. The impedance of the traces as a function of time is tested using the Time Domain Reflectometer (TDR) equipment. These tests allow an operator for understanding whether there is an impedance-difference, and the impact it has on the measurements. According to the measured data, represented in Figure 2.9, the trace impedances vary within several Ohms for the lines of the TRL calibration patterns.

The identical signal propagation through connectors and traces is the most significant criterion for designing the appropriate TRL calibration patterns. The violation of this criterion would decrease the quality of the TRL calibration and lead to errors and uncertainties. Further experimental investigation is needed to estimate numerically the degradation of the calibration.

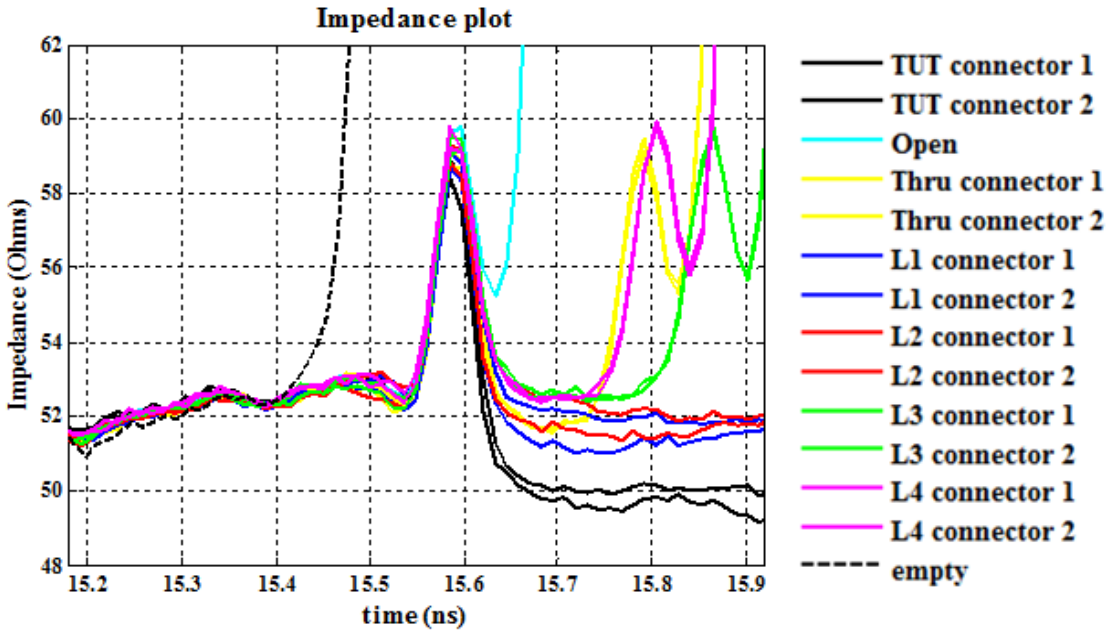


Figure 2.9 Impedance measurements using TDR

2.2.3. Effects Due to Conductor Surface Roughness. Errors and uncertainties could occur due to not taking into account surface roughness of the conductor in the extraction algorithm. The conductor surface roughness starts to significantly affect the extracted DF values (and less for the DK values) at frequencies above approximately 5 GHz.

However, to correctly separate conductor loss α_C and the pure dielectric loss α_D from the total measured loss α_T has always been a challenge. Currently, in the material parameter extraction method adopted in this work, there are two ways of separation of the conductor and dielectric loss.

The first is the so-called **"root-omega"** approach [2]. In this case, conductor surface roughness is not taken into account. The total loss is curve-fitted by the three terms proportional to the powers of the angular frequency, $\sqrt{\omega}$, ω, and ω^2, as $a\sqrt{\omega}+$

$b\omega + c\omega^2$. The conductor loss is assumed to be proportional to the $\sqrt{\omega}$ term, as in the absolutely smooth conductor, and the dielectric loss behaves as the sum of the rest ω, and ω^2 components. Though this approach has shown that it is not very accurate for significantly rough conductors, especially at frequencies above ~5 GHz, it can be applied in the case, when the conductor surface roughness is unknown and cannot be easily determined, and if the transmission line geometry is not known. This algorithm has been employed in the Matlab code to extract DK and DF parameters of the test vehicles, when the cross-sectional geometry of the test lines is not available, and the destructive cross-sectional analysis of the test boards is not possible.

If the test line cross-sectional parameters, such as the signal trace average width and thickness, the distances between the trace and the ground planes, the average peak-to-valley roughness amplitude, and the spatial quasi-period of the surface roughness function, are known, then a small perturbation model based on Sanderson's theory of roughness as a periodic or random function can be applied [22]. In the current version of the Matlab code, which is developed for the DK and DF extraction, the Sanderson's small perturbation technique has been realized for the one-dimensional sawtooth roughness functions [1].

An overview of both methods in the procedure for extracting dielectric parameters from measured S-parameters using VNA is presented in the flowchart published in [3], and this flow-chart is also presented in Figure 2.10.

However, any analytical or numerical model of surface roughness is an approximation to some extent, because it is extremely difficult, if not impossible, to characterize surface roughness, which has the statistical nature, by any deterministic

parameters, which could be included in a model. For this reason, experiment-based techniques to separate conductor and dielectric loss may be reasonable alternatives to analytical and numerical techniques [3].

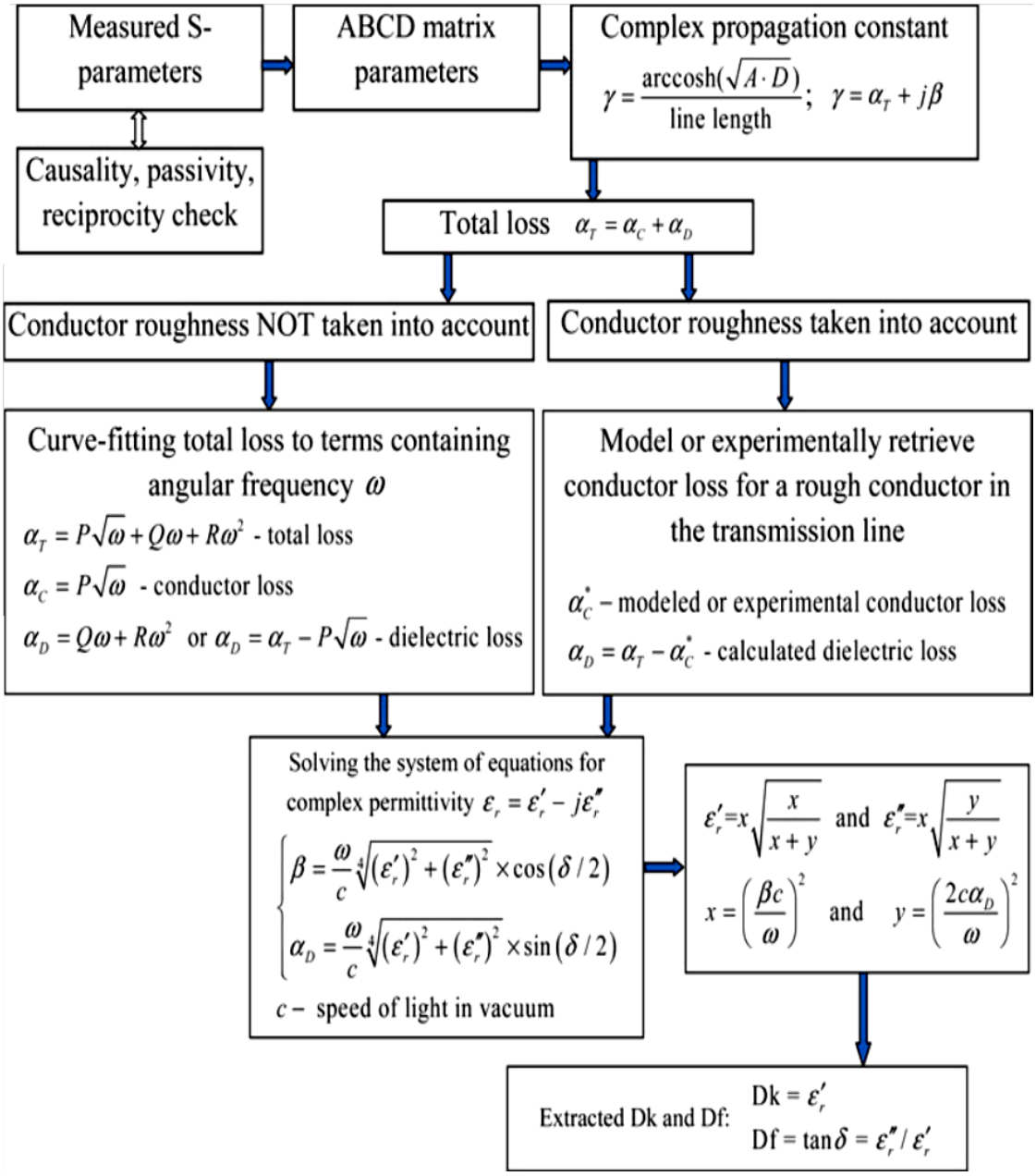


Figure 2.10 Flowchart of the procedure for extracting dielectric parameters from S-parameters [3]

As is mentioned above, in the "root-omega" procedure, the conductor loss is associated with $\sqrt{\omega}$ behavior, while dielectric loss is retrieved from the ω and ω^2 terms in the total curve-fitted loss. But in reality, conductor loss always deviates to some extent from the pure $\sqrt{\omega}$ behavior, since conductor roughness lumps into ω and ω^2, as is shown in [3]. If the conductor roughness profile is known, *e.g.*, retrieved from mechanical or laser profilometry, optical microscopy, scanning electron microscopy, or even more advanced atomic-force microscopy, then the conductor loss could be modeled using an adequate numerical or analytical method. Alternatively, a new experimental technique "DERM", proposed by Dr. M. Koledintseva and published in [3], can be applied, if at least three test vehicles with identical geometries and identical dielectric, but different conductor roughness profiles are available. It is also possible to separate conductor loss and dielectric loss, if at least three test vehicles with the same conductor roughness and the same dielectric, but different trace widths, are available ("DERM-W" technique) [23]. Then the dielectric loss would be simply calculated by subtraction of the conductor loss from the total loss [2].

Currently there are three main groups of foils used in industry. The difference between those groups is in the level of the foil roughness. The convenient parameter to characterize surface roughness is average peak-to-valley R_z. It is defined as

$$R_z = \frac{\sum_{i=1}^{5} | Y_i^{peak} | + \sum_{i=1}^{5} | Y_i^{valley} |}{5} \tag{2.8}$$

where Y_i^{peak} are the amplitudes of the five highest peaks, and Y_i^{valley} are the amplitudes of the five deepest valleys of the roughness profile [3], [9].

The first group is the standard (STD) foil, which has the highest roughness. The typical level of its R_z is on the order of ~10 μm and may be even exceeding10 μm. The second group has medium roughness with $R_z \sim 5 - 10$ μm and includes foils with very low profile (VLP) and reverse treated foil (RTF). The third group includes the smoothest hyper very low profile (HVLP) foils with R_z up to 5μm.

There are several different methods to retrieve the information about conductor surface roughness. In current work, surface roughness data has been extracted from the scanning electron microscopy (SEM) images of trace cross section. The algorithm of preparing samples for SEM cross-sectional analysis is described in Appendix D. Figure 2.11 presents the cross-sectional images of three foil classes obtained using the Hitachi 4700 SEM machine, available at the Missouri S&T Materials Research Center.

The algorithm which has been used to extract surface roughness data from SEM images in the current work is implemented in a semi-automatic tool. Stripline geometry and surface roughness information could be retrieved from an SEM image using this tool. Detailed description of the tool is published in [9].

To understand the importance of including surface roughness loss in calculating total loss, a set of test vehicles with identical dielectric of the same resin content and fiber-glass structure, and the same single-ended stripline geometry were measured. The conductors on all PCB were made of electrodeposited copper. These test vehicles differ only by the type of copper foil roughness: STD, VLP, and HVLP. Difference in measured data would be only due to the difference in roughness.

The difference in the insertion loss (S_{21}) leads to the difference in the corresponding extracted dielectric constant (DK) and dissipation factor (DF) values, if

applying the "root-omega" extraction procedure, which does not take into account surface roughness. This is described in [10] and can be seen in Figure 2.12. The difference in the slopes of the insertion loss curves in Figure 2.12 is solely due to the surface roughness, since these three test vehicles have the same geometry and the same dielectric.

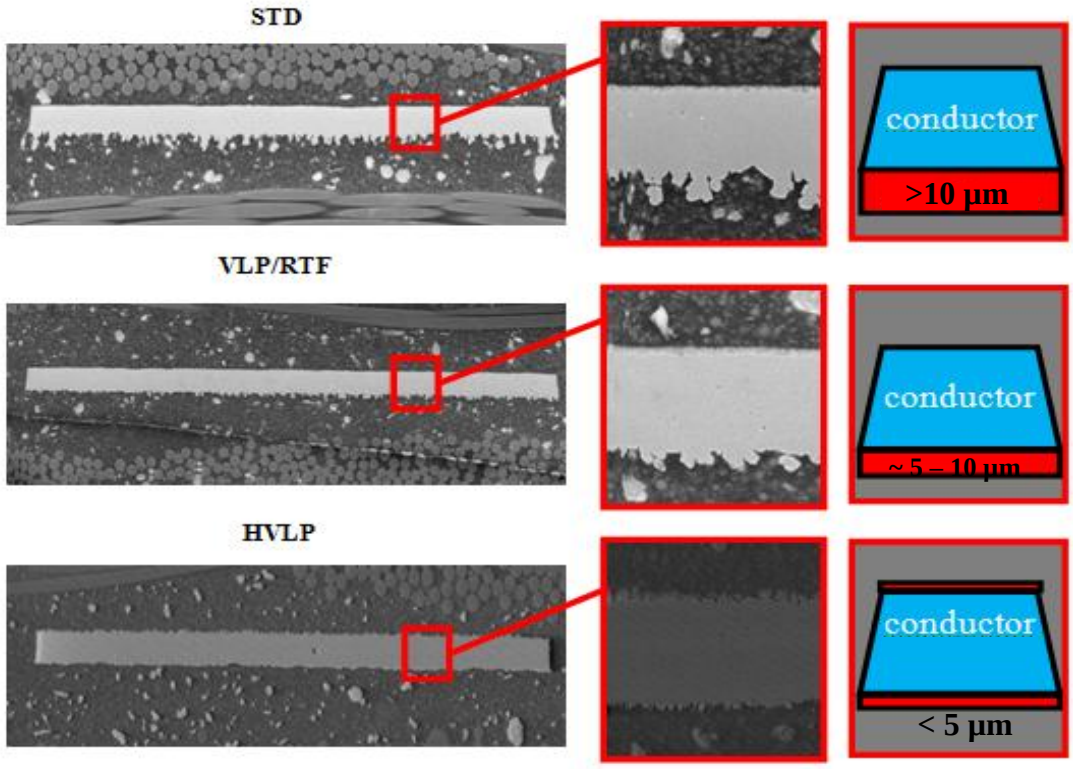


Figure 2.11 Cross-sectional SEM images of three types of foil used in current work

If surface roughness is not taken into account and the "root-omega" algorithm is applied, the DK and DF values for exactly the same dielectric turn out to be different, as is seen from Figure 2.13. This ambiguity is the consequence of the fact that the surface roughness is not "extracted out" of the DK and DF values properly. The "root-omega"

procedure does not separate dielectric loss from conductor surface roughness loss. The latter is lumped in the DK and DF values.

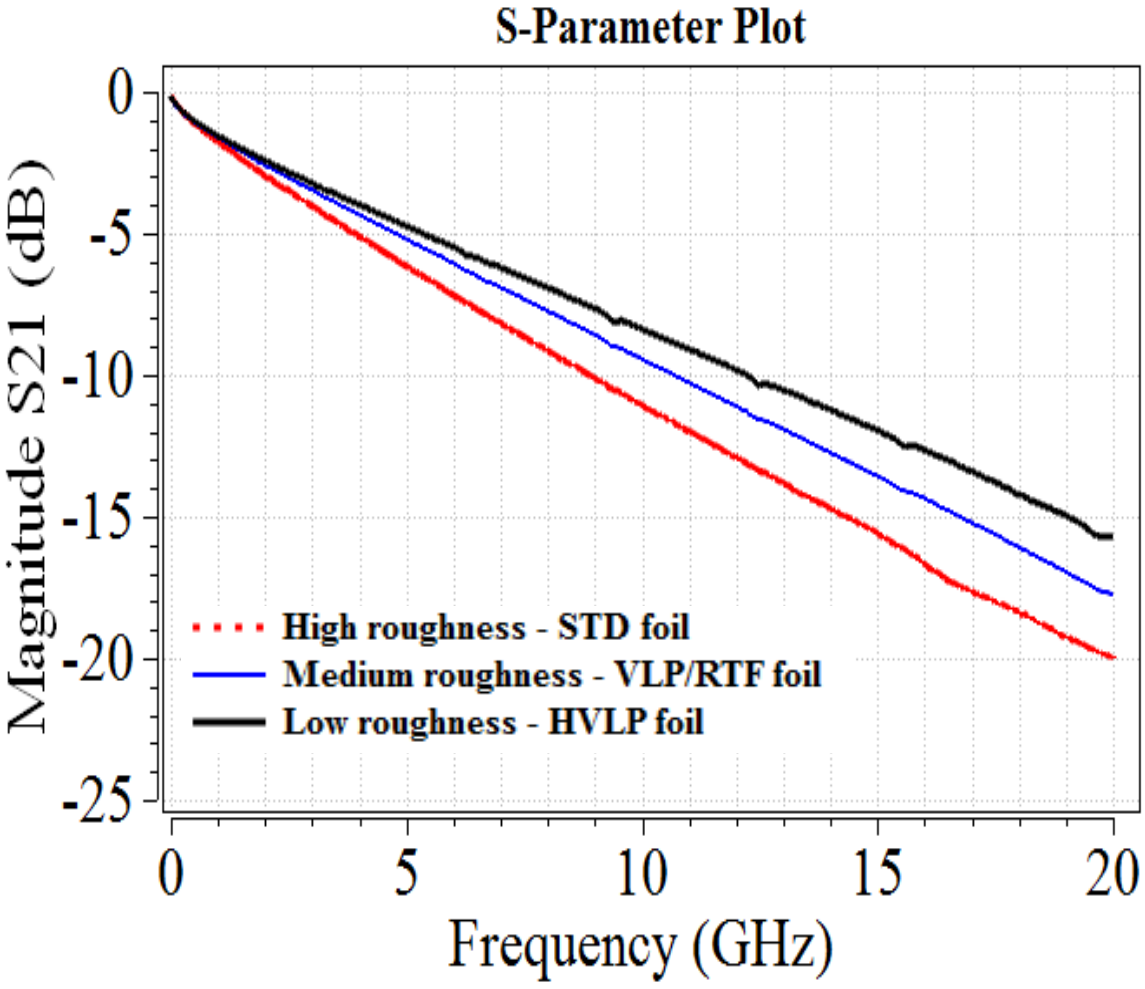


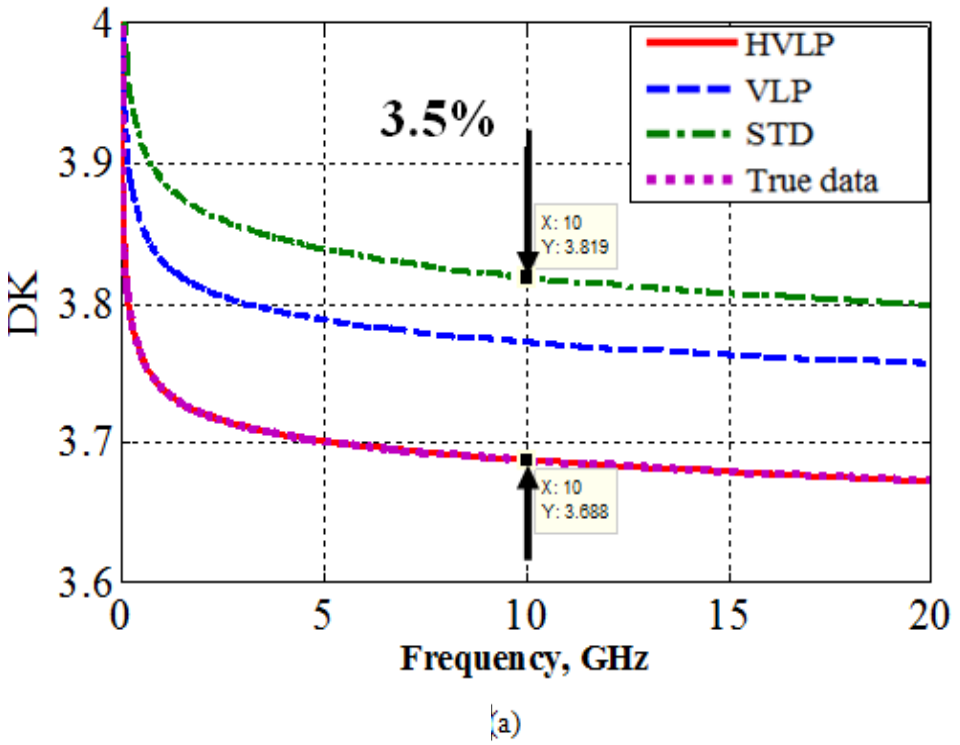
Figure 2.12 Insertion loss (S21) comparison between different types of foil

When the differential extrapolation method “DERM” [3] was applied to separate dielectric and rough conductor losses in printed circuit boards, this method allowed for extracting the pure dielectric losses, the same for all the test vehicles, independently of

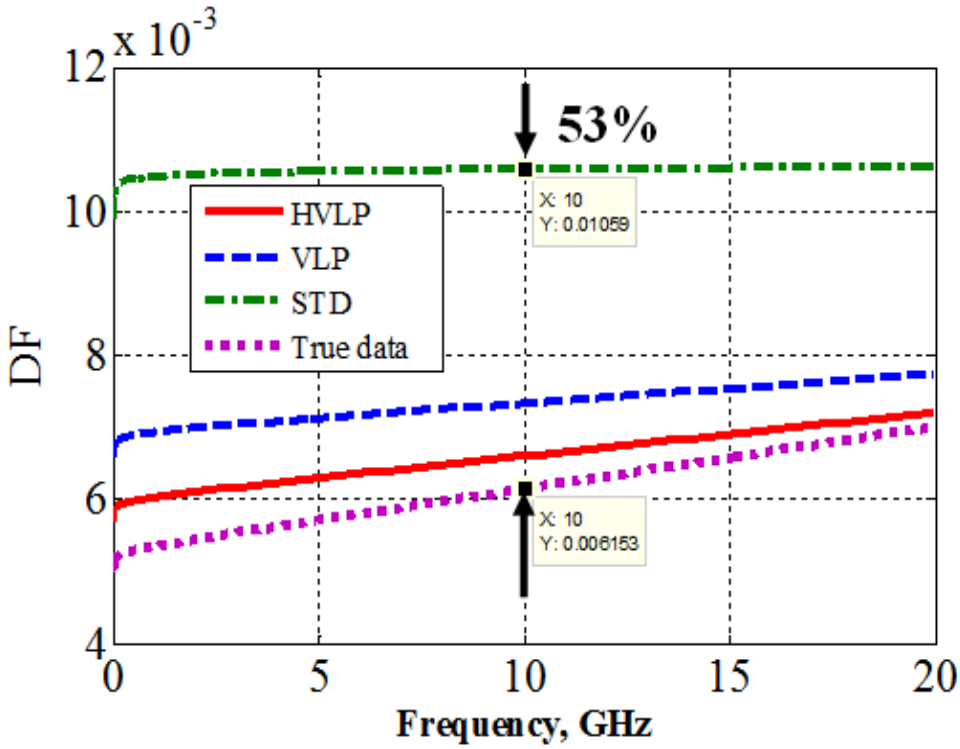
the conductor roughness. The resultant value with “zero roughness” could be used as a reference in comparison with rough STD, VLP, and HVLP foils. The extracted DK and DF of the pure, “free from the roughness”, PCB laminate dielectric (in this case it was Megtron 6) are presented in Figure 2.13 as a purple dashed line. The DK value matches the one for the test vehicle with the HVLP foil, which has the lowest surface roughness, and thus was taken as the true dielectric constant value for the further DF extraction. The true dielectric data extracted using the DERM technique is lower than the DK and DF values extracted using the “root-omega” procedure, because in the DERM technique the surface roughness is removed.

2.2.4. Non-Ideal Effects Due To Test Fixture Artifacts. A transmission line with losses has a transmission coefficient, the magnitude of which decreases monotonically with frequency, or the magnitude of the insertion loss (in dB below zero) should be a monotonous function of frequency. However, the insertion loss (|S21|, dB) curves, measured on the majority of the PCB test vehicles designed for this project, are not monotonous: some periodic resonances can be seen. The same periodic “peaks” can be seen on the return loss (|S11|, dB) curves. These artifacts are shown in Figure 2.14. The measurements are done using Agilent E8364B 50-GHz Precision Network Analyzer (PNA).

It has been noticed that these artifacts have the resonance shape, and they repeat approximately every 3.1 GHz. Any discontinuities close to the transmission line could cause reflection of the wave traveling along the line. In fact, in the current PCB design there are equidistant ground vias located along the transmission line with one-inch spacing. Pairs of ground vias form ½ wavelength resonator for the TEM mode.



(a)



(b)

Figure 2.13 Dielectric parameters extracted using different methods to compare rough foils with perfectly smooth conductor
a) DK. b) DF

The fundamental mode frequency of such resonator, assuming that the dielectric constant of the test board dielectric is around 4.0, can be estimated as

$$f_0 = \frac{c}{2L\sqrt{\varepsilon_r}} = \frac{3 \cdot 10^8 \frac{m}{s}}{2 \cdot 0.0254m \cdot \sqrt{4}} \approx 3.1\ GHz \quad (2.9)$$

where L is the length of the spacing between ground vias, and c is a speed of light in the free space.

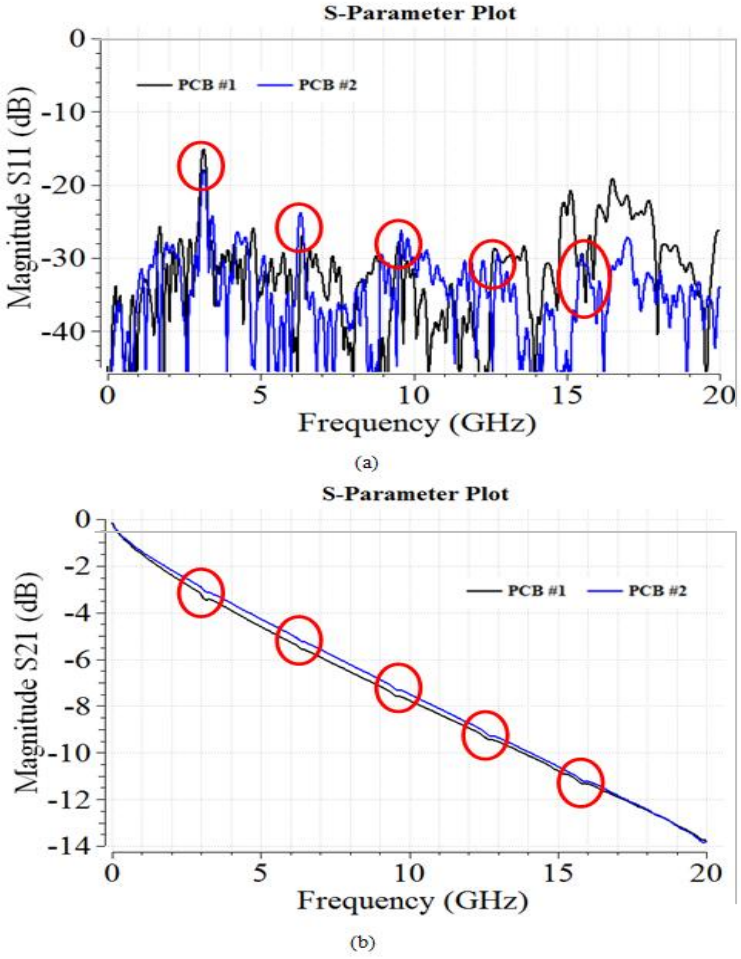


Figure 2.14 S-parameters measured over 16 inch transmission line. Artifacts are highlighted by red circles. a)Return loss. b) Insertion loss

The resonance frequency, calculated in equation (2.7), is very close to a frequency of artifacts in the measurements. An interesting observation is that the magnitude of these resonances increases as surface roughness increases, thus, for the test vehicles with STD foil these artifacts are more pronounced than for the test vehicles with VLP and HVLP foils. This effect suggests that the surface roughness "helps" to dissipate (absorb) energy stored in these "resonators" formed by the stripline and corresponding periodic via wall.

2.3. OVERVIEW OF ERRORS AND UNCERTIANTIES ASSOCIATED WITH TRAVELING WAVE METHOD, AND POSSIBLE SOLUTIONS

Analysis of errors, limitations, and uncertainties is important for making accurate measurements, as well as for improving a test vehicle design. Sources of troubles, which have an effect on current measurements up to 20 GHz, definitely will have an impact on the results of measurements as frequencies increase, and will be even more important when designing a new test vehicle for measurements up to 50 GHz. The main goal of the current work is to design such a test vehicle to be able to conduct measurements up to 50 GHz using a VNA. To achieve this goal, the factors, described above, need to be taken into account in a new design.

Table 2.2 summarizes the most significant problems and possible solutions, applicable both to the 20-GHz and 50-GHz test vehicles. Most of the solutions have been taken into account in the new PCB test vehicle design, and they will be detailed in Section III.

Table 2.2 Challenges and possible solutions

Challenge	**Possible solution(s)**
Unwanted resonances in S-parameters due to via stub	Eliminate stubs in a new test vehicle design
Surface roughness artifacts in Df	Use smooth foils and/or separate conductor roughness loss from dielectric loss
Unwanted periodic resonance in S-parameters due to via wall	Eliminate via wall in a new test vehicle
Sensitivity of TRL calibration patterns to small errors in mounting and manufacturing	Study of errors by numerical/analytical simulations
Phase offset at very low frequencies and phase instability	Determine errors
Mismatch effect	Determine maximum acceptable RL and associated errors
Insufficient line length	Determine minimum line length and errors associated IL and phase of S_{21}

3. DESIGN OF A TEST VEHICLE UP TO 50 GHZ

An increase of the bandwidth of the PCB test fixtures to get more wideband PCB laminate dielectric characterization is one of the biggest practical challenges. In the past few years, the data rate of high-speed electronics using PCBs has reached 25 Gb/s and that number is steadily increasing. This increase necessitates the study of PCB dielectric parameters at frequencies no less than 50 GHz.

The present-day PCB test vehicle design, with a frequency range limited to 20 GHz, needs to be improved. And the frequency range should be extended to 50 GHz. Those features of the design which should be improved will be described in this section.

3.1. OVERVIEW OF BOTH THE GEOMETRY AND STACK-UP OF CURRENT PRINTED CIRCUIT BOARD DESIGN

The single-ended stripline test vehicle was developed to investigate the behavior of dielectric parameters, such as both DK and DF, up to 20 GHz. Printed circuit boards had the same stack-up and layout, which are fully explained in [1] and [11]. The cross-sectional geometries, conductor roughness (due to different foils), and a laminate dielectric are individual on each printed circuit board. Dielectric material of the same type and from the same manufacturer, taken from different batches, may contain differences in their dielectric characteristics.

Both the dimensions and layout of the 6-layer PCB test vehicle currently used for PCB material characterization are presented in Figure 3.1. The length of the trace under test was approximately sixteen inches (15,410 mils). Both launching and receiving ports

with surface mount connectors were placed on both sides of the trace. Layer 2 in the stack-up contains three single-ended striplines, each with a different trace width to reach the target impedance of 48, 50, and 52 ohms. The difference in trace impedances allowed for choosing the trace with the impedance closest to 50 ohms, even if the manufacturing process would have an error. Likewise, differential pairs with 96, 100 and 104 ohms impedances are presented on Layer 5.

Besides the single-ended and differential traces under test on the PCB, there are the TRL calibration patterns, as well as additional five-inch and ten-inch single-ended striplines

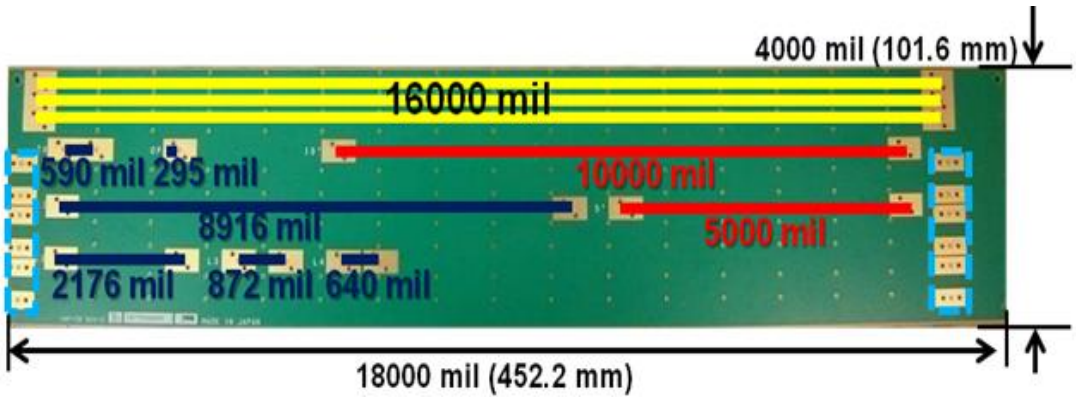


Figure 3.1 Dimensions and layout of the test vehicle.
Traces under test are highlighted with yellow color, TRL calibration patterns are dark blue, launch for differential pairs are blue, and additional traces are red.

Knowing the TRL calibration patterns allows for the de-embedding of systematic errors associated with both the inductance and capacitance of the launch vias and connectors. In principle, measurements can be taken using any type of calibration. The position of the reference planes for E-calibration (or the coaxial SOLT calibration) is

typically at the end of the precision cables, connected to the 50-GHz VNA. This calibration includes uncertainties of connectors and via-to-trace transition. TRL calibration allows for shifting the reference plane from the cable connectors further into the trace. That takes port effects away from the measurements. Patterns were designed so that the frequency range from 50 MHz to 50 GHz is divided into four segments. The length of each TRL calibration line was calculated according to the relative frequency breakpoints. Figure 3.1 illustrates that there were four TRL lines. Hence, there were five frequency breakpoints. 'Line 1' was 8416 mil (213.7 mm) long. The frequency range was between 50 MHz and 281.17 MHz. 'Line 2' was 2176 mil (55.3 mm). This frequency range was between 281.17 MHz and 1.581 GHz. The frequency range from 1.581 GHz up to 8.891 GHz is covered by the 872-mil (22.1-mm) long 'Line 3'. 'Line 4' is 640 mil (16.3 mm). The frequency ranges was between 8.891 GHz and the stop frequency of 50 GHz. There were'Through' and 'Open' standards with frequency ranges between 50 MHz and 50 GHz. The lengths of those standards were 590 mil (15 mm) and 295 mil (7.5 mm), respectively.

During both the calibration and measurements, the precision cables were attached to the SMA connectors using a torque wrench, minimizing variation in the contact resistance. The launching structure presented as a pad surface was designed to accept a flange-mount, compression-fit SMA connector. In the outer-layers, the pad size of Layer 1 and Layer 6 was 30 mil (0.765 mm). For any other inner layers, the diameter of the signal via was 9.8 mil (0.25 mm). An antipad had 100-mil (2.54-mm) diameter. This was intended to isolate the signal via from any ground and reference layers. If measurements are up to 20 GHz, it is sufficient to use the SMA connector MOLEX SN 73251-1850.

The maximum frequency for operating this connector is 26.5 GHz, according to a manufacturer's official rating. The dimensions and the overview of the connector are shown in Figure 3.2. The metal body of the connector provided the return path. Two plated-through holes for screws were drilled through all six layers. Each connector was mounted using two screws of certain dimensions. The quality of the signal transition between the connector and PCB via pad primarily on the quality of screws and connectors. Before making calibration and measurements, it is very important to make sure that the connectors and screws are not broken or damaged, otherwise, the calibration procedure have falied and measurements would have been incorrect.

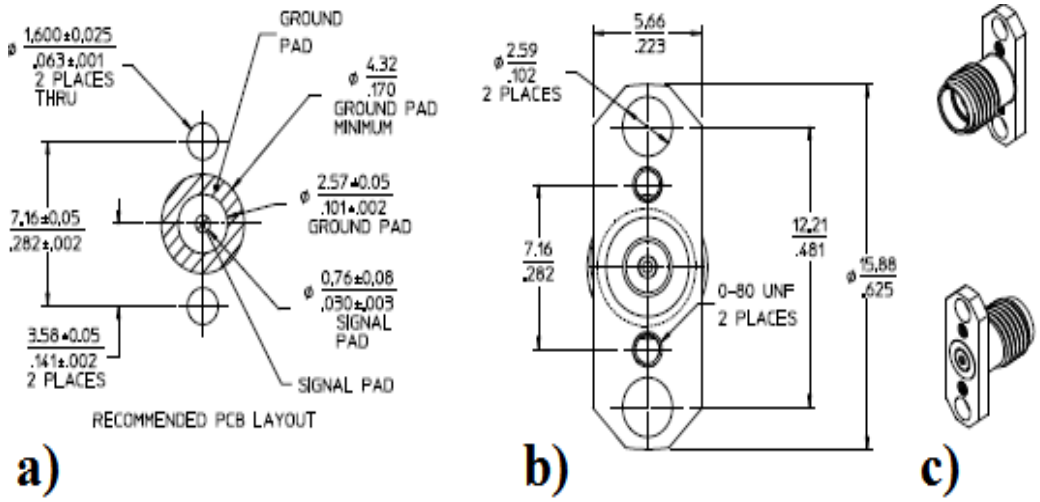


Figure 3.2 Geometry and overview of the SMA connectors.
(a) Recommended PCB layout. (b) Schematic of geometry of the connector (c) Outlook of the connectors.

The PCBs under study had the six-layer structure. According to the test vehicle stack-up, the connectors were to mounted on Layer 6, when single-ended traces are under

test and on Layer 1, or when the differential pairs are to be tested. Choosing the proper side for mounting connectors would minimized the length of the via stub.

The design of the stack-up, illustrated in Figure 3.3, contained the balanced-stripline signal traces on Layer 5 (impedance-tuned for 48, 50 and 52 ohm). On Layer 2, the single-ended traces were replaced with an analogous structure of the differential pairs (impedance-tuned for 96, 100, 104 ohm). Layers 1, 3, 4, and 6 have the identical ground planes. Between Layers 1 and 2, as well as between Layer 5 and 6, there are prepregs with approximately 50% finished resin content. Copper-clad cores comprised both Layers 2 and 3 and Layers 4 and 5. They were chosen as close as possible to the 50% resin content. The dielectric between Layers 3 and 4 provides the mechanical rigidity to a finished board, and has no influence on measurements. This is the reason of not using expensive dielectrics to fill the spacing between Layers 3 and 4. Only prepregs and cores were located between Layers 1 and 2 and Layers 2 and 3, have an impact on measurements of the single-end stripline, described in this work.

Besides the connector frequency limitation, the maximum frequency range for measurements was also determined by the signal via design. Herein, the via design was optimized to work up to 35 GHz, which is sufficient for measurements up to 20 GHz. The via structure needed to be significantly modified to provide measurements up to 50 GHz. Both the design and dimensions of the signal via are presented in Figure 3.4

A circle of eight ground stitching vias, passing though all six layers of the PCB, was located outside of the anti-pad. Both provided shielding of the signal via and raised the current return path. Eight ground stitching vias were equally distributed in a circle. All sizes were calculated and optimized using a Multilayer Via Transition Tool (MVTT).

This tool is described in [12] and will be discussed further in Section 3.2 of this work. As a reference for the dielectric constant, DK has been defined as 4. The signal via went through six layers. But the single-ended trace is located on Layer 5. The via part from Layer 5 to Layer 6 was the via stub. The size of via stub is 10.8 mil. The resonance frequency associated with via stub, in this case, is above 35 GHz.

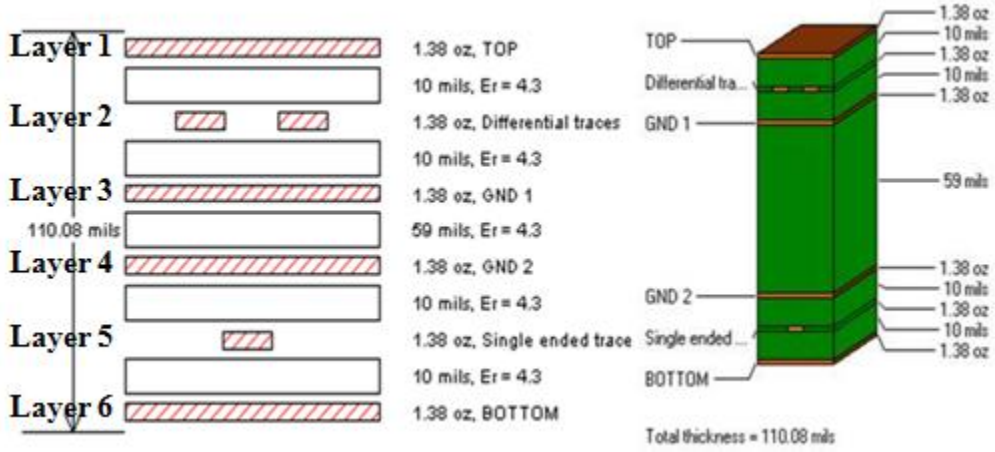


Figure 3.3 Stack-up details of 6-layer PCB

Via have been designed to work up to approximately 30 GHz. In practice, however, the measurements become incorrect around 33 GHz. Today's industry needs to know dielectric parameters up to 10 GHz for designing more accurate models. The frequency range of the current measurements is from 10 MHz till 20 GHz, both covers the point of interest for the industry and stays below the maximum frequency point. Even if the TRL calibration de-embeds the port effects, including via transitions, the characteristics of the via transition must still be known. If the return loss at a certain frequency is- significantly high (approximately more than -7 dB), and the insertion loss is

low (approximately -10 dB), sufficient amount of signal could not pass the via, this and calibration would fail. To understand the behavior of the via transition up to 50 GHz, the model has been designed using the full-wave numerical electromagnetic software CST Microwave Studio. Via has been modeled with the same geometry as in the MVTT optimization tool with the 300-mil stripline. From the plots presented in Figure 3.5 and Figure 3.6, the via transition could be analyzed with a certain percentage of accuracy.

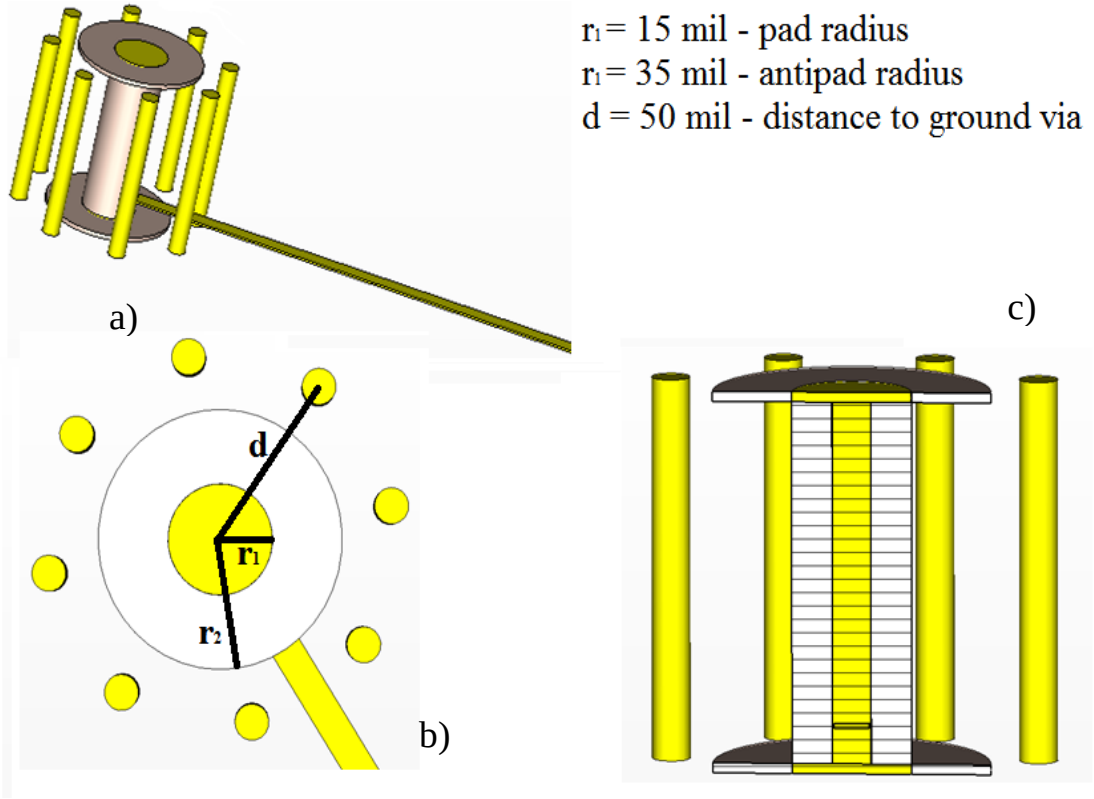


Figure 3.4 CST model of the via structure for 20-GHz test vehicle
a) Prospective view. b) Top view. c) Side view

Up to 20 GHz the return loss is below -10 dB, allows for getting the TRL calibration and extracting the relatively correct data from measurements. The TRL calibration fails at about 28 GHz, because the level of the return loss is significantly high.

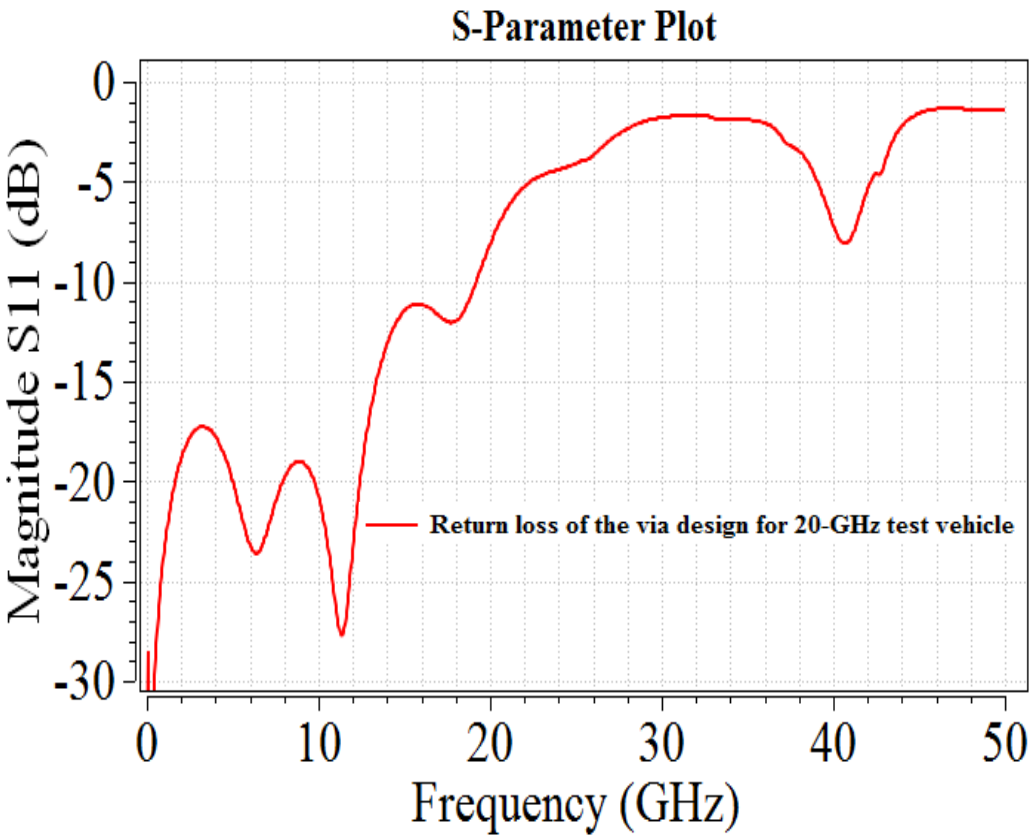


Figure 3.5 Return loss of the via modeled in full-wave CST

Looking at the insertion loss in Figure 3.6, it is easy to notice that after 28 GHz there is much loss. Having the insertion loss around -10 dB would not provide a sufficient signal for either calibration or measurements. The return loss characterizes the magnitude of the signal reflected from the via structure, and the insertion loss shows how much signal would go through the transmission line. In practice, it is very useful to have the higher return loss (magnitude of S_{11} is approximately below -8 dB) and the insertion loss as low as possible (less than 6 dB). If the magnitude of the return loss exdceeds the magnitude of the insertion loss, that more energy is reflected from via structure than it is going through the via. The effect of the increased mismatched loss on the systematic

error of measuring DK and DF is considered in Appendix C. As shown in Figure 3.7, return loss begins to exceed insertion loss near 26 GHz.

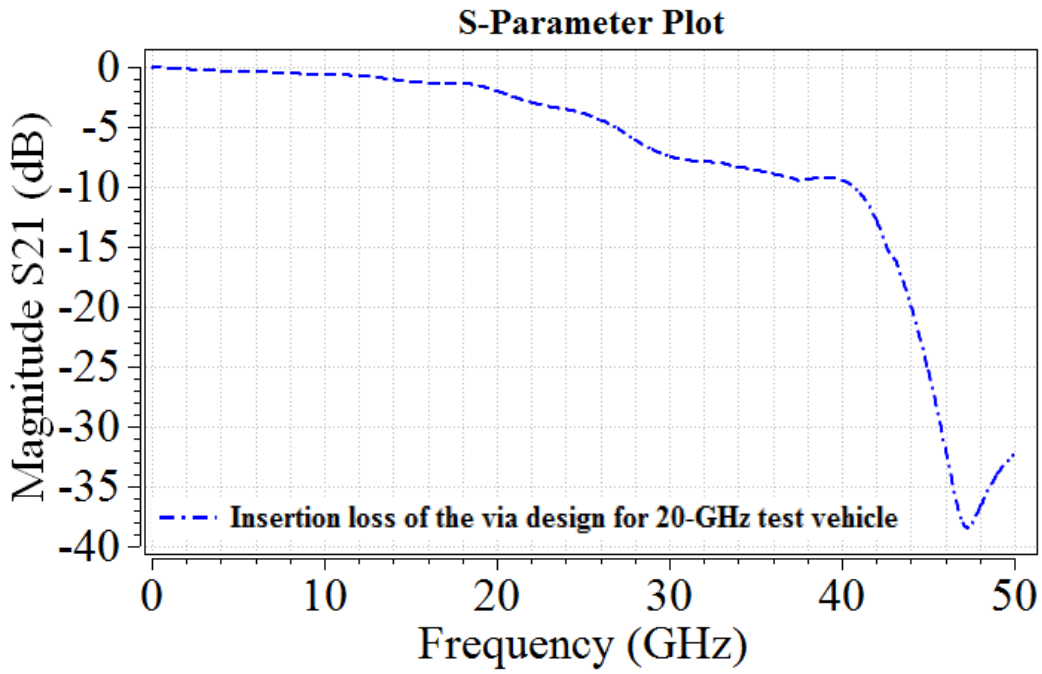


Figure 3.6 Insertion loss of the via modeled in full-wave CST

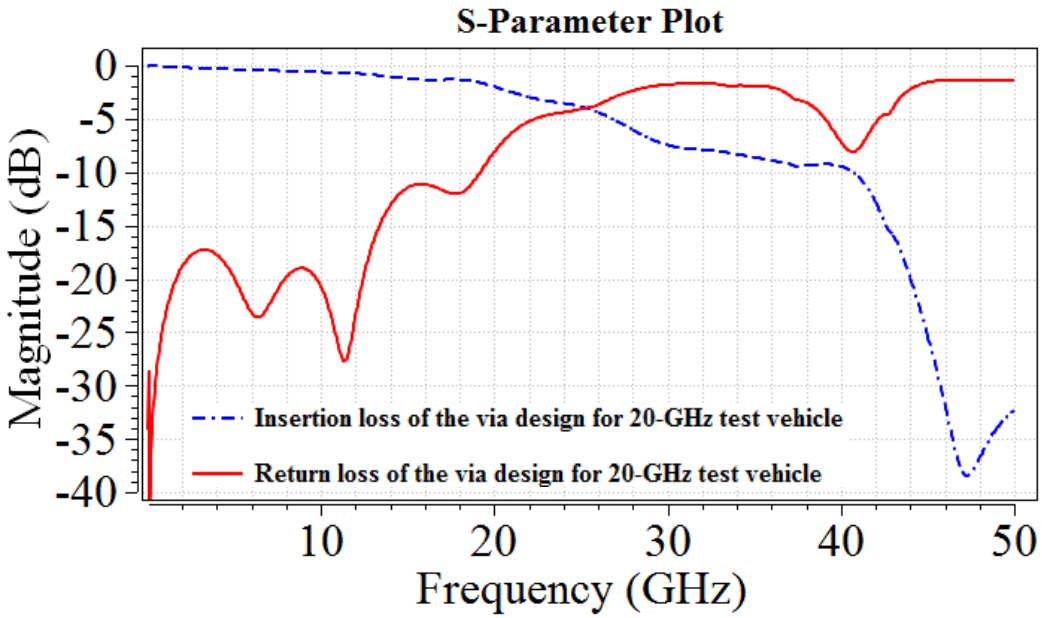


Figure 3.7 Insertion loss and return loss of the via modeled in full-wave CST on the same comparison graph

Another important indicator of the via transition quality is the phase of insertion loss. This loss needs to be both stable and linear over the entire frequency range. Figure 3.8 illustrates a phase of insertion loss for the modeled via. Linearity of the phase fails around 26-27 GHz.

Simulation of the via transition in the full-wave simulation tool in CST Microwave Studio was made. Modeling shows the approximate frequency limit of the via structure and characterizes the optimized via geometry. The frequency range of the current measurements was below 26 GHz. This may provide a good quality of measurements.

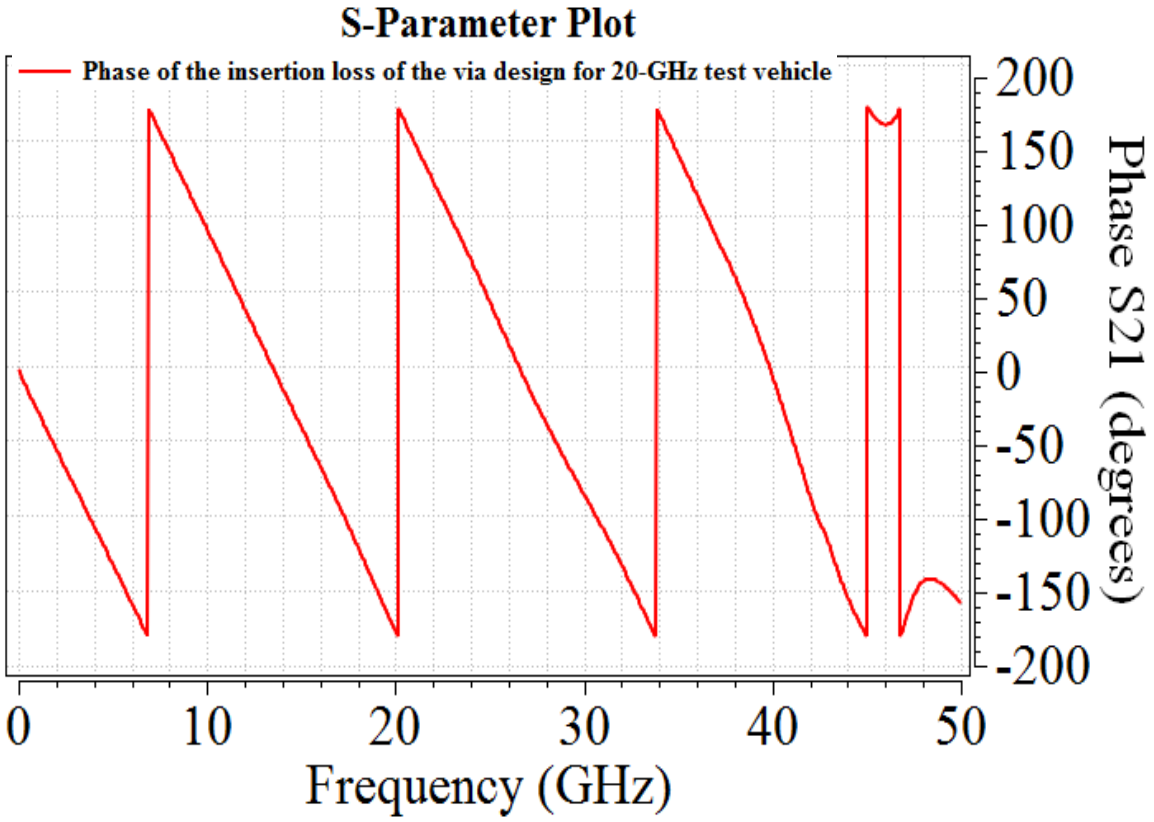


Figure 3.8 Phase of insertion loss of the via modeled in full-wave CST

In addition to stitching ground vias around the signal via, there are other ground vias on the board which provide the current return path. All vias are equidistant with one inch spacing between vias. Such geometry of the via wall creates a resonance effect, detailed in Section 2.2.

As previously mentioned, the primary goal of this work was to design a new PCB test vehicle with a frequency limit up to 50 GHz. For accomplishing this goal, the current design of the test vehicle, described in Section 3.1, will be used as a reference. Analysis of errors and uncertainties, explained in Section 2.2, will be taken into account to avoid additional problems with the test vehicle design.

3.2. MODIFICATION AND IMPROVEMENT OF TEST VEHICLE DESIGN

Test vehicles with the current design up to 20GHz were used to obtain dielectric properties with measurements up to 20 GHz. The frequency limit of the existing PCB test vehicles with current design up to 20 GHz is approximately 26-30 GHz. This frequency is dependent on the dielectric constant of the PCB laminate dielectric material.

The decision to improve the design was made after analyzing limitations and possible uncertainties in measurements due to the current 20-GHz test vehicle design. Both signal via and via stub had significant influence on the cut-off frequency of the measurements. The design of the signal via needed to be modified to allow for measurements up to 50 GHz. However, even if the via design is improved, calibration and measurements still may fail unless new, proper connectors are used. The cut-off frequency of the SMA connectors used in the current test vehicle design was

approximately 35 GHz. 2.4-mm connectors with a 50-GHz cut-off frequency were used for the new PCB test vehicle design. A new TRL pattern was designed for calibration over a frequency range between 50 MHz and 50 GHz. According to the error analysis presented in Section 2.2, via wall in the test vehicles also needed to be modified. Periodic one-inch spacing between stitching ground vias creates unwanted resonances every 3.1 GHz.

Summary of future improvements presented in Figure 3.9.

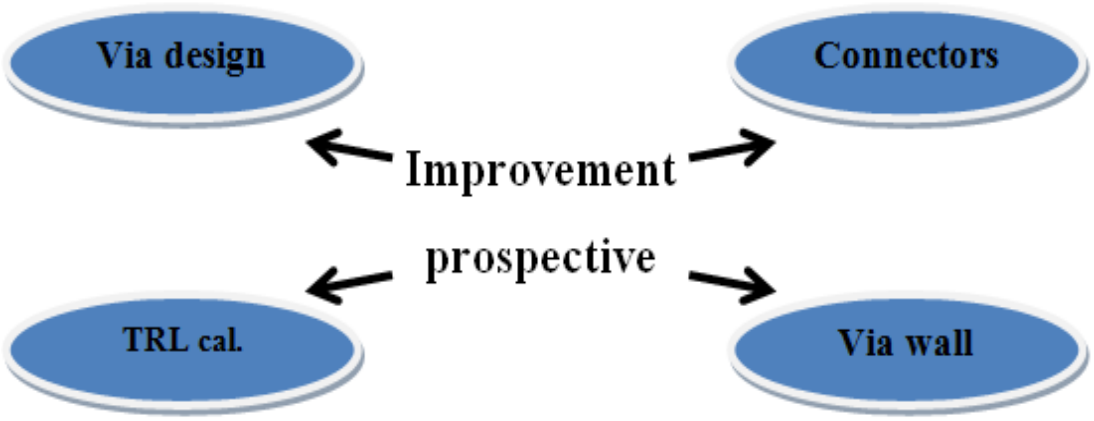


Figure 3.9 Summary of the issues for improving

3.2.1. Improvement In Via Design. Design and optimization of a connector launch structure up to 40-50 GHz is challenging. Distance from the center of the signal via to center of each stitching ground via (which forms a coaxial structure around the signal via) needs to be calculated and optimized. As well as size of pad and dimensions of anti-pad. The algorithm to develop a new via structure is given in Figure 3.10.

The genetic algorithm (GA) employed in the MVTT (Multi-via transition tool) software has been used for the first-stage optimization. The full description and manual

for the MVTT have been published in [12]. After using the MVTT as the first stage of the optimization, the full-wave electromagnetic simulations using the CST Microwave Studio, both in frequency domain and in time domain, were then run to verify results of the MVTT optimization. At the final stage, the CST model was tuned to achieve the best possible results. The final version of the via design was compared to the via model used in the 20-GHz test vehicles.

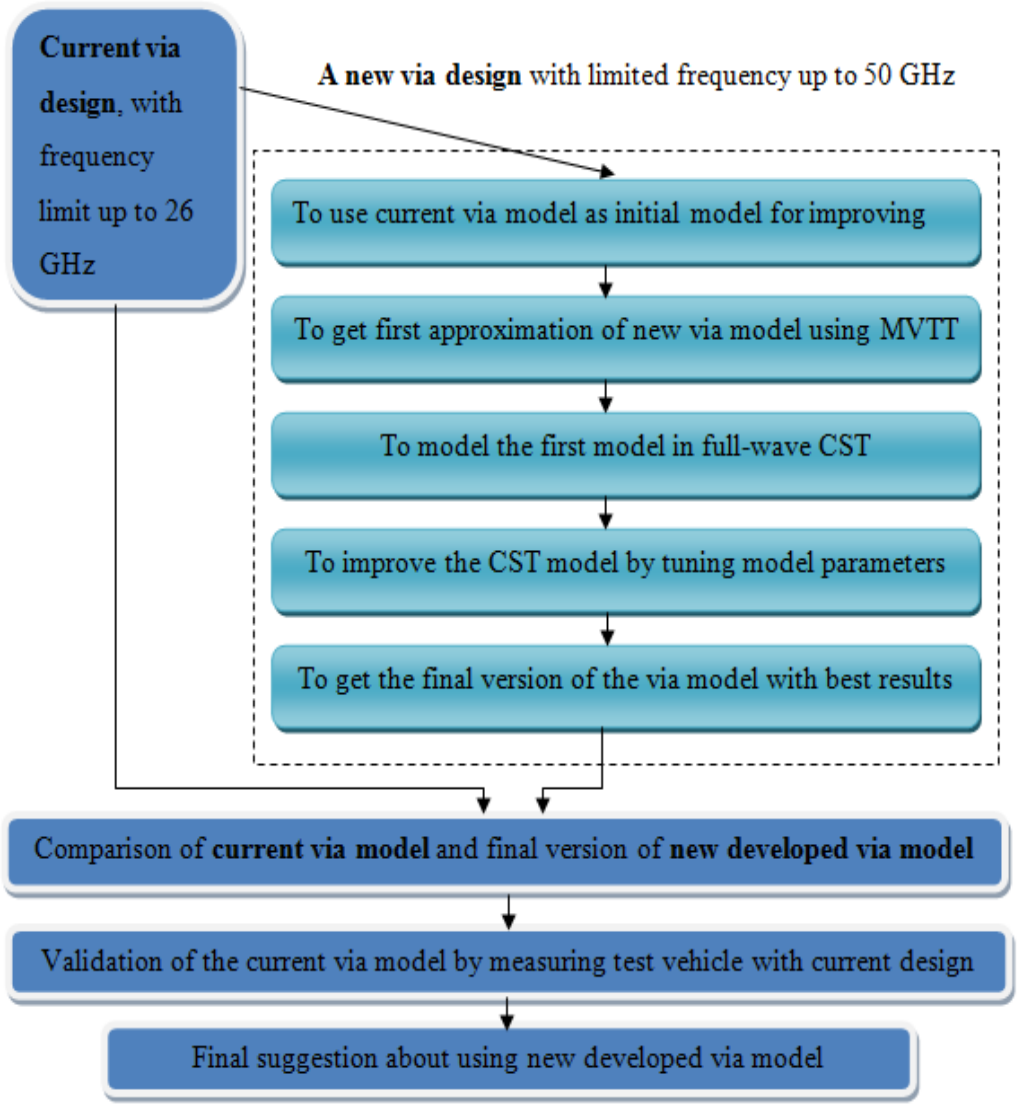


Figure 3.10 Algorithm of the new via design development

The advantage of the MVTT tool is a wide variety of input parameters. Structure's model, however, should remain comparatively simple.A 70 Ghz stop frequency was for the new design. In the previous via design for 20-GHz test vehicle this frequency was set as 40 GHz. The dielectric parameters of the laminate dielectric on the test vehicle were set at DK=3.5 and DF=0.005. In the previous design these values were DK=4.25 and DF=0.095. Stack-up information for the 50-GHz test vehicle remained the same as that for the 20-GHz test vehicle.

Figure 3.11 illustrates three ground via configurations analyzed using the MVTT. A 50 mil distance between the signal via and the stitching ground via was chosen as the initial parameter. During optimization, this parameter changed. The current design (20-GHz) has 8 stitching ground vias placed in a circle around the signal via. This design has been analyzed in earlier works: [8] and [11]. The ground via ring was intended to suppress the cavity mode created due to the coaxial structure around the signal via. In the case of 8 ground vias located 50 mil away from the signal via, the resonance will be at approximately 40 GHz. To increase the shielding effect of ground vias around the signal via, the number of ground vias will be increased as well. However the distance between the ground vias in the model with 24 ground via (as in Figure 3.11 c), is too small. That spacing does not meet manufacturing requirements regarding the minimum distance in the layout. The optimal model presented in Figure 3.11 (b) is the ring of 16 stitching ground vias.

Optimization of only the geometry of a single ring ground via and varying a number of vias does not result in the optimal via design. Such optimization only gives expectations for a future design of 50-GHz test vehicle. Figure 3.12 is a snapshot of both

the numerically calculated return loss and the insertion loss using the MVTT for the model of 16 ground stitching vias. According to these calculations, the resonance frequency of the natural cavity mode is near 50 GHz, however, (see Figure 3.12 b) the unwanted resonance occurs at 46 GHz. This resonance is due to the 10.8 mil via stub. Having either no via stub or a very small via stub would eliminate this unwanted 46-GHz resonance

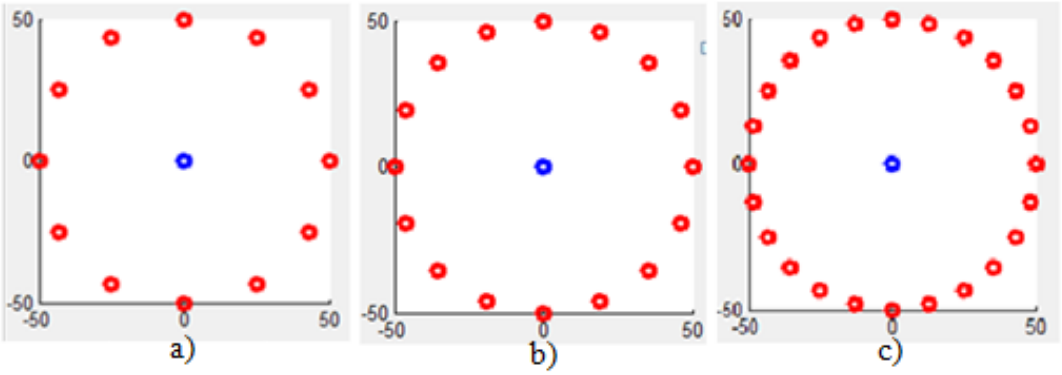


Figure 3.11 The top view of via models, analyzed using MVTT
a) Single ring 12 ground vias. b) Single ring 16 ground vias. c) Single ring 24 ground vias

There are three output parameters optimized in the MVTT using the genetic algorithm: (1) the radius of the pad, (2) the radius of the antipad, and (3) the distance between the ground via and a signal via. The MVTT generates these three parameters, taking into account both initial parameters and ranges established by a user. Tuning the impedance of the via to 50 Ohm at the optimization stage. The optimization results also depend significantly on the initial dielectric parameters. The results for the optimized parameters are giving in Table 3.1. They are depend on the chosen DK and DF values of the PCB test board dielectric.

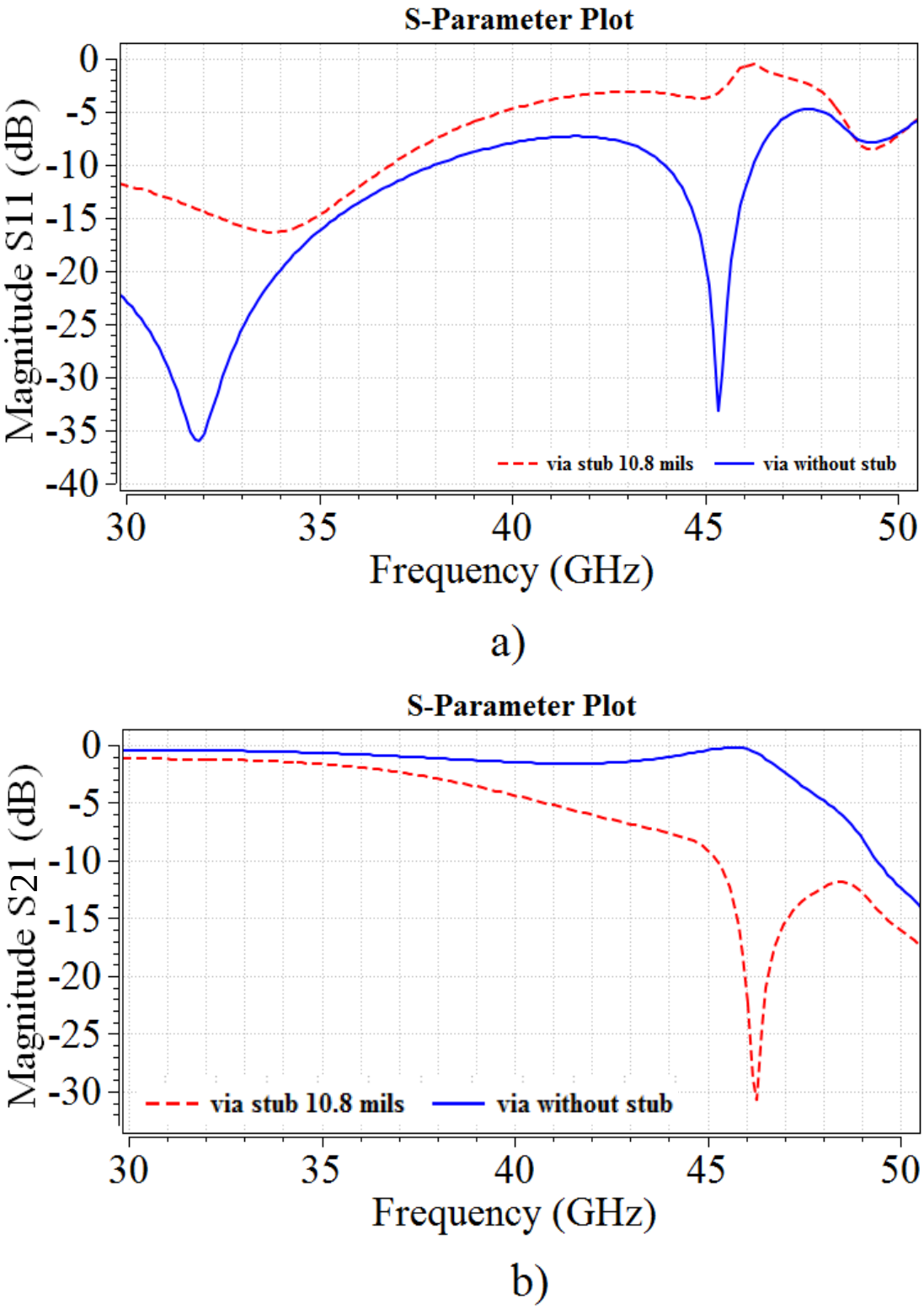


Figure 3.12 Calculated S-parameters using the MVTT (snapshot)
The model with a 10.8 mil via stub is shown in red. Via without the stub is in shown in blue a) Magnitude S_{11}. b) Magnitude S_{21}

Table 3.1 Overview of the optimization for via geometry parameters for different DK, DF

Df	0.	0.0	**0.0**	0.0
Dk	3.	3.4	**3.2**	3
Via pad,	18	18.	**20**	19.
Via	27	26.	**25**	25
Distance	58	56	**54**	40

The optimized dimensions of both the via pad and anti-pad, were obtained for the DK=3.2. The size of the via must match the size of the SMA connector pin for getting an acceptable signal transition between the connector and the via. Both types of SMA connectors (the 3.5mm and 2.4mm) have a connector pin diameter of 20 mil.

During the second stage of the via transition design, the via structure (which has been optimized using the MVTT software) was modeled using the full-wave CST Microwave Studio tools (further referred as CST). According to the results of the MVTT via geometry optimization, 16 stitching ground via, each located at 54 mil away from the center of the signal via, were needed. The two closest to the trace ground stitching vias were too close to the single-ended stripline. They need to be moved away from the trace. The via pad was 20 mil in diameter, while the via anti-pad diameter was 25 mil. The via stub should be either shorter, or even completely eliminated from the via structure. The DK was set at 3.2, and the loss tangent was DF=0.01. Both the CST model overview and the corresponding via geometry are presented in Figure 3.13.

The model in the CST was designed according both the calculations and optimization obtained using the MVTT. The simulated data given in Figure 3.14, however, is unacceptable.

The modeled insertion loss was comparatively high (>-20 dB) at frequencies above approximately 15 GHz. The return loss was greater than the insertion loss over the frequency range approximately from 26 to 32 GHz. These factors may cause the TRL calibration to fail. That affects measurement accuracy.

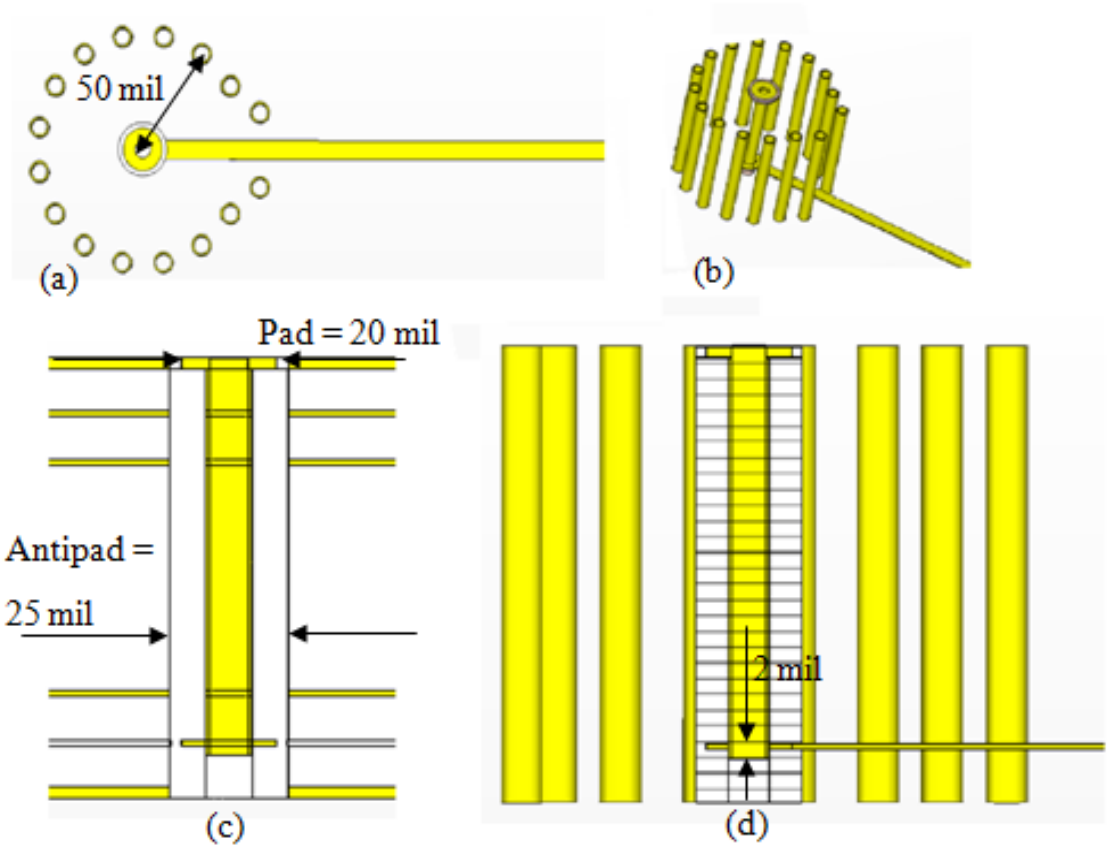


Figure 3.13 Overview of the first via geometry CST model
a) Top view. b) Prospective view. c) Front view. d) Side view

During the third stage of the via design, the optimized and modeled via dimensions must be tuned to decrease the return loss and possibly remove the natural resonance of the cavity mode or move it closer to the target 50 GHz

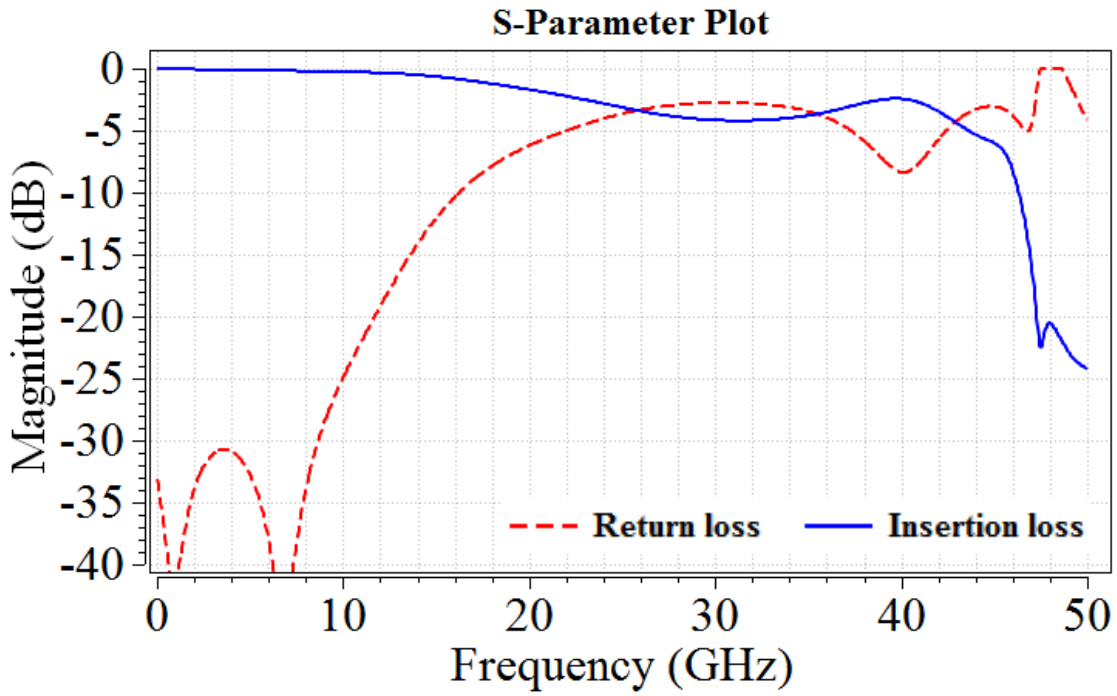


Figure 3.14 Results of modeling of improved via model in CST. Blue curve indicated |S21|, red curve corresponds to |S11|

Several special techniques are available to improve the via design. Several of these techniques have been implemented at the initial stage of modeling in CST. Reducing the via stub from 10.8 mil to 2 mil allowed for avoiding an unwanted resonance close to 50 GHz. A tear-drop structure could be applied to eliminate sharp angles/edges at the via-trace transition. However, after modeling the tear-drop geometry in the CST, little improvement was observed. An unwanted cavity coupling to the other structures, such as via, traces, via wall on the PCB could be suppressed by adding an additional, second, stitching ground via ring. The dual ring ground via structure provides the better isolation for coupling. The closest outer ring of the ground vias may be located at 70 mil away from the center of the signal via. On the one hand, having the second ring closer than 70 mil to the center of signal via, cannot satisfy manufacturing requirements.

As compared to the initial CST model, illustrated in Figure 3.13, only two changes in the next CST model were made. These changes included both adding a second ring of ground vias 70 mil away from the center of the signal via and using a wider antipad. The clearance between the signal pad and the first ring of ground vias was increased to prevent having short between inner pin of the 2.4 mm SMA connectors and the ground plane of the PCB, while running calibration and measurements. In the latest new CST model, the diameter of the antipad is 34 mil. Figure 3.15 shows the via design and gives information about its dimensions.

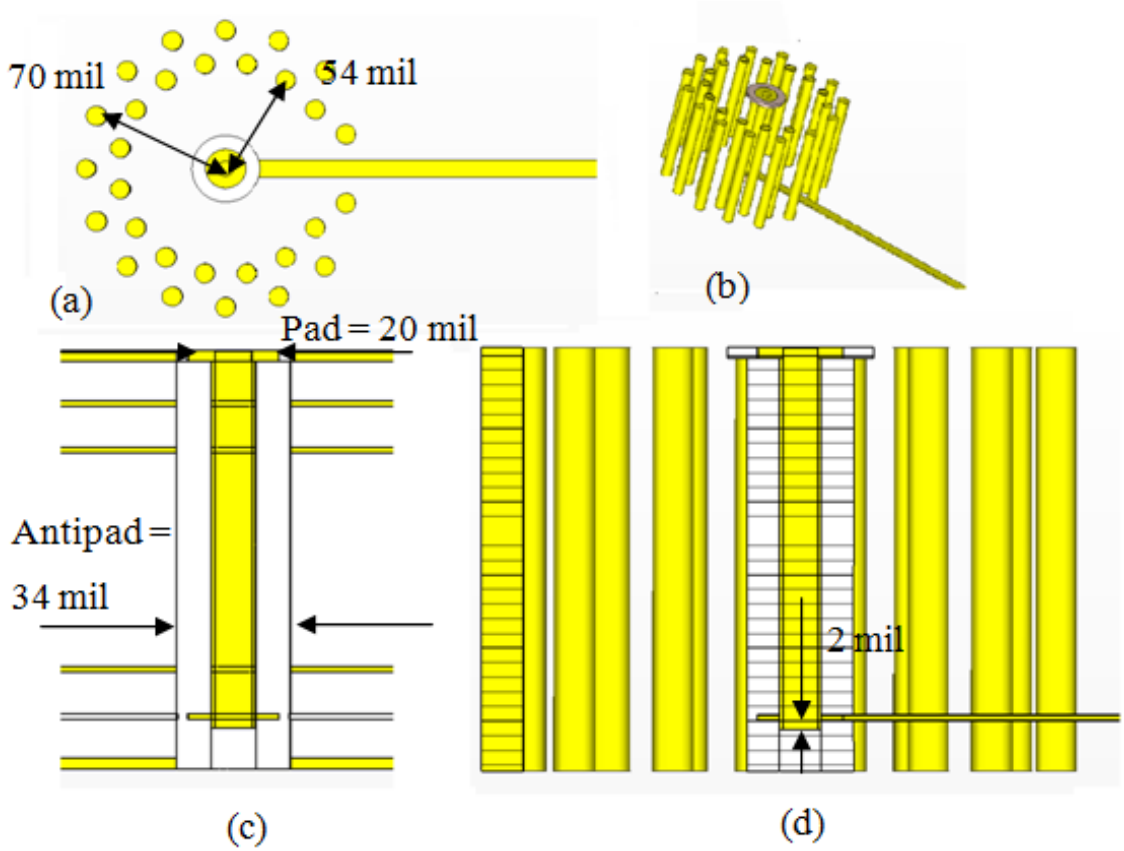


Figure 3.15 Overview of the second CST design via model
a) Top view. b) Prospective view. c) Front view. d) Side view

Even with small changes in the via model design, the simulated CST results (illustrated in Figure 3.16) were better than the results from the previous design. The magnitude of return loss of the second via model did not exceed the magnitude of the insertion loss over the entire frequency range until above 46 GHz, where the natural resonance of the cavity mode occurs. The chance of TRL calibration failure during measurements with this latter via-trace transition design was reduced when compared to the initial design. The phase of the insertion loss (shown in Figure 3.17) remained both linear and stable up to 46 GHz, also indicating a better quality of the second model.

After analyzing the simulation results, shown in Figures 3.16 and 3.17, the decision to use the latest version of the via model as a via design for new test vehicle has been made. The CST model shows that there is an unwanted resonance at frequency of about 48 GHz. This resonance is clearly seen in Figure (3.16) on the insertion loss curve. It can limit the frequency range of the new via design.

The possible explanation of the resonance observed in Figure (3.16) is the higher-order mode (TE_{11}) in the coaxial structure. The internal radius of the structure corresponds to the radius of the via radius of the via itself (a = 10 mils). The outer radius corresponds to the radius of the inner ground via ring (b = 27 mils). According to [4, pp 144-145], the cut-off frequency is calculated as

$$f_c = \frac{c \cdot k_c}{2\pi\sqrt{\varepsilon_r}} \tag{3.1}$$

where k_c is the cut-off wave number, which is approximately found according

$$k_c = \frac{2}{a+b} \tag{3.2}$$

Herein, the cutoff frequency equals to

$$f_c = \frac{3 \cdot 10^8 \cdot 0.2165 \cdot 10^4}{2 \cdot 3.1415 \cdot 1516} = 52 GHz \tag{3.3}$$

This calculation is approximate, it does not take into account imperfect electric conductor and imperfect discrete shield of the ground via ring, which would load this resonance and shift it to the lower frequency (~ 48 GHz)

However, if the calibration and measurements are done correctly up to 46 GHz, the extracted DK and DF values can be extrapolated up to 50 GHz and even higher, since dielectric properties of the PCB laminates should be monotonic over this frequency range.

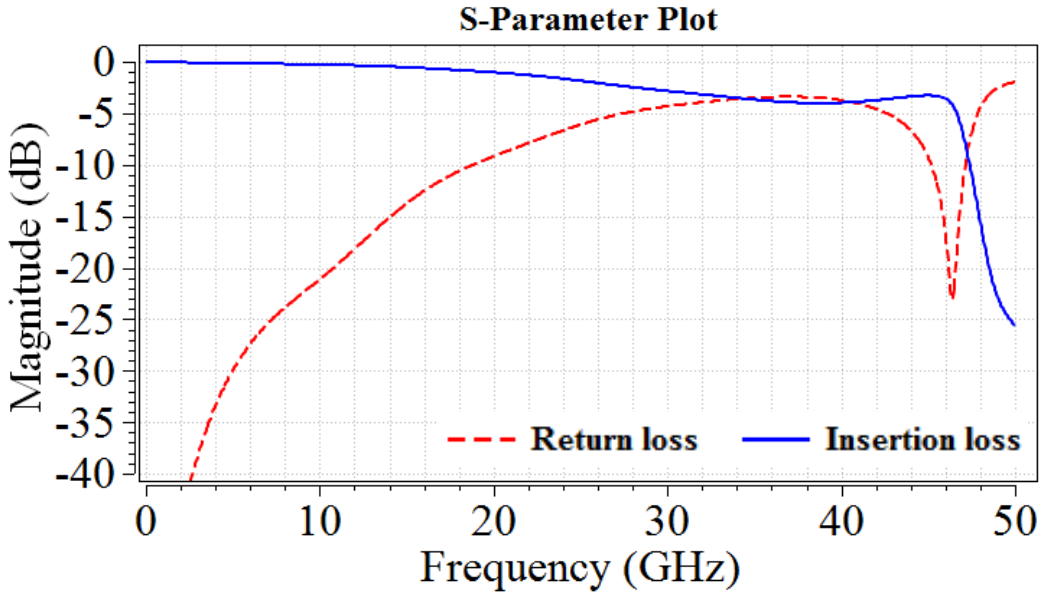


Figure 3.16 Results of modeling new 50-GHz via design in CST
Blue curve indicates S_{21}, and the red curve corresponds to S_{11}

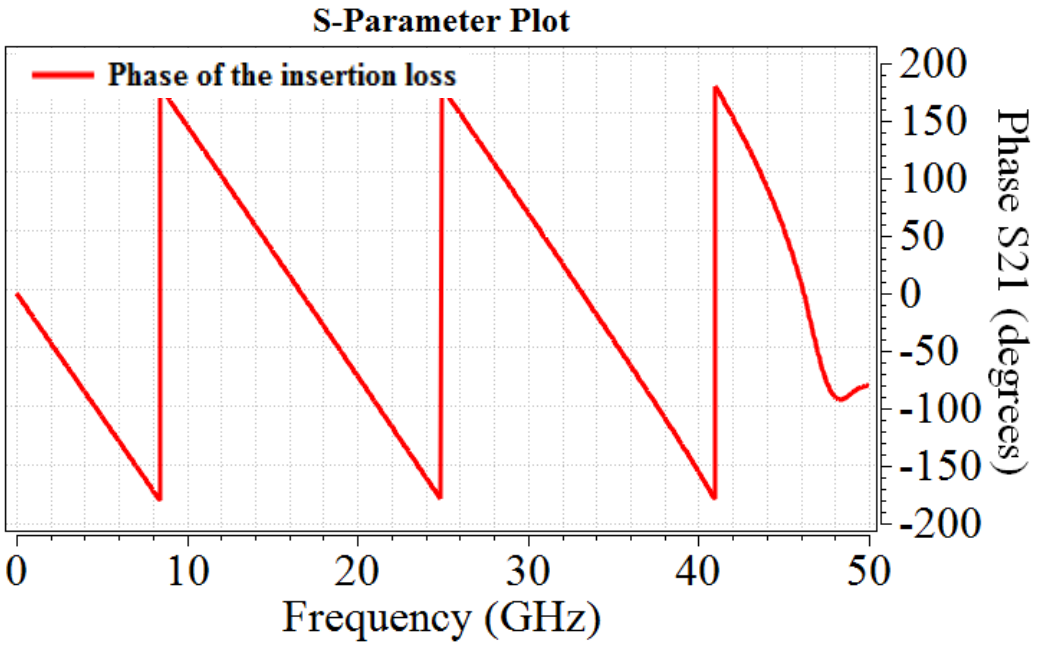


Figure 3.17 Simulated phase of S21. in the second CST 50-GHz via model

Prior to sending out to the data for a new test vehicle design to a PCB manufacturer, it is important to compare the new via model, shown in Figure 3.18 (b), with the via model in the current 20 GHz test vehicles, presented in Figure 3.18 (a). With the new via design, the upper limit of the measurements should be at least 45 – 50 GHz.

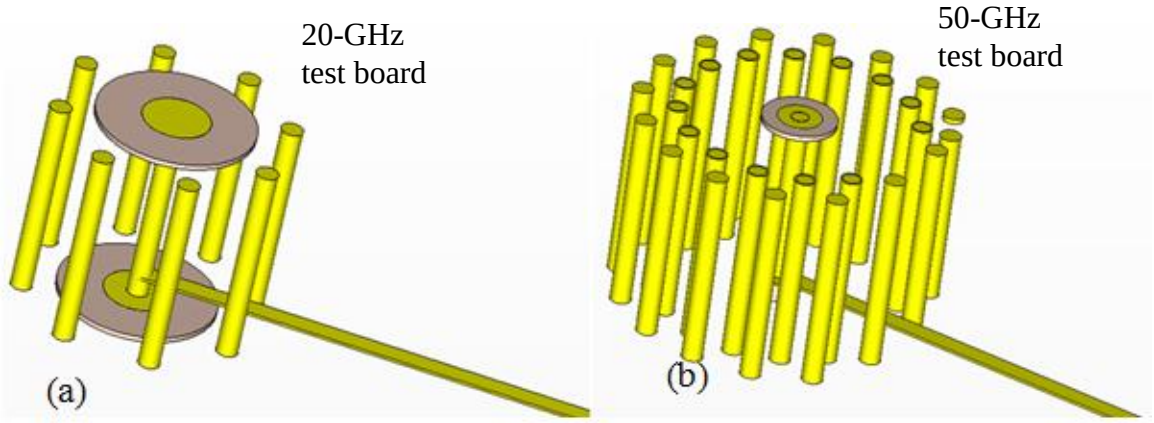


Figure 3.18 Prospective views on the CST via models
a) The existing via design for measurements up to 20 GHz. b) Future via design for measurements up to 50 GHz

Simulation results for the currently existing and the future via geometries are plotted in Figure 3.19. Looking at the S-parameters, it is easy to see the difference due to the via design. The cutoff frequency is defined as the frequency point, at which the signal gets reflected rather than going through the transmission line. In terms of the S-parameter data, the cut-off frequency is determined when the return loss exceeds the insertion loss. The return loss and the insertion loss for the current via design in the 20-GHz test vehicles are plotted in Figure 3.19.

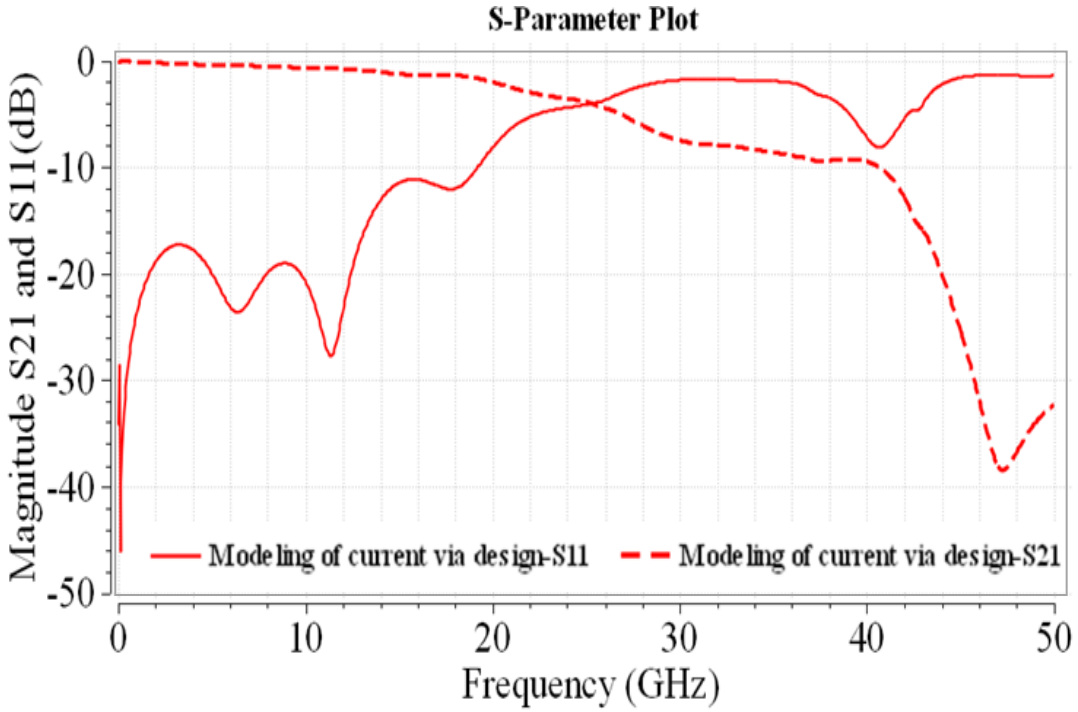


Figure 3.19 Return and insertion losses of the via structure developed for the 20-GHz test vehicle

It is seen that the cut-off frequency for this via model is approximately 26 – 28 GHz. Performing the TRL calibration for de-embedding port effects above the cut-off frequency would lead to the failure of the calibration and measurements, because of high

return loss and low insertion loss. That is the reason the current via model could not be used for measurements up to 50 GHz. The cut-off frequency of the via model developed for obtaining S-parameters up to 50 GHz is around 46 – 48 GHz, since the return loss exceeds the insertion loss only around 46 GHz. Simulated S-parameters of the via model designed for developing a test vehicle up to 50 GHz are presented in Figure 3.20.

The comparison of the via geometry characteristics is shown in Table 3.2. In the new 50-GHz structure, the pad and antipad are smaller than in the currently used 20-GHz structure, but the size of the pad is sufficient enough to have good contact with the connector pin. The dual ring ground vias in the new model provide better shielding of the signal via. The shorter via stub would allow for shifting the natural resonance of the cavity mode to the higher frequency above 50 GHz.

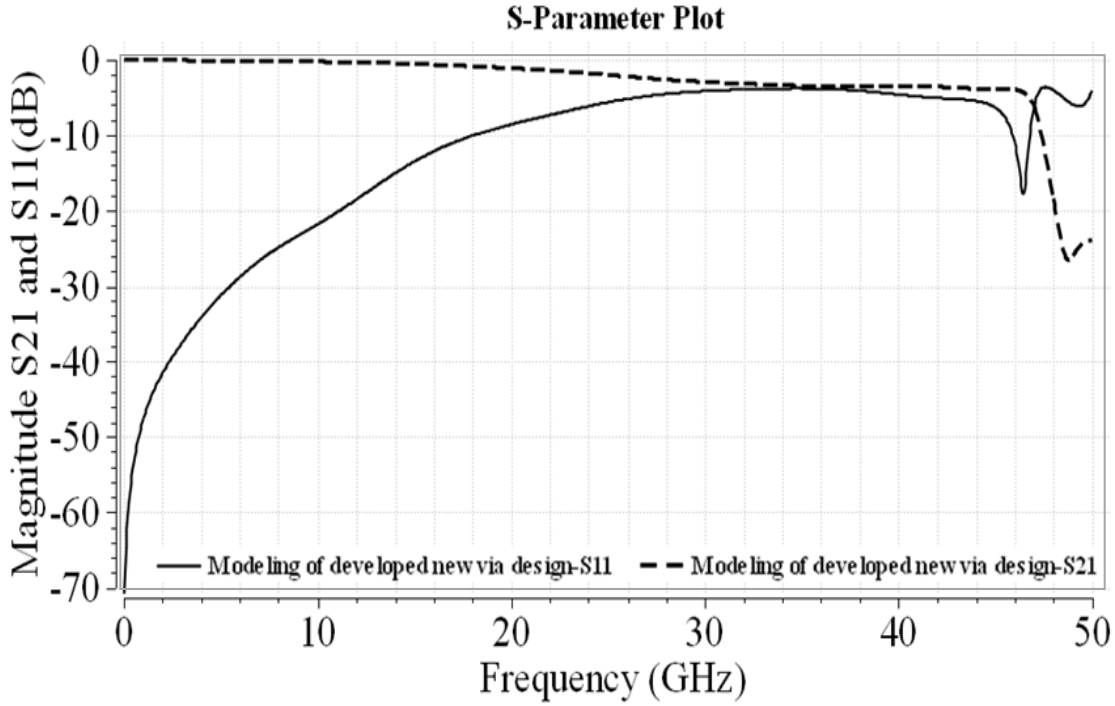


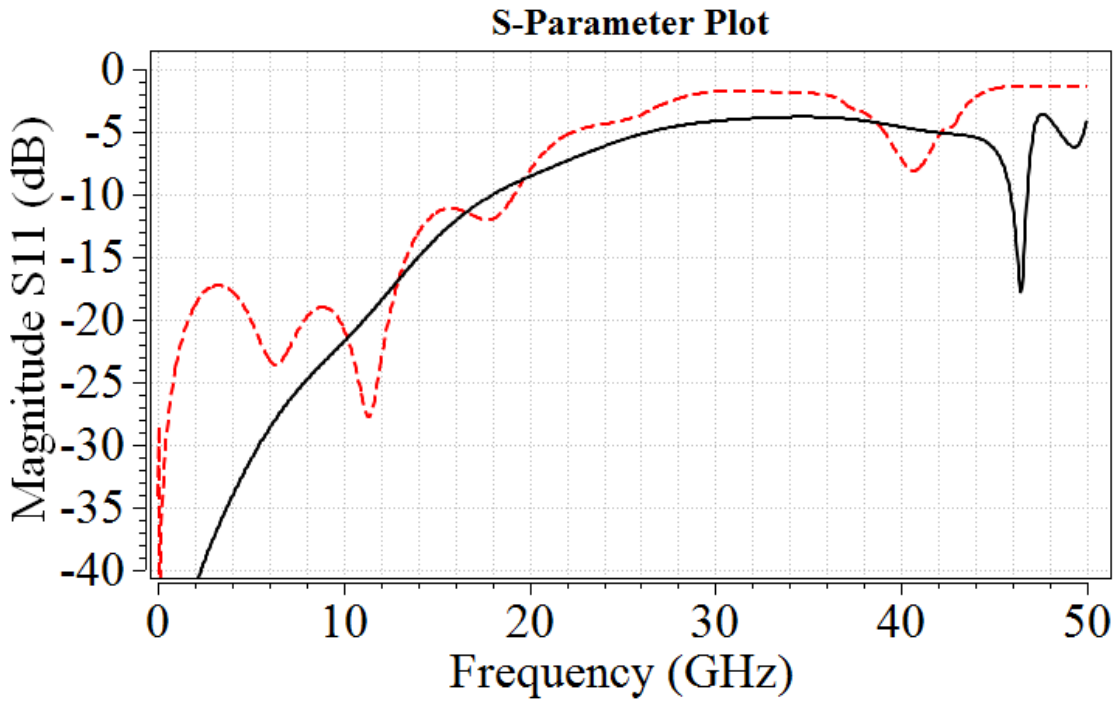
Figure 3.20 Return and insertion loss of the via structure, developed for the 50-GHz test vehicle

Table 3.2 Geometry and parameter comparison of the two via designs

Parameter	**Current via model**	**Developing via model**
Stack-up	Same	Same
Via length	91.3 mil	82.5 mil
Pad diameter	30 mil	20 mil
Antipad diameter	70 mil	34 mil
Finished diameter of the ground PTH vias	9.8 mil	9.8 mil
Length of the via stub	10.8 mil	2 mil
Distance(-s) between center of the signal via and center of any ground via	50 mil	The first ring ground via is 54 mil away. The second ring is 70 mil away
Approximate cutoff frequency	26 – 28 GHz	46 – 48 GHz

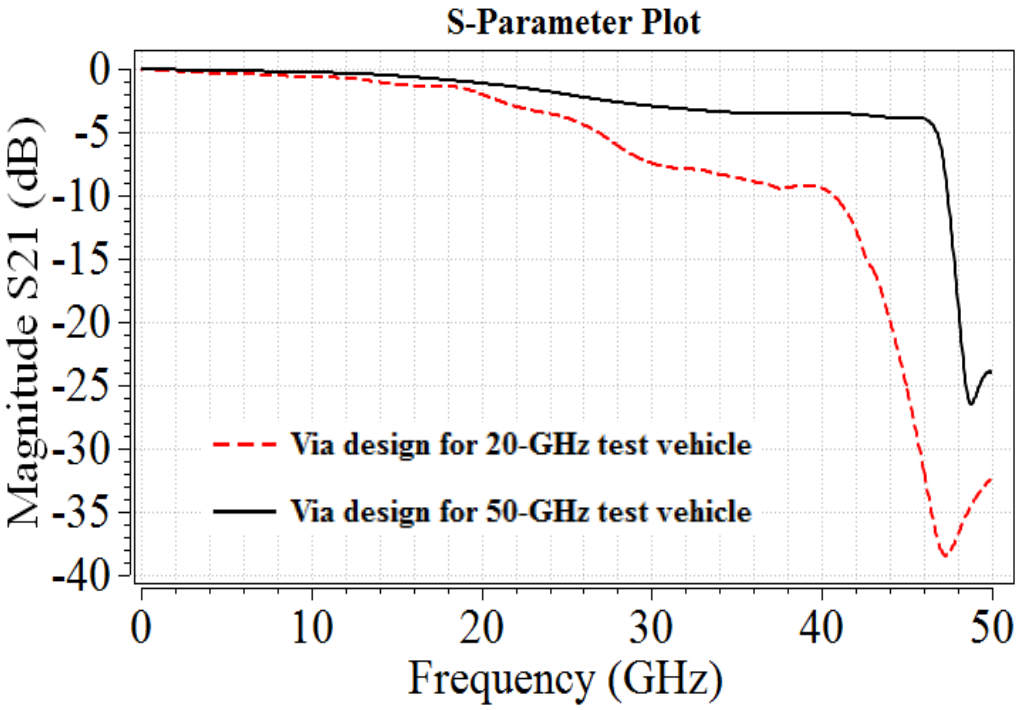
To better understand the difference in the performance of two via designs, one can compare the simulated S-parameters by plotting S_{11} on the same graphs, as well as plotting the corresponding magnitudes and phases of S_{21}. Such comparison is presented in Figure 3.21. The black curve represents the new via design developed for measurements up to 50 GHz, and the red line indicates the current 20-GHz via design. The magnitude of the return loss for the new design is lower than for the current design, and this indicates the improvement in the new via design compared to the current via model. For the 50-GHz design, the insertion loss, shown in Figure 3.21 (b), is closer to zero, and the phase of the insertion loss is more linear and stable, as is shown in Figure 3.21 (c). These results demonstrate the advantage of the new via design over the via structure, used in the current 20-GHz test vehicles.

Before the 50-GHz target was set up, the goal of the research was to characterize dielectric parameters of PCB dielectrics using 16'' stripline structures up to 20 GHz. Obviously, the TRL calibration and measurements would fail 26.5 GHz due to the frequency limitations of the 3.5-mm SMA connectors. However, measurements on a 16'' stripline even up to 30 GHz can validate the simulated data for the current via design. In addition to the via stub resonance problem, the insertion loss after 30 GHz starts deviating from the linear behavior. Figure 3.22 shows that there is a failure of TRL calibration and measurements above 30 GHz due to the 3.5-mm connector limitations in the test vehicle with the 16'' trace under test.

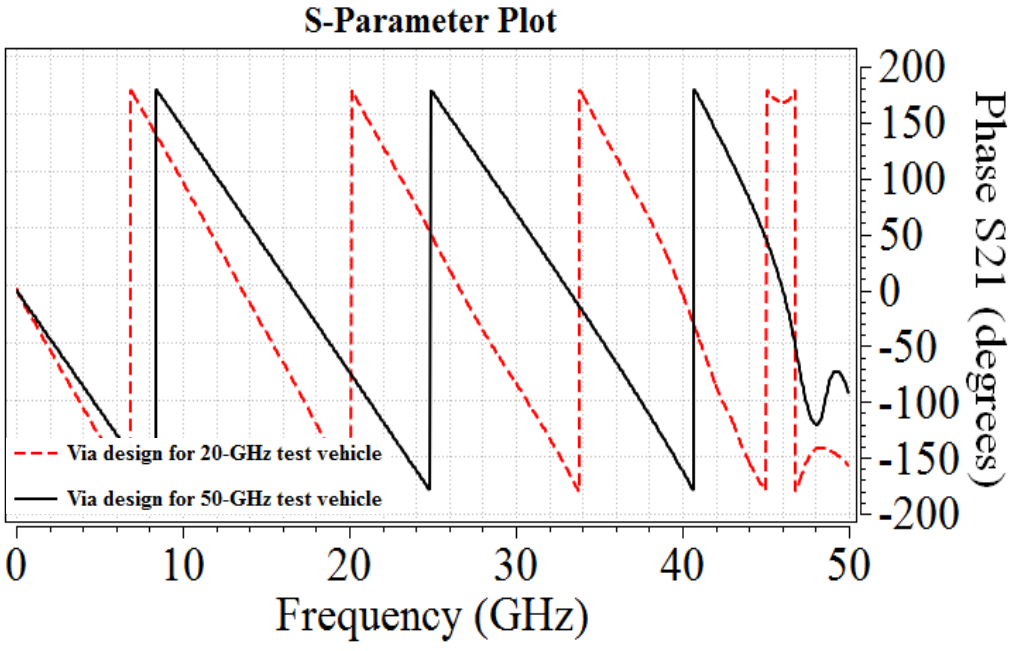


a)

Figure 3.21 Comparison of the current via design and new via design, simulated in CST. a) Magnitude of S_{11}. b) Magnitude of S_{21}. c) Phase of S_{21}



b)



c)

Figure 3.21 Comparison of the current via design and new via design, simulated in CST. a) Magnitude of S_{11}. b) Magnitude of S_{21}. c) Phase of S_{21} (cont.)

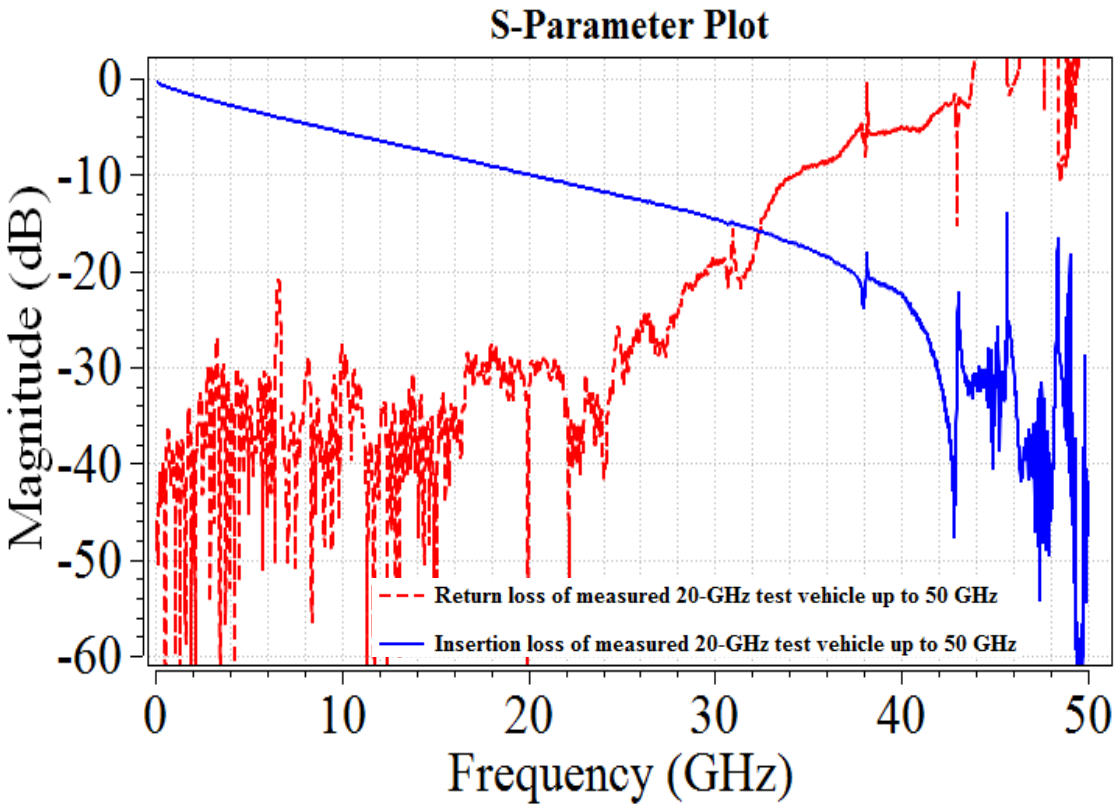


Figure 3.22 Return loss (red) and insertion loss (blue) extracted from S-parameter measurements of a test vehicle with 16'' trace under test applying 3.5mm SMA connectors

The final version of the via design, presented in Figure 3.18 (b), has been developed for measuring PCB test vehicles up to 50 GHz. Taking into account the CST simulated results, comparison of the models, and via analysis, fully detailed in the current Section, the decision to use the proposed via structure in the future PCB design for dielectric material characterization has been made. The new via design will allow for measuring dielectric properties of PCB laminates at least up to 45 GHz, with the further extrapolation of the measured results up to 50 GHz and potentially even higher.

3.2.2. Connector Replacement. The current project requires measuring S-parameters on many PCB test vehicles with different dielectrics. Connectors are used between a test vehicle and cables attached to the measuring equipment, such as a VNA or a TDR. There are 13 connectors to be mounted on each test vehicle to make dielectric measurements. If the set of connectors could not be reused after measuring one board, the cost of measurements would significantly increase. Therefore surface mount SMA connectors are used, and they can be used many times on different boards.

For measurements with the currently used test vehicles up to 20 GHz, Molex SMA 3.5-mm connectors (part number is 0732511851) are used. Technical drawings and specifications can be found in [14]. There are only a few requirements for proper usage of the SMA connectors. The first one is to secure the connector to a board by threading two 0-80 screws from the bottom side of the board through the connector holes. Screws must not broken or twisted. Another requirement is the suitable PCB launch structure. In Section 3.2a, the details about the launch structure are given.

The cut-off frequency for the currently used 3.5 mm SMA connectors is 26.5 GHz, which is not sufficient for measuring the test vehicles up to 50 GHz. Figure 3.22 illustrates this.

For measuring dielectric properties on the PCB test vehicles up to 50 GHz, different types of connectors from the same surface mounted connector family have been found. These are the 2.4-mm SMA connectors from SV Microwave (part number is SF 1621-60003), which have the cut-off frequency of 50 GHz. The technical drawing and specifications of the new 2.4-mm SMA connectors are presented in Appendix E. There is some difference in the connector geometry, but the 2.4-mm connectors still allow for

using the same PCB layout and launch structure as with the 3.5-mm connectors. The currently used via model was designed up to 26 GHz. It was tested with the new 2.4-mm SMA connectors in the measurements performed up to 50 GHz. S-parameters were measured using the same test vehicle, but with two different connector types. Figure 3.22 presents measurement results for the test board with the 3.5-mm SMA connectors, and Figure 3.23 shows the results for the same PCB, but with the 2.4-mm SMA connectors.

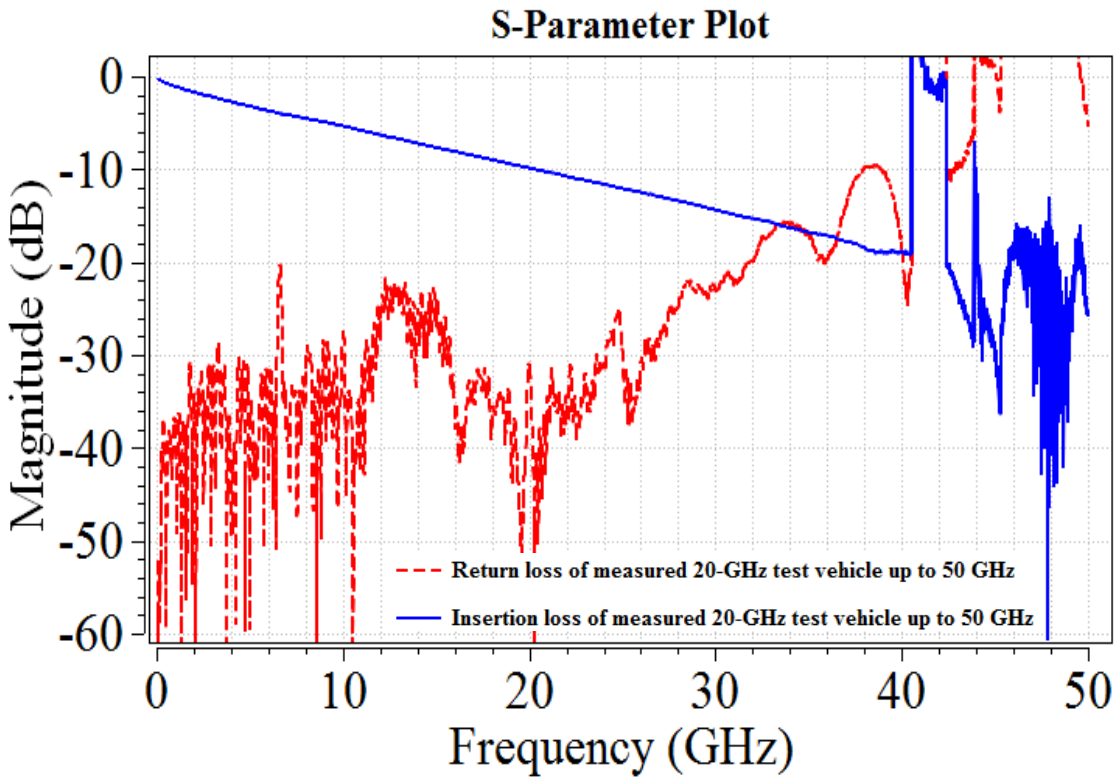


Figure 3.23 Results of measuring PCB with 2.4 mm SMA connectors applied

The return loss (red line) in Figure 3.23, has been improved in frequency range from 32 GHz to 40 GHz, as compared to the return loss shown in Figure 3.22. However,

the main source of trouble at the higher frequencies remains: this is the via design, which is applicable only up to 26 GHz.

The main requirement for having acceptable measurements up to 50 GHz using the 2.4-mm SMA connectors is to have via structure designed for frequency range up to 50 GHz as well. In Section 3.2.1, such via design has been proposed.

3.2.3. Modification In TRL Calibration Patterns. Measurements of S-parameters have been done using the 50-GHz Agilent VNA. There are systematic and random measurement errors in measurements using a VNA, and there also could be a zero drift error. Some artifacts in PCB test vehicle manufacturing, which may affect measurements accuracy and repeatability as well. To reduce measurement errors associated with ports, the possibility of the TRL calibration technique has been included in the PCB design. The test vehicles have the TRL calibration patterns designed for frequency range from 50 MHz to 50 GHz, as is described in [8].

In the currently used (20-GHz) test vehicle there are six auxiliary lines for the TRL calibration. Four lines of different lengths are responsible for the 'Line' standard. There is also one 'Thru', and one 'Reflect' standard.

However, for the new 50-GHz PCB test vehicle design, the TRL calibration pattern will be modified.

Instead of four, there will be five auxiliary lines of different lengths, corresponding to the new frequency breakpoints. The 'Thru' standard and the 'Open' standard will have the same length and frequency ranges as before. The new TRL calibration pattern has been designed according to the same design steps as in [8], but the calculation procedure has been improved. The design algorithm based on the generalized

formulas has been implemented in the new Matlab GUI, which is easy to use for the entire TRL calibration pattern design process.

The TRL calibration pattern design for the new PCB test vehicle contains three stages. At the first stage, the entire frequency range is divided into five segments. The start and stop frequencies are predetermined, they are 0.05 GHz and 50 GHz, respectively. The optimal frequency breakpoints are the geometrical mean values, which satisfy the following equation [8]

$$f_i = \sqrt{f_{i-1} \cdot f_{i+1}} \tag{3.1}$$

But the initial data contains $f_1 = 0.05\ GHz$ and $f_n = 50\ GHz$, where n is the number corresponding to the stop frequency, and for the case of the five TRL calibration lines, n=6. Then, the formula for calculating breakpoints can be generalized as

$$f_{i+1} = f_i^{\frac{n-i-1}{n-i}} \cdot f_n^{\frac{1}{n-i}} \tag{3.2}$$

Thus, for calculating all the frequency breakpoints, one needs to know only the start and stop frequencies. This formula has been implemented in the Matlab GUI, which will be described below.

The second stage of the TRL pattern design is calculating the S_{21} phase difference between the 'Thru' and 'Line' standards. It must be between (20° and 160°) $\pm n \times 180°$ for

a quarter wave length [8]. The S_{21} phase difference must be calculated two times for each line.

$$P_{start_i} = \frac{360^o \cdot f_i \cdot \lambda_q}{c/\sqrt{\varepsilon_r}} = \frac{180^o \cdot f_i}{f_i + f_{i+1}}$$
$$P_{stop_i} = \frac{360^o \cdot f_{i+1} \cdot \lambda_q}{c/\sqrt{\varepsilon_r}} = \frac{180^o \cdot f_{i+1}}{f_i + f_{i+1}} \quad (3.3)$$

Where,

$$\lambda_q = \frac{1}{4} \cdot \frac{c/\sqrt{\varepsilon_r}}{(f_i + f_{i+1})/2} = \frac{c}{2\sqrt{\varepsilon_r}(f_i + f_{i+1})} \quad (3.4)$$

Two formulas for calculating the S_{21} phase difference have been implemented in the Matlab GUI as well. These calculated phase differences must be between 20° and 160°.

The final stage of the TRL calibration procedure, according to [8], is to calculate the length of the pattern lines. The 'Open' standard can be easily calculated knowing the length of the 'Thru' standard as $O = \frac{T}{2}$. Length calculation for the 'Line' standards is more complicated.

Since the difference between 'Line' and 'Thru' must be equal to the quarter wavelength in the PCB dielectric, then the implemented formula in Matlab GUI for the length in mils of each TRL calibration pattern line could be derived from $L - T = \lambda_q$ as

$$L_i = T + \frac{c}{2\sqrt{\varepsilon_r}\left(f_i + f_{i+1}\right)} = T + \frac{59055.12 \cdot 10^8}{\sqrt{\varepsilon_r}\left(f_i + f_{i+1}\right)} \text{ [mils]} \quad (3.5)$$

,

where $c = 118110.23 \cdot 10^8 \frac{mil}{\sec}$, T indicates the length in mils of the 'Thru' standard known from the initial data, and frequency is in Hz. The input data are the length of the 'Thru' line, the number of the desirable lines on the PCB test vehicle, the start and stop frequencies, and also an estimate value for the relative permittivity, ε_r of the material under test. However, the exact ε_r value of the dielectric is not known, since these are the DK and DF parameters of the laminate which should be determined from the measurements. Since the DK used in calculating the TRL calibration pattern is different from the DK of the actual material, this discrepancy may lead to an uncertainty, which is discussed in Section 2.2.2. It may be reasonable to develop several different PCB layouts with different lengths of the TRL calibration patterns, depending on the expected DK value, and then use the PCB layout, in which the TRL design permittivity is closest to the expected value of DK for the dielectric under test. However, this may be costly. In the current project, the deviation of DK values from board to board is not very significant (the range is from 3.8 - 4.2), so the DK=4.0 was used. The PCB laminate dielectrics, whose DK and DF should be measured up to 50 GHz, will be then used in the high-speed digital design up to 50 GHz. These dielectrics are expected to have lower DK and DF values compared to those used in the 20-GHz designs. Hence, in the new test vehicles for measurements up to 50 GHz, the TRL calibration pattern will be designed with the DK value as low as 3.5, and the same DK=3.5 was used in full-wave CST

simulations of via structures. The algorithm for calculating TRL calibration patterns implemented in Matlab GUI is presented in Figure 3.24.

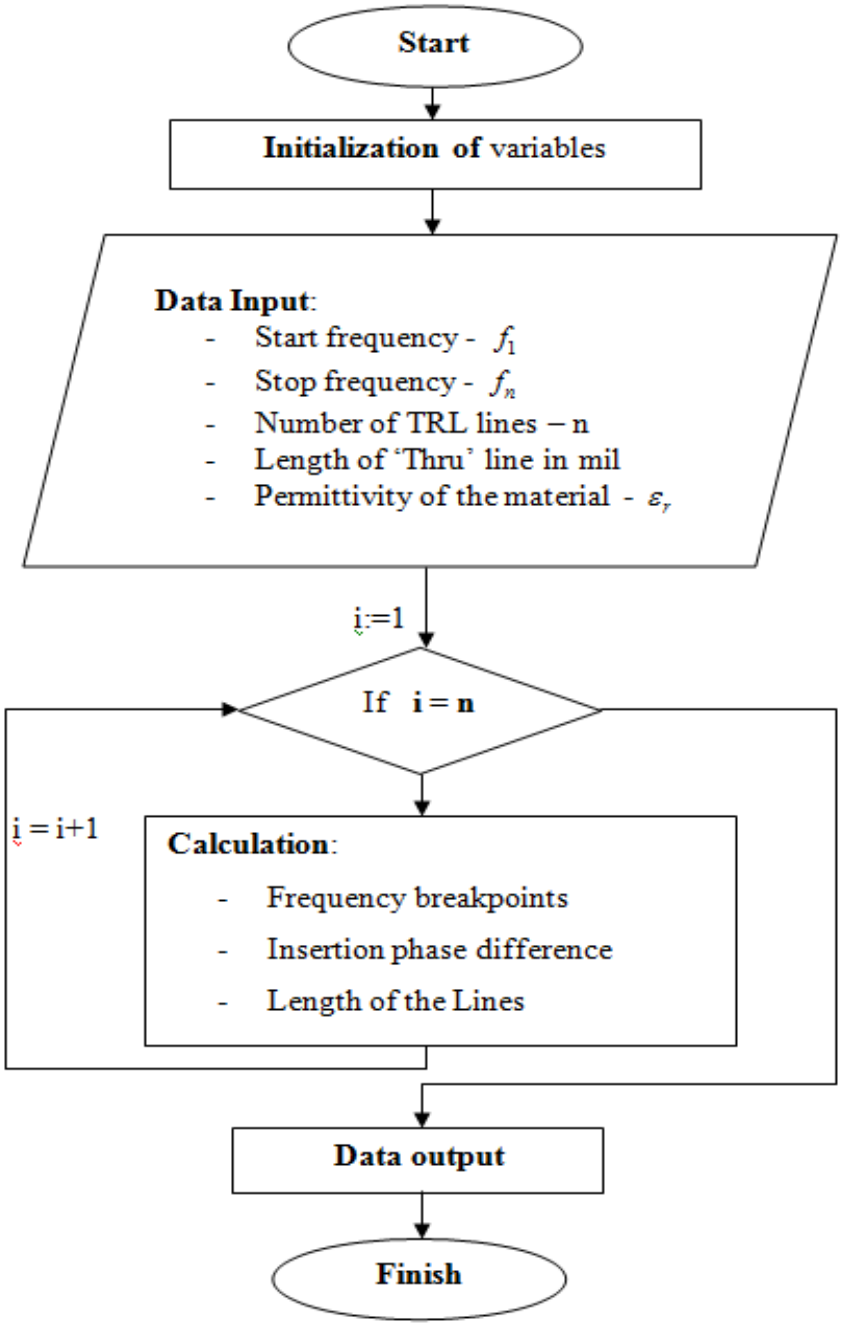
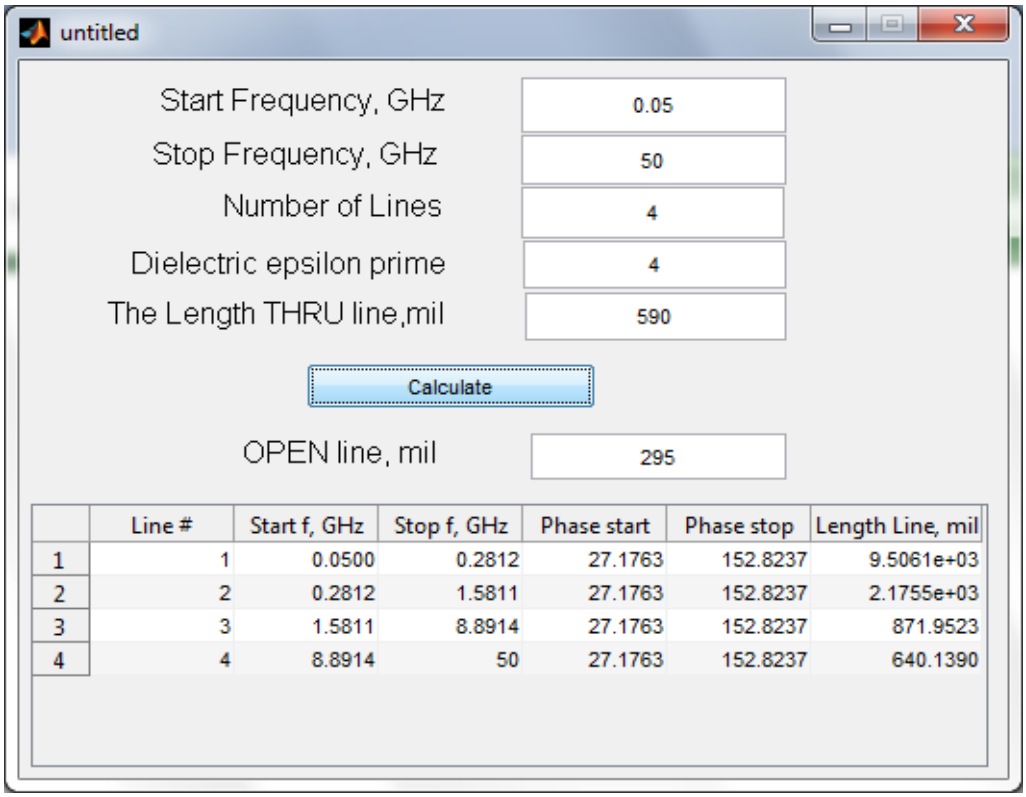


Figure 3.24 Algorithm of the Matlab GUI for calculating TRL calibration patterns

After developing the tool to calculate TRL calibration patterns, the functionality of the tool has been checked by using the data from TRL calibration pattern design for the current (20-GHz) test vehicles. The results, shown in Figure 3.25, agree well with the data published in [8] and shown in Figure 3.26.



	Line #	Start f, GHz	Stop f, GHz	Phase start	Phase stop	Length Line, mil
1	1	0.0500	0.2812	27.1763	152.8237	9.5061e+03
2	2	0.2812	1.5811	27.1763	152.8237	2.1755e+03
3	3	1.5811	8.8914	27.1763	152.8237	871.9523
4	4	8.8914	50	27.1763	152.8237	640.1390

Figure 3.25 Results for calculating TRL calibration patterns for current PCB design using Matlab GUI

It should be mentioned that, in [8], an error in Line 1 length calculations has been noticed: the length of the Through Line has been missed in calculating the length of the Line 1. The tool developed herein corrects this mistake.

For the new developed TRL calibration pattern, it was decided to use the same line length for the ‘Thru’ and ‘Open’ lines as in the previous, 20-GHz, design, and to

leave the same frequency range, while the number of lines has increased from 4 to 5, and permittivity of the dielectric has decreased from 4 to 3.5. The results of the calculations are presented on Figure 3.27.

Length of the TRL calibration patterns

T1 (mils)	O1 (mils)	L1 (mils)	L2(mils)	L3 (mils)	L4 (mils)
590	295	8916.1	2175.535	871.94	640.11

Frequency breakpoints

Line	Start Frequency (MHz)	Stop Frequency (MHz)
Line 1	50	281.17
Line 2	281.17	1581
Line 3	1581	8891
Line 4	8891	50000

Insertion phase difference

$$P_{11} = \frac{180^0 \times 0.05}{0.05 + 0.28117} = 27.17^0$$

$$P_{12} = \frac{180^0 \times 0.28117}{0.05 + 0.28117} = 152.82^0$$

$$P_{21} = \frac{180^0 \times 0.28117}{0.28117 + 1.581} = 27.19^0$$

$$P_{22} = \frac{180^0 \times 1.581}{0.28117 + 1.581} = 152.9^0$$

$$P_{31} = \frac{180^0 \times 1.581}{1.581 + 8.891} = 27.1^0$$

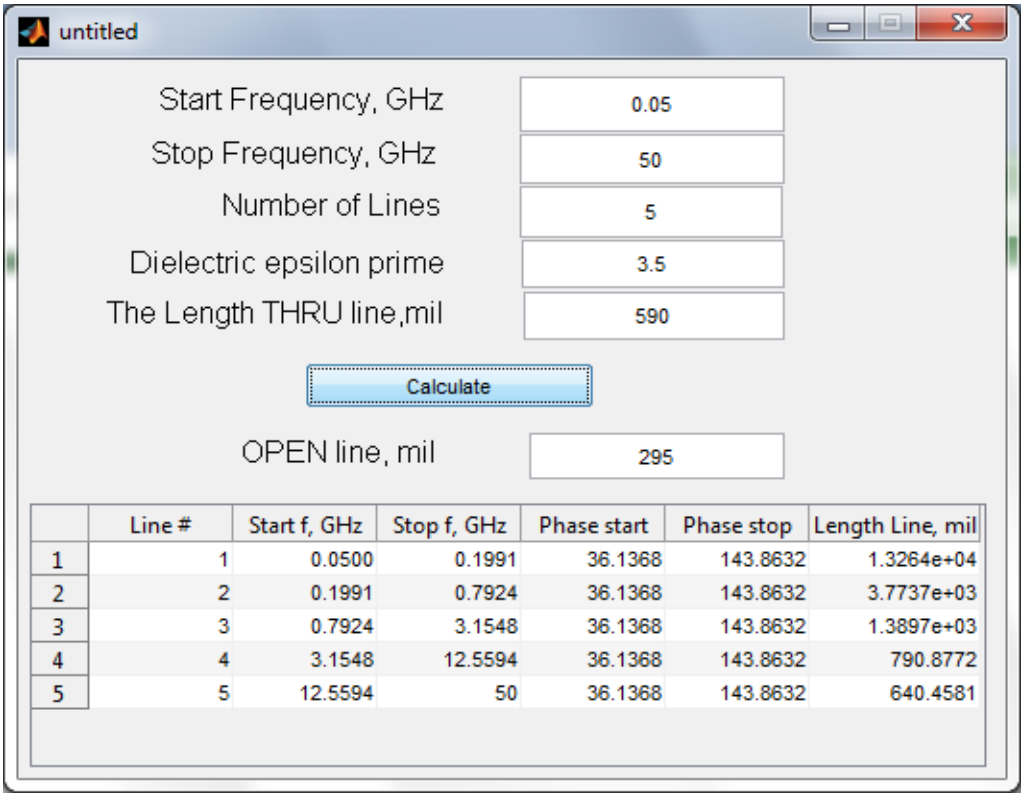
$$P_{32} = \frac{180^0 \times 8.891}{1.581 + 8.891} = 152.82^0$$

$$P_{33} = \frac{180^0 \times 8.891}{8.891 + 50} = 27.17^0$$

$$P_{41} = \frac{180^0 \times 50}{8.891 + 50} = 152.82^0$$

Figure 3.26 Results of the TRL patterns calculation for current PCB design

The new TRL calibration pattern will have five ‘Line’ standards, one ‘Thru’ standard, and one ‘Open’ standard. The summary of the TRL patterns characteristics is presented in Table 3.3.



	Line #	Start f, GHz	Stop f, GHz	Phase start	Phase stop	Length Line, mil
1	1	0.0500	0.1991	36.1368	143.8632	1.3264e+04
2	2	0.1991	0.7924	36.1368	143.8632	3.7737e+03
3	3	0.7924	3.1548	36.1368	143.8632	1.3897e+03
4	4	3.1548	12.5594	36.1368	143.8632	790.8772
5	5	12.5594	50	36.1368	143.8632	640.4581

Figure 3.27 Results for calculating TRL calibration patterns for current PCB design using Matlab GUI

Table 3.3 Summary of the TRL calibration pattern characteristics for the new developed test vehicle

Pattern	**Line length, mil**	**Start frequency, GHz**	**Stop frequency, GHz**
Line 1	13264	0.05	0.20
Line 2	3773.7	0.20	0.79
Line 3	1389.7	0.79	3.15
Line 4	790.9	3.15	12.56
Line 5	640.5	12.56	50
Thru	590	0.05	50
Open	295	0.05	50

3.2.4. Correction In Via Wall Design. Ground stitching via wall is the most disputable issue in the current test vehicle design. There are many pros and cons of using via wall. Usually, it has been used to maintain low impedance and short current return path. The main reason why the via walls are currently present on test boards is to provide the short return path. This is discussed in [8] and [15].

All the currently used 20-GHz test vehicles have via wall with an inch spacing between vias. The presence of the via wall does not have any negative impact on measurement results unless a very low loss material is tested. Having a low loss material means that a signal propagates through the trace with less attenuation, and its magnitude is higher than it would be in a more lossy medium. As is explained in Section 2.2.4, there may be artifacts due to the via wall. An unwanted equidistant resonance with the periodicity around 3 GHz is clearly seen in Figure 2.15. The corresponding resonating structure on the test board, is one inch long, which is the spacing between vias. Assuming that the DK of the laminate dielectric is 3.8, this 1-inch distance along the line corresponds to approximately 3.0 GHz periodicity. This can be calculated using a simplified formula for estimating the resonance frequency

$$f_0 = \frac{1}{2}\frac{1}{\sqrt{\varepsilon_r}}\frac{c}{L}, \tag{3.6}$$

where c is a speed of light, and L is a length of the resonating structure.

In future, the PCB test vehicles, similar to those developed in this work, should be employed for characterization of super low loss dielectric materials. Therefore, it is very

important to develop a new test vehicle design free from the via wall artifacts. There are a few ways to avoid undesirable resonances.

The first way is to decrease the spacing between stitching vias in order to push unwanted resonances above 50 GHz. Then, according to the above formula (3.6), the length of the structure should be decreased by the factor of four to five. However, intensity of unwanted resonances will increase as the spacing between ground vias decreases. This is undesirable, and hence an alternative way of eliminating unwanted resonances should be considered.

This second alternative approach is to violate periodicity, *i.e.*, place vias in an aperiodic order, even along the same line. This would still create a resonating structure, but the resonances will decrease compared to the case with the periodic structure. The random distribution of the via could be applied for placing the via wall on the board.

Finally, the third way to avoid unwanted resonances due to the via wall is not to put any via walls on the board. Since measurements have been done on the single-ended stripline traces, the absence of the via walls should not affect measurement results. Stitching ground vias would be important for differential pair measurements only. Moreover, in stripline structures over the gigahertz frequency range, the electromagnetic energy is concentrated and canalized around the signal trace, so the presence of the stitching ground vias at the distance of a few widths of the trace does not affect signal propagation along the line, and thus these via walls are excessive.

To compare the effectiveness of the second and third method with the currently existing periodic structure of the via wall, the full-wave numerical simulations using the CST Microwave Studio software have been done. For the aperiodic via structure, the

random Gaussian distribution with mean value equal to 0.5 inches and standard deviation of 0.2 inches was accomplished. In the CST models, the fine structures of the connectors and vias have not been taken into account. Only 16- inch long stripline trace with the existing PCB stack-up geometry, and the via wall structure have been simulated. The results presented on Figure 3.28 show the difference in the proposed methods of the via wall resonant structure elimination. The green line indicates the model without any vias along the stripline. There are no resonances present. The red curve with significant resonances corresponds to the periodic via wall structure implemented in the current 20-GHz test vehicle PCB design. Compared to the level of resonances in the red color (the periodic via structure), the unwanted resonances in the blue color (an aperiodic via wall structure), are significantly less (by at least 5 dB). This means that both the aperiodic wall and absence of the wall will allow for getting rid of the via wall artifact.

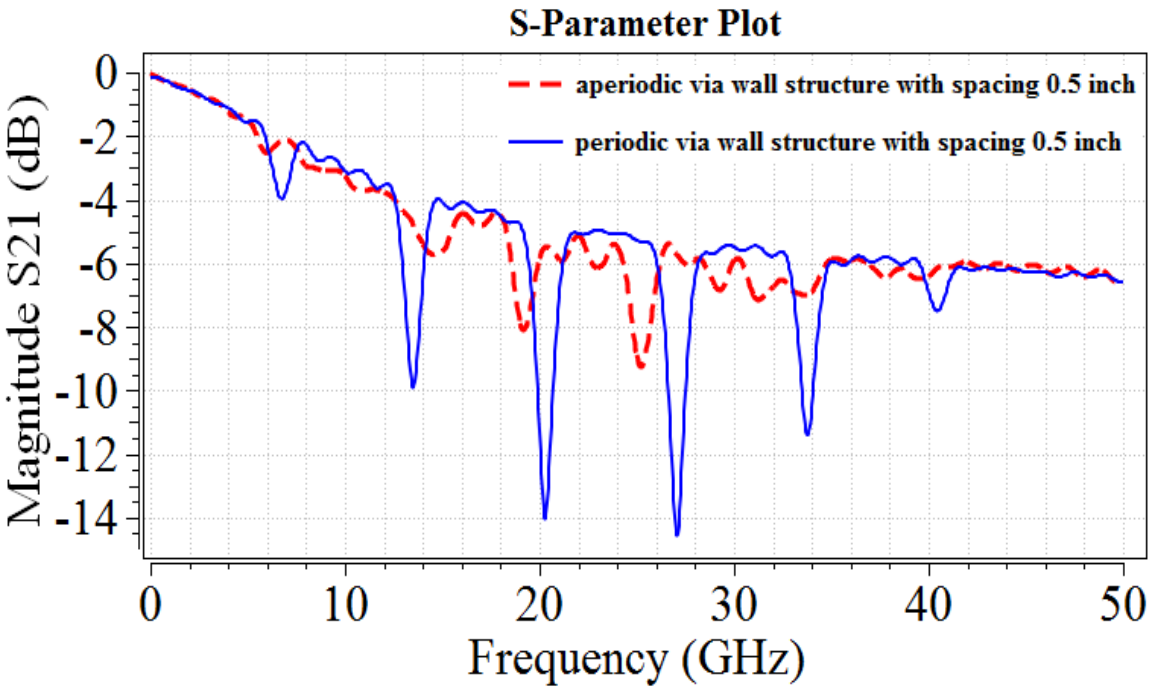


Figure 3.28 Simulated results of the via wall artifact

The decision to use both methods in a new first test vehicle design has been made. To understand the difference in performing S-parameter measurement technique, two sets of boards with the same material and geometry, but with the different via wall method applied will be manufactured. The final decision of which via wall model to implement in all future test vehicles will be made after obtaining S-parameters from the measurements.

3.3. SUMMARY OF MODIFICATIONS FOR 50-GHZ TEST VEHICLE

Currently, PCB laminate dielectric characterization can be performed only up to 20 GHz using the PCB test vehicles with the existing design.

However, nowadays it has become important to investigate the behavior of dielectric constant and dissipation factor of PCB laminate dielectrics over the wider frequency range, at least up to 45-50 GHz. New dielectrics which will be used for high-speed digital designs up to 50 GHz are less lossy than their 20-GHz counterparts, and the dielectric constants of these materials are consequently lower. These factors lead to the new goals. It is important improve the current PCB test vehicle design significantly to allow for measurements up to 50 GHz. In addition to using the traveling wave method for PCB laminate dielectric characterization, it has been decided to apply alternative measurement techniques. These are the resonance techniques based on the split-post dielectric resonator (SPDR) and split cylindrical resonators (SCR). These resonator techniques use the different measuring concept, and they allow for only narrow-band measurements of the DK and DF of non-metalized dielectric thin plates. These two techniques may be used to verify results obtained from measuring S-parameters using the

traveling wave method, though the measurement results may deviate within some limits due to the dielectric anisotropy of test samples.

The SPDR measuring approach will be explained in Section 4.

For completing the development of the new test vehicle layout, the comparison between new 50-GHz test vehicle design and current 20-GHz test vehicle design is presented in Table 3.4.

Table 3.4 Comparison overview of current and new test vehicle designs

Part of the PCB model	**Current design up to 20 GHz**	**New design up to 50 GHz**
Geometry of the board	Same	Same
PCB Stack up		
Differential pair structure		
The length of single-ended stripline traces	Same - 16 inch	Same - 16 inch
Via structure	- Single ring of 8 ground vias around the signal via - 10.8 mil via stub - Cut-off frequency at 26 GHz - Diameter of via pad is 30 mil - Diameter of via antipad is 70 mil - Distance from signal via to ground vias is 50 mil	- Dual ring of 29 ground vias in total - 2 mil via stub - Cut-off freqency at 50 GHz - Diameter of via pad is 20 mil - Diameter of via antipad is 34 mil - Distance from signal via to ground vias are 54 mil and 70 mil
Connectors	Molex 3.5 mm SMA connectors up to 35 GHz	SV Microwave 2.4 mm SMA connectors up to 50 GHz
TRL calibration patters	4 lines, thru and open standards	5 lines, thru and open standards
Via wall	Periodic structure with 1 inch spacing between vias	- Aperiodic structure with random distribution - No via wall
5 inch and 10 inch striplines	Presented on current test vehicles	Eliminated

The design of the test vehicle used in measurements up to 20 GHz has been overviewed in Section 3.1. In Section 3.2, all possible modifications needed for extending the PCB test vehicle frequency range to 50 GHz have been discussed. The comparison of two designs (20-GHz and 50-GHz) is summarized in Table 3.4. The full list of all changes in the current test vehicle design to achieve the 50-GHz performance is presented in Appendix F.

4. DIELECTRIC MATERIAL CHARACTERIZATION USING SPLIT POST DIELECTRIC RESONATOR (SPDR)

Dielectric properties could be measured using several different methods. The measurement technique described in Sections 2 and 3 can be classified as one of the transmission-reflection methods [16-18]. It has been used in measurements of dielectric properties of PCB laminate dielectrics. The main advantage of this technique is the ability to extract dielectric constant and dissipation factor over a wide frequency range of measurements in every frequency point of the range, over which measurement is done. However, one of the biggest issues with any transmission-reflection method is when it is applied to very low loss materials. To apply transmission-reflection techniques for very low-loss materials, one needs comparatively long transmission lines to accumulate sufficient loss to be measured. If a material has a low dielectric constant, transmission line techniques may be not effective either. Long lines are needed to get a measureable phase progression to obtain the DK value accurately. In this case, another type of measurement technique could be used to obtain accurate results for dielectric parameters. The resonance method is the most effective kind of measurement for very low loss material and it also has high measurement accuracy [16]. The most distinguished difference between this method and traveling wave techniques is that resonance methods are narrowband. This means that a resonance technique could be applied only for one, or maximum, a few discrete frequency points over a range of measurements. To get wideband measurement results, one needs multiple test fixtures designed specifically for a number of desirable frequency points within the frequency range of interest.

Moreover, numerous individual test vehicles with the designed layouts, *e.g.*, which include TRL patterns, should be manufactured. This may be quite expensive.

Both split post dielectric resonator (SPDR) [18] and split cylindrical resonator (SCR) [17] use resonance measurements in the vicinity of a single frequency point. SPDRs and SCRs are supposed to be the alternative methods to extract dielectric parameters or to compare with the results obtained using the traveling wave method. In this Section, the SPDR technique and the SPDR measurement procedure are explained.

The detailed step-by-step measurement procedure using the SPDR method is described in Appendix G for SPDRs designed for measurements at 10 GHz, 15 GHz, and 20 GHz.

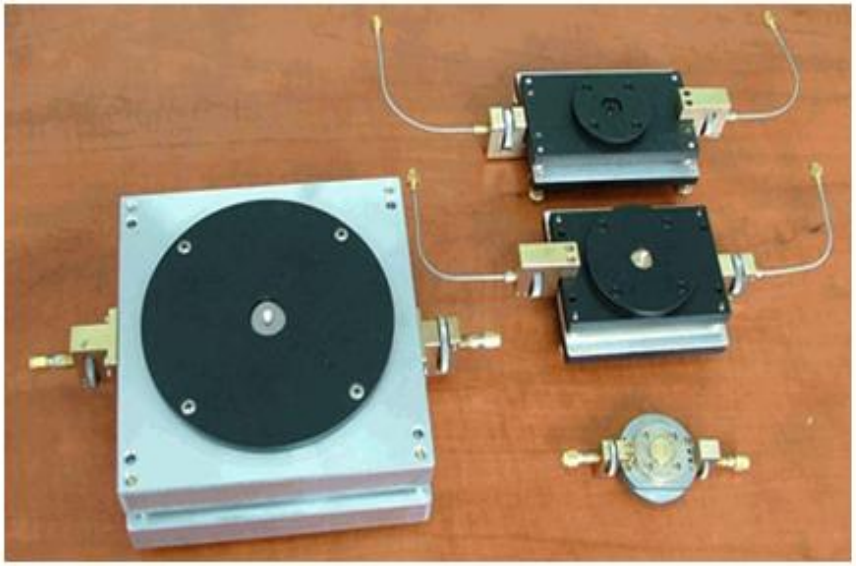
4.1. THEORETICAL OVERVIEW OF THE 'SPLIT POST DIELECTRIC RESONATOR' MEASUREMENT TECHNIQUE

The SPDR method has been developed to measure dielectric parameters on low loss materials. This method is simple and convenient, because it does not need special sample preparation or complicated test vehicle development. However, there are several main requirements for the sample under test.

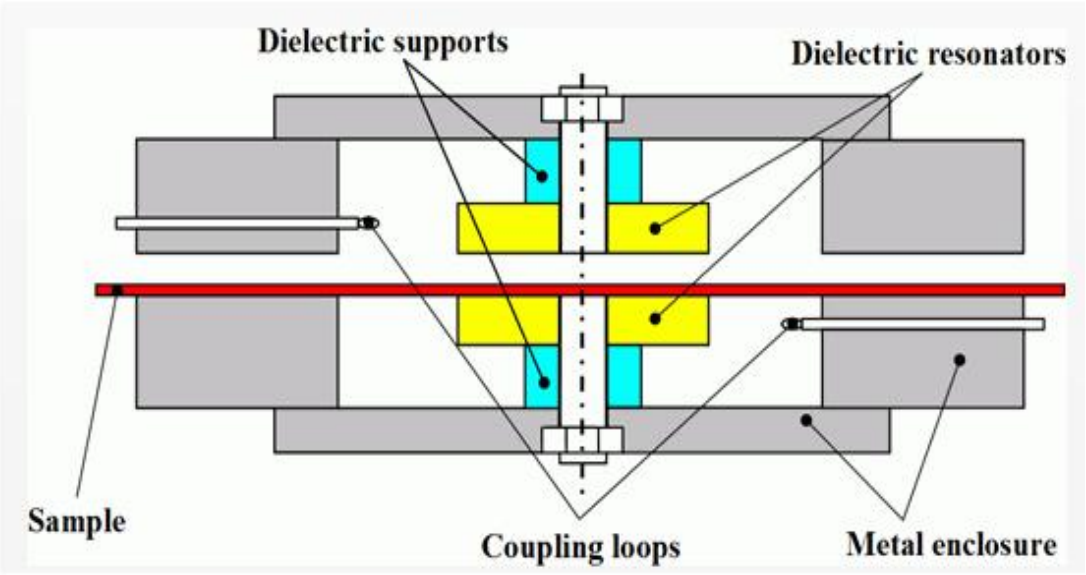
The outlook and the cross-section of the SPDR are presented on Figure 4.1 [19].

An SPDR operates with the $TE_{01\delta}$, which has the only azimuthal component. This means that the electric field in the resonator is parallel to the surface of the sample. In this case, the sample must have a flat surface and constant thickness across the entire sample. For making measurements, the sample should be placed in the gap between two dielectric resonators, shown in Figure 4.1 (b). The spacing between those two dielectric resonators and the sizes of resonators are fixed. That means the dimension of the sample depends on the dimensions of the resonator. The approximate sample dimensions are given in Table 4.1 [19]. Those sample sizes have been suggested by the main SPDR manufacturer, the

Polish company QWED [19]. However, SPDR sizes could vary depending on the manufacturer.



(a)



(b)

Figure 4.1 Split post dielectric resonator (SPDR).
a) Fixture outlook of several SPDR models. b) Cross-section of the resonator [19]

Table 4.1 The minimum sizes of sample according to the operating frequency suggested by QWED [19]

Nominal frequency [GHz]	**Minimum sizes of sample [mm]**	**Maximum thickness of sample [mm]**
1.1	120x120	6.0
1.9	70x70	4.0
3.2	50x50	3.0
5 ÷ 6	30x30	2.0
9 ÷ 10	22x22	1.0
13 ÷ 16	15x15	0.6
18 ÷ 20	10x10	0.5

The resonance method of dielectric characterization using an SPDR is described in detail in [16]-[19]. The resonance frequency, unloaded SPDR Q-factor, and other parameters of the SPDR have been obtained using Rayleigh-Ritz method. The goal of the measurements is to provide all needed parameters for computing dielectric parameters. Figure 4.2 presents the summary of the measurement procedure from the first step of the sample thickness measurement till getting the measurement results. Parameters obtained from each step are used in the extraction of dielectric parameters.

The SPDR technique, like many resonance techniques, uses the shift of the resonance frequency and the effect of resonance amplitude decrease ("de-Q-ing effect") due to the loading the dielectric sample under test, in the empty resonator.

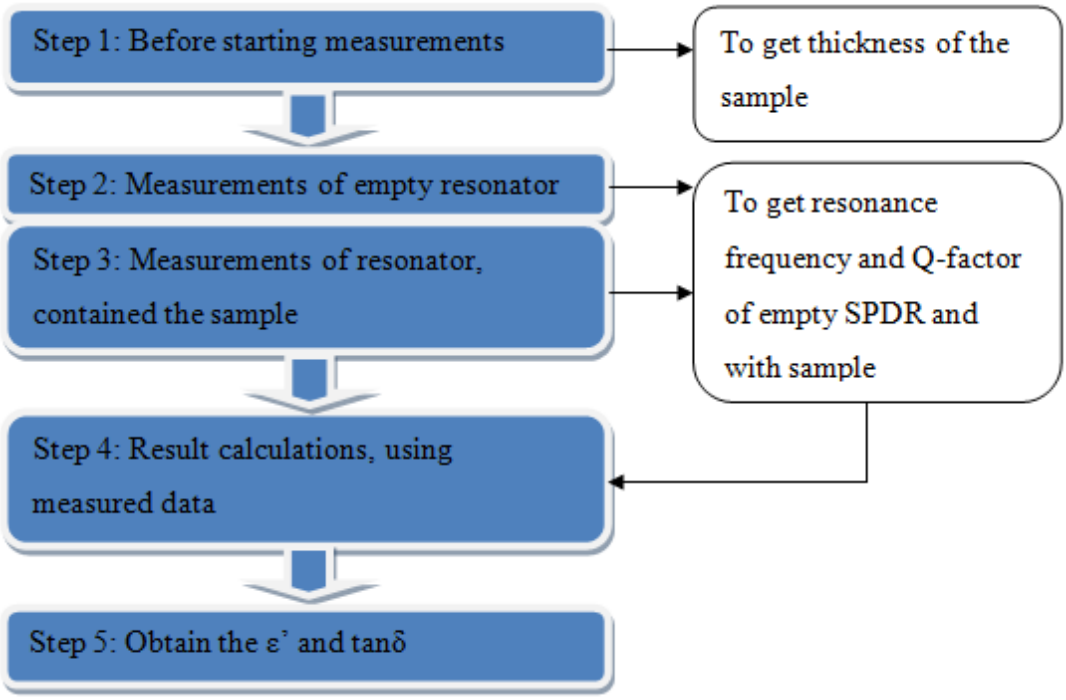


Figure 4.2 The procedure of measurements and computing data

According to the theory published in [16]-[19], calculations of the dielectric constant and loss tangent are done using the following expressions:

$$DK = \varepsilon'_r = \frac{1 + f_0 - f_s}{h f_0 K_s\left(\varepsilon'_r, h\right)}, \tag{4.1}$$

$$DF = \tan\delta = \frac{Q^{-1} - Q^{-1}{}_{DR} - Q^{-1}{}_{C}}{p_{es}}, \tag{4.2}$$

where h is the thickness of the sample, f_0 is the resonance frequency of the empty SPDR, and f_s is the resonance frequency of the SPDR with a dielectric sample inside. These parameters are directly measured. Q is the unloaded quality factor of the resonant fixture containing the dielectric sample. Q_C is the quality factor of the empty resonator,

and Q_{DR} is the quality factor of the resonator loaded with dielectric sample. These quality factors are also measured, and then they are used in the formula for a loss tangent.

Q_C is a Q-factor dependent on metal loss for the SPDR and could be derived as a product of a Q-factor dependent on metal loss for empty SPDR - Q_{c0}, and the function $K_2\left(\varepsilon'_r, h\right)$.

$$Q_c = \frac{\iiint \mu_0 H H^* dv}{R_S \oiint H_t H_t^* ds} = Q_{C0} K_2(\varepsilon'_r, h) \tag{4.3}$$

Q_{DR} is a Q-factor dependent on dielectric losses in the sample in the SPDR. For deriving this parameter Q_{DR0}, which is a Q-factor dependent on dielectric losses for the empty SPDR, one should know the resonance frequencies of SPDR with the dielectric sample, and without it.

$$Q_{DR} = Q_{DR0} \frac{f_0}{f_s} \frac{p_{eDR0}}{p_{eDR}} \tag{4.4}$$

The loss tangent is also dependent on the parameter, p_{es}, which is associated with the electric energy filling factor of the sample. This parameter, p_{es}, is the function of the dielectric permittivity, ε'_r, and the sample thickness, h.

$$p_{es} = \frac{W_{es}}{W_{et}} = \frac{\iiint_{V_s} \varepsilon_s EE^* dv}{\iiint_{V_s} \varepsilon(v) EE^* dv} = h\varepsilon'_r K_1\left(\varepsilon'_r, h\right) \tag{4.5}$$

The parameters p_{eDR} and p_{eDR0} are electric energy filling factors for the sample and for the dielectric split resonator, respectively. Similar to K_s, K_1, and K_2 are functions of ε'_r and h, which are computed using interpolation and tabulated for specific values of ε'_r and h, [16]-[18].

These derivations are implemented in the commercial software from QWED [19], which has been used in this work for extracting dielectric parameters from SPDR measurements. Using the software from QWED for each specific SPDR, the dielectric parameters are extracted. The operator only has to use the measured thickness of the sample, Q-factor, and the resonance frequency of the empty resonator and of the resonator loaded with sample as input data. The output data contains dielectric parameters DK and DF. The interface of the QWED software for 20-GHz SPDR is presented in Figure 4.3, as an example.

The QWED tool description, the manual, and how to do the SPDR measurements are presented in Appendix G as a part of the measurement procedure overview.

The only disadvantage of the tool is that it does not allow for the direct computing of measurement uncertainties. Typically, the acceptable measurement uncertainties are in the range of ±(1-1.5) %. In the case of the SPDR measurement, the accuracy range remains the same.

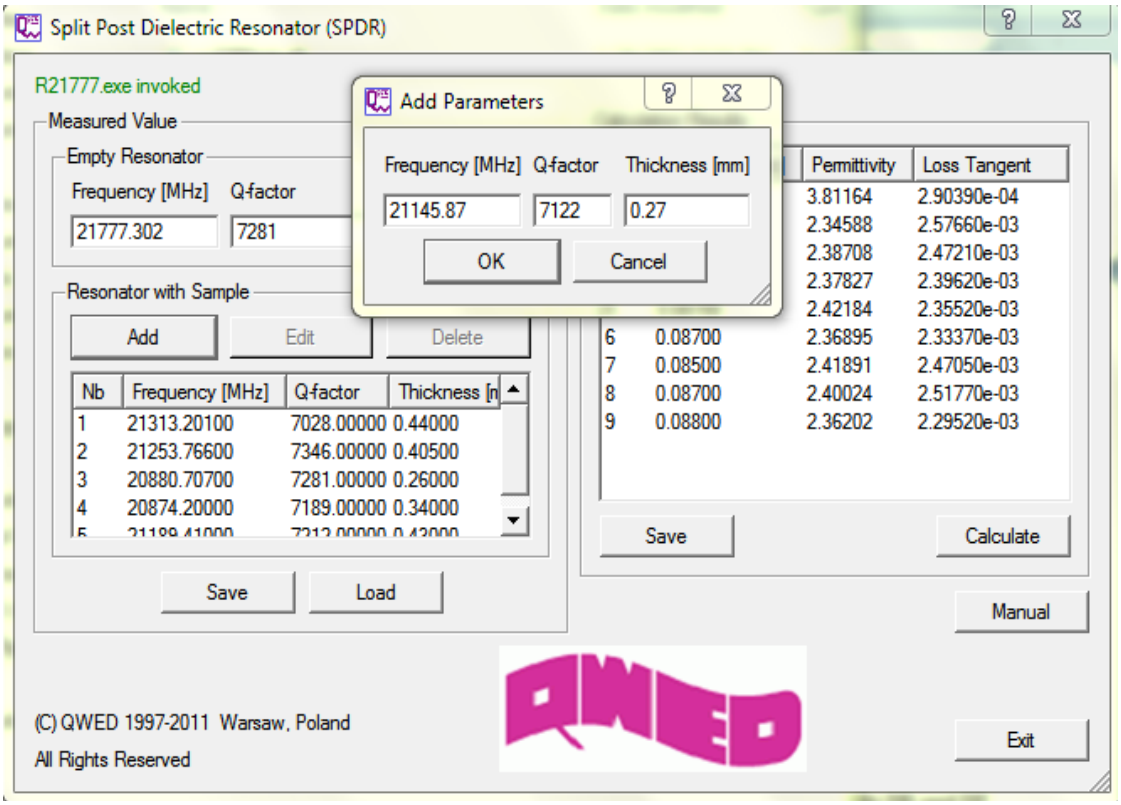


Figure 4.3 Example of computing dielectric parameters using QWED software. Input data presented on the left side of the tool, results of the right side

According to the abovementioned expressions, for the dielectric permittivity, the uncertainties raise up mostly with inaccurate measurement of the sample thickness. The parameter, K_s , has been numerically analyzed in [16] and [18]. It is possible to compute K_s for specific resonant structure with uncertainties better than 0.15 %. (0.0015). This means that the uncertainties of the DK would depend mostly on uncertainties in measuring thickness of the sample as

$$\Delta\varepsilon'_r \le \left(0.0015 + 1 \cdot \frac{\Delta h}{h}\right)\varepsilon'_r \qquad (4.6)$$

An accuracy of the DF measurement depends on many factors. The Q-factor and the electrical energy filling of the sample are the main factors. There is no accurate formula to calculate the uncertainty in the loss tangent. All expressions vary, along with the DK uncertainty. The most common idea is that DF deviates within 3% of the result.

$$\Delta \tan\delta \le 0.03 \cdot \tan\delta . \tag{4.7}$$

Calculation of uncertainties has been published in [16]-[19].Formula (4.6) and (4.7) has not been implemented in QWED software. However the Matlab script for calculating uncertainties has been developed, and it is described in the measurement instructions in Appendix G.

4.2. ANALYSIS OF THE MEASUREMENT PROCEDURE AND RESULTS

Measurement procedure requires using a VNA. An application of the Agilent VNA with 85071E Material Measurement software with option 300 is preferable, since it significantly simplifies the process of computing the extracted dielectric parameters.

A step-by-step measurement procedure is described in Figure 4.4. The more detailed instruction for measurements is presented in Appendix G.

As a first step of the measurement, an operator has to know the thickness of the sample. A micrometer or caliper may be used as a measurement device. In this work, the high-precision digital micrometer, Mitutoyo #227-211, has been used. The most effective method is to measure a sample's thickness in a number of different places, for

example, in five different places across the sample plane, and then to find the average thickness value. The difference in the thickness measurement will be used for calculating measurement uncertainties.

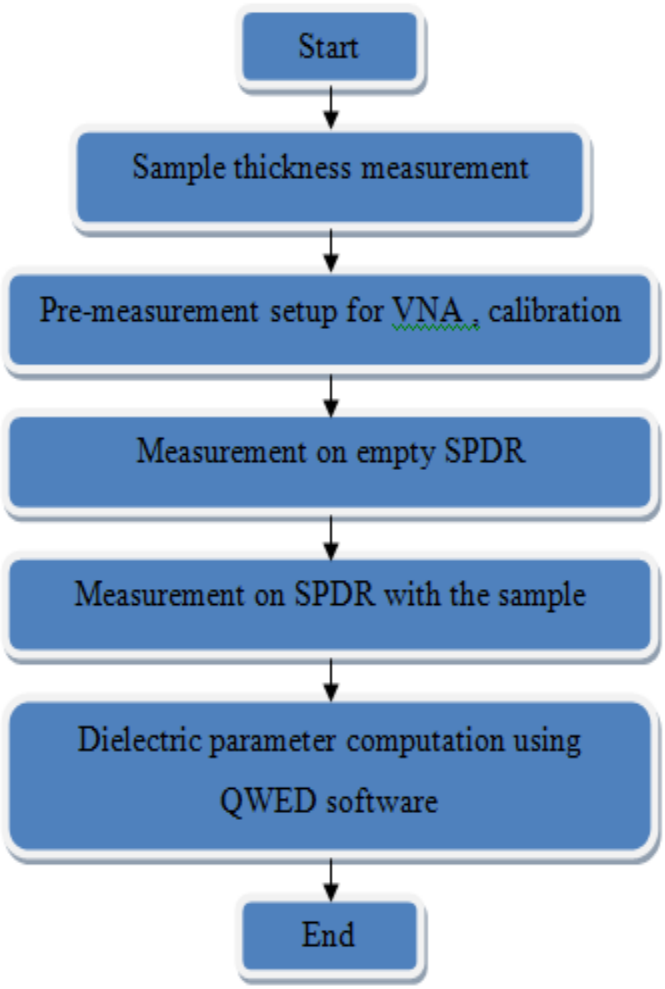


Figure 4.4 Measurement step-by-step procedures

After measuring the thickness of the sample, the VNA calibration should be performed. The E-calibration allows for eliminating the cable effect by setting the

calibration plane at the end of the cable connector. The schematic illustration of the measurement setup is presented in Figure 4.5.

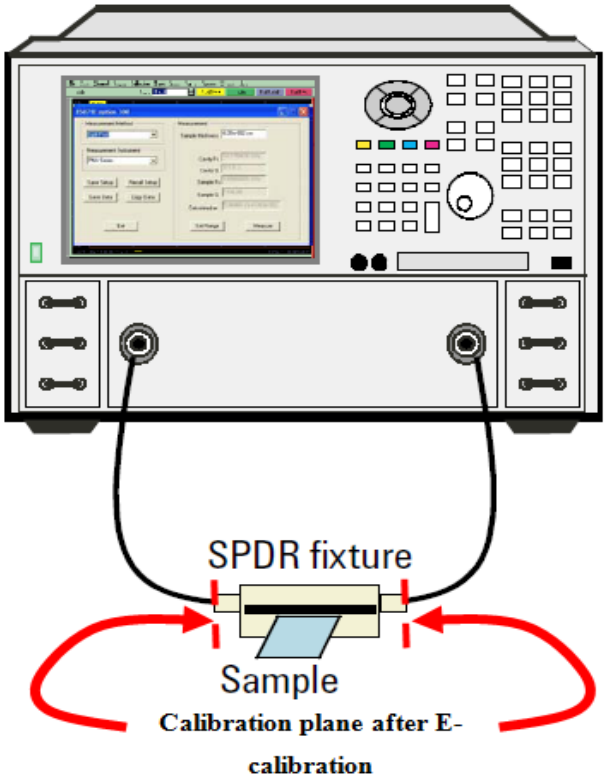


Figure 4.5 The measurement setup [16]

At the next stage, the settings of the SPDR setup must be tuned. The main requirement to the SPDR setup is the achievement of the similarity between the magnitudes of S_{11} and S_{22}. There is only one way of tuning those parameters, which is by adjusting the coupling loops inside the SPDR. The position of the coupling loop at Port 1 inside the SPDR corresponds with the resonance in S_{11}. Similarly, the position of the coupling loop at Port 2 is corresponds with the resonance in S_{22}. Changing the position of the coupling loops can only be done using nuts on both sides of the SPDR, as is indicated on Figure 4.6.

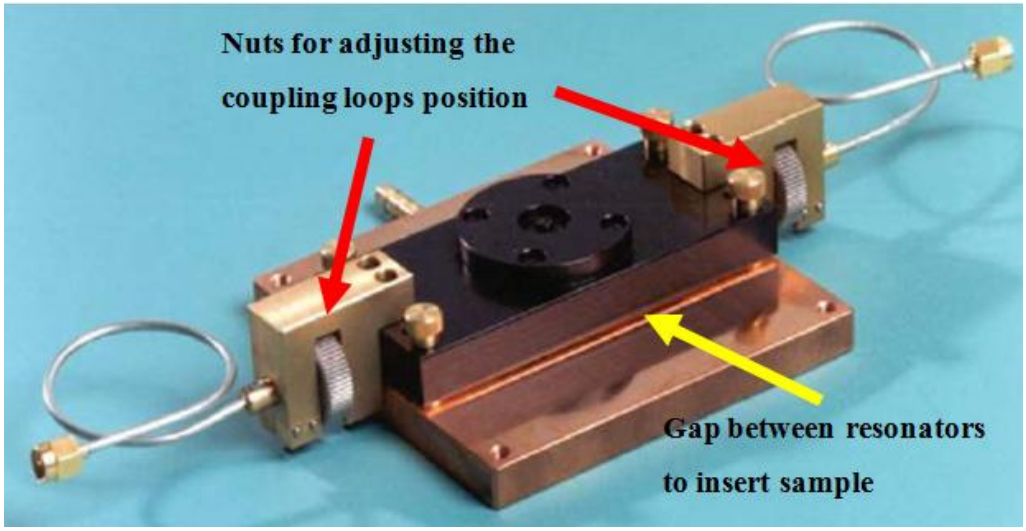
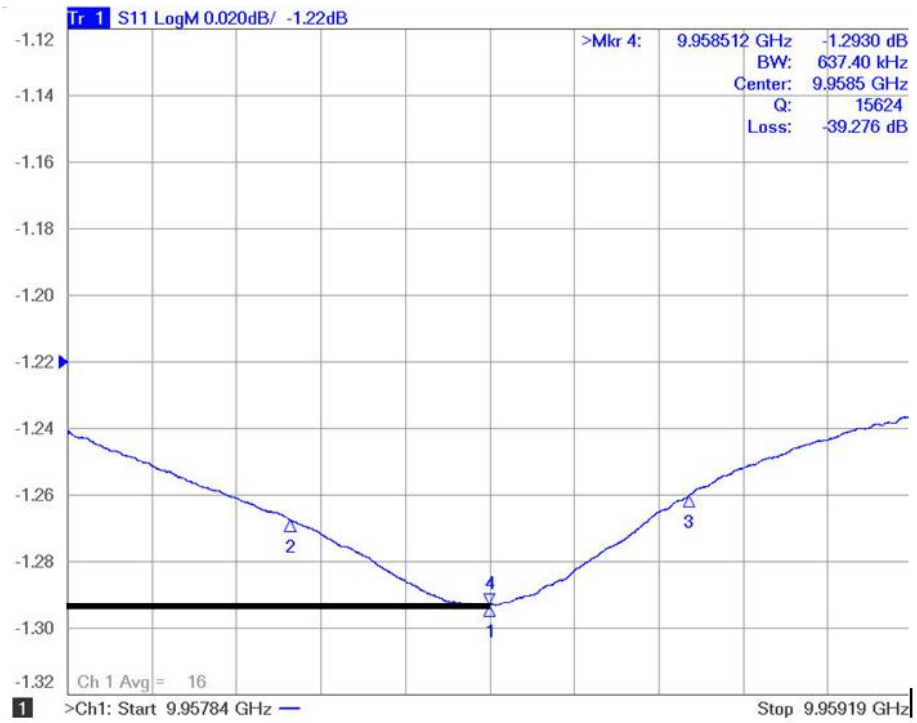


Figure 4.6 Picture of the SPDR fixture [16]

It is easier to change the positions of both coupling loops simultaneously, rather than to try to adjust one nut after fixing position of another nut. An example of a good matching of the minima in the magnitude of S_{11} and of S_{22} for 10-GHz SPDR after the adjustment of the coupling loops is presented in Figure 4.7.

After obtaining the similar values for magnitudes of S_{11} and S_{22}, the maximum magnitude of S_{21} is supposed to be around the level of -40 dB, as is shown in the example in Figure 4.7. Indeed, the resonance frequency of the empty resonator indicated on the curve for the magnitude of S_{21} as f_s, has to be very close to the value of the operating frequency of SPDR. In this case, the SPDR setup will be completed, and measurement may be performed with confidence.

During the measurements, it is very important to remember that the resonators are very sensitive to the environmental temperature and humidity, equipment temperature, and the level of moisture inside the SPDR.



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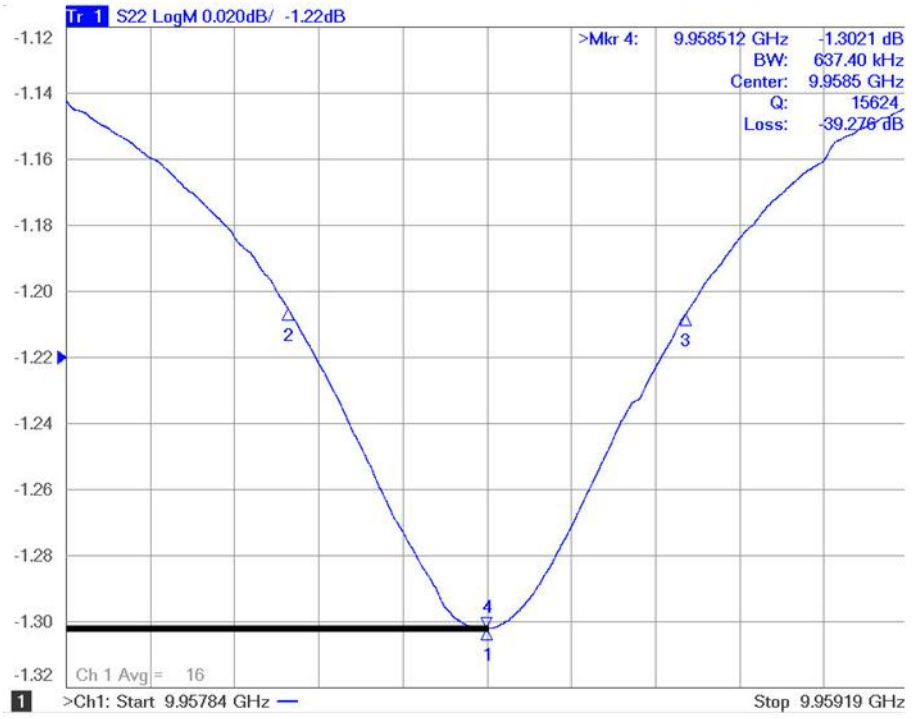
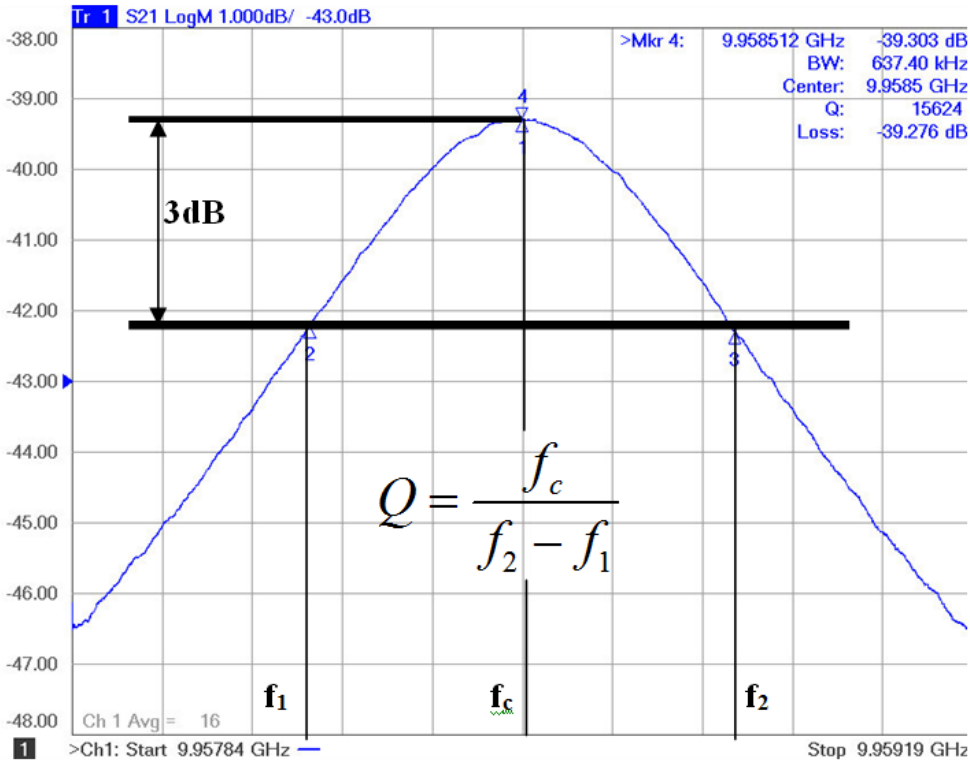


(b)

Figure 4.7 Example of the S-parameters after well adjusted coupling loops
a) magnitude of S_{11} b) magnitude of S_{22} c) magnitude of S_{21}



(c)

Figure 4.7 Example of the S-parameters after well adjusted coupling loops a) magnitude of S_{11} b) magnitude of S_{22} c) magnitude of S_{21} (cont.)

Parameter f_c is a center frequency. If the resonance has been measured for empty resonator, then $f_c = f_0$. In case the resonator is loaded with the sample - $f_c = f_s$.

After the SPDR has been properly tuned, measurements can be started. First of all, the Q-factor and the resonance frequency of the empty SPDR should be measured. Agilent 50-GHz VNA, which has been used in this work, has an option which allows for automatic detection of those parameters. The information appears in the top right corner of the screen, as is indicated in Figure 4.7. But the Q-factor may also be calculated manually, if the resonance frequency, f_s, and two frequencies at the -3dB bandwidth level, f_2 and f_1, are known.

By the final stage of measurement, the thickness of the sample is known, the SPDR is tuned, and the Q-factor and resonance frequency of the empty resonator are known. Then, the Q-factor and the resonance frequency of the SPDR loaded with the sample under test should be measured. For measuring those parameters, the dielectric sample, which has to satisfy requirements explained above, should be placed in the gap between two resonators, as is indicated in Figure 4.6. The area of two resonators has to be covered completely. The air gap between the sample and the resonator does not affect measurement results.

After obtaining all the needed parameters from the measurements, computation can be performed. For extracting DK and DF values from the SPDR measurements, the QWED software is used. Since there are several standard tabulated functions in the calculations, each SPDR requires its own specific version of the software.

In this work, there are three SPDRs that have been used for obtaining dielectric parameters at 10 GHz, 15 GHz, and 20 GHz. Each requires a unique QWED software, even if the procedure and interface of the tools remain the same.

In order to check the performance of all three SPDRs, two standards have been measured several times, using the same procedure, and have been analyzed in this Section. The calculated DK and DF have been compared with the reference data, provided by QWED.

The first sample is Fused Silica. It is a noncrystalline (glass) form of silicon dioxide (SiO_2, sand, quartz). Nearly zero thermal expansion, low DK, and low DF are several key properties of the material. This test sample has been received from the

QWED Company as a reference standard material. Thickness of the sample is 0.36 mm. The sample is uniform and thickness deviation is not significant.

The DK value of this standard sample has been measured at 15 GHz, and it is 3.805 ± 0.019. The DF at 15 GHz is 0.000146 ± 0.00003. The Fused Silica sample has been measured several times, and every time has been compared to standard values. Most of the time, the deviation was within the acceptable range. Table 4.2 contains the summary of the measurements from several different dates for the Fused Silica sample. This data proves the consistency of the measurement technique and sufficient accuracy of the results.

According to the data in Table 4.2, as frequency increases, the DK and DF values also increase. The DK values deviate less and always stay within the acceptable range. The resultant data overall are very consistent, even with small deviation of the Q-factor and resonance frequency for the same SPDRs, but taken at different time.

Another sample is Polytetrafluoroethylene (PTFE, Teflon). This is the most universal material with very well-known parameters., However, the official reference data for its dielectric constant and dissipation factor is not very accurate, because for industry the dielectric parameters for PTFE are not very precise. The standard DK for Teflon is 2.1, and the standard DF is around 0.0002. But when using the SPDR technique, the dielectric parameters can be extracted with higher accuracy. The dielectric parameters of the same PTFE sample have been measured both in this work (EMC Lab, Missouri S&T), and at National Institute of Standards and Technology (NIST) in Boulder, CO, using the same SPDR technique, but physically different SPDR devices with the same

resonance frequency of 10 GHz. The comparison of the measurement from EMC Laboratory (Rolla, MO) and from NIST (Boulder, CO) is presented in Table 4.3.

Table 4.2 Summary of measurement on Fused Silica

17 October 2011					
SPDR	Setup	Freq., MHz	Q-factor	DK	DF
10 GHZ	Empty	9958.582	15440	-	-
	Fused Silica	9842.149	14552	3.79	0.00014
15 GHz	Empty	15534.003	10001	-	-
	Fused Silica	15286.700	9285.4	3.80	0.00019
20 GHz	Empty	21777.470	7221.6	-	-
	Fused Silica	21400.137	6688.5	3.81	0.00029
3 March 2012					
SPDR	Setup	Freq., MHz	Q-factor	DK	DF
10 GHZ	Empty	9958.567	15392	-	-
	Fused Silica	9842.806	14517	3.79	0.00014
15 GHz	Empty	15531.761	10335	-	-
	Fused Silica	15285.383	9488.6	3.80	0.00021
20 GHz	Empty	21778.053	7236.6	-	-
	Fused Silica	21401.42	6765.2	3.80	0.00026
14 May 2012					
SPDR	Setup	Freq., MHz	Q-factor	DK	DF
10 GHZ	Empty	9958.479	15121	-	-
	Fused Silica	9843.511	14245	3.79	0.00013
15 GHz	Empty	15530.579	10525	-	-
	Fused Silica	15284.516	9522.5	3.81	0.00021
20 GHz	Empty	21777.818	7439.5	-	-
	Fused Silica	21400.779	6967.6	3.82	0.00028

The measurement in EMC Laboratory has been made one time, using average thickness of the sample. Three thickness measurements for the same sample were conducted at NIST to check repeatability. There are two different SPDRs (EMC Lab's and NIST's) involved in the measurement setup, and this explains the difference in the Q-factor and resonance frequency of the empty resonators. However, the difference in the SPDRs does not affect the discrepancy in the measured results. The maximum variation in DK and in DF between measurements in different places is less than 1 %. This validates the high accuracy of the measurement technique used in the EMC Laboratory.

The measurement performed for the same sample thickness gave the smallest difference in the DK values and in the DF values. The discrepancy increases if the thickness of the sample is less. This is related to the uncertainty of the thickness measurements – the thinner the sample, the higher the uncertainty.

Measurements on the Fused Silica and PTFE show that measurement technique and actual results are consistent and stable, even if measurements have been done at different times and in different places, using different SPDRs. Although the measurement setup is very sensitive to mechanical motions, the results still could be very accurate and repeatable.

Table 4.3 Comparison of results obtained from measurement in EMC Laboratory and National Institute of Standards and Technology

EMC Laboratory (8/11/11) *Empty:* *Q = 15002* *f = 9.95777301 GHz*		**Difference in results**	**NIST (8/4/11)** *Empty:* *Q = 9370* *f = 10.073045GHz*	
Thickness, mm	Results		Results	Thickness, mm
0.381	*f*res= 9.912314 GHz Q = 14373 Dk = 2.03670 Df = 0.00017827	**1.1%** **n/a** **0.28%** **0.15%**	*f*res= 10.0224 GHz Q = n/a Dk = 2.031 Df = 0.000178	0.381
		1.1% **n/a** **0.45%** **0.41%**	*f*res=10.0224 GHz Q = n/a Dk = 2.046 Df = 0.000179	0.380
		1.1% **n/a** **0.84%** **0.94%**	*f*res= 10.0224 GHz Q = n/a Dk = 2.054 Df = 0.00018	0.377

4.3. ON POSSIBILITY OF COMPARING SPDR AND TRAVELING WAVE METHOD RESULTS

The SPDR is a very simple, fast, and accurate enough method for characterizing dielectric parameters. For the lossy materials this method could be used as verification of results, measured using traveling wave method, or any other standards. For low loss materials, the SPDR method could be used as the primary measurement method, because

results obtained with a traveling wave method may have errors and uncertainties higher than those of the SPDR method.

The theoretical background of the SPDR method, explained herein, shows simplicity of the concept, and at the same time, sufficiency in the performance.

The SPDR method does not need special preparation of the sample under test, while the traveling wave method, explained in Section 2 and 3, requires designing and manufacturing of the special test vehicles for measurements. It is also cheaper to use the SPDR method as compared to the traveling wave method.

The extracted DK and DF values using SPDR method are not very sensitive to the changes in Q-factor or resonance frequency, but very dependent upon the environmental conditions. This has been demonstrated in the present Section.

Finally, the implementation of dielectric parameters, as well as uncertainties does not require complicated calculations.

However, there is the major difference between the SDPR method and the traveling wave method. The SPDR measurement is narrowband, while the traveling wave method is broadband. Besides obtaining dielectric parameters, the traveling wave method allows for studying many other signal integrity issues, such as surface roughness and via design, while SPDR technique gives only the data on the dielectric properties.

However, it is not quite correct to directly compare the extracted dielectric data (DK and DF) from the SPDR and from the traveling wave technique on a PCB test vehicle. The reason is that the majority of PCB laminate dielectrics are inhomogeneous and anisotropic composite materials, containing fiber-glass bundles embedded in a resin matrix.

For example, as is described in paper [24], when studying dielectric properties of PCB laminates of the same group, from the same manufacturer, but with different resin contents, it was found that the slopes of the DK and DF dependences upon resin contents depend not only on frequency, which is expected, but also on the measurement technique (traveling wave technique versus SPDR). There is a substantial difference in the extracted dielectric properties, when using different measurement techniques, in which the electromagnetic field exciting the structure has different polarizations, *i.e.*, different directions of the E-vector with respect to the fiber-glass bundles of the laminate dielectric. In [24] the discrepancy between the results is explained from the point of view of anisotropy and mixing theory (series and parallel mixing rules) for effective permittivity of the composite. Hence, as shown as Figure 4.8, for dielectrically anisotropic media, the comparison of the measurement results using the SPDR and traveling wave techniques is not straightforward, though the transition formulas can be developed using the mixing rules for dielectric/dielectric composites.

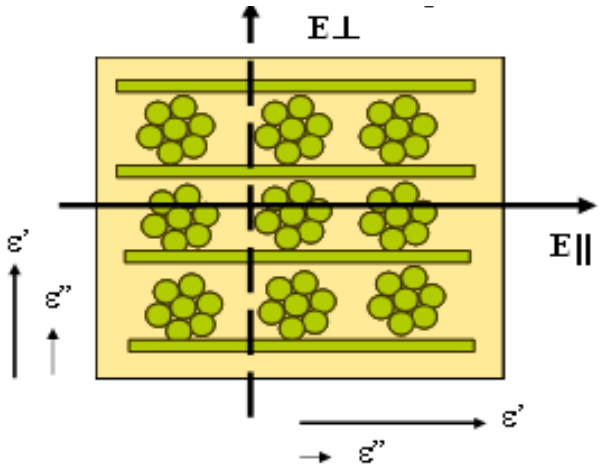


Figure 4.8 An effect of anisotropy [24]
The electric field vector orientation with respect to the fiber glass bundles: perpendicular for the traveling wave method and parallel in the SPDR

The SPDRs currently available in the EMC Lab of Missouri S&T are designed for just three central frequencies – 10 GHz, 15 GHz, and 20 GHz. There are technological limitations in extending SPDR resonance frequency to the higher frequencies. It is theoretically possible to use the higher-order harmonics for measurements, however, the sensitivity of resonators drastically drops. For this reason, an alternative 50-GHz split cylindrical resonator has been developed, and it is currently under investigation.

5. CONCLUSION AND FUTURE SCOPE

The current “in situ” wideband traveling-wave technique based on measuring S-parameters of the PCB test vehicles with auxiliary ‘through-reflect-line” (TRL) calibration patterns has been extensively applied to the material characterization of PCBs up to 20 GHz. In this work, the possibility of extending the frequency range for testing PCB laminate dielectrics up to 45-50 GHz is explored.

The laminate dielectrics which will be used in the high-speed digital design up to 50 GHz (and potentially even higher) will have lower loss and, consequently, lower dielectric constants compared to those PCBs which currently operate and are tested up to 20 GHz. These factors increase the requirements to the accuracy, sensitivity, and stability of measurements. The increased accuracy, sensitivity, and repeatability of measurements are intrinsically related to the design features of the 50-GHz test vehicles. For this reason, various sources of errors and uncertainties for extracting DK and DF values have been analyzed experimentally and numerically (using MVTT and CST Microwave Studio software) for both the present 20-GHz and the new perspective 50-GHz test vehicles.

The possibility of the frequency range extension requires the development of a new PCB test vehicle, which is different from its 20-GHz analog. The 50-GHz test vehicle uses new 2.4-mm SMA connectors, which have the cut-off frequency of 50 GHz. The test vehicle has an improved via transition design, with the parasitic via structure resonance pushed to about 45-46 GHz. The new test board layout includes an improved TRL pattern design with five auxiliary lines of different lengths, as well as “open” and “through” standards. The generalized formula for the TRL calibration pattern design has been derived and incorporated in a simple Matlab GUI to automate calculation of the

frequency breakpoints and line lengths. Also, it was found that it is necessary to modify (make aperiodic), or even completely remove the via wall structure around the signal traces, if measurements will be done using the single-ended striplines. This will allow for getting rid of the parasitic resonances related to the periodicity of the via wall structure, which is present in the 20-GHz test vehicles.

Frequency range extension up to 50 GHz requires paying special attention to a problem of the conductor surface roughness, since the latter increasingly contributes to the total loss on the line as frequency increases. This problem has been addressed in this work as well, and separation of the conductor and dielectric losses should be done at the stage of the dielectric parameter extraction and included in the extraction algorithm.

All these measures synergistically allow for extending the frequency range of measuring dielectric properties of PCB laminate dielectrics up to 50 GHz.

An alternative technique for measuring dielectric parameters of PCB laminate dielectrics is using split-post dielectric resonator (SPDR). This narrowband technique is applied to measurements of thin dielectric plates at frequencies 10 GHz, 15 GHz, and 20 GHz, and can be used for comparison with the results extracted using the travelling wave technique. However, some disagreement in the DK and DF values obtained by these two techniques is expected due to anisotropy of fiber-filled PCB laminate dielectrics.

An application of the new designed 50-GHz split cylindrical resonator may be a good alternative to SPDR technique when extending the frequency range of measurements.

APPENDIX A

DERIVATION OF THE FORMULAS TO CALCULATE ε'_r AND ε''_r IN THE EXTRACTION PROCEDURE

Let's define the complex propagation constant for the medium, according [4, p.18] as

$$\gamma = \alpha_T + j\beta = (\alpha_C + \alpha_D) + j\beta \tag{A.1}$$

For calculating DK and DF of the dielectric material let's assume $\alpha_C \sim 0$, then from (A.1)

$$\gamma_D = \alpha_D + j\beta_D \tag{A.2}$$

From another hand the complex propagation constant is

$$\gamma_D = \frac{j\omega}{c}\sqrt{\left(\varepsilon'_r - j\varepsilon''_r\right)} \tag{A.3}$$

Since $\varepsilon'_r - j\varepsilon''_r = |\varepsilon_r| \exp\left(-j \arctan\left(\frac{\varepsilon''_r}{\varepsilon'_r}\right)\right) = |\varepsilon_r| \cdot e^{-j\delta}$, (A.3) would be represented as

$$\gamma_D = \frac{j\omega}{c}\sqrt{|\varepsilon_r|} \cdot e^{-j\frac{\delta}{2}} \tag{A.4}$$

where $\sqrt{|\varepsilon_r|} = \sqrt[4]{\left(\varepsilon'_r\right)^2 + \left(\varepsilon''_r\right)^2}$ and $e^{-j\frac{\delta}{2}} = \left(\cos\frac{\delta}{2} - j\sin\frac{\delta}{2}\right)$. And taking into account these expressions, the formula (A.4) could be presented as following

$$\gamma_D = \frac{\omega}{c}\sqrt[4]{\left(\varepsilon'_r\right)^2 + \left(\varepsilon''_r\right)^2} \cdot \left(\sin\frac{\delta}{2} + j\cos\frac{\delta}{2}\right) \tag{A.5}$$

Comparing (A.5) and (A.2) notice

$$\alpha_D = \mathrm{Re}\{\gamma_D\} = \frac{\omega}{c}\sqrt[4]{\left(\varepsilon'_r\right)^2 + \left(\varepsilon''_r\right)^2} \cdot \sin\frac{\delta}{2} \tag{A.6}$$

$$\beta_D = \mathrm{Im}\{\gamma_D\} = \frac{\omega}{c}\sqrt[4]{\left(\varepsilon_r^{'}\right)^2 + \left(\varepsilon_r^{''}\right)^2}\cdot\cos\frac{\delta}{2} \qquad \text{(A.7)}$$

Since $\delta \to 0$, from trigonometry $\sin\left(\frac{\delta}{2}\right) = \frac{\delta}{2}$ and $\cos\left(\frac{\delta}{2}\right) = 1$, then (A.6) and (A.7)

$$\alpha_D = \frac{\omega}{2c}\sqrt[4]{\left(\varepsilon_r^{'}\right)^2 + \left(\varepsilon_r^{''}\right)^2}\cdot\left(\frac{\varepsilon_r^{''}}{\varepsilon_r^{'}}\right) \qquad \text{(A.6)}$$

$$\beta_D = \frac{\omega}{c}\sqrt[4]{\left(\varepsilon_r^{'}\right)^2 + \left(\varepsilon_r^{''}\right)^2} \qquad \text{(A.7)}$$

Let's assign $x = \left(\frac{\beta\cdot c}{\omega}\right)^2$ and $y = \left(\frac{2\alpha_D\cdot c}{\omega}\right)^2$, then let's solve the system of equations

$$x^2 = \left(\varepsilon_r^{'}\right)^2 + \left(\varepsilon_r^{''}\right)^2 \qquad \text{(A.8)}$$

$$y^2 = \left(\left(\varepsilon_r^{'}\right)^2 + \left(\varepsilon_r^{''}\right)^2\right)\left(\frac{\varepsilon_r^{''}}{\varepsilon_r^{'}}\right)^4 \qquad \text{(A.9)}$$

After simple arithmetic calculations $\varepsilon_r^{'}$ and $\varepsilon_r^{'}$ could be represented as

$$\varepsilon_r^{'} = x\sqrt{\frac{x}{x+y}} \qquad \text{(A.10)}$$

$$\varepsilon_r^{''} = x\sqrt{\frac{y}{x+y}} \qquad \text{(A.11)}$$

where $x = \left(\frac{\beta\cdot c}{\omega}\right)^2$ and $y = \left(\frac{2\alpha_D\cdot c}{\omega}\right)^2$

The formulas (2.1) – (2.4) of current work have been developed according abovementioned derivations.

APPENDIX B

FORMULAS TO EXTRACT DK AND DF BASED ON MEASURED S-PARAMETERS

The derivations below are done assuming a low loss material and microwave mismatch does not affect measurements.

Based on [4], propagation constant could be presented such as

$$\beta \cong \frac{\omega}{c}\sqrt{\varepsilon_r^{'}} = \frac{2\pi f}{c}\sqrt{\varepsilon_r^{'}} \tag{B.1}$$

Taking into account that $\beta l = [\varphi_{21}]_{unwrapped}$, then it is easy to show

$$\varepsilon_r^{'} = \left(\frac{c}{2\pi}\right)^2 \left(\frac{[\varphi_{21}]_{unwrapped}}{lf}\right)^2 \tag{B.2}$$

Considering magnitude of measured S_{21} as

$$|S^{dB}_{21}| \cong -8.686 \cdot \alpha_T \cdot l \tag{B.3}$$

Since total loss consists of conductor loss and dielectric loss, (B.3) could be presented such as

$$|S^{dB}_{21}| \cong -8.686 \cdot \alpha_C \cdot l - 8.686 \cdot \alpha_D \cdot l \tag{B.4}$$

From (B.4) dielectric loss could be presented, because conductor loss is neglected

$$\alpha_D = \frac{|S^{dB}_{21}|_D}{-8.686 \cdot l} \tag{B.5}$$

From [4, p. 111], dielectric loss also could be presented in terms of DF

$$\alpha_D = \frac{\omega}{2c}\sqrt{\varepsilon'_r}\tan\delta = \frac{\omega}{2c}\sqrt{\varepsilon'_r}\frac{\varepsilon''_r}{\varepsilon'_r} \tag{B.6}$$

Let us determine ε''_r from (B.6)

$$\varepsilon''_r = \frac{2c}{\omega}\cdot\sqrt{\varepsilon'_r}\cdot\alpha_D \tag{B.7}$$

Knowing $\omega = 2\pi f$ and expression for dielectric loss from (B.6), formula (B.7) would be

$$\varepsilon''_r = \frac{c}{\pi\cdot 8.686}\cdot\frac{\sqrt{\varepsilon'_r}}{f\cdot l}\cdot\left(-|S^{dB}{}_{21}|_D\right) \tag{B.8}$$

According (B.2) and (B.8) need to find DK and DF

$$DF = \tan\delta = \frac{\varepsilon''_r}{\varepsilon'_r} = \frac{-|S^{dB}{}_{21}|_D}{4.343\cdot[\varphi_{21}]_{unwrapped}} \tag{B.9}$$

$$DK = \varepsilon'_r = \left(\frac{c}{2\pi}\right)^2\left(\frac{[\varphi_{21}]_{unwrapped}}{lf}\right)^2 \tag{B.10}$$

DK and DF calculation s according to expressions (B.9) and (B.10) based on magnitude and unwrapped phase of measured S_{21}.

APPENDIX C

CALCULATTIONS OF SYSTEMATIC ERRORS IN DK AND DF

The systematic errors in calculating DK and DF still could be present, even if the TRL calibration is applied to remove port effects, and if the full set of complex S-parameters is used for calculating DK and DF in the extraction procedure as in Figure 2.11. Based on calculation of DK and DF (B.9) and (B.10), derived in Appendix B, the systematic error for calculating DF and DK may be found as

$$\Delta DF = \left(\frac{\partial DF}{\partial(-|S^{dB}{}_{21}|_D)} \Delta(|S^{dB}{}_{21}|_D) \right) + \left(\frac{\partial DF}{\partial\left([\varphi_{21}]_{unwrapped}\right)} \Delta[\varphi_{21}]_{unwrapped} \right) \quad \text{(C.1)}$$

$$\Delta DF = \frac{1}{4.343} \left(\frac{\Delta(|S^{dB}{}_{21}|_D)}{[\varphi_{21}]_{unwrapped}} + \frac{\Delta[\varphi_{21}]_{unwrapped}}{[\varphi_{21}]^2{}_{unwrapped}} \right) \quad \text{(C.2)}$$

$$\Delta DK = \left(\frac{c}{2\pi} \right)^2 \frac{1}{l \cdot f} \left(\Delta[\varphi_{21}]_{unwrapped} \right) \quad \text{(C.3)}$$

Analyzing (C.2) and (C.3) it is clear that the DF and DK systematic errors are affected by the phase error and the error in magnitude of the measured S_{21}. There are several major sources of uncertainties for unwrapped phase of S_{21}. These include a possible zero-frequency shift, errors in Matlab unwrapping function, .and violation of translational invariance due to possibly uneven geometry of the trace. The conductor surface roughness affects the magnitude of S_{21}. The ground via wall also may affect the magnitude and phase of S_{21}.

If the TRL calibration does not completely remove port effects, or there are some artifacts on the line (like via walls or violation of translation invariance), then there may be significant return loss due to mismatch on the line. This mismatch could be taken into

account in the uncertainties calculations. After converting the S-parameters to ABCD matrix, A-parameter in the unmatched case $\tilde{A}$ is

$$\tilde{A} = A + \Delta A = \left(\frac{1 + |S_{21}|^2}{2|S_{21}|} - \frac{|S_{11}|^2}{2|S_{21}|} \right) e^{-j[\varphi^{rad}{}_{21}]} \tag{C.4}$$

where A corresponds to the matched case, and

$$|\Delta A| = -\frac{|S_{11}|^2}{2|S_{21}|} \tag{C.5}$$

is a relatively small deviation $|\Delta A| << |A|$

The propagation constant in the mismatched case in symmetric system (A-parameter is equal to D-parameter) can be expressed as

$$\tilde{\gamma} \cdot l = \arccos h(A + \Delta A) \approx \arccos h(A) + \frac{d\left(\arccos h(A)\right)}{dA} \Delta A \tag{C.6}$$

and since $\frac{d\left(\arccos h(A)\right)}{dA} = \frac{1}{\sqrt{A^2 - 1}}$, *for* $A \neq 1$

$$\tilde{\gamma}\cdot l \approx \arccos h(A) + \frac{\Delta A}{\sqrt{A^2-1}},\ for\ A \neq 1\ and\ \frac{|\Delta A|}{A} << 1 \qquad (C.7)$$

Also known $\tilde{\gamma}\cdot l \approx \arccos h(A) + \Delta\alpha \cdot l$, that means

$$\Delta\alpha_D = \frac{|S_{11}||S_{22}|}{2|S_{21}|l} = \frac{|S_{11}|^2}{2|S_{21}|l} \qquad (C.8)$$

Formula (C.8) represents the systematic error due to mismatch (if TRL calibration is imperfect). According to [4, p.111] loss tangent is

$$DF = \tan\delta = \frac{2\alpha_D c}{\omega\sqrt{\varepsilon'_r}} \qquad (C.9)$$

The systematic error in DF could be calculated based on (C.9) as

$$\Delta DF = \frac{2c}{\omega}\left(\frac{\Delta\alpha_D}{\sqrt{\varepsilon'_r}} + \left(\frac{\alpha_D\cdot\Delta\varepsilon'_r}{2\sqrt{\varepsilon'^{3}_r}}\right)\right) \qquad C.10)$$

Considering $\alpha_D = \frac{|-S^{dB}{}_{21}|}{8.686\cdot l}$ and (C.8) one can get the final expression for the systematic error in DF.

$$\Delta DF = \frac{c}{\omega\sqrt{\varepsilon_r^{'}}}\frac{|S_{11}|^2}{|S_{21}|\,l} + \frac{c}{\omega\sqrt{\varepsilon_r^{'3}}}\frac{|-S^{dB}{}_{21}|}{8.686\cdot l}\Delta\varepsilon_r^{'} \qquad \text{(C.11)}$$

The first term of (C.11) shows that the systematic error increases with increasing reflection (mismatch). It is more difficult to measure the DF accurately for short lines, very low loss materials, and comparatively low DK. The second term shows that the error in DF may increase due to surface roughness and via wall effect. For the development of the 50-GHz test vehicles this factors become very important.

APPENDIX D

SAMPLE PREPARATION FOR THE SCANNING ELECTRON MICROSCOPY

Preparation of the sample for scanning electron microscopy (SEM) or optical microscopy (OM) consists of four stages:

I. Cutting a sample from a PCB of interest

II. Putting the sample in the epoxy

III. Polishing the epoxy sample using grinding/polishing equipment

IV. Taking high magnification images of the sample using SEM or OM

Herein, all stages will be described in detail.

A. Cutting a sample from a PCB of interest.

1) A test vehicle which needs to be cut has to be identified. To do so, the chosen PCB has to be taken out of storage where all PCBs are located according to the systematic order. In Figure D.1, an uncut PCB is presented.

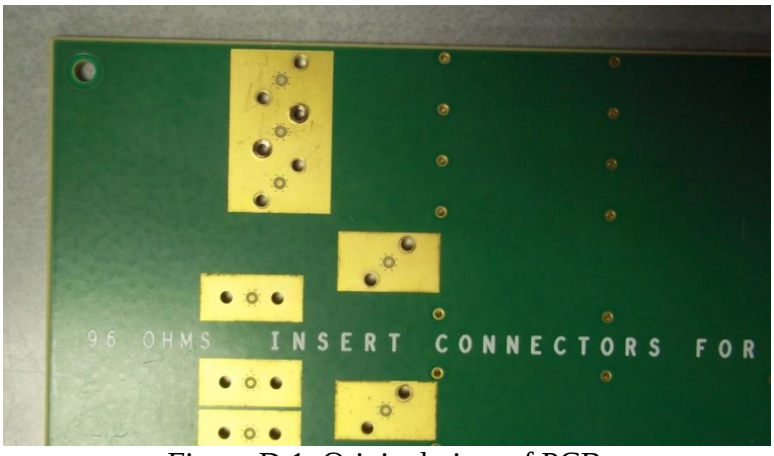


Figure D.1. Original view of PCB

2) To cut the PCB, take it to a SKIL 9-inch (229 mm) Benchtop 2 Speed Band Saw, indicated as 1 in Figure D.2. If band saw is not available, use a hand saw,

indicated as 2 in Figure D.2. When using a hand saw, to keep the PCB stable, use vice grips, indicated as 4 in Figure D.2. How to use the hand saw and vice grips to cut the PCB will be shown in Figure D.3.

Figure D.2. Setup for cutting sample using band saw. SKIL 9-inch (229 mm) Benchtop 2 Speed Band Saw is indicated as 1. Hand saw is indicated as 2. Safety goggles are indicated as 3. Vice grips are indicated as 4

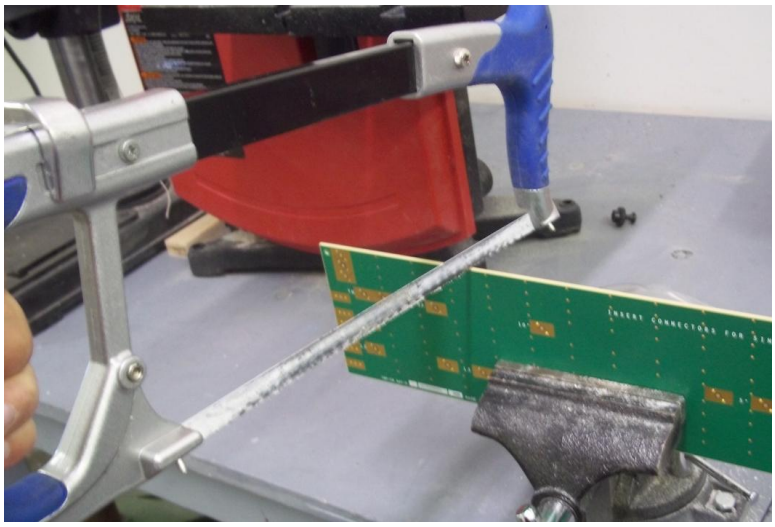


Figure D.3 Setup for cutting sample using hand saw and vice grips

3) Setup of the band saw is shown in Figure D.4. For better alignment of the PCB, the sample to be cut could be drawn on the PCB with a ruler and pencil.

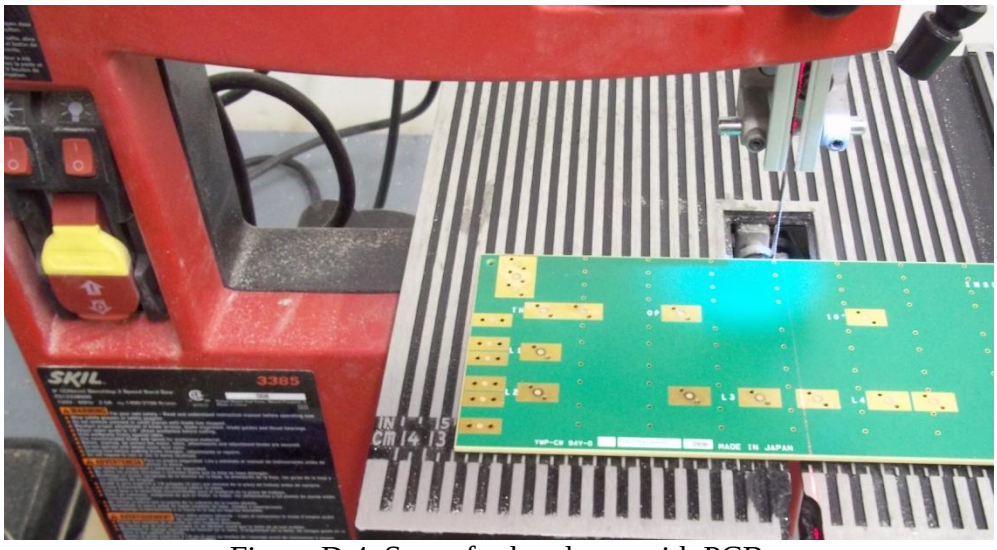


Figure D.4. Setup for band saw with PCB

4) The length of the sample being cut has to be less than 1.2 inches (30 mm) to be able to fit in the mold which will contain the epoxy sample as shown in Figure D.5.

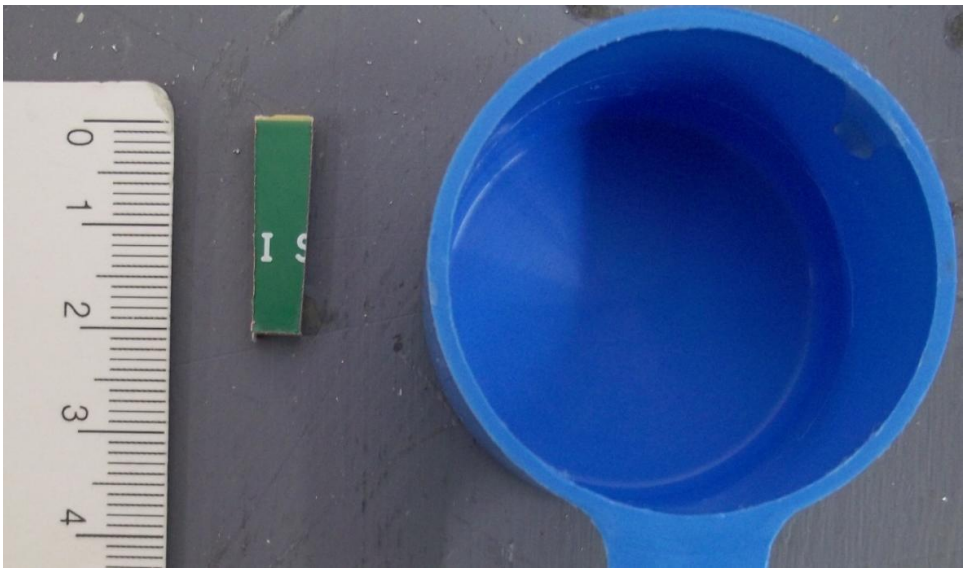


Figure D.5. Dimensions of the sample and the mold

5) To get rid of artifacts on the sample, caused by cutting, a hand file or sandpaper should be used. The difference between the sample directly after cutting and the sample after filing is shown in Figure D.6. This is the first polishing step.

Figure D.6. Comparison between sample before rough polishing (a) and after (b)

The sample, which has been cut and roughly polished, needs to be put in epoxy. The process of putting the sample in epoxy will be described in the next section.

B. Putting the sample in the epoxy

For applying epoxy to the sample (cold mounting), SamplKwick Fast Cure Acrylic Kit 20-3560 from Buehler should be used. The contents of the kit are presented in Figure D.7.

- SamplKwick Fast Cure Acrylic Kit 20-3560 Box (1)
- SamplKwick Liquid Fast Cure Acrylic 20-3564 (2)
- SamplKwick Powder Fast Cure Acrylic 20-3562 (3)
- Forceps (4)
- Stirring Stick (5)
- Mold (6)
- Disposable Cup for Mixing (7)
- Sample (8)

Figure D.7 SamplKwick Fast Cure Acrylic Kit 20-3560 with indicated parts

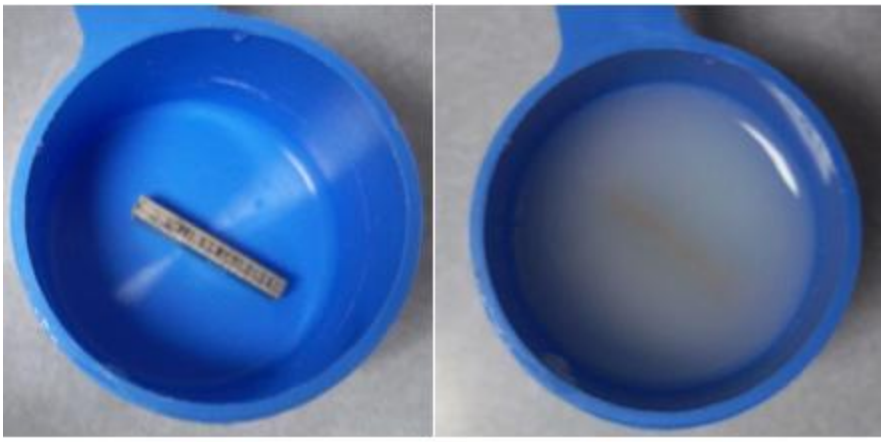
6) In order to cold mount the sample, mix by volume two parts powder (3 in Figure D.7) and one part liquid (2 in Figure D.7) in a small disposable cup (7 in Figure D.7), as shown in Figure D.8. For a lower viscosity, mix three parts powder with two parts liquid.

7) Stir the mixture with a stirring stick (5 in Figure D.7) for 15 to 20 seconds.

8) The sample needs to be placed, using forceps (4 in Figure D.7), perpendicular to the surface of the bottom of the mold. The side which has been roughly polished should be facing the bottom of the mold. It is a good habit to mark the sample if there are multiple samples involved in the polishing process. Then, mark the side as a reference on SEM picture. Also, to prevent the mixture from disrupting the position of the sample, use perpendicular pieces of plastic to hold the sample in place, as indicated in Figure D.10. Pour the mixture into the mold, (6 in Figure D.7) covering the sample (8 in

Figure D.7) with the mixture, as demonstrated in Figure D.9.b. Before removing mold, cure at room temperature for one hour.

Figure D.8 Mixing powder and liquid for making an epoxy



(a) (b)

Figure D.9. Sample in the mold. a) before pouring the epoxy mixture. b) fully covered with epoxy mixture

Figure D.10. Example of labeling the sample, and using plastic holders

After waiting at least one hour for the mixture to set and cool, it will be clear and hard. Now, the sample will be able to be extracted, as shown in Figure D.11. For transportation of the sample to the polishing machine, a sample holder needs to be used to prevent the sample from scratching. In Figure D.12, the holder for multiple samples is presented. In the next stage, the sample will be polished delicately. The polishing process will be described in the next section.

(a) (b)

Figure D.11 Sample after extraction from the mold. a) the top view. b) the bottom view

Figure D.12 Example of the sample holder for transportation

C. Polishing the epoxy sample using grinding or polishing equipment

In the current project, for polishing samples, a Buehler Polisher ECOMET III Grinder, presented in Figure D.13, has been used.

Figure D.13. Buehler Polisher ECOMET III Grinder has been used for polishing

9) Before polishing, make sure the sample is properly marked so the side which needs to be photographed by the SEM will be easily recognizable after polishing.

10) For the first level of polishing, use a '120 Grit' layer from storage, shown in Figure D.14, and bottle of water, as presented in Figure D.15.

Figure D.14 Storage for polishing layers

(a) (b) (c)

Figure D.15 Supply for the first stage polishing. a) Washing bottle of water. b) '120 Grit' layer, front side. c) '120 Grit' layer, back side.

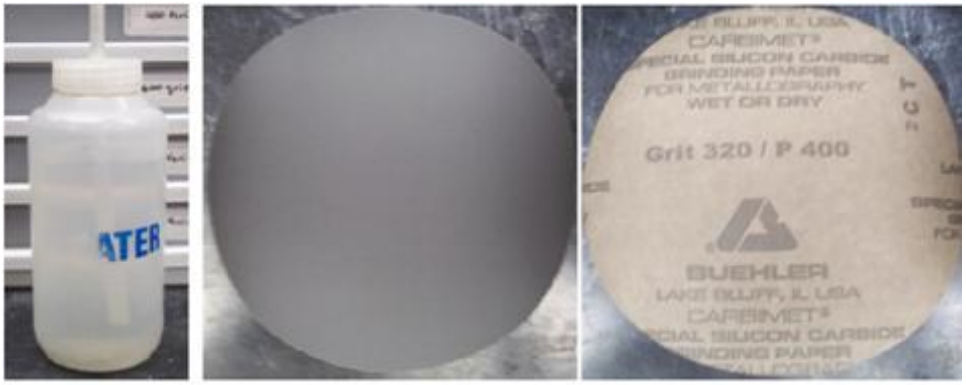
Apply the '120 Grit' layer to the Buehler Polisher ECOMET III Grinder. Set the speed at 5 to 6 D.C. Milliamperes. Spray water on the grit and move the sample

clockwise (opposite the grit's counterclockwise motion). The desired side of the sample needs to be touching the grit, as demonstrated in Figure D.16. In order to achieve the best results, the grinding process needs to be done for 2 to 3 minutes with medium pressure on the sample.

The purpose of the first level of polishing is to grind the surface of the mold down enough that the surface of the PCB sample is available.

Figure D.16 Example of polishing process. Direction of the sample rotation is indicated with red color.

11) For the second level of polishing, use a '400 Grit' layer and bottle of water, as shown in Figure D.17.



(a) (b) (c)

Figure D.17. Supply for the second level of polishing. a) Washing bottle of water. b) '400 Grit' layer, front side. c) '400 Grit' layer, back side.

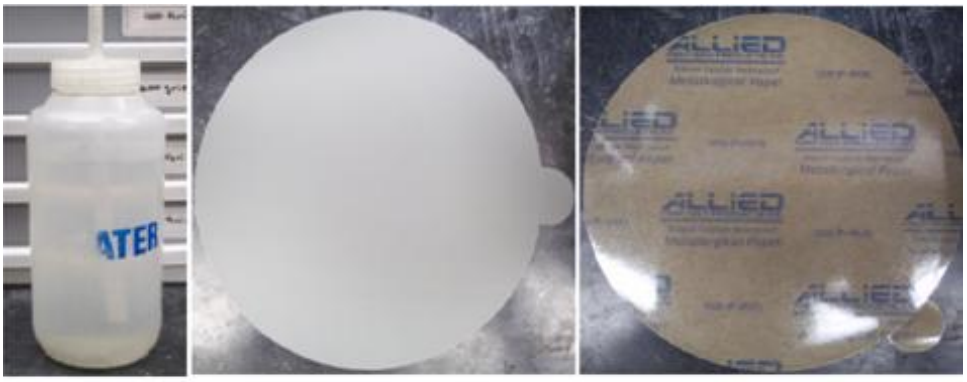
Take the '120 Grit' off of the machine and apply the new '400 Grit' to the machine. Repeat the process described in Step 2 with the new '400 Grit'.

12) Change the '400 Grit' layer to an '800 Grit' layer, shown in Figure D.18, which needs to be taken from storage. Using the water bottle and the '800 Grit' layer, repeat the process in Step 2.

(a) (b) (c)

Figure D.18. Supply for the second level of polishing. a) Washing bottle of water. b) '800 Grit' layer, front side. c) '800 Grit' layer, back side.

13) Take a ‘1200 Grit’ layer, presented in Figure D.19, from storage. After removing the ‘800 Grit’ layer, apply the ‘1200 Grit’ to the machine and repeat the previous process from Step 2.



(a) (b) (c)

Figure D.19. Supply for the second level of polishing. a) Washing bottle of water. b) ‘1200 Grit’ layer, front side. c) ‘1200 Grit’ layer, back side.

14) After polishing with all four grits, it is necessary to check for scratches on the sample. To check the sample, use a microscope, as shown in Figure D.20.

Figure D.20 Optical microscope with medium magnification

It is critical to the project that there are no deep scratches on the sample. If deep scratches are present, repeat the previous step with the ‘1200 Grit’ layer. If there are no deep scratches, the next level of polishing can be started.

15) For the next level of polishing, apply a ‘Microcloth’ to the machine and use Buehler MetaDi Monocrystalline Diamond Suspension 6µm (yellow liquid), as shown in Figure D.21. For safety purposes, wear nitrile gloves.

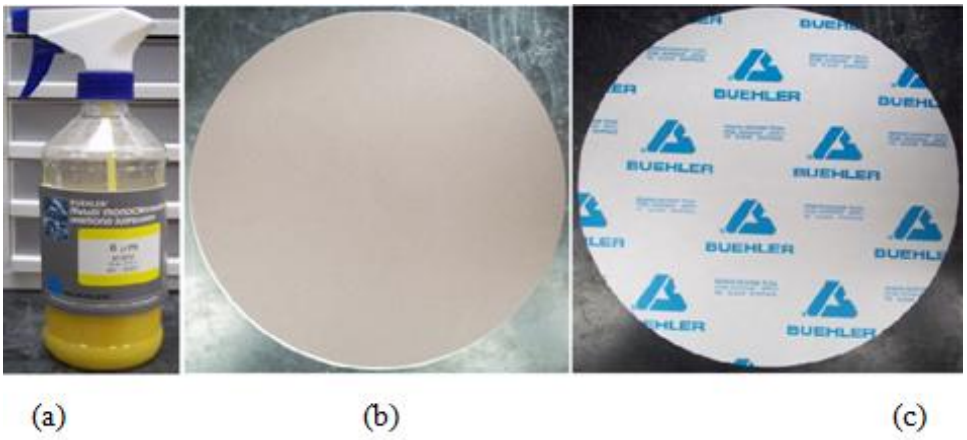


Figure D.21. Supply for the second level of polishing. a) Buehler MetaDi Monocrystalline Diamond Suspension 6µm (yellow liquid). b) ‘Microcloth’ layer, front side. c) ‘Microcloth’ layer, back side.

Set the speed of the machine to 6 to 7 D.C. Milliamperes and spray the liquid on the microcloth layer. Move the sample clockwise for 1 to 2 minutes with minimal pressure. After 1 to 2 minutes of grinding, put the sample in the UltraSonik machine, which is shown in Figure D.22.

Set the knob labeled ‘Power’ to maximum and the knob labeled ‘Degas’ to minimum. Place the sample, on its side, into one of the beakers filled with water. After the sample has been immersed for about 2 minutes, take the sample out and let it air dry. When the sample is dry, use the microscope to check the texture of the surface, which

should be smooth. The operator will then decide whether or not the surface is smooth enough to continue to the next level of polishing.

Figure D.22. Ultrasonic equipment.

16) Apply a new 'Microcloth' and use Buehler MetaDi Surpreme Polycrystalline Diamond Suspension 3µm (green liquid), shown in Figure D.23.

(a) (b) (c)

Figure D.23. Supply for the second level of polishing. a) Buehler MetaDi Monocrystalline Diamond Suspension 3µm (green liquid). b) 'Microcloth' layer, front side. c) 'Microcloth' layer, back side.

Repeat the previous step.

The purpose of this step is to reduce the number of minor scratches that could be present on the PCB sample and to make the surface smoother.

17) Change the ‘Microcloth’to an ‘8” MASTERTEX PSA’ from Buehler and use Buehler MetaDi Monocrystalline Diamond Suspension 1µm (blue liquid), shown in Figure D.24.

(a) (b) (c)

Figure D.24. Supply for the second level of polishing. a) Buehler MetaDi Monocrystalline Diamond Suspension 1µm (blue liquid). b) ‘8” MASTERTEX PSA’ layer, front side. c) ‘8” MASTERTEX PSA’ layer, back side.

Repeat Step 7.

18) In this stage of the polishing process, the sample should be very smooth with no scratches. If the sample has the desired surface texture, place the sample on its side in the UltraSonik machine for 5 to 10 minutes.

19) If there are still scratches present on the sample, use a new ‘8” MASTERTEX PSA’ and Buehler MetaDi Supreme Polycrystalline Diamond Suspension 0.25 µm (gray liquid), as shown in Figure D.25.

(a) (b) (c)

Figure D.25. Supply for the second level of polishing. a) Buehler MetaDi Monocrystalline Diamond Suspension 0.25µm (grey liquid). b) '8" MASTERTEX PSA' layer, front side. c) '8" MASTERTEX PSA' layer, back side.

Repeat Step 7 and 10.

The result of this polishing process needs to be a sample which is smooth, has no scratches on the surface, and is dry and therefore ready to be photographed by the SEM or an optical microscope.

D. Taking high magnification images of the sample using scanning electron microscopy (SEM) or optical microscopy (OM).

For optical microscopy, the sample can be used immediately after polishing. For scanning electron microscopy, the sample needs to be Au/Pd coated and prepared before photographing. To do so, the operator should use the Denton Au/Pd Coater, presented in Figure D.26, according to operating instructions.

If the sample will be used for SEM immediately after coating, it needs to be placed on the holder. Otherwise, the sample has to be protected from any dust particles in case the SEM won't be used immediately.

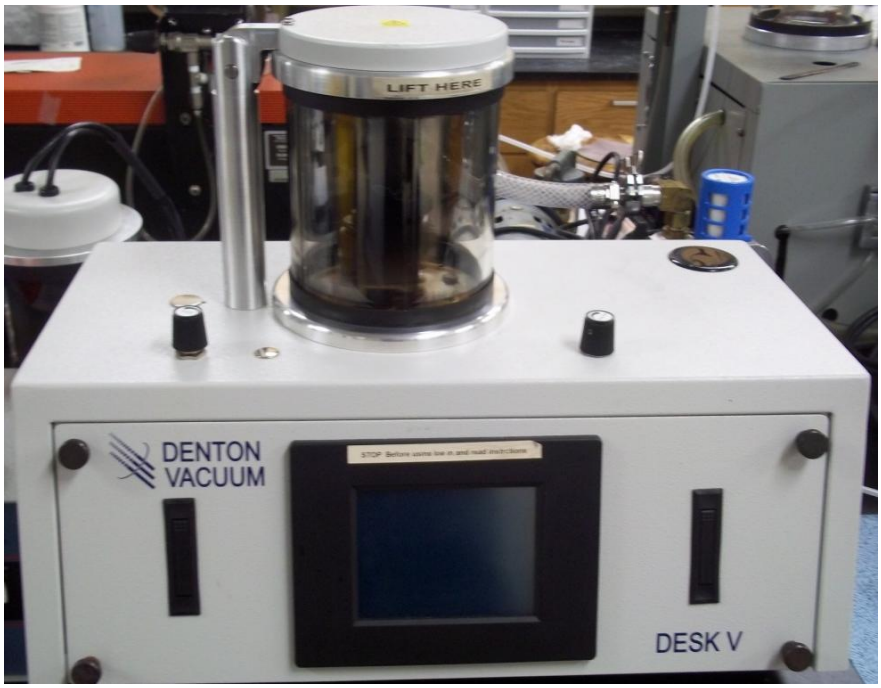


Figure D.26 Denton vacuum Au/Pd coater

To place the sample, cover the holder in double stick carbon tape to attach the sample to the holder. To assist the electron microscopy, connect the surface of the sample to the metal holder using conductive copper tape. The sample which is ready for SEM use is shown in Figure D.27.

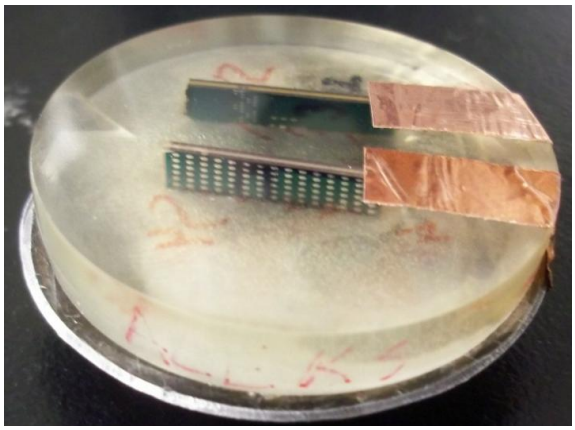


Figure D.27. Example of completely polished sample and prepared for the SEM

SEM equipment can be used only by authorized users, who have specific certificates. Before taking SEM images, the preparer has to know the location of the samples and be able to find the desired trace using the reference.

After taking SEM photographs, the files need to be stored and transferred for further image processing analysis.

APPENDIX E.

DATASHEET OF THE ‘SV MICROWAVE’ 2.4 MM SMA CONNECTOR WHICH WILL BE USED IN NEW PCB DESIGN

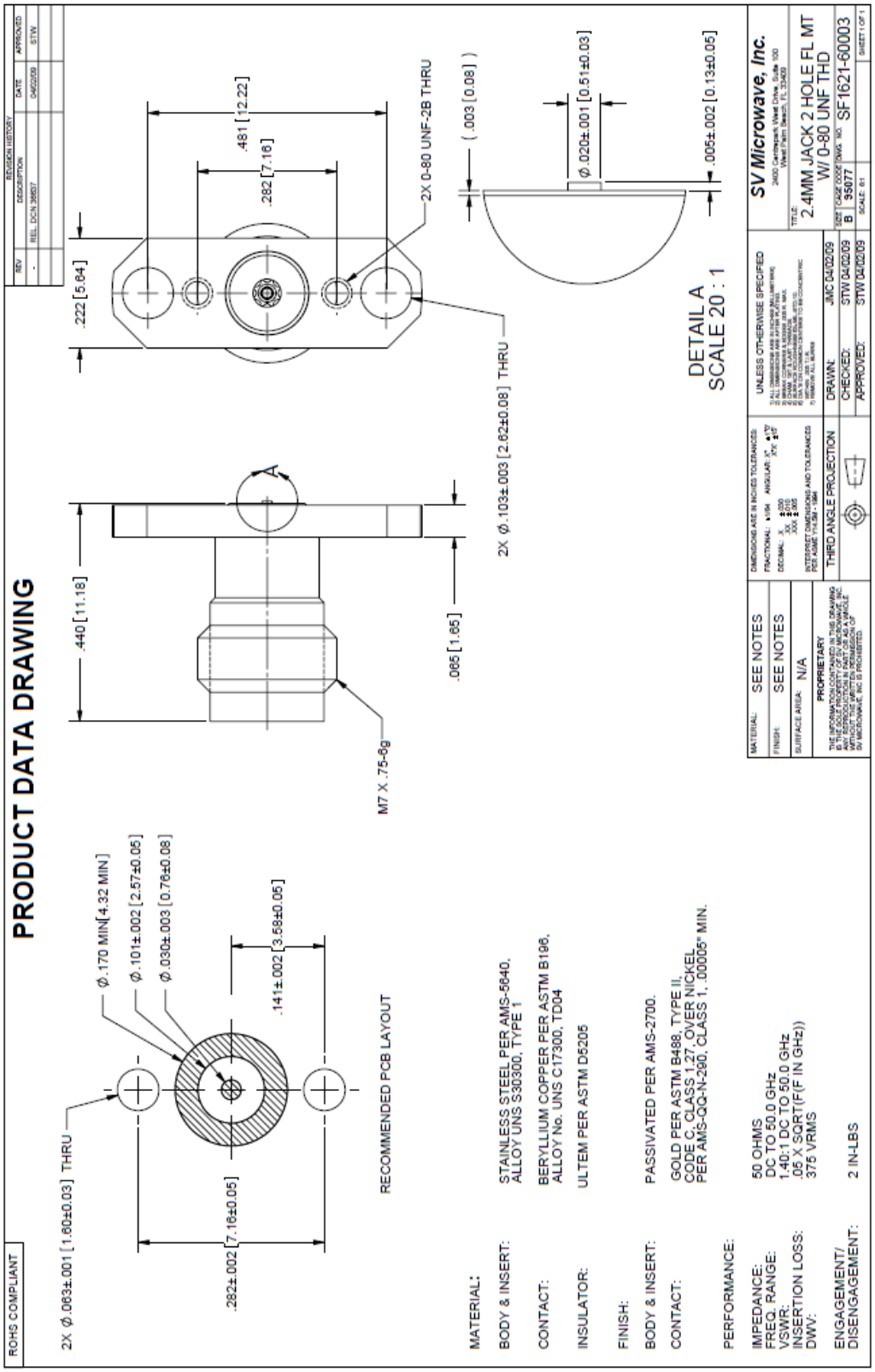


Figure E.1 Technical drawing of the SV Microwave 2.4 mm SMA connectors

APPENDIX F.

DETAILS OF THE NEW TEST VEHICLE DESIGN

After developing the new, improved test vehicle model, the PCB layout has to be changed properly. The current PCB layout has been taken as the initial model for modifying.

In Appendix C, a summary of the new design model is presented.

Via design

The via model has been developed in the full-wave electromagnetic numerical simulation software CST Microwave Studio. Two main objects of focusing are illustrated in Figure F.1.

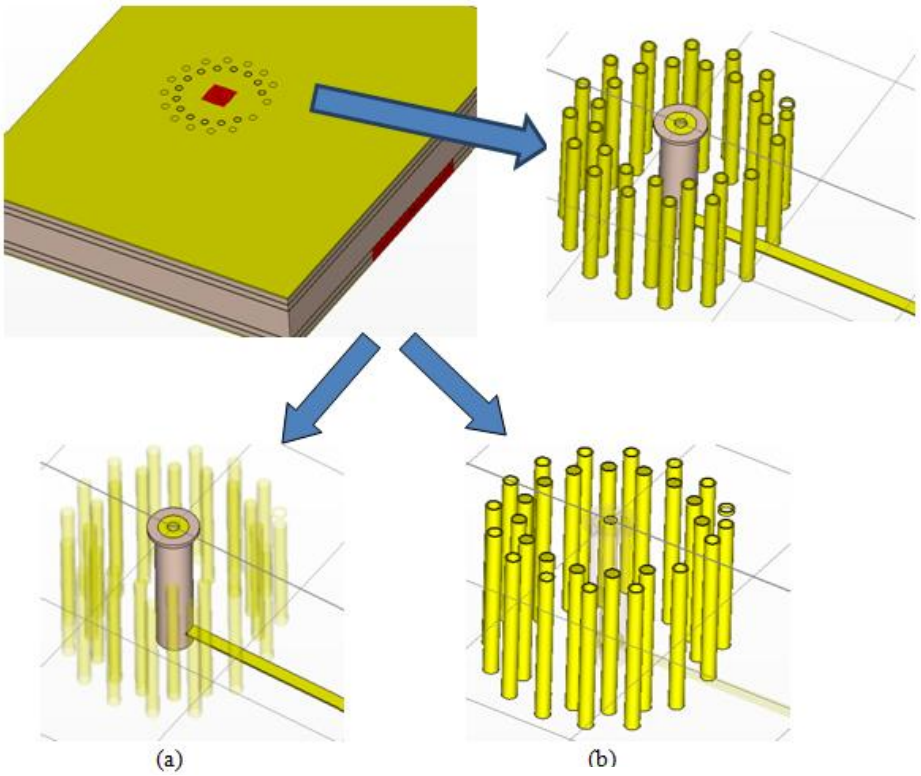


Figure F.1 Overview of the via model. a) Signal via b) Ground vias

A launching structure includes a signal via, a dual ring ground via, and holes for mounting connectors. Dimensions of the signal via in the launching structure are shown

in Figure F.2. Dimensions of the dual ring ground vias are indicated in Figure F.3. The reference point (0,0,0) has been chosen as a center of the pad surface of the signal via.

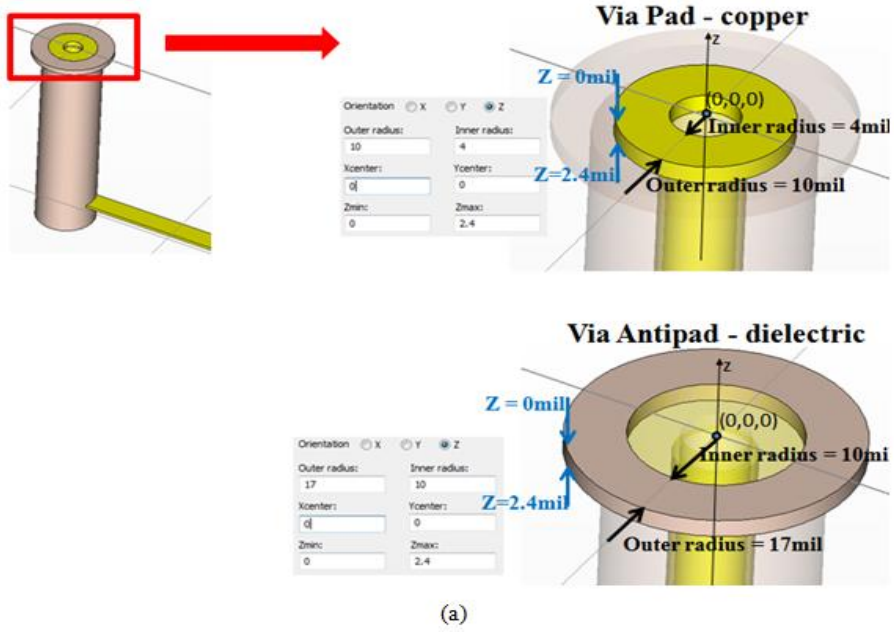


Figure F.2 Dimensions of the signal via in PCB launch structure. a) Overview of the top part of the signal via. b) Overview of the middle part of the via. c) Overview of the bottom part of the via. d) Top view of the signal via

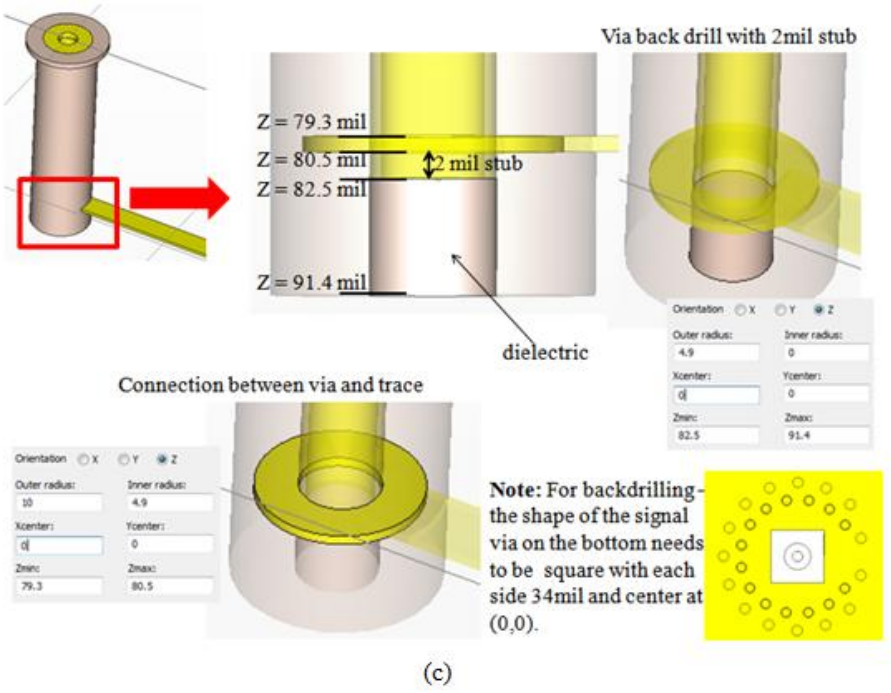


Figure F.2 Dimensions of the signal via in PCB launch structure. a) Overview of the top part of the signal via. b) Overview of the middle part of the via. c) Overview of the bottom part of the via. d) Top view of the signal via (cont)

All ground vias presented as the dual ring ground vias have the same design and dimensions. The only difference is in their location, which has been pre-calculated. Via

coordinates are presented in Figure F.3c and in Figure F.3d. The via numbers indicated in Figure F.3b correspond to a via number in Figure F.3c and in Figure F.3b.

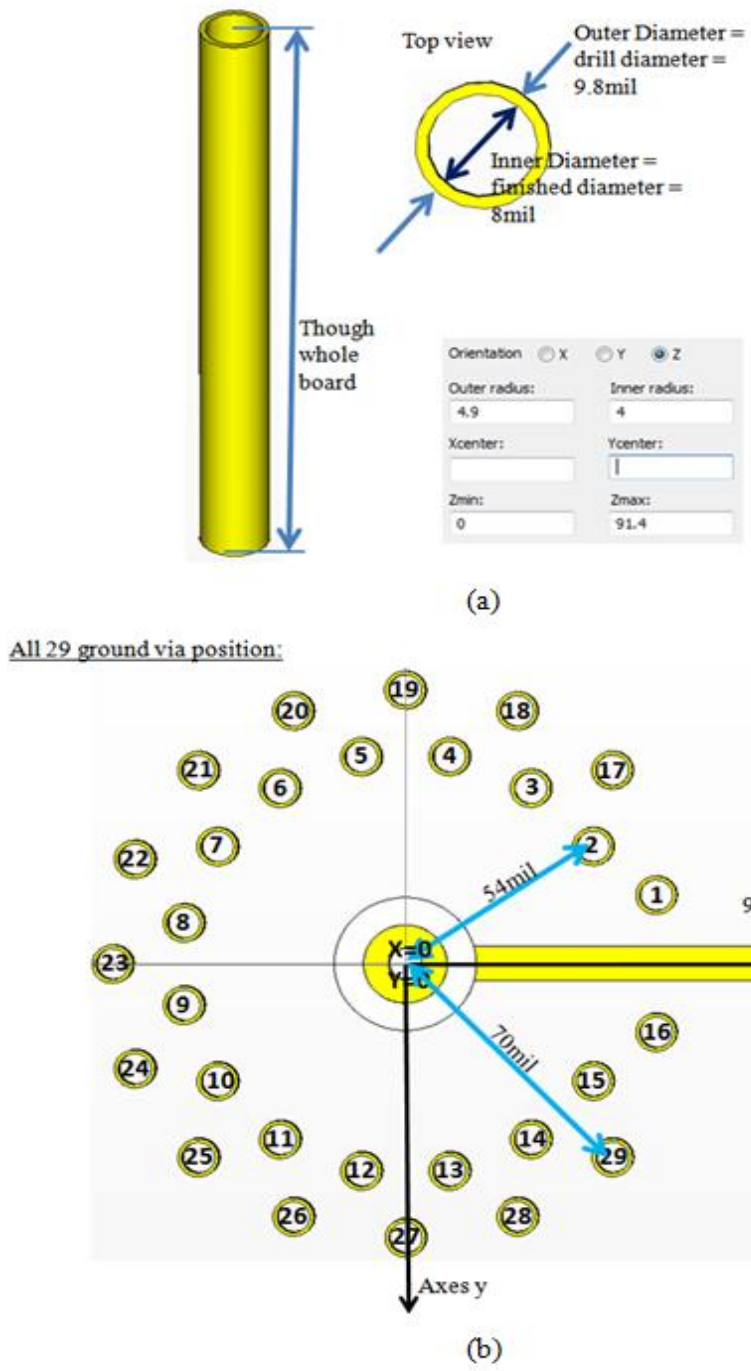


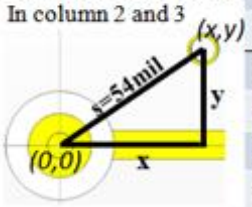
Figure F.3 Dimensions of the dual ring ground vias. a) Overview of the ground via model design. b) Location of the ground vias. c) Coordinates of the inner ring ground vias. d) Coordinates of the outer ring ground vias

For the first circle of ground via:
Distance from center of signal via to center of any ground via:
s= 54 mil

Except #1 and #16

Via number	X center coordinate	Y center coordinate	X center coordinate, mil	Y center coordinate, mil
1			59.96	-17.53
2	(cos33.75°)*s	-(sin33.75°)*s	44.89	-30.00
3	(cos56.25°)*s	-(sin56.25°)*s	30.00	-44.89
4	(cos78.75°)*s	-(sin78.75°)*s	10.53	-52.96
5	-(cos78.75°)*s	-(sin78.75°)*s	-10.53	-52.96
6	-(cos56.25°)*s	-(sin56.25°)*s	-30.00	-44.89
7	-(cos33.75°)*s	-(sin33.75°)*s	-44.89	-30.00
8	-(cos11.25°)*s	-(sin11.25°)*s	-52.96	-10.53
9	-(cos11.25°)*s	(sin11.25°)*s	-52.96	10.53
10	-(cos33.75°)*s	(sin33.75°)*s	-44.89	30.00
11	-(cos56.25°)*s	(sin56.25°)*s	-30.00	44.89
12	-(cos78.75°)*s	(sin78.75°)*s	-10.53	52.96
13	(cos78.75°)*s	(sin78.75°)*s	10.53	52.96
14	(cos56.25°)*s	-(sin56.25°)*s	30.00	44.89
15	(cos33.75°)*s	-(sin33.75°)*s	44.89	30.00
16			59.96	17.53

Example of calculation In column 2 and 3

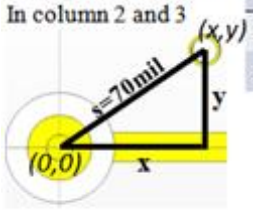


(c)

For the second circle of ground via:
Distance from center of signal via to center of any ground via:
s= 70 mil

Via number	X center coordinate	Y center coordinate	X center coordinate, mil	Y center coordinate, mil
17	(cos45°)*s	-(sin45°)*s	49.49	-49.49
18	(cos67.5°)*s	-(sin67.5°)*s	26.78	-64.67
19	(cos90°)*s	-(sin90°)*s	0	-70
20	-(cos67.5°)*s	-(sin67.5°)*s	-26.78	-64.67
21	-(cos45°)*s	-(sin45°)*s	-49.49	-49.49
22	-(cos22.5°)*s	-(sin22.5°)*s	-64.67	-26.78
23	-(cos0°)*s	-(sin0°)*s	-70	0
24	-(cos22.5°)*s	(sin22.5°)*s	-64.67	26.78
25	-(cos45°)*s	(sin45°)*s	-49.49	49.49
26	-(cos67.5°)*s	(sin67.5°)*s	-26.78	64.67
27	(cos90°)*s	(sin90°)*s	0	70
28	(cos67.5°)*s	(sin67.5°)*s	26.78	64.67
29	(cos45°)*s	(sin45°)*s	49.49	49.49

Example of calculation In column 2 and 3



(d)

Figure F.3 Dimensions of the dual ring ground vias. a) Overview of the ground via model design. b) Location of the ground vias. c) Coordinates of the inner ring ground vias. d) Coordinates of the outer ring ground vias (cont.)

TRL calibration pattern design

All details about designing TRL calibration patters have been explained in Section 3.2c. In Figure F.4, the design of the current test vehicle and directions for improving the current design are presented.

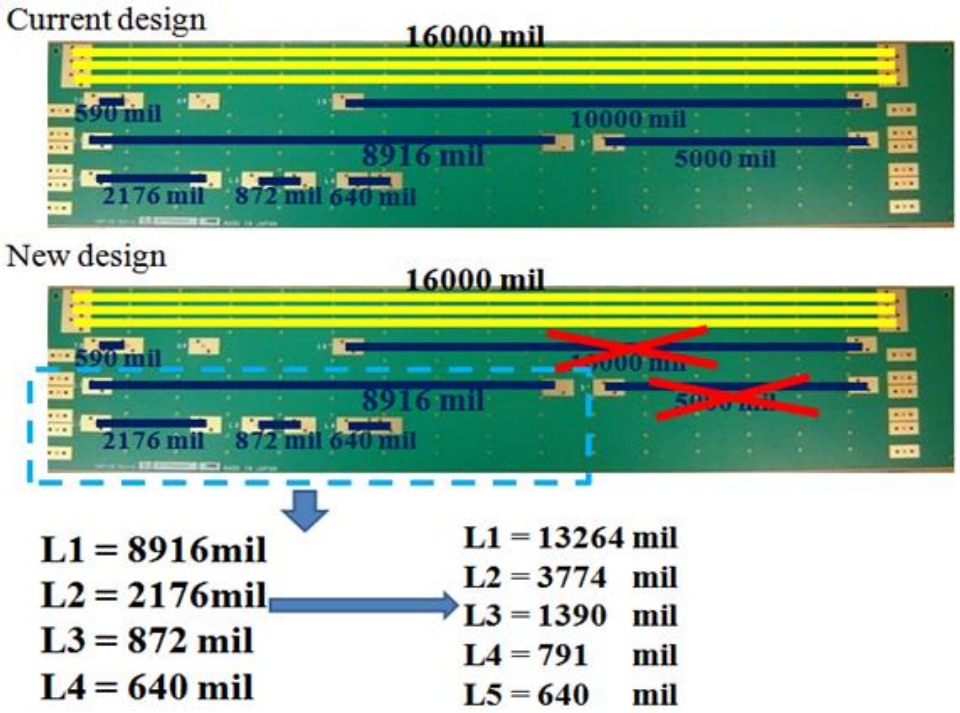
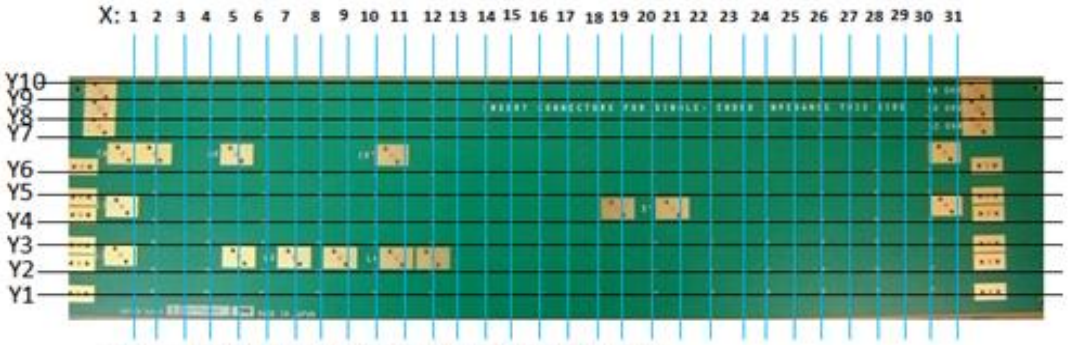


Figure F.4 Overview of the current PCB design and possible changes for developing new test vehicle design

Ground via wall design

As is mentioned in Section 3.2d, the via wall in the new test vehicle will either have an aperiodic structure, or there will be no via wall at all. For the test boards with aperiodic structure, information about the via wall design is presented in Figure F.5. The size and dimension of each ground via are the same as in the current PCB test vehicle design, only location will be different. The coordinates are calculated using the random (Gaussian) distribution with the mean value being equal to 0.5 inches and standard deviation being not greater than 0.2 inches.



Z coordinates for all via in via wall are the same
Y coordinates for all via in via wall are the same

Changes:

1) Instead 15 columns of via there are 31 column

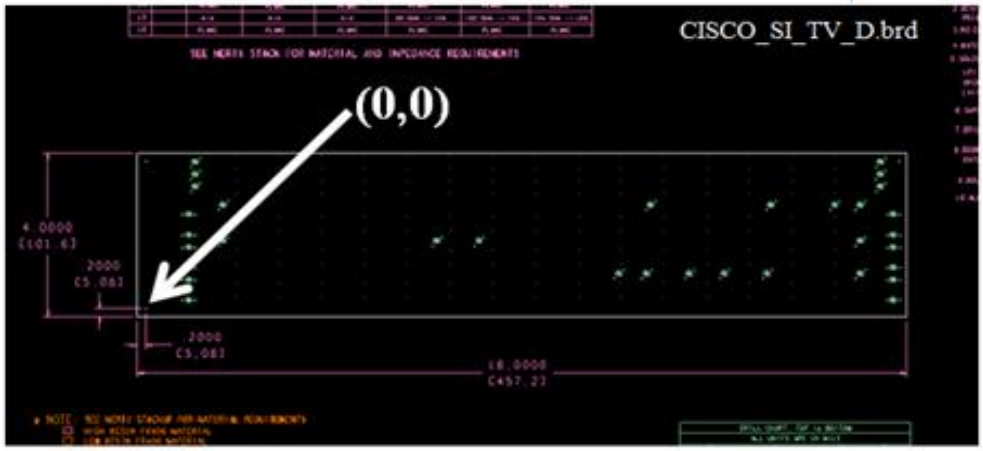
2) Coordinates of points, according image above

(x1,y10)(x2,y10 (x3,y10)(x4,y10)(x5,y10)(x6,y10) .... (x31,y10)
(x1,y9) (x2,y9) (x3,y9) (x4,y9) (x5,y9) (x6,y9) .... (x31,y9)
(x1,y8) (x2,y8) (x3,y8) (x4,y8) (x5,y8) (x6,y8) .... (x31,y8)
.....
(x1,y1) (x2,y1) (x3,y1) (x4,y1) (x5,y1) (x6,y1) .... (x31,y1)

(a)

According coordinates from previous design, this coordinates have been recalculated

X1 = 1600 mil	X17 = 9400 mil	X9 = 5490 mil	X25 = 13360 mil	Y10 = 3725 mil
X2 = 2290 mil	X18 = 9770 mil	X10 = 5950 mil	X26 = 13850 mil	Y9 = 3425mil
X3 = 2780 mil	X19 = 10280 mil	X11 = 6200 mil	X27 = 14460 mil	Y8 = 3125 mil
X4 = 3200 mil	X20 = 10680 mil	X12 = 6760 mil	X28 = 15180 mil	Y7 = 2825 mil
X5 = 3450 mil	X21 = 11340 mil	X13 = 7060 mil	X29 = 15240 mil	Y6 = 2225 mil
X6 = 3780 mil	X22 = 11750 mil	X14 = 7590 mil	X30 = 16090 mil	Y5 = 1875 mil
X7 = 4310 mil	X23 = 12250 mil	X15 = 8340 mil	X31 = 16670 mil	Y4 = 1425 mil
X8 = 4890 mil	X24 = 12690 mil	X16 = 8960 mil		Y3 = 1075 mil
				Y2 = 625 mil
				Y1 = 275 mil



(b)

Figure F.5 Information about location of the via wall and coordinates for each of the ground via. a) Overview of the location. b) Coordinates (x and y) for each ground via.

APPENDIX G.

MEASURING PROCEDURE OF DIELECTRIC PARAMETERS USING SPLIT POST DIELECTRIC RESONATOR TECHNIQUE

Two measurement procedures using SPDRs [20]

Split-post dielectric resonators (SPDRs) manufactured by the company QWED (Poland) are intended for determination of complex permittivity of materials. For some resonators, this requires two precise measurements of the resonance frequency and Q-factor: in the presence and absence of the dielectric sample under test. Once resonance frequencies, Q-factors, and dimensions of the sample are measured, appropriate computations have to be performed using software provided QWED. There are two ways of performing the calculations.

The users who have an access to one of the PNA/ENA Series network analyzers by Agilent Technology equipped with 85071E Material Measurement software with option 300, simply upload software files from the Agilent directory to the network analyzer. Agilent directory is available on the CD disk attached to the resonator. The final results are shown directly on the network analyzer display. Detailed information about the measurement procedure with SPDR and the above software version is provided by Agilent.

The users working with different network analyzer configurations need to upload QWED software and the results of network analyzer measurements on a standard PC computer. The final results are shown on the PC display. Detailed information about the measurement procedure for this case is provided below.

Measurement procedure with network analyzer and PC:

This method is being used in the current project for measurements at 10 GHz, 15 GHz, and 20 GHz. Techniques are the same, the only differences are operating frequency and sample dimensions. In the current Appendix, the step-by-step procedure is presented.

The required equipment presented on Figure G.1:

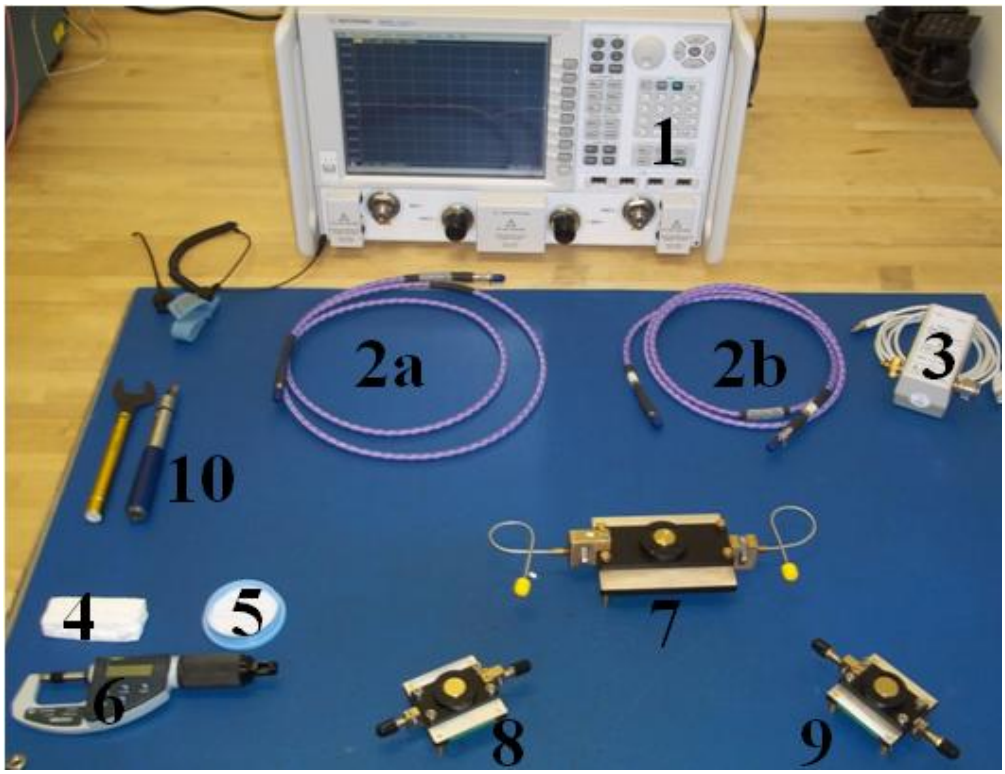


Figure G.1 measurement setup.

- Agilent VNA 50Ghz (1)
- 2 precision cables, 2.4 female – 3.5 female (2a, 2b), possible adaptors
- E-calibration kit – Agilent N4691-60004 300kHz-26.5GHz(3)
- Sample holder for thickness measurements (4)
- Standard material – fused silica(5)
- Micrometer Mitutoyo #227-211 (6)
- SPDR 10 GHz (7)
- SPDR 15 GHz (8)
- SPDR 20 GHz (9)
- Torque wrenches 09-10, and torque wrench 5/16 (10)

Sample preparation and thickness measurement

The sample under test needs to be cleaned applying puff with ethanol 92% alcohol. Put the sample in the sample holder (part 4 on Figure G.1) and using a micrometer (part 6 on Figure G.2), as shown on Figure G.2, measure the thickness in 6-9 different locations on the sample. Very important requirements for the thickness measurement are to hold the micrometer and sample perpendicular to each other, and to properly set up the force of the micrometer.

Figure G.2 Sample thickness measurement

For calculations, average thickness of the sample, minimum thickness and maximum thickness would be used.

Calibration

Connect two precision cables (2a and 2b on Figure G.1) to port 1 and port 2 of Agilent 50-GHz VNA. The cables must have 3.5mm female connectors at the end which is not connected to VNA.

Connect E-calibration kit to USB port of 50-GHz VNA using USB cable and wait for about 5 minutes, until the light indicator ‘ready’ is green.

When E-calibration would be ready to operate, set the frequency range of the measurements, number of sweep points, and averaging:

Press button ‘Sweep’ on the VNA interface, choose ‘Number of points’, input 6401, and press button ‘OK’;

Press button ‘Freq’ on the VNA interface, choose ‘Start’, input 7GHz, press button ‘OK’, then choose ‘Stop’, input 25GHz, and press button ‘OK’.

Press button ’Avg’ on VNA interface, choose ‘Averaging ON’, input 16 and press button ‘OK’.

After that, the measurement setup should be such as:

Start frequency – 7 GHz

Stop frequency – 25 GHz

Number of point – 6401

Average – 16

For performing E-calibration:

Press interface button ‘Cal’, choose ‘Start cal’, and then ‘Cal wizard’. In the new dialog window, choose option ‘Use Electronic Calibration (ECal)’, and press ‘Next’, as shown on Figure G.3.

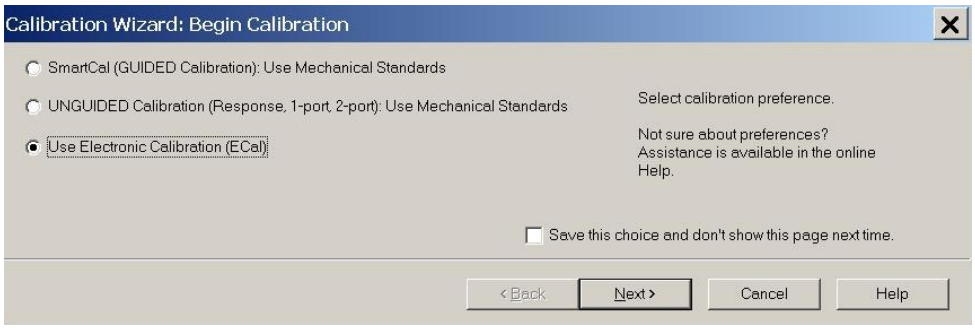


Figure G.3 E-calibration, step 1

In the next dialog window choose ‘2 Port Ecal’, and click ‘Next’ (Figure G.4).

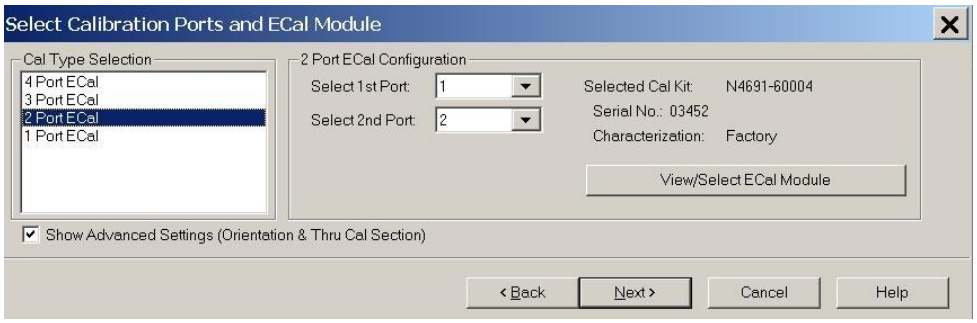


Figure G.4 E-calibration, step 2

Then VNA is supposed to detect the E-calibration kit which has been used. The operator has to choose ‘APC3.5 male’ in Port 1 as well as in Port 2. Then click ‘Next’, as presented on Figure G.5.

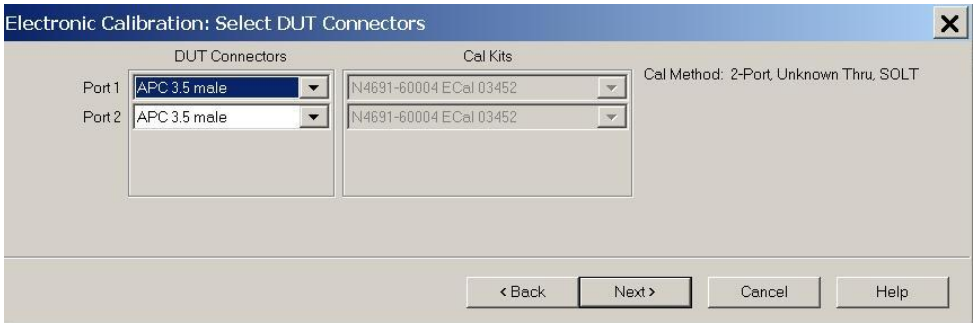


Figure G.5 E-calibration, step 3

Make sure that the new dialog window is the same as indicated on Figure G.6. Then press ‘Next’.

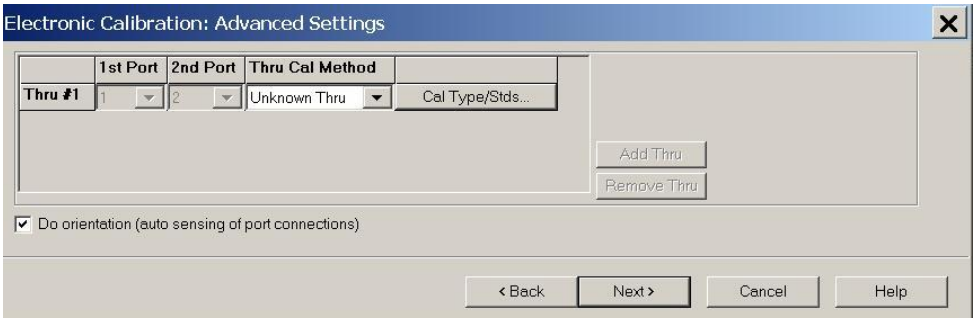


Figure G.6 E-calibration, step 4

According to the calibration procedure, at the next step, Port 1 has to be connected to E-calibration kit (Figure G.7). Then, Port 2 needs to be connected to E-calibration kit (Figure G.8), and finally, Port 1 and Port 2 must be connected to each other using ‘3.5 mm male to 3.5 mm male’ adaptor (Figure G.9).

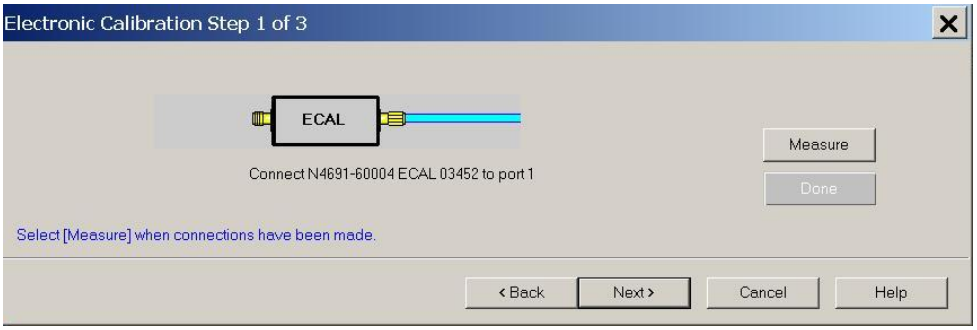


Figure G.7 E-calibration, step 5

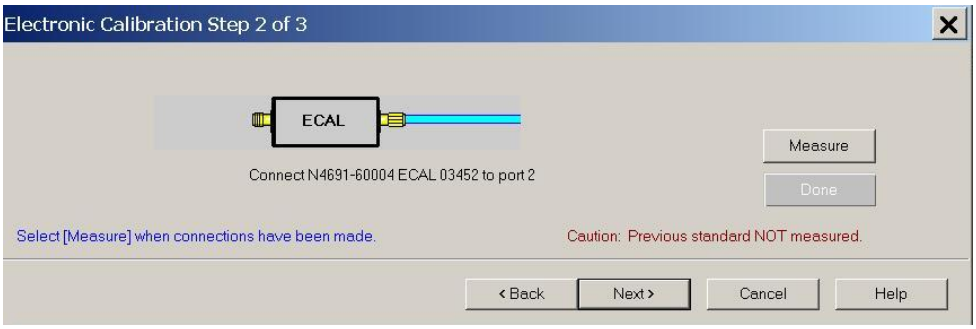


Figure G.8 E-calibration, step 6

Figure G.9 E-calibration, step 7

After performing E-calibration, the calibration plane for measurement would be set at the end of the cable connectors or adaptor, if that was a part of the calibration setup.

Performing measurements

The measuring procedure presented in the current section remains the same for SPDR of any operating frequency.

Connect SPDR to VNA using 2 precision cables. It is very important to make sure that the connectors on the cables match in diameter with the connectors on SPDR. For better stability of the measurement setup, it is recommended to use fix cables and SPDR, since semi-rigid cable, which are parts of the SPDR, are very sensitive.

Enable option S_{21} magnitude of the VNA, by pressing interface button ‘Meas’, and choosing S21.

Set the center of frequency band to nominal operating frequency of used SPDR. Operating frequency of the SPDR is usually labeled on the other side of the SPDR.

Enable 3dB bandwidth calculation on the VNA by clicking on the main menu ‘Marker/Analysis’, choosing ‘Marker Search’, and clicking ’Bandwidth’, as shown in Figure G.10. That brings up two additional markers (numbers 3 and 4) and provides automatic estimation of Q-factor.

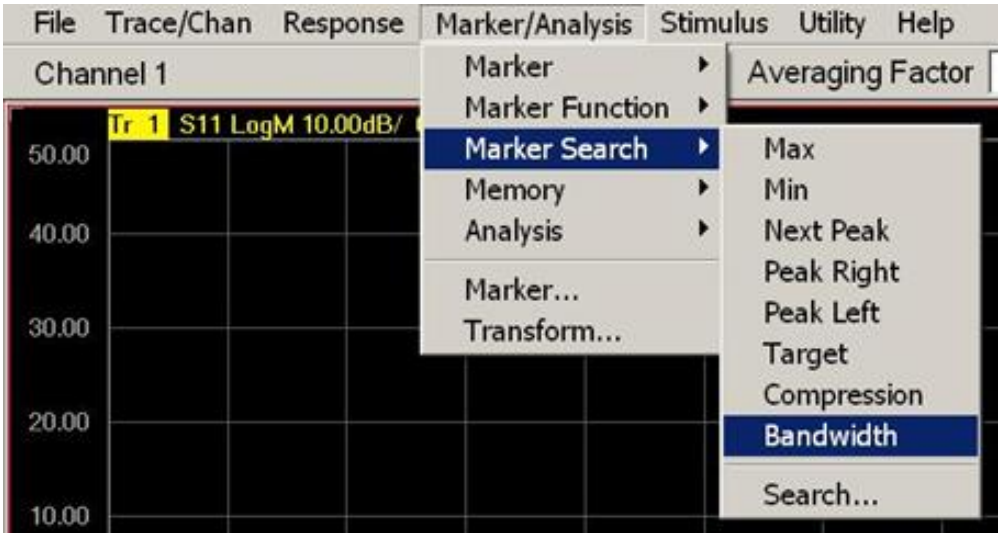


Figure G.10 Set up the 3dB bandwidth analysis

Choose a logarithmic scale of the vertical axis and set the value of division to 1 dB. When the maximum of the resonance curve is moved to reference position, markers 3 and 4 would define the 3 dB bandwidth. All necessary information would be indicated in the top left corner. Proper S21needs to be such as that in Figure G.11.

Switch to measurement of S_{11} magnitude and read the minimum value of S_{11}. Take a note of this minimum value. Repeat the measurement for S_{22}. Compare minimum

values of S_{11} and S_{22}. They need to be similar (ignoring differences smaller than the second decimal place). If they differ, adjust the position of coupling loops by rotating nuts of the SPDR, indicated in Figure D.12

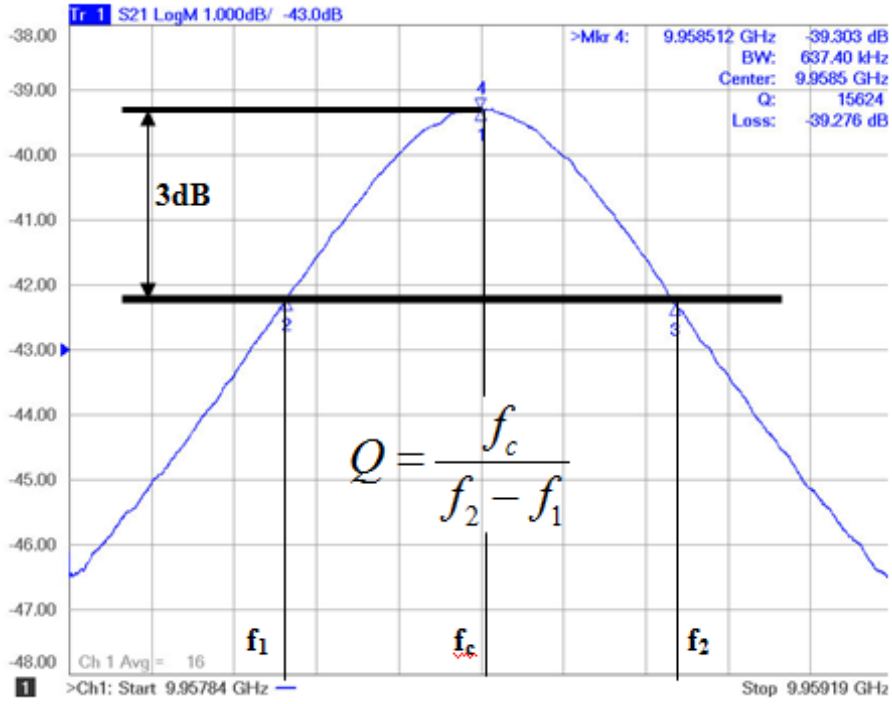


Figure G.11 Example of proper adjust SPDR coupling loops, S_{21}

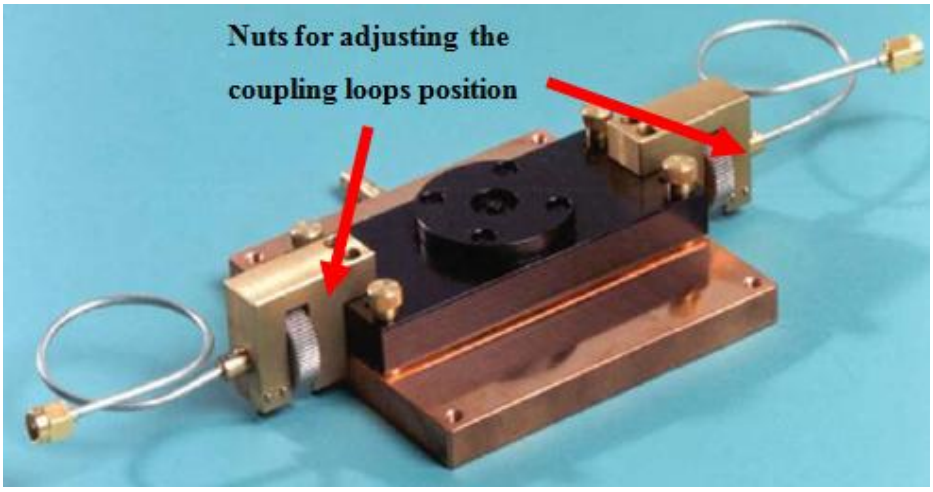
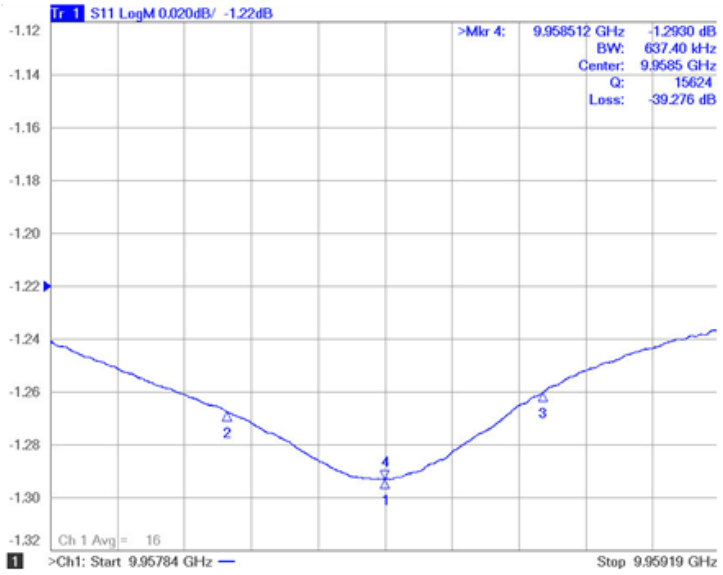
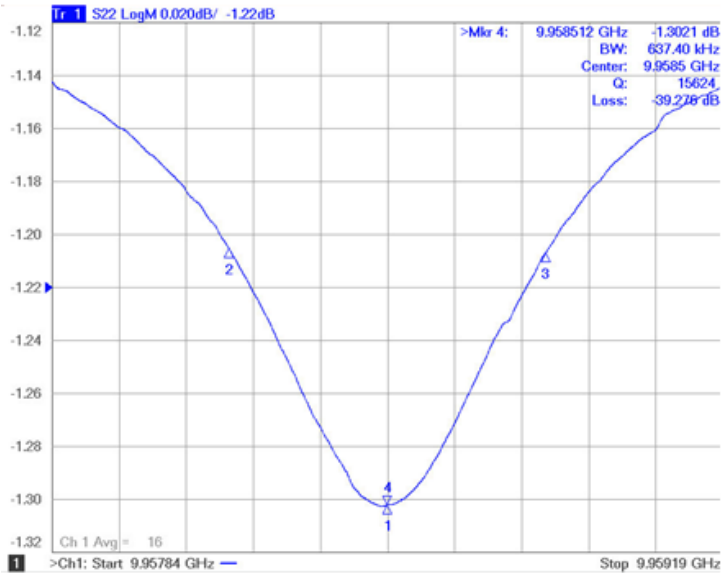


Figure G.12 Indication of SPDR nuts used for adjusting coupling loops

A more effective way to adjust coupling loops for matching S_{11} and S_{22} magnitudes is to move both nuts at the same time, trying to reach the average value. Well adjusted coupling loops have matching magnitudes of S_{11} and of $S_{22.}$ Magnitude of S_{21} should be around -40 dB level. S_{11} and S_{22} are presented in Figure G.13.



(a)



(b)

Figure G.13 Example of proper adjusted SPDR coupling loops. a) S_{11}. b) S_{22}

After getting proper values for S_{11}, S_{22}, and $S_{21,}$ data of the empty resonator can be collected.

Switch back to S_{21} magnitude measurement. Define span value (frequency band) to be not more than 30% beyond the limits of the 3dB bandwidth. In the top right corner of the display, the resonance frequency and Q-factor need to be collected as parameters of the empty resonator.

Without touching the measurement setup, place the standard sample, fused silica, into the cavity through the slot at the center of the resonator. The sample inserted into the cavity causes a shift of the resonant frequency and decreases the Q-factor. Increase the span to enable location of the resonant curve maximum. Then, move maximum of the resonant frequency to the center of the screen. Decrease the span to be not more that 30% beyond the limits of the 3dB bandwidth.

Collect measured resonant frequency and Q-factor of the resonator with fused silica.

After that, any material sample, matching the size of the SPDR, can be measured, repeating steps h) and i).

After collecting measured data for all investigated samples, all data would need to be transferred to PC with QWED software installed. The resonant frequency and the Q-factor of the empty resonator, the resonant frequency and the Q-factor of the resonator with loaded sample, and the thickness of each sample are the initial data, which need to be used as input.

It is good practice to calculate DK and DF first, for the fused silica, because dielectric parameters of the standard are well known. Matching of the results could be a

good indicator of properly executed measurements. If DK and DF of fused silica differ more than 15%-20%, measurements would need to be redone.

Conversion of measured data to material data using QWED software [20]

To run the software for calculation of dielectric properties of measured samples for the first time, please insert a CD disk supplied with the resonator to the CD drive of your computer. The initial screen should appear automatically. If the initial screen does not appear, go to the main CD disk folder and run '*start.exe'* file.

The view of the initial window is shown in Figure G.14. The window enables two options: '*Manual'* and '*Software Setup'*. The '*Manual'* button will enable reading of user guide for measurement and calculation procedure using Split Post Dielectric Resonator. To read the manual, Adobe Reader has to be installed on your system.

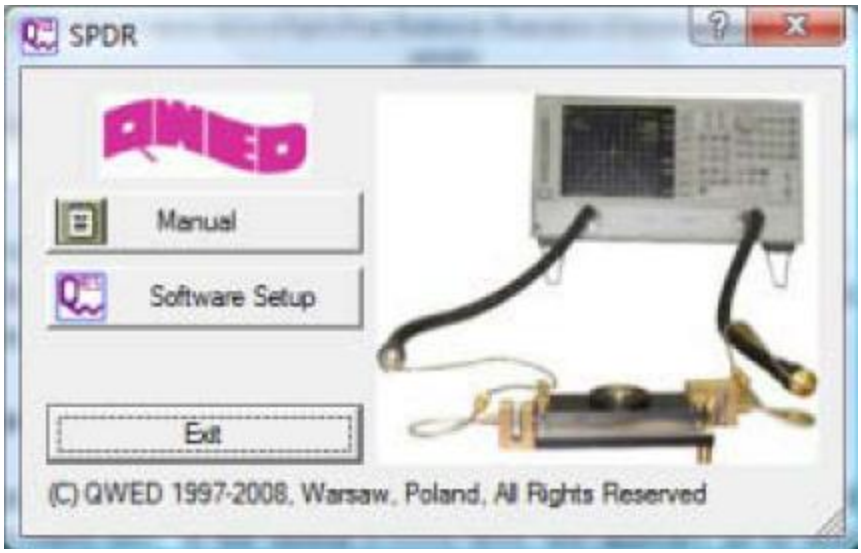


Figure G.14 Initial window which appears during first run of the software

The '*Software Setup'* button will prepare the software for the first run. When the '*Software Setup'* button is pressed, the '*Browse For Folder'* window (Figure G.15) appears. To choose the folder, browse the tree of folders and mark selected. To make a

new folder in chosen folder, press '*Make New Folder'* button and insert the name of the folder being created.

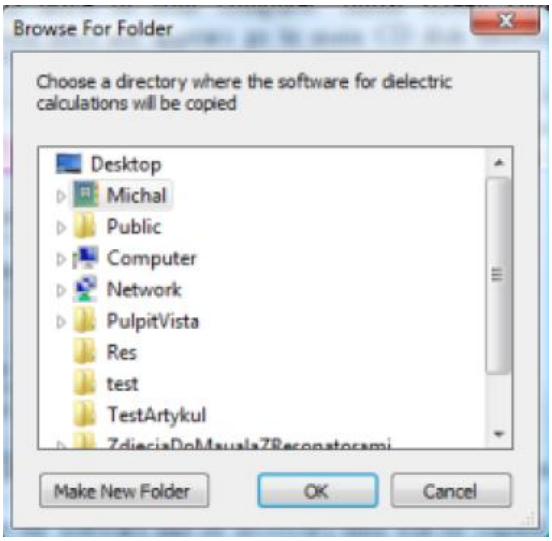


Figure G.15 Browse for folder window

When the folder is finally chosen, press '*OK'* button to copy the files. A progress bar will appear and inform the user of the status of copy operation. When the files are successfully copied, the dialog window appears (Figure G.16). If you want to run the software later, press the '*NO'* button inside this window. For any further run of the software, refer to the directory where the software was copied and run *SPDR.exe* file. If you decide to run the software now press the '*OK'* button.

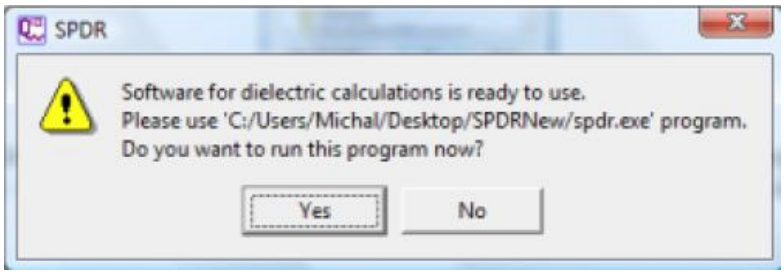


Figure G.16 Dialog window with information about the software directory

The main software window is shown in (Figure G.17). The name '*R1093.exe invoked'* (only for 10 GHz SPDR, for 15 GHz and 20 GHz different frequencies are invoked) from the top left corner of the main software window denotes the additional software module which takes part during the calculation of dielectric properties of the measured sample. The number *1093* from the above name is a nominal operating frequency of your Split Post Dielectric Resonator, expressed in MHz. The values of the resonant frequency and the Q-factor of the empty resonator are inserted to editable areas below the name of each parameter of '*Empty Resonator'* group. The value of resonant frequency has to be expressed in MHz. To add the values of resonant frequency, the Q-factor of the resonator with the measured sample and the sample thickness press '*Add'* button from '*Resonator with Sample'* command group.

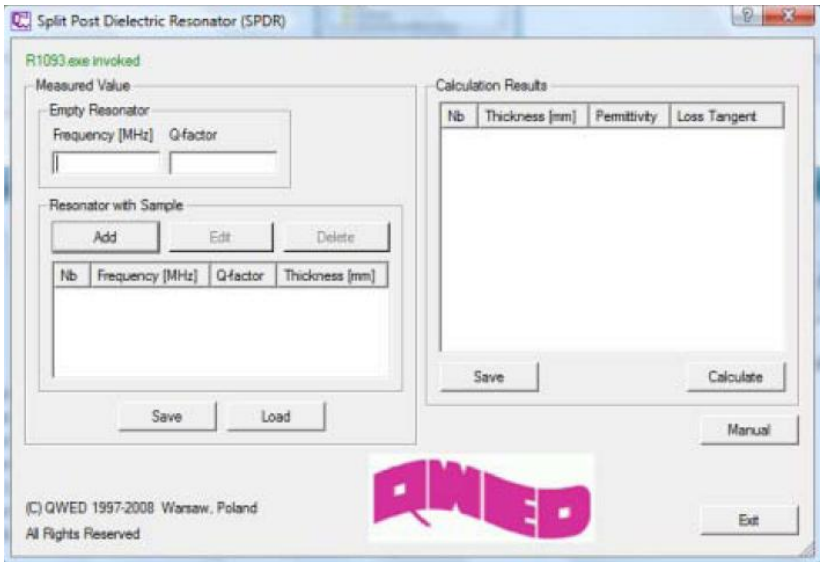


Figure G.17 Main window of the software for calculation dielectric parameters

When the '*Add Parameters'* (Figure G.18) dialog window appears, insert the measured values to the editable areas below the name of each parameter. The value of

resonant frequency has to be expressed in MHz. The thickness of the measured sample has to be expressed in millimeters. Press '*OK'* to accept the changes.

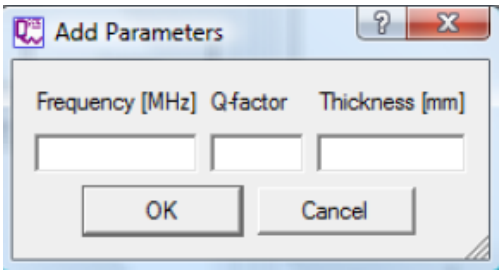


Figure G.18 Add parameters dialog window

The user can add values of resonant frequency and the Q-factor of the resonator with the measured sample and thickness of the sample from one or several measurements. The added parameters are automatically displayed on the list located in '*Resonator with Sample'* command group. Each parameter can be edited and changed using the '*Edit'* button from '*Resonator with Sample'* command group. To delete inserted values, mark the value and use the '*Delete'* button. The inserted values for the empty resonator and the resonator with investigated sample can be saved to the text file using the '*Save'* button from '*Resonator with Sample'* command group. To load from a file of previously saved data, use the '*Load'* button.

To perform calculation, press '*Calculate'* from *Calculation Results* command group, located on the right hand side of the main window. The calculated results will be displayed on list located in *Calculation Results* command group. The calculated dielectric properties of measured material can be saved to text file using the '*Save'* button.

The ‘*Manual’* button will enable reading of the user guide for measurement and calculation procedure using Split Post Dielectric Resonator. To read the manual Adobe Reader has to be installed on your system.

The ‘*Exit'* button closes the software for calculation.

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