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A Thermal-aware DC-IR Drop Analysis for 2.5D IC

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***Abstract*— With the trend of higher integration, 3D/2.5D IC solutions such as CoWoS (Chip-on-wafer-on-substrate) have become more popular in recent years. Power integrity (PI) is always a critical part of the design especially when the power consumption requirements are important specs for high-performance computing. DC-IR drop is one of the criteria within power integrity considerations. However, ordinary electrical-only simulation for DC-IR drop will be an underestimation because it neglects the copper conductivity dropping due to the temperature rising. Thus, an engineering solution for electrical-thermal co-simulation is important to help to provide both an accurate PI analysis and the proper mitigations of the IR drop along the power rails. This paper uses a 2.5D IC chiplet as an example to conduct the thermal-aware DC-IR simulation workflow. By iterating and exchanging the power map and temperature map files between an electrical simulator and a thermal simulator, detailed layer-by-layer IR drops and the temperature map results can provide good insights for efficiently mitigating the IR drop for PI by establishing a better cooling condition in thermal solution.**

Keywords*— DC-IR, thermal, 2.5D IC, package, chiplet, interposer, co-simulation.

I. INTRODUCTION

With the increasing demands on high-performance computing capabilities, cutting-edge technologies have adopted more advanced packaging techniques such as CoWoS (Chip-on-wafer-on-substrate) to enable 3D/2.5D solutions [1]. Thus, aggressive I/O density and higher bandwidth channels will be available. With the capacity of higher-density interconnections in the interposer layer, chiplet has become a popular choice in the post-Moore era [2]. Inevitably, these innovations bring up more challenging designs to ensure the proper functionalities such as signal integrity and power integrity (SIPI) [3]. Power integrity (PI) is an important consideration in the system design for the robustness of the functioning device. Although power distribution network (PDN) design has been well studied over the past years on the printed circuit board (PCB) level, it becomes more challenging when it comes to the package level or even chip level, especially when utilizing advanced packaging. Besides the control of the voltage ripples on the power rails by looking into the frequency-domain performance [4], voltage droop is also one of the critical criteria for PI consideration to keep a stable voltage supply level to the integrated circuits (ICs). Voltage droop happens when the load changes along the power rails. Due to the resistance along the power rails, when the current loading increases, the voltage drop in the path will increase accordingly, which creates a voltage droop at the supply point to the ICs. Although this issue has been aware of for a long time and there are mature solutions to it such as using the voltage sensing pins to monitor the supply voltage level and dynamically adjust the power management IC (PMIC) or voltage regulator module (VRM) output to compensate for the path loss. A good PDN design also helps to mitigate voltage fluctuations. However, due to the slow response of the PMIC to react to a transient response and finite PDN impedance, the voltage droop cannot be completely eliminated although those solutions will limit the fluctuations within a certain range.

Therefore, the DC-IR simulation is always one of the important steps in the design sign-off because no matter whether the system is equipped with the sensing feedback loop or not, mitigations on the resistance along the power rails will always have a positive impact on PI. Electrical-only DC-IR simulations analyze the IR-drop assuming an ambient temperature condition (by default usually 20 Celsius degrees). Unfortunately, this will be an underestimation because it neglects the copper electrical conductivity decreasing due to the temperature rising. Thus, the Multiphysics simulation methodologies for complicated system design also have become more and more critical. Researchers have spent efforts developing Multiphysics computational algorithms to simulate the scenarios [5][6][7]. However, for industrial usage, engineers have a higher preference for matured commercial simulation tools in the design flow. Conventional thermal-aware DC-IR simulation will run a thermal simulation for the system including the PCB. Then the temperature map will be imported to conduct the DC-IR simulation. However, this workflow has some drawbacks/limitations.

In this paper, instead of using the conventional method, an enhanced engineering workflow using the existing commercial simulation tools will be discussed for this co-simulation. From the result analysis, the accuracy improvement will be compared to electrical-only and conventional co-simulation analysis. Furthermore, based on the results, IR-drop can be further mitigated by adopting a proper cooling solution. Thermal treatment measures can improve electrical performance in the end.

II. Realistic DC-IR Drop With Temperature Considered

As discussed, thermal-aware DC-IR simulation is critical for achieving higher accuracy, which needs the temperature map as the input. According to Fourier's law, thermal conductivity is associated with the proportional heat flux versus temperature gradient:

$$\vec{q} = -\vec{\kappa} \cdot \nabla T \tag{1}$$

where $\vec{q}$ is the heat flux, $\vec{\kappa}$ is the material thermal conductivity, and T is the temperature. The heat flows from the hot to the cold environment, so there is a negative sign in equation (1).

For planar structures like PCBs, the thermal conductivity is represented in the orthotropic type:

$$\vec{\kappa} = \kappa_x \hat{x} + \kappa_y \hat{y} + \kappa_z \hat{z} \tag{2}$$

A. Simplified Thermal-aware DC-IR Simulation Limitations

For the simplified thermal simulations, devices and components considered usually include: PCB, heatsink, cooling fan, chassis, etc. In most cases, heat sources in the electronic systems will only include the ICs (e.g. CPU, PMIC/VRM). The ICs are usually simplified as blocks with certain heat dissipation power ratings. The PCBs, unlike in electrical simulations, are often treated as layered structures with blurred information about routings. As a result, the horizontal thermal conductivity will be considered equal, and be determined by the layered copper percentage and the stack-up. A similar treatment is applied to package substrate modeling.

However, this simplification will introduce errors in two aspects: 1) The actual thermal conductivity map on each layer determined by the detailed layout is different from the approximated horizontally uniform one; 2) Vias are good vertical thermal conduction paths but are neglected in the modeling. Thus, more detailed modeling is preferred. Besides the simplification of the modeling, the one-way thermal-to-electrical simulation workflow is not perfect. As Fig. 1 shows, when the major heat sources (such as ICs) are captured in the thermal simulation, the temperature rises and affects the copper electric conductivity, then, the IR drop becomes severer. However, further temperature rising caused by Joule heating and further IR-drop caused by heating are not included if only a one-way simulation is conducted. Therefore, to obtain more accurate estimations, a more complicated two-way coupling co-simulation is needed.

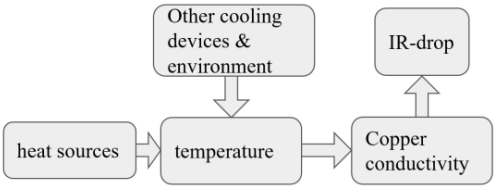


Fig. 1. Demonstration of simplified electrical-thermal DC-IR simulation.

B. Improved Thermal-aware DC-IR Simulation Workflow

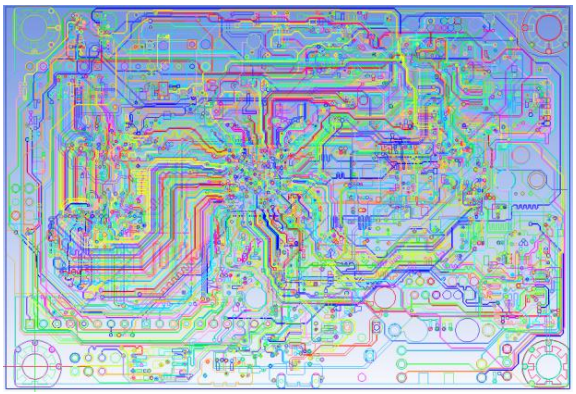


Fig. 2. Imported ECAD example for PCB including geometry and thermal conductivity information.

Based on the discussion in Part A, the improvements of the co-simulation are done in two aspects: more accurate modeling and a more complete simulation workflow. The ordinary modeling method for PCB and package substrate usually assumes uniform thermal conductivity in the directions. In other words, $\kappa_x = \kappa_y = \kappa_{h0}$ and $\kappa_z = \kappa_{v0}$ in (2), where κ_{h0} and κ_{v0} are constant coefficients determined by the copper percentage and stack-up. As Fig. 2 shows, the PCB can be imported into a thermal simulator (Ansys Icepak in this work) with a detailed ECAD model (here an example case was used for demonstration purpose without reveal confidential information). When the trace routing and via information are included, a more detailed representation will be available:

$$\overrightarrow{\kappa_{(x,y,z)}} = \kappa_{x_{(x,y,z)}} \hat{x} + \kappa_{y_{(x,y,z)}} \hat{y} + \kappa_{z_{(x,y,z)}} \hat{z} \tag{3}$$

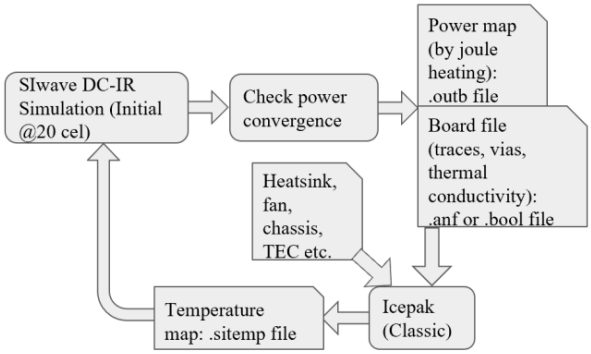


Fig. 3. Improved two-way coupling co-simulation workflow.

For the other aspect, the co-simulation workflow can be refined by two-way iterating between electrical and thermal simulations. As Fig. 3 demonstrates, the initialization starts from a DC-IR simulation assuming ambient temperature - 20 Celsius degrees. Besides the ECAD files for PCB and package substrate, power maps caused by the Joule heating from IR-drop will be imported as the additional distributed heat sources. The Joule heating power map of layered structures like PCB and package substrate can be treated similarly as Fig. 4 shows. Then a thermal simulation will be conducted (this work in

Ansys Icepak) and a temperature map will be updated and imported into an electrical simulator (e.g. Ansys SIwave), and repeat the DC-IR simulation. Thus, iterations between the two simulators will keep running until reaching a convergence. For illustration purpose, the convergence criteria used here was set to be 1% in Joule heating power differential between two consecutive sets. One may use other percentages rather than 1%, or the observation of the temperature as the convergence criteria, according to the applications and user's requirement. This two-way coupling workflow enables thermal-aware IR-drop analysis with better accuracy. Also, this methodology takes full advantage of the existing commercial simulation tools without the requirement for a real multi-physics computational solver.

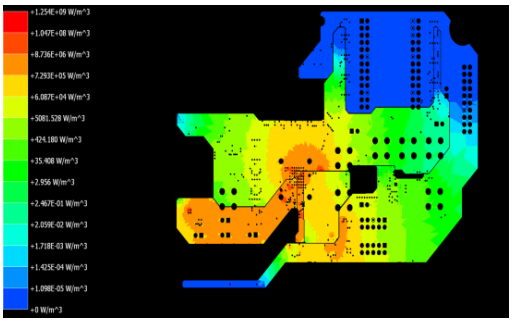


Fig. 4. DC-IR Joule heating power maps: (a) Joule heating power density on PCB (a portion on layer 2); (b) power map on a package substrate (a portion on layer 3).

The focus of this section is the demonstration of the co-simulation workflow, so only PCB and package substrate are used. However, this workflow is still effective to investigate even more complicated scenarios. It is also worth mentioning that some simulation tools such as SIwave have implemented the thermal solver inside to consider the effect. However, the functionalities are still limited by at least two aspects: lacking the capability for more complicated components/devices modeling such as fans, chassis/frame, TEC (thermoelectric cooling), and lacking the complete fluent solver to enable both laminar and turbulent flow regime when convection is an important factor for cooling.

To demonstrate the improvement of accuracy in both electrical and thermal aspects, a simplified case is adopted with only PCB, package substrate, and a flip-chip die landing directly on the substrate. In this example, the die is considered to be a uniform block with 0.5-Watt power dissipation for illustration purpose. For other applications with either higher power dissipation or larger die size, this methodology will follow the same workflow but just change the power dissipation rating or use a detailed die map in the simulations. Forced convection 1 m/s air flow from +x direction is applied. For the advanced simulation methodology, both the die dissipation and the DC-IR Joule heating (only one power rail enabled for simplification) are taken into consideration, and the coupling between IR-drop and temperature change is achieved by iterating between the electrical and thermal simulation tools. Moreover, the PCB and package substrate are treated as discussed with detailed geometry information in thermal simulation to enable a more accurate representation of the thermal conductivities. To make the comparison, the simplified conventional simulation flow is conducted, where the electrical-thermal coupling is ignored due to the one-way simulation workflow. Besides the methodology, the PCB and package substrate in the thermal analysis are treated as equivalent blocks with orthotropic thermal conductivities determined by the stack-up and copper percentages.

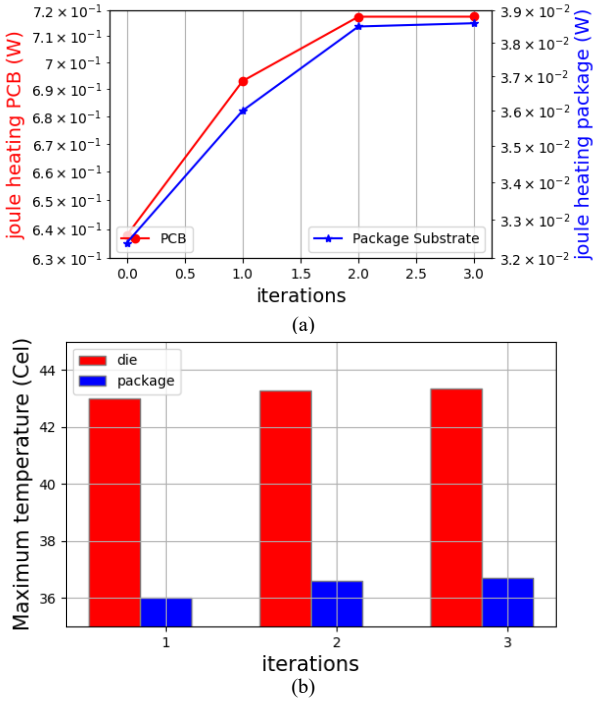
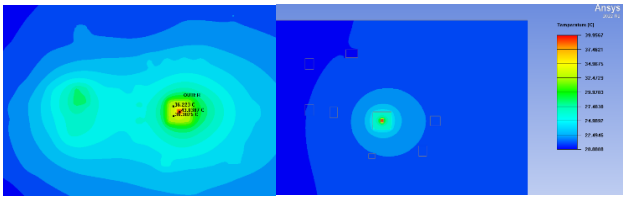


Fig. 5. Two-way iteration convergence: (a) SIwave: Joule heating caused by IR-drops (b) Icepak: peak temperatures.

As Fig. 4 shows, for the proposed simulation workflow, the initial DC-IR simulation annotated as iteration 0 is under the condition of 20 Celsius degrees ambient temperature environment. Then by updating the temperature maps and Joule heating maps, both the temperature and Joule heating will increase until reaching convergence. The converged Joule heating due to IR-drop increases by about 9 % compared to the initial value. And the maximum temperature has close to a 1 Celsius degree difference after taking the IR-drop heating fully into consideration. Therefore, taking the electrical-thermal coupling effect into account, both IR-drop and temperature estimations are more accurate. The eventual temperature map is shown in Fig. 6. (a). However, if everything keeps the same except for the simulation flow and the modeling method as

mentioned before, then the temperature map is shown in Fig. 6. (b). It can be observed that not only the peak temperature shows differently. Due to neglecting the Joule heating of the traces and components (the second dominant hotspot is caused by a sensing 30 mOhm resistor placed in series on the power rail), the less dominant temperature rising in other areas will not be captured.



(a) (b)

Fig. 6. Comparison of the proposed workflow vs conventional one: (a) results of the proposed workflow (b) results of the conventional workflow.

TABLE I. COMPARISON OF THE IMPROVED AND CONVENTIONAL CO-SIMULATIONS

Method	Improved co-simulation (two-way coupling, detailed ECAD)			Conventional co-simulation (one-way coupling, uniform κ_x, κ_y, κ_z)			Electrical-only simulation		
Part	PCB	Package	Die	PCB	Package	Die	PCB	Package	Die
Maximum temperature (unit: Celsius)	30	36.7	43.4	23	33.8	40	20	20	20
Joule heating power by IR-drop (unit: W)	0.718	0.0386	N/A	0.677	0.038	N/A	0.638	0.0324	N/A
	Sum: 0.756			Sum: 0.71			Sum: 0.67		

The final simulation results for different methodologies are collected in Table. I. Notice that the recorded peak temperature values on PCB stand for the observation locations far away from the chip (because the power dissipation on the chip is typically the dominant heat source and naturally the hotspot will most likely be present beneath the chip). As Table. I summarizes, thermal-aware co-simulation is necessary as there is a noticeable difference in Joule heating caused by IR-drop shown between the electrical-only simulation result and the co-simulation result. However, with the thermal effect considered, the conventional one-way coupling method is still not accurate and has about a 6.5 % difference in IR-drop Joule heating power and about 3 Celsius degrees difference in temperature (much larger difference exception for PCB, because one-way coupling does not capture the Joule heating from the traces) compared to the proposed method. Also, it can be observed that the relative difference in IR-drop heating of the package substrate is smaller than that of the PCB. From the simulation results, the Joule heating caused by IR-drop on the package substrate only has a 1.5 % increase with a 3 Celsius degree temperature increase. Approximately, using the temperature-dependent copper resistance formula:

$$R_T = R_{T_0}(1 + \alpha_{copper}(T - T_0)) \quad (4)$$

where R_T and R_{T_0} are the copper trace resistances under temperature T and T_0, respectively. α_{copper} is the temperature coefficient for copper, $\alpha_{copper} = 0.00393$. With a 3 Celsius degree increase, the estimation on Joule heating increase using (4) is about 1.3 %, which is very close to the simulation results. Therefore, as the dimensions shrink down, the assumption that the thermal conductivities are uniform along axes respectively will be more reasonable and closer to the realistic situation. Thus, practically, the modeling for small-dimension parts may use blurred thermal conductivities while maintaining good accuracy.

III. THERMAL-AWARE DC-IR CO-SIMULATION ANALYSIS AND MITIGATION FOR 2.5D IC CHIPLET

As discussed in Section II, the improved co-simulation workflow has better performance in both electric and thermal aspects. The methodology is applied to a more complicated scenario with interposer and chiplet involved in this section, and the results before and after necessary cooling measures are given. Moreover, a detailed analysis is provided to understand the contribution and mitigation priorities among different portions of the entire system.

A. Modeling for 2.5D IC Chiplet

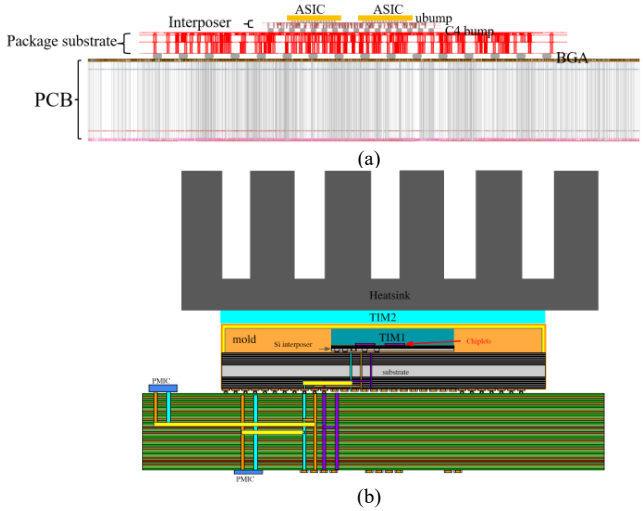


Fig. 7. Modeling explanation for the 2.5D chiplet: (a) explanation for the electric part modeling (b) complete modeling explanation for thermal aspect.

The more complicated system involves not only the PCB and package substrate, but the silicon interposer and multiple ASICs are also included as shown in Fig. 7. The interposer is placed between the dies and the substrate to provide higher-density interconnections for the chiplet. Thus, the entire DC-IR analysis will start from the PMIC/VRM on PCB as voltage source and end at micro-bumps (ubumps) to the ASICs as current sinks. As for the thermal simulation, as Fig. 7. (b) demonstrates, for PCB and package substrate parts, detailed ECAD models are used to enable the geometry-dependent thermal conductivities. ASICs are modeled as heat source blocks. For the package designs, thermal interface material (TIM) is also an important part and researchers have been investigating it [8]. Here the TIM1 is applied between the ASICs and the shielding can. Any void space inside the shielding can is filled with mold material. For additional cooling purposes, heatsink, fan, and other components/devices

may be added. This example uses the simplest scenario with an extruded-fin heatsink and a cooling intake fan included. Another TIM2 material is used between the base of the heatsink and the surface of the metal can.

It is worth mentioning the modeling of the interposer separately with more details. As discussed and concluded in Section II, when the dimensions are small, modeling the thermal conductivities with blurred geometry information is sufficient. For the silicon interposer design, since TSVs from the C4-bumps to the metal layers occupy most of the thickness [9] and go vertically upwards (usually several tens to one hundred microns for TSV, and several microns for each metal layer on top of that). The interposer is reasonably sliced into two pieces for the modeling. The thicker slice contains the through-silicon-vias (TSVs) which occupy a major portion of the entire thickness. And the thinner slice contains several metal layers and vias that eventually go up to the ubumps. Previous studies provide approximations of the TSV thermal conductivities determined by the diameter and pitch [10]. For engineering purposes, the equivalent thermal conductivities are expressed by the following empirical equations:

$$\kappa_{eq,z} = 150 + 180\,(D/P)^2 \tag{5}$$

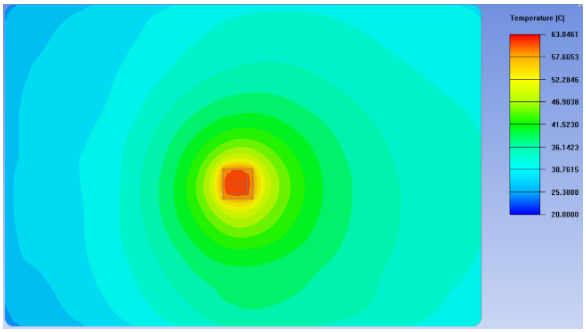
$$\kappa_{eq,x} = \kappa_{eq,y} = 150 + 105\,(D/P)^2 \tag{6}$$

where $\kappa_{eq,x}$, $\kappa_{eq,y}$, $\kappa_{eq,z}$ are annotated as the equivalent thermal conductivities orthotopically. D and P are the diameter and pitch of TSVs. The thinner slice with metal layers, vias, and ubumps will be modeled according to the stack-up and metal percentages on each layer. Thus, the modeling for the interposer has been properly implemented. As the simulation is conducted for the entire system within the computational domain, mesh generation will the done for all objects. The technique for modeling the interposer part described above will greatly reduce the meshing cells while maintaining good accuracy.

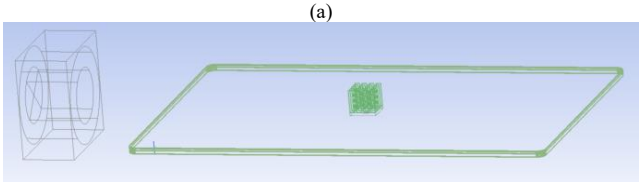
The modeling methods for all the portions have been covered and the system-to-chip level thermal-aware DC-IR simulation is ready.

B. DC-IR and Temperature Mitigation With Proper Cooling

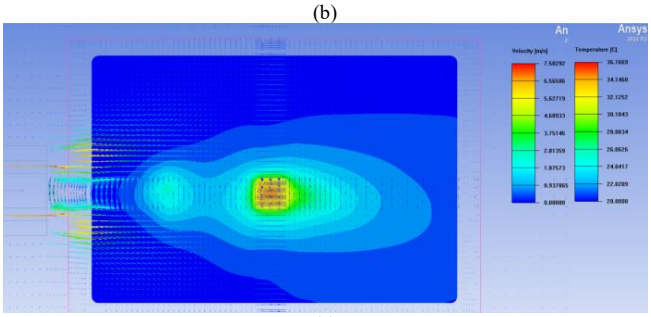
With all the necessary portions correctly modeled according to the descriptions in Part A, the PCB assembled with the IC was simulated under two conditions: one without additional cooling components (heatsink, TIM2, and fan) under natural convection; the other with those cooling devices to help heat dissipation under forced convection.



(a)



(b)



(c)

Fig. 8. Simulated results with 2.5D IC chiplet: (a) simulated board assembly without additional cooling (b) additional cooling components (c) simulated assembly with cooling components (both temperature and airflow)

The entire board assembly with a 2.5D IC chiplet was simulated without additional cooling devices. As shown in Fig. 8. (a), the temperature is high, especially at the ASICs location. The entire PCB temperature was also ramped up due to the heat conduction transfer from the sources. Of course, for proper operations, necessary cooling measures are needed to reduce the temperature. For a simple example, an extruded-fin aluminum heatsink, and an intake fan were added as described in Fig. 8. (b). Then the entire assembly was simulated again, and the final converged results are shown in Fig. 8. (c). The peak temperature at the IC dropped significantly.

TABLE II. DC-IR ANALYSIS OF CO-SIMULATIONS

	No additional cooling (ref)	With heatsink, TIM2, and fan	Difference
Maximum temperature (Celsius)	63.0	36.2	-23.8 (-38%)
IR-drop on PCB (mV)	91	81.6	-9.4 (-10.3%)
IR-drop on package substrate (mV)	6	5.2	-0.8 (-13.3%)
IR-drop on interposer (mV)	20.9	17.4	-3.5 (-16.7%)

The thermal-aware DC-IR simulations in SIwave for the mentioned two scenarios are concluded in Table II. Besides the dramatic drop in the temperature, it can be observed that the IR drops caused by different parts were also noticeable. Notice that the drop on PCB is abnormally large because of the sensing resistor on the rail for this test board. From the IR-drop levels and their relative percentages of the change due to cooling, it can be seen that the interposer draws significant IR-drop and is the most sensitive part to temperature change. This is a reasonable expectation due to the thinner metal width and thickness [11], higher temperature, and larger temperature variance. Therefore, it is critical to implement good thermal solutions for the electronic device's lifetime and safety and for better electrical performance such as DC-IR drop in PDN design. Moreover, if there is a criterion for the IR-drop sign-off, engineers can give a rough but quick prediction for the temperature requirements for cooling solutions, as the temperature-dependency of the metal electric conductivity has easy access online.

IV. Conclusions

This paper demonstrates an engineering electrical-thermal co-simulation methodology with better accuracy using matured commercial simulation tools. The two-way coupling iterations properly consider the effect of temperature rising on more IR-drop and the effect of Joule heating on temperature increase. Experience with proper modeling methods is discussed using the 2.5D IC chiplet example. Larger dimension parts are preferred to be represented in more detail and tiny parts such as interposers can be modeled more uniformly. The proposed methodology was applied to the chiplet case and the detailed DC-IR drops are analyzed with and without cooling. The interposer draws a noticeable IR drop and is more sensitive to temperature change. Therefore, the thermal solution is critical for better electrical performance, and an accurate thermal-aware co-simulation workflow is important to enable the IR-drop analysis and what-if predictions.

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