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Effective Roughness Dielectric in a PCB: Measurement and Full-wave Simulation Verification

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Abstract— Surface roughness topography of printed circuit boards (PCBs) needs to be included in SI simulations in order to accurately predict the insertion loss of the structure. An effective roughness dielectric (ERD) model can be used to substitute an inhomogeneous interface between copper foil and laminate dielectric in a PCB. Herein, this approach is tested for verification using 3D full-wave numerical simulations. These effective roughness dielectric layers with the appropriate complex permittivity are included in the modeling of stripline examples. The parameters of an ambient laminate dielectric free of conductor roughness effects in the stripline are determined using differential extrapolation roughness measurement teachnique (DERM). The agreement of the results of 3D full-wave modeling simulations with the proposed approach and measurements justifies the proposed approach.

I. Introduction

Designers of high-speed electronics, operating into the gigahertz frequencies, need to accurately predict dissipation and dispersion on transmission lines. Accurate characterization of laminate dielectrics on printed circuit boards is crucial for high-speed electronics designs. Conductors on printed circuit boards are deliberately roughened to aid the adhesion of the metal to the laminate dielectric. Adequate modeling of conductor roughness effects over a wide frequency range is known to be important for signal integrity.

II. Measurements and Effective Roughness Dielectric Approach

Traveling-wave stripline technique is used to extract dielectric properties of PCB laminates over a wide frequency range (currently up to 50 GHz) [1]. The picture of the test board and its stack-up are shown in Fig. 1. The frequency range of such a testboard application is up to 30 GHz, which is determined by the connectors and via-to-signal trace transition structure.

The dielectric material parameter extraction technique is based on measuring the full set of complex S-parameters of a test board with an appropriate "through-reflect-line" (TRL) calibration pattern. The total measured loss can be fitted as

$$\alpha_T = K_1\sqrt{\omega} + K_2\omega + K_3\omega^2 \ , \qquad (1)$$

where the smooth conductor loss is assumed to behave as $\sqrt{\omega}$, while the pure dielectric loss behaves as the sum of ω and ω^2 terms [2].

The similar curve-fitting is done for the total measured phase constant,

$$\beta_T = B_1\sqrt{\omega} + B_2\omega + B_3\omega^2 \ . \qquad (2)$$

The rough interface between a conductor and a dielectric contributes to all three terms in both (1) and (2).

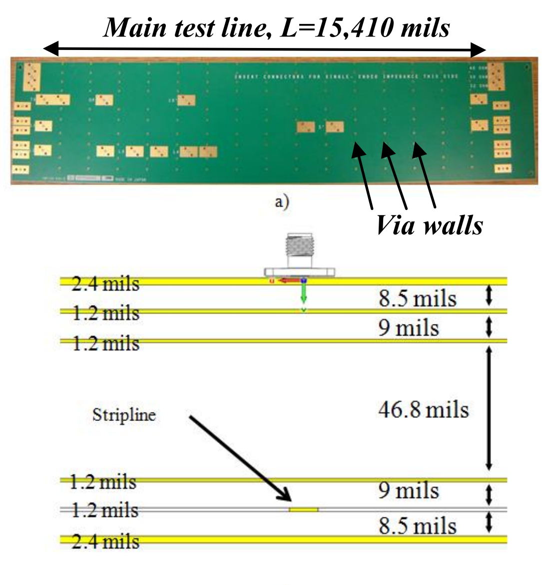

Fig.1. The picture of the test board (a) and stack-up (b)

In this work, three test vehicles with embedded 50-Ohm striplines of the same length, 39.4 cm (15,410 mils), have been studied. They have different types of copper foil (with different surface roughness profiles): standard (STD), very-low-profile (VLP), and hyper-very-low-profile (HVLP) [2]. However, in every other way these test vehicles are almost identical, having the same geometry, the same laminate fiber-glass filled epoxy resin composite dielectric, from the same

manufacturer and the same batch. Scanning electron microscopy (SEM) pictures of signal traces with different types of foils are shown in Fig. 2. Geometrical and roughness data for the test vehicles are given in Table I.

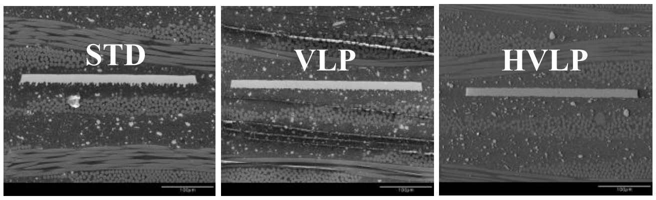

Fig. 2. SEM pictures of signal traces in PCB striplines with different types of foil.

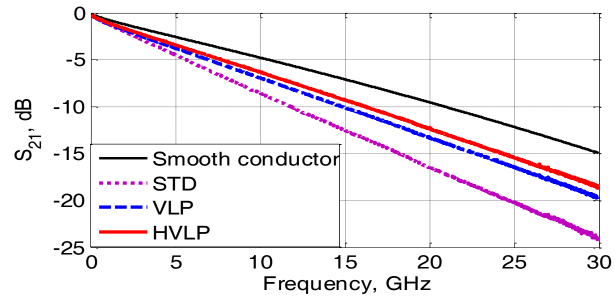

Fig. 3. Measured insertion loss in three test vehicles and in the equivalent test vehicle with smooth conductors

TABLE I. GEOMETRICAL AND ROUGHNESS DATA FOR SET OF TEST VEHICLES

	w_1, µm	w_2, µm	H, µm	P, µm	h_1, µm	h_2, µm	A_{r1}, µm	A_{r2}, µm	Λ_1, µm	Λ_2, µm	QR_1	QR_2	QR
STD	337.9	343.2	16.44	712.8	308	286	0.85	6.2	25	14.2	0.034	0.44	0.474
VLP	364.3	368.5	16.8	769	308	286.4	0.87	2.38	24.7	13	0.035	0.18	0.215
HVLP	329.3	331.3	15.3	691.7	303	292	1.25	1.13	14.3	19.2	0.087	0.06	0.147

The difference in insertion loss between the samples, shown in Fig. 3, is solely due to the roughness of the copper foils. Also in figure 3, is the calculated insertion loss, in the equivalent stripline, with perfectly smooth conductor (upper black solid line). This calculation is done using the differential extrapolation roughness measurement (DERM) technique [2].

The DERM procedure herein is applied to both real and imaginary parts of the total measured propagation constant $\gamma_T = \alpha_T + j\beta_T$ as is discussed in [3]. The curve-fitting coefficients as in (1) and (2) are used to generate auxiliary functions of the roughness parameter. In [2], this roughness parameter was an average peak-to-valley amplitude A_r taken on the roughest side of a signal trace. In [3], it is proposed to use, for the same purpose, a more comprehensive total roughness parameter (roughness factor) QR.

The total roughness parameter QR on a signal trace consists of two terms, corresponding to partial roughness parameters on the "oxide side" (the upper side as shown in Fig. 2) and on the "foil side" (the lower side) of the trace,

$$QR = \left.\frac{A_{r1}}{\Lambda_{r1}}\right|_{oxide} + \left.\frac{A_{r2}}{\Lambda_{r2}}\right|_{foil} \qquad (3)$$

The values A_r and Λ_r are the average peak-to-valley roughness amplitude and roughness function quasi-period, respectively. They are defined as in [4]. These values are obtained from the analysis of optical and/or SEM pictures of stripline micro-sections.

If the auxiliary curves (curve-fitting coefficients standing before the $\sqrt{\omega}$, ω, and ω^2 terms built as the functions of the roughness parameter) are extrapolated to zero roughness, the resultant coefficients at zero roughness would correspond to the perfectly smooth conductor and refined dielectric. Using this extrapolation, the loss contributions from the dielectric and the conductor can be separated.

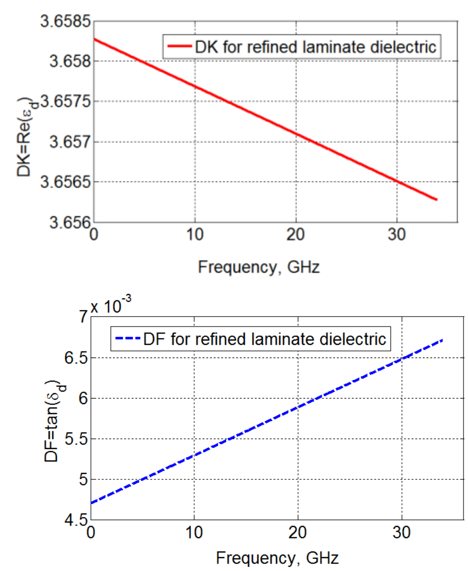

Fig. 4. DK and DF for all three sets of test vehicles

The refined dielectric loss in this example is $\alpha_d = 1.51\times10^{-11}\omega + 3.0\times10^{-23}\omega^2$, and the corresponding phase constant in the laminate dielectric refined from copper effects is $\beta_d = 6.38\times10^{-9}\omega - 0.8\times10^{-23}\omega^2$. The dielectric constant DK= ε'_d and dissipation factor DF= $\varepsilon''_d / \varepsilon'_d = \tan\delta_d$ of the refined dielectric are calculated from α_d and β_d by

solving a system of equations for ε_d' and ε_d'' as is shown in [2, Fig. 1]. The extracted frequency dependences for DK and DF of the laminate dielectric under study are almost linear as is shown in Fig. 4. Then, they are used in the 3D full-wave numerical modeling of the corresponding stripline structures.

The smooth conductor loss is extracted as $\alpha_{c0} = 2.15\times10^{-6}\sqrt{\omega}$. The surface roughness can then be included in a simulation by adding another dielectric material layer with its own dispersive parameters. This is an effective roughness dielectric (ERD) as discussed in [5], [6].

III. Full-Wave Numerical Model of a PCB Stripline with Conductor Roughness

A cross-section view of a 3D full-wave stripline model for this study is shown in Fig. 5. Metals are modeled as lossy copper - which takes the skin effect into consideration. The stripline is filled by an ambient dielectric with the parameters as in Fig. 4, entered in tabular form. Two "roughness dielectric" layers -"oxide layer" and "foil layer" are shown positioned on the top and bottom sides of the signal trace, respectively. The corresponding layers are also placed on the ground planes: "foil layer" is on the lower ground plane, and "oxide layer" is on the upper ground plane. The height of the dielectric layers is taken as the doubled average peak-to-valley roughness, T_r=2A_r. The length of the stripline is the same as in the test vehicles under study: 15.410 inches, or 391.41 mm – this is a significant length for comparison of measured and modeled results needed for the validation of the ERD approach. The structure was modeled using CST STUDIO SUITE™ [7].

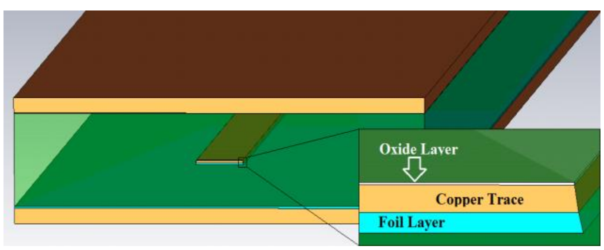

Fig.5. Cross-sectional view of a stripline model for full wave simulation

The extracted dielectric properties of the ERD layers on the "oxide" and "foil" sides for the test vehicles with STD, VLP, and HVLP foils are shown in Fig. 6. These parameters are determined from adding an appropriate slope in the insertion loss (magnitude of S_{21} in dB) as a function of frequency as compared with the smooth conductor case, as well as assuring proper phase of S_{21} behavior over the entire frequency range of study. The parameter VR in Fig. 6 (c) is defined as

$$VR = \varepsilon_r''\times T_r = \varepsilon_r'\times\tan\delta_r\times T_r\,. \quad (4)$$

The parameter VR is introduced to better compare volume loss in different roughness dielectrics. Since we deal with identical cross-sectional geometries, except for the thickness of roughness dielectric layer, the parameter VR describes volume roughness dielectric loss.

As it is seen from Figs. 7-9, the measured and simulated frequency dependences of the insertion loss in all the three cases agree well. In the HVLP case, the measured and simulated results lay on top of each other over the entire frequency range up to 35 GHz, while in the STD and VLP cases the results are very close up to 30 GHz, with a slight discrepancy of a fraction of a decibel at the higher frequencies.

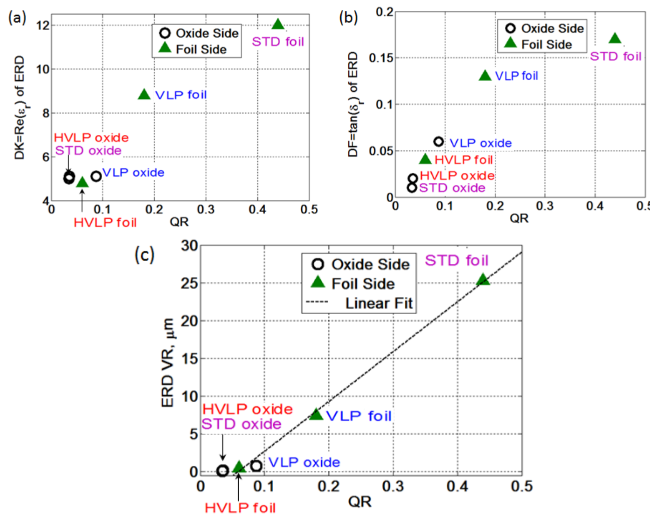

Fig.6. Scatter plots for dielectric constant (a), loss tangent (b), and the parameter VR (c) of the ERD on the oxide (circles) and foil (triangles) sides as functions of the corresponding roughness parameter *QR* on each side for STD, VLP, and HVLP foils.

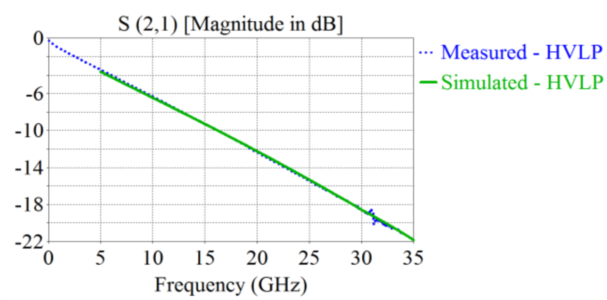

Fig. 7. Comparison of the measured and 3D full wave simulated insertion loss for the HVLP case

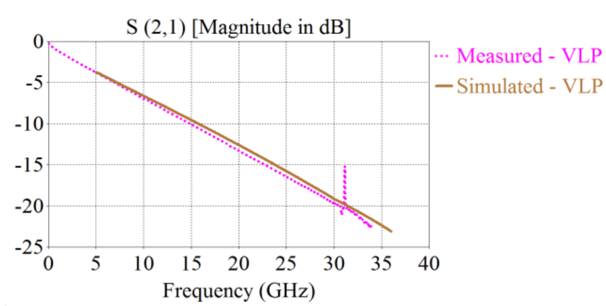

Fig. 8. Comparison of the measured and 3D full wave simulated insertion loss for the VLP case

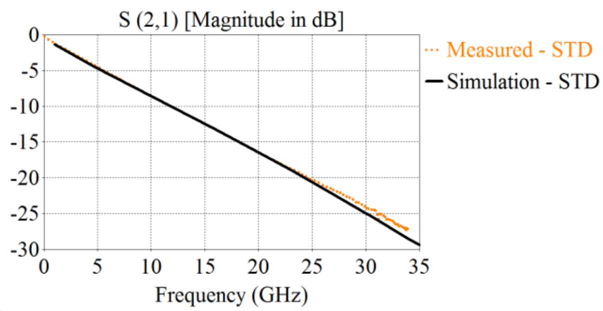

Fig. 9. Comparison of the measured and 3D full wave simulated insertion loss for the STD case

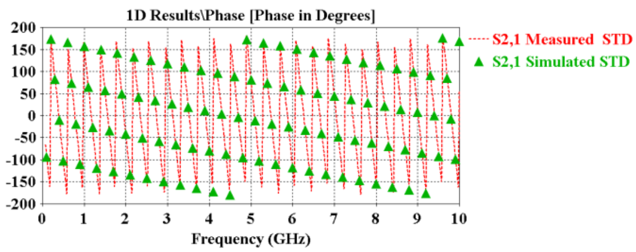

Fig. 10a. Comparison of the measured and 3D full wave simulated phase of S_{21} for the STD case from 0-10GHz

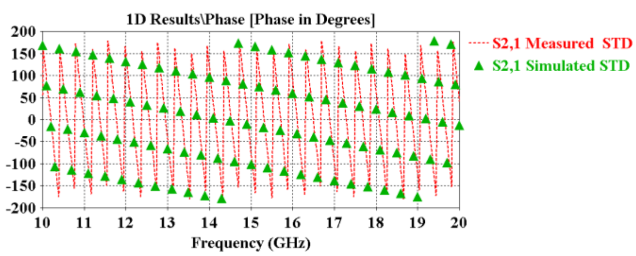

Fig. 10b. Comparison of the measured and 3D full wave simulated phase of S_{21} for the STD case from 10-20GHz

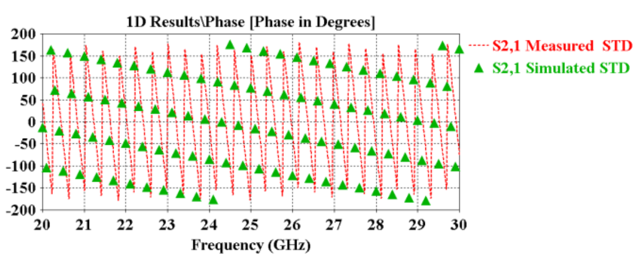

Fig. 10c. Comparison of the measured and 3D full wave simulated phase of S_{21} for the STD case from 20-30GHz

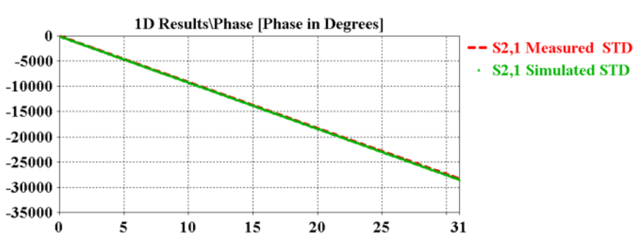

Fig. 10d. Comparison of the unwrapped measured and 3D full wave simulated phase of S_{21} for the STD case full frequency band

There is also a satisfactory agreement between the measured and modeled phase of S_{21}, and Fig. 10 demonstrates this for the case of the stripline with the STD foil.

The simulated power dissipation portions in each modelled object/material (smooth copper; ambient dielectric (matrix), and "oxide" and "foil" roughness layers) for the HVLP, VLP, and STD cases are shown in Fig. 11-13. The average stimulated power is 0.5 W (rms). It is seen that at the lower frequencies (below approximately 6 GHz) power dissipation in metal (smooth copper) is dominating. At the frequencies above 6 GHz, the overall loss in the ambient dielectric matrix is dominating. However, for the STD case, conductor roughness contribution to power loss is significant and is comparable to the loss in the smooth copper and dielectric loss, especially in the "foil" roughness layer. Power loss in the "oxide" roughness layer in STD case is the least, because surface roughness on the oxide side of the trace in this case is minimal. Power loss due to roughness in the VLP and HVLP cases are smaller than in the STD case, but increases with frequency, especially due to the "foil" side roughness.

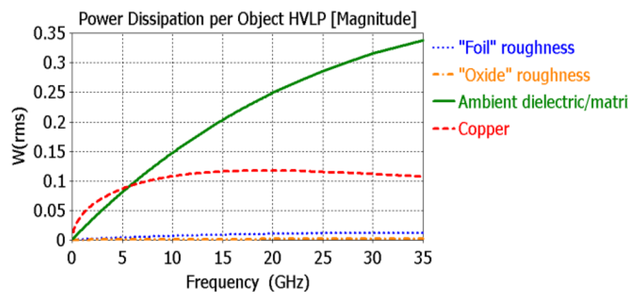

Fig. 11. Simulated power dissipation in each modeled object for HVLP case.

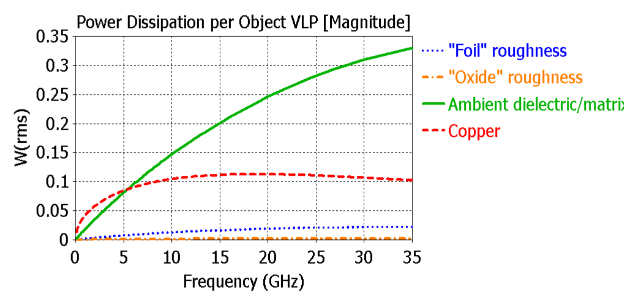

Fig. 12. Simulated power dissipation in each modeled object for VLP case

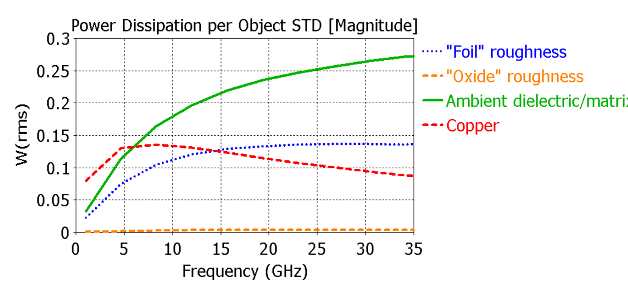

Fig. 13. Simulated power dissipation in each modeled object for STD case.

IV. Conclusion

Herein, the effective roughness dielectric (ERD) approach to represent an inhomogeneous interface between copper foil and laminate dielectric in a PCB is tested for verification using 3D full-wave numerical simulations. The parameters of an ambient laminate fiber-glass filled composite dielectric used in the modeling of a PCB stripline are determined using differential extrapolation roughness measurement teachnique (DERM). The agreement of the results of 3D full-wave modeling simulations with the proposed approach and measurements justifies the proposed approach.

Therefore, roughness of the copper foil can be easily incorporated in the numerical simulation tools of PCB designs by evaluating the effective dielectric properties of "roughness dielectrics" corresponding to the existing foils with different roughnesses. It is important to know the geometry of the transmission line to be modeled, the correct roughness-independent DK and DF data of the laminate dielectric used in this line, and the particular foil roughness profile.

If an electronics designer does not have the capability of foil roughness inspection, *e.g.*, using an SEM or optical microscopy cross-sectional analysis, the recommended pre-computed values of complex permittivity and thickness of "roughness dielectrics" for the known types of foils may still be used in the numerical modeling.

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References

[1] A. Koul, P. K.R. Anmula, M.Y. Koledintseva, J.L.Drewniak, and S. Hinaga, "Improved technique for extracting parameters of low-loss dielectrics on printed circuit boards", *Proc. IEEE Symp. Electromag. Compat.,* Aug. 17-21, Austin, TX, 2009, pp. 191-196.

[2] A. Koul, M.Y. Koledintseva, J.L. Drewniak, and S. Hinaga, "Differential extrapolation method for separating dielectric and rough conductor losses in printed circuit boards", *IEEE Trans. Electromag. Compat*., vol. 54, no. 2, pp. 421-433, Apr. 2012.

[3] M.Y. Koledintseva, A.V. Rakov, A.I. Koledintsev, J.L. Drewniak, and S. Hinaga, "Improved experiment-based technique to characterize dielectric properties of printed circuit boards", *IEEE Trans. Electromag. Compat.*, 10.1109/TEMC.2014.2317812 to be published.

[4] S. De, A.Y. Gafarov, M.Y. Koledintseva, S. Hinaga, R.J. Stanley, and J.L. Drewniak, "Semi-automatic copper foil surface roughness detection from PCB microsection images", *IEEE Symp. Electromag. Compat.*, Pittsburg, PA, 2012, pp. 132-137.

[5] M.Y. Koledintseva, A. Razmadze, A. Gafarov, S. De, S. Hinaga, and J.L. Drewniak, "PCB conductor surface roughness as a layer with effective material parameters", *IEEE Symp. Electromag. Compat.*, Pittsburg, PA, 2012, pp. 138- 142.

[6] M.Y. Koledintseva, "Extraction of permeability of thin flexible magneto-dielectric materials", 21th *Int. Conf. Electromagnetic Fields and Materials (Fundamental Physical Research)*, Moscow, MPEI-NRU, 15-17 Nov. 2013, pp. 545-554.

[7] CST STUDIO SUITE®, CST AG, Germany, www.cst.com.