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Equivalent Capacitance and Multilayer Models for Effective Roughness Dielectric in PCBs

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Abstract— Effective Roughness Dielectric (ERD) is used to substitute copper foil roughness in printed circuit board (PCB) interconnects. In this work, the the equivalent capacitance approach is used to get the ERD parameters based on the understanding that there is a gradual variation of concentration of metallic inclusions in the transition layer between the dielectric and foil. The metallic concentration profile can be extracted from scanning electron microscopy (SEM) or high-resolution optical microscopy. The proposed model of equivalent capacitance with gradient dielectric is applied to standard (STD), very-low-profile (VLP), and hyper-very-low profile (HVLP) foils, and the frequency-dependent dielectric parameters of the homogenized ERD are calculated. The analytically calculated ERD parameters are used in 2D-FEM and 3D full-wave numerical models of the stripline structures with various types of foils. There are two types of 3D numerical models: with homogeneous ERD parameters and multilayer "space map" model. All the models show excellent agreement with measurements, and the analysis of the results of different models is provided.

I. Introduction

The Effective Roughness Dielectric (ERD) concept was introduced in [1]-[3]. ERD is a homogeneous lossy dielectric layer of certain thickness T_r with effective (averaged) dielectric constant DK_r and dissipation factor DF_r. This layer is modeled to substitute an inhomogeneous transition between a conductor and laminate substrate dielectric in a printed circuit board (PCB). This concept has been successfully applied to model conductor (copper foil) roughness in PCBs when designing high-speed digital electronics devices [4], [5]; it has been implemented and tested in a number of numerical electromagnetic modeling tools, see, *e.g.*, [6]-[9]. The ERD "design curves" determining the ranges of the DK_r and DF_r parameters for different types of PCB copper foils were developed in [3], [10], [11]. To use these "design curves" for reasonable estimation of foils roughness effects, it is sufficient to know which type of foil is used in the PCB under test. Average values DK_r, DF_r, and ERD thickness T_r corresponding to the type of the foil within the given ranges of data in the "design curves" can be used for simple implementation in numerical modeling.

The "design curves" were developed using fitting between the measured and modeled S-parameters, but it is always desirable to have an analytical model. This model was recently presented in [12].

There is a transition layer between the dielectric and foil where the concentration of metallic inclusions varies gradually. The effective dielectric properties of the roughness layer (DK_r and DF_r) can be dervied from the equivalent capacitance of the capacitor with dielectric properties varying according to the concentration profile of metallic particles in this layer. This concentration profile can be obtained from SEM or high-resolution optical microscopy [13]-[15]. As concentration of metallic particles increases along the axis normal to the laminate dielectric and foil boundary, two regions can be determined: insulating and conducting. Rates of the effective loss (or effective conductivity) variation in these two regions are significantly different.

The proposed model of equivalent capacitance with gradient dielectric is applied to different types of foils, and the results are validated using comparison of 2D-FEM and full-wave 3D numerical electromagnetic simulations and measurements.

II. Analytical Model

An average contents (volume concentration) of metallic particles in the roughness layer varies as a function of the coordinate z normal to the surface (see Fig. 1). It can be approximated, as will be shown below, by an exponential function

$$v_{incl}(z) = a \times \exp(K_1 z), \qquad (1)$$

where a and K_1 are the fitting parameters.

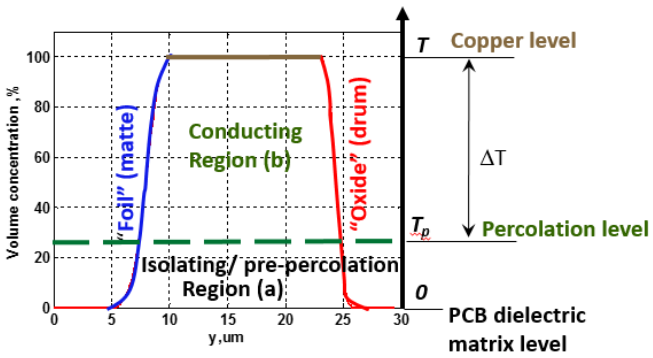

Fig. 1. Schematic diagram of PCB matrix dielectric – copper roughness – "flat" copper transition layer

Two regions of effective roughness dielectric will be considered: (a) $0<z<T_p$ and (b) $T_p<z<T$. They are shown in Fig. 1. Region (a) is adjacent to the dielectric matrix of the PCB, and the mixture in this region remains in the dielectric phase, *i.e.*, in pre-percolation state. Herein, T_p is the distance within the layer at which percolation is reached. Region (b) is adjacent

to the smooth foil level and is conducting, since the concentration of metallic inclusions in it is higher than the percolation threshold.

The total thickness of the ERD layer is

$$T = T_p + \Delta T, \tag{2}$$

where ΔT is the thickness of the region (b).

The perclation threshold concentration v_p for the metallic particles in the roughness dielectric layer can be obtained empirically, *i.e.*, estimated from the microscopy pictures.

First, let us consider the region $0<z<T_p$. This is the dielectric layer with relative permittivity varying from the matrix dielectric properties ε_m (at z=0) to the final pre-percolation value ε_p (at $z=T_p$). The T_p value can be obtained by solving the equation following from (1):

$$v_p = a \times \exp(K_1 T_p). \tag{3}$$

The dielectric function in region (a) varies with z as

$$\varepsilon(z) = \varepsilon_m v_{incl}(z). \tag{4}$$

The effective permittivity of such a layer can be calculated through the equivalent capacitor consisting of series connection of thin sublayer capacitors. The capacitance of such a capacitor with variable properties of the dielectric is

$$C = C_0 d / \int_0^{Tp} dz/(1+\varepsilon(z)), \tag{5}$$

where C_0 is the capacitance of the corresponding air-filled rectangular parallel-plate capacitor of thickness T_p. The effective dielectric properties of the region (a) are then

$$\varepsilon_d = T_p / \int_0^{T_p} dz/(\varepsilon_m(1+v_{incl}(z))). \tag{6}$$

This permittivity is complex, $\varepsilon_d = \varepsilon_d' - j\varepsilon_d''$. The equivalent conductivity in this region is

$$\sigma_d = -\omega\varepsilon_0\varepsilon_d''. \tag{7}$$

Since region (a) is the comparatively lossy dielectric, its conductivity σ_d will not be high.

However, region (b) is conductive, and its conductivity increases exponentially towards smooth copper level until it reaches the conductivity of the pure copper. Therefore,

$$\sigma_p = \sigma_d \times e^{K_2 T}, \tag{8}$$

where K_2 is the exponent after percolation. It can be solved from the equation, when σ_p reaches the level at the percolation threshold. As a reminder, T is the entire thickness of the ERD layer. The typical percolation threshold is assumed to be 25% of volume concentration of copper inclusions in the epoxy-resin fiber-filled dielectric matrix [16]. At the beginning of percolation, we assume that the concentration by two orders of magnitude is less than that of copper, $\sigma_p = 0.01\sigma_{Cu}$. Then K_2 is calculated from (8).

The conductivity profile with respect to the coordinate z in region (b) will be

$$(z) = \sigma_d \times e^{K_2 z}. \tag{9}$$

The dielectric profile function in region (b) is then

$$\varepsilon_p(z) = \varepsilon_d + \frac{\sigma_d}{j\omega\varepsilon_0} \times e^{K_2 z}. \tag{10}$$

The effective permittivity of the two lossy dielectric layers is calculated through the equivalent capacitor containing two capacitors in series.

$$\varepsilon_{eff} = T/(\int_0^{T_p} dz/(\varepsilon_m(1+v_{incl}(z)) + \int_{T_p}^{T} dz/(\varepsilon_p(1+v_{incl}(z))))). \tag{11}$$

Then the ERD parameters $DK_r = \varepsilon_{eff}'$ and $DF_r = \tan\delta_{eff} = \varepsilon_{eff}''/\varepsilon_{eff}'$ are obtained from (11). Integrals in (11) can be calculated analytically (herein the expressions are omitted, since they are cumbersome), or numerically.

III. Copper Roughness Profile Analysis

Cross-sectional microscopic (SEM or optical) analysis is used to characterize roughness profile of the foil by cutting a signal trace perpendicular to the direction of the quasi-TEM wave propagation. The roughness profile quantification is based on digital image processing and the analysis of pixels [13]-[15]. An example of a binary image of the trace cross-section is shown in Fig. 2. The bottom ("foil", or "matte")

side of this foil is rougher that the top ("oxide", or "drum") side. The extracted average peak-to-valley magnitude A_r of the "foil" side is also shown.

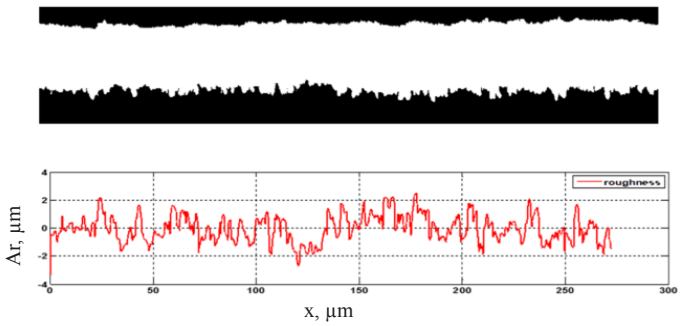

Fig. 2. Binary image of the signal trace of black oxide VLP foil and extracted roughness profile on the bottom side of the trace

In many cases, though not necessarily, surface roughness is isotropic, *i.e.*, identical in x and y directions.

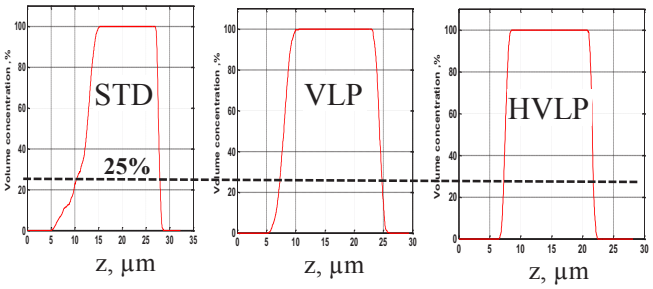

Fig. 3. Volume fraction of metallic inclusions in STD, VLP, and HVLP foils

Performing summation for each column of pixels, one can get the volume concentration of metallic inclusions in the region between pure dielectric to pure metal. Fig. 3 shows the function $v_{incl}(z)$ for different types of foils. It is seen that 0% concentration corresponds to dielectric matrix, while 100% to smooth copper. The transitions are comparatively smooth – the left-hand front corresponds to the "foil" side, and the right-hand side to the "oxide" side. The smoother the conductor side, the more abrupt the metallic concentration slope is. In Fig. 3, the dashed line corresponds to the percolation threshold of 25%.

The profiles on the "foil" and "oxide" sides can be fitted using exponential functions $a\exp(K_1 z)$ as in (1), which are simple for analytical calculation of (11). The fitting data for a number of samples (black-oxide foils, Megtron 6 substrates) are presented in the first two columns of Table I. Confidence bounds in this fitting are 95%. This table also contains T_p and T data extracted from the concentration profiles and equivalent capacitance model. Roughness factor QR=A_r/Λ_r is obtained from SEM pictures using the procedure [15], [17]. Note that the average peak-to-valley roughness amplitude A_r obtained from from the "in situ" cross-sectional analysis based on SEM pictures is close to the value T extracted from the profile concentration dependence, but not exactly the same. Concentration dependence provides data from the exact pixel counting, while A_r values are extracted from image processed profile based on the skin-depth criterion and combining closely placed peaks, to some extent imitating R_z measurments, but with arbitrary number of peak and values (not necesseraly five as when calculating R_z).

TABLE I. EXPONENTIAL FITTING OF PROFILE FUNCTIONS ON "FOIL" AND "OXIDE" SIDES OF COPPER FOILS

		a	K_1	T_p, μm	T, μm	QR
STD	"Foil"	3.03	0.379	4.99	9.0	0.447
	"Oxide"	2.829	2.075	0.93	1.7	0.034
VLP	"Foil"	5.991	0.748	1.61	3.8	0.181
	"Oxide"	5.665	1.180	1.07	2.6	0.035
HVLP	"Foil"	5.537	2.182	0.46	1.3	0.064
	"Oxide"	6.193	1.827	0.64	1.6	0.087

IV. ANALYTICAL CALCULATION OF ERD PARAMETERS

The proposed equivalent capacitance model was applied to calculate the ERD parameters of the three types of foils (STD, VLP, and HVLP, on both "foil" and "oxide" sides) as in Table I. Fig. 4 shows the calculated frequency dependences for DK_r and DF_r of the corresponding ERD layers. The thicknesses of the layers are also determined from the metallic concentration profiles. Note that in [3], [10], [11], the ERD parameters were independent of frequency, but the new analytical model accounts for frequency dependence. This is expected to provide the better agreement between the measured and modeled results at the higher frequencies.

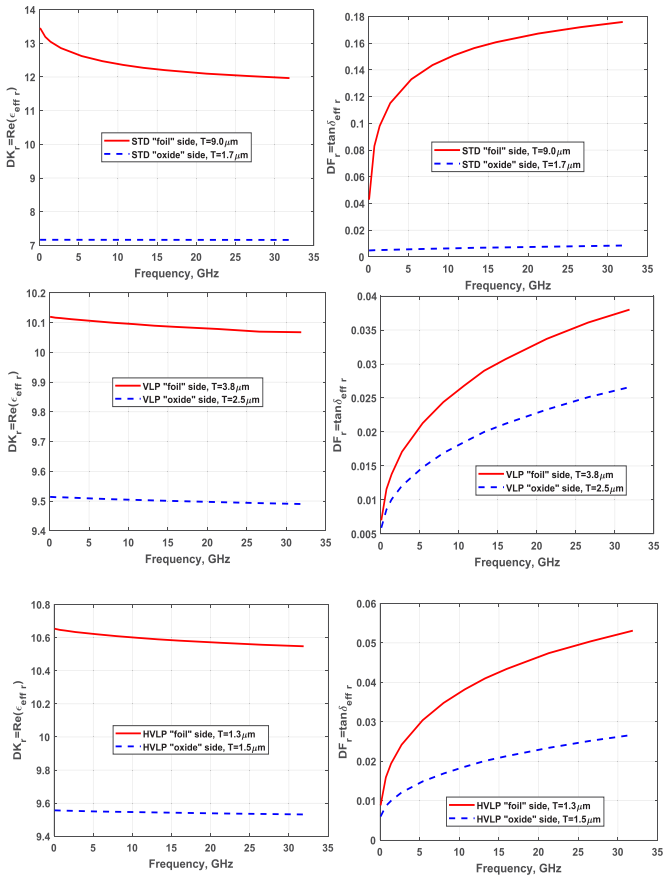

Fig. 4. ERD parameters for STD, VLP, and HVLP foils

V. NUMERICAL SIMULATIONS

Validation of the equivalent capacitance model is first conducted using 2D-FEM simulations with ERD layers on the traces of the striplines and on the return (ground) planes. The model setup is shown in Fig. 5. In particular, ANSYS Q2D was used for this modeling, similar to [1], [3]. The dielectric matrix parameters in the model were set as DK=3.65 and DF=0.0074 with causal (Djordjievic-Sarkar [18]) approximation that fits the frequency dispersion of Megtron 6 accurately in the frequency range of interest, up to 30 GHz. Conductor surface roughness was modeled as homogeneous ERD layers with values as in Fig. 4 and with constant DK_r and DF_r as in Table II.

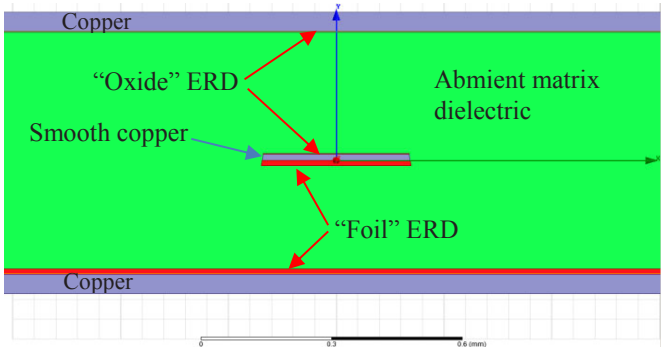

Fig. 5. 2D-FEM model setup example

Note that the thicknesses of ERD layers in these two 2D-FEM models (with constant and with frequency-dependent ERD parameters) slightly differ. For the extraction of the constant values of DK_r and DF_r, the corresponding roughness parameters A_r for foils were measured from SEM pictures[13]-[15], and then the "design curves" [3] suggested that each ERD layer thickness is taken as the doubled A_r. For the frequency-dependent ERD parameters, the values of thickness T were as in Table I.

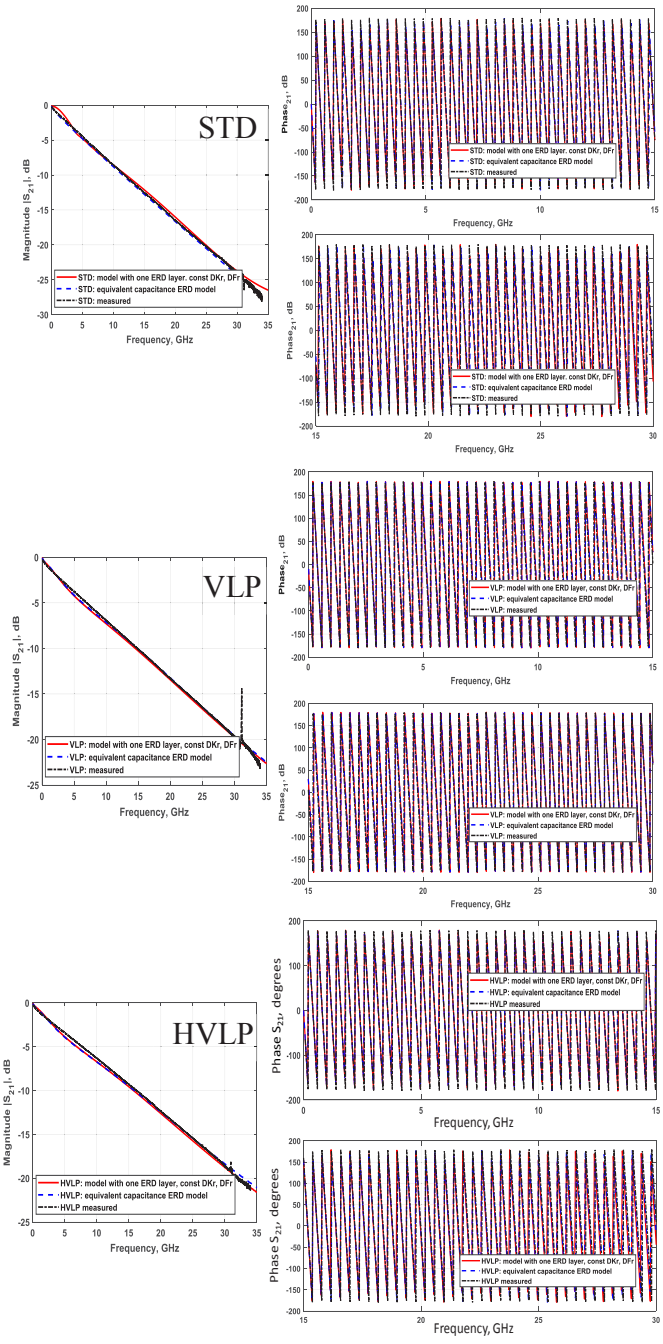

Fig. 6. Measured and modeled S_{21} for STD, VLP, and HVLP foils; frequency-independent homogenized ERD data as in [3], and the extracted using equivalent capacitance model as in Fig. 4.

TABLE II. MODELED CONSTANT ERD PARAMETERS ON "FOIL" AND "OXIDE" SIDES OF COPPER FOILS

Type of foil	Foil side	DKr	DFr	Tr=2Ar, μm
STD	"Foil"	12.0	0.17	12.4
	"Oxide"	5.00	0.01	1.7
VLP	"Foil"	8.00	0.14	4.76
	"Oxide"	0.14	0.02	1.74
HVLP	"Foil"	4.80	0.04	2.3
	"Oxide"	5.10	0.06	2.5

The measured and the 2D-FEM modeled data for the frequency range up to 30 GHz are shown in Fig. 6. The agreement between the modeled and measured results for all the three foil types validate the proposed analytical approach. The discrepancy for $|S_{21}|$ is <0.5 dB over the entire frequency range; the phase difference is within $\pm 10^0$, but depends on the particular frequency. It is seen that the results with equivalent capacitance approach fit better measurements in the high-frequency region (>25 GHz) than the results with the constant DK_r and DF_r ERD parameters.

The 3D full-wave numerical model (in CST Studio [6]) with a single-ended stripline was also created. It includes the dielectric, the material parameters of which are obtained through the extrapolation to zero roughness technique (or differential extrapolation roughness measurement - DERM), as in [19], [20], and thin layer objects representing conductor surface roughness as the ERD. The dielectric matrix parameters in these simulations were accurately approximated with the same values of DK=3.65 and DF=0.0074 (constant fit set at 40 GHz) as in the 2D-FEM models.

Fig. 7 shows a cross-sectional view of the CST model setup. The ERD layers are placed above the trace ("foil" side), below the trace ("oxide" side), and on the corresponding reference/ground planes. The tested length of the stripline structure was 391.414 mm (15.4 inches); stripline traces were 17.5 μm thick (0.5-oz copper) and 340 μm (13.5 mil) wide. The impedance of the stripline was 50 Ohms. Cross-sections for all the three test lines were identical, except for the foil roughness.

Two types of 3D full-wave models were simulated. The first was with homogenized frequency-dependent ERD parameters DK_r and DF_r extracted using the equivalent capacitance model (as in Fig. 4), and the second was with roughness modeled as a single homogeneous layer. The ERD parameters for the latter were as in Table II.

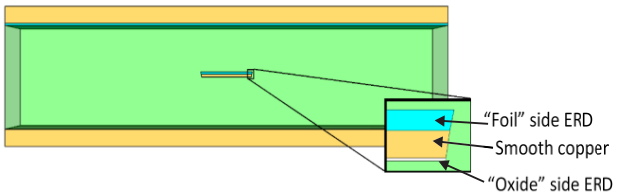

Fig. 7. Numerical model setup

The models were simulated across wide frequency bands using a time domain solver (the Finite Integral Technique) [6]. A mesh size in the models resulted in about 2 million cells. The waveguide ports were used for excitation of the striplines. To reduce the computational domain in the comparatively long

striplines (391.414 mm), the lines were cut into two halves, and later on the results were cascaded.

The results of measurements and the CST models with the homogenized frequency-dependent ERD caluclated using the equivalent capacitance model are shown in Fig. 8. The agreement between the measured and the numerically simulated data using the equivalent capacitance model for ERD is as good as in Fig. 6 for the 2D FEM model.

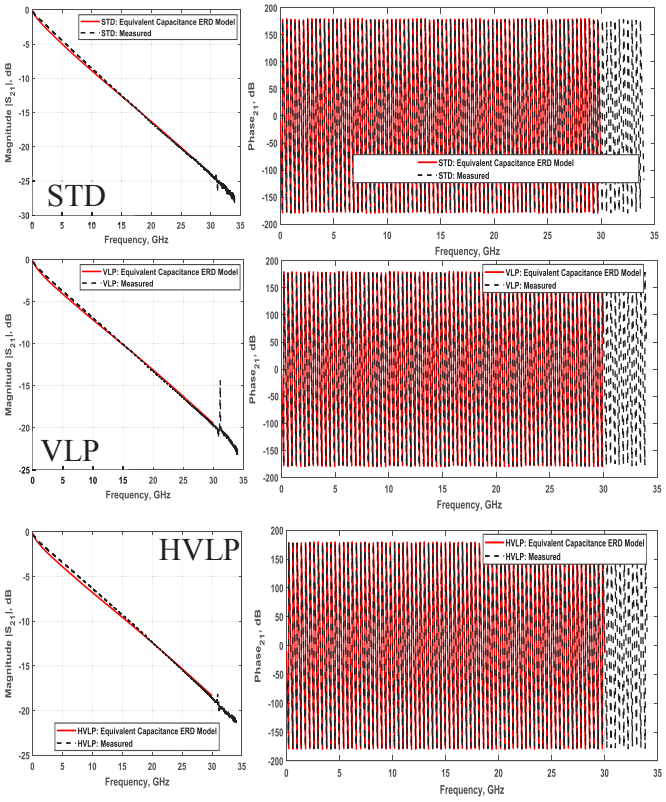

Fig. 8. Measured and nemerically modeled (full-wave FIT) S_{21} results for STD, VLP, and HVLP foils; homogenized ERD layers are extracted using equivalent capacitance model

Then the second roughness model, the multilayer one, was set up similarly to other models. The idea of modeling a conductor of a planar transmission line as a multilayer structure was proposed in [21], where conductor losses were treated in terms of surface impedances. However, [21] dealt with skin depth rather than conductor surface roughness. The idea of modeling a rough conductor on a PCB as a multilayer structure seems reasonable, because it also agrees with the considered above equivalent capacitance model which subdivides roughness in slices (or layers) and two regions – pre-percolation and percolation. In our multilayer model, the conductor roughness is specified differently. This new approach was tested for the test board with STD foil only. In the model for the STD "foil" side, the roughness dielectric properties are split into three parts: the top 1/3rd part (close to metal) has DK_r = 16, the middle 1/3rd part has DK_r= 12, and bottom 1/3rd part (next to matrix) has DK_r=8. In this case, each layer would be very thin, adding significant mesh count and therefore increasing simulation time. However, to treat such a multilayer structure, a different approach based on "space mapping" [22] is applied. In this case, the total ERD layer is not split into three separate layers/objects with homogeneous dielectric constants, but the object material properties change depending on the position within the object according to the specified "space map". Note that this "space map"-based model does not introduce any new material, but is used to define a generic spatial distribution for a normal (or anisotropic) material. This allows for modeling inhomogeneous materials. In this work, the ERD itself is specified within the dielectric matrix material.

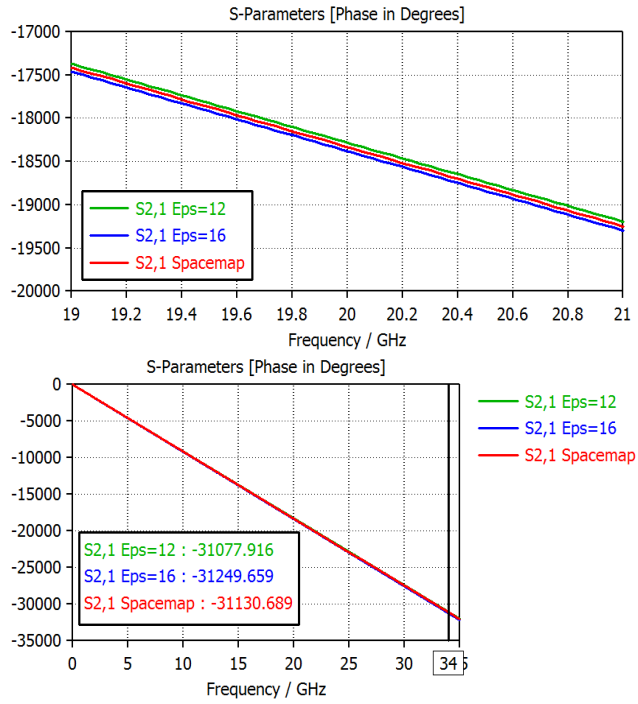

Fig. 9. Phase comparison for three cases: with DKr=12, DKr=16, and multilayer "spacemap" model of ERD.

TABLE III. PHASE IN DEGREES OF ERD MODELS AND MEASUREMENTS AT FREQUENCIES: 7, 15, 20, 25, 30, AND 34 GHZ

	DKr=12	DKr=16	Multilayer "spacemap"	Measured
7 GHz	-6407.888	-6441.267	-6415.979	-6436.3764
Compared to measured	-28.4884	+4.8906	-20.3974	0
15 GHz	-13713.986	-13786.089	-13739.383	-13753.362
Compared to measured	-39.376	+32.727	-13.979	0
20 GHz	-18281.827	-18379.124	-18333.479	-18318.775
Compared to measured	-36.948	+60.349	+14.704	0
25 GHz	-22848.556	-22971.673	-22937.485	-22880.175
Compared to measured	-31.619	+91.498	+57.31	0
30GHz	-27414.943	-27564.914	-27458.922	-27435.057
Compared to measured	-20.114	+129.857	+23.865	0
34GHz	-31077.916	-31249.659	-31130.689	-31078.478
Compared to measured	-0.562	+171.181	+52.211	0

In Fig. 9 and Table III, the phases of S_{21} are compared for the four cases – three modeled and one measured. The first two cases are with the regular ERD layers: DK_r=12 and DK_r=16 on the "foil" sides of both the trace and the corresponding ground plane; and DF_r=0.17 for both DKr=12 and 16. The third case is the proposed multilayer "space map" model for the "foil" side only; there is no space mapping on the "oxide" sides; they are are incorporated in the model as regular single layers. This is because for STD foils, the "oxide" side is very smooth, and its ERD is thin (Tr=1.7 μm). Note that loss tangents currently cannot be modeled with space mapping in CST, therefore, only phases are compared. Anyway, loss does not affect phase results much, but phase is chosen for comparison because it is the most sensitive to the choice of the model parameters. As Table III shows, there is an excellent agreement between the measured and the multilayer model results in terms of phase: the measured data practically overlaps with the case of the "space map" and is not shown in the plots in Fig. 9. The data in Fig. 9 is given in the narrower frequency range 19-21 GHz, and for the entire frequency range 10 MHz-35 GHz, too. From Table III, the difference between these two results is indeed small (within a few degrees) when compared to the overall unwrapped phase. Incorporation of loss in the space mapping approach is the further work, which is expected to improve matching of magnitudes of $|S_{21}|$, dB in the space mapping with measurements and with the other presented herein modeling approaches.

VI. Conclusions

In this work, an analytical model to calculate effective roughness dielectric (ERD) parameters for conductor surface roughness of a PCB foil is presented. A concentration dependence of metallic inclusions in the transition between the ambient dielectric matrix and copper is used to calculate analytically the equivalent capacitance associated with the roughness layer. Then the parameters of the effective roughness dielectric are extracted from this equivalent capacitance. The ERD parameters obtained from this model appear to be frequency dependent unlike in the previous works; therefore, they can describe the high-frequency behavior of PCB interconnects more accurately than the frequency-independent models. The proposed model is applied to three stripline test scenarios with three different types of foils - STD, VLP, and HVLP, and is validated by an excellent agreement between the 2D-FEM modeling, full-wave 3D numerical modeling, and measurements. Two types of numerical models are developed in this work: with homogeneous ERD and with multilayer representation of the roughness layer and "space map". The multilayer roughness model provides the closest to the measured result when S_{21} phases are compared. The further work will inlcude incorporation of loss in space mapping approach that will allow for more accurate modeling of $|S_{21}|$ magnitude.

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