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Accurate and Time Efficient Signal Integrity and Power Integrity Modeling of High-Speed Digital Systems

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ACCURATE AND TIME EFFICIENT SIGNAL INTEGRITY AND POWER INTEGRITY MODELING OF HIGH-SPEED DIGITAL SYSTEMS

by

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This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology.

Paper I: found on pages 5-38; Electrical Characterization of Dielectric Liquid at Multiple Frequencies Based on A Cylindrical Cavity Resonator, has been submitted to IEEE Transactions on Signal and Power Integrity.

Paper II: Pages 39-71; Mode-Decomposition-Based Equivalent Model of High-Speed Vias Up to 100 Ghz, has been published in IEEE Transactions on Signal and Power Integrity.

Paper III: Pages 72-84; Impedance Converter Based Probe Characterization Method for Magnetic Materials Loss Measurement, has been published in 2022 IEEE International Symposium on Electromagnetic Compatibility, Signal and Power Integrity.

ABSTRACT

Signal integrity (SI) and power integrity (PI) play an important role in the modern high-speed digital system design, which are closely related to the printed circuit board (PCB) dielectric material property, the PCB interconnect performance, and the power delivery network (PDN) on PCB. Generally, the full-wave simulation is used to accurately analyze and evaluate the designed PCB. But full-wave simulation is not a good option for the complex PCB structure with high aspect ratio, for example, PCB vias, and PDN, which will require significant computing time and storage resources. Equivalent circuit models have been developed to efficiently predict the electrical performance of those complex PCB structures. To get the accurate and time-efficient signal integrity and power integrity modeling and analysis of high-speed digital systems, some works related to the PCB dielectric material characterization, the high-speed PCB via modeling, and the on-chip PDN impedance modeling have been done in the paper. The paper can be categorized into three parts, PCB material characterization based on cylindrical cavity resonator (CCR), high-bandwidth and high-accuracy physics-based circuit model of high-speed PCB via, and on-chip PDN impedance model based on layer Green's function and partial element equivalent circuit (PEEC). In part I, the CCR apparatus is designed and manufactured to measure the PCB dielectric liquid permittivity. The physics-based equivalent circuit model of the high-speed PCB via is detailed in part II. The equivalent circuit of PCB via is extracted based on the mode-decomposition and domain-decomposition theory. An equivalent circuit model based on layer Green's function and PEEC is proposed to efficiently predict the impedance of the on-chip PDN in part III.

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1. INTRODUCTION

1.1. SIGANL AND POWER INTEGRITY OF THE HIGH-SPEED DIGITAL SYSTEM

Typically, a high-speed digital system comprises three main components: the integrated circuit (IC) chip, the package module, and the printed circuit board (PCB), as illustrated in Figure 1.1. To assess the signal integrity and power integrity of such a system, accurate modeling of the PCB substrate, high-speed interconnects (e.g., vias on PCB and package), and the power delivery network (PDN) is essential. Additionally, high-speed digital systems often face thermal challenges due to their high-power requirements. Immersion cooling, depicted in Figure 1.1, is a method used to address these thermal issues, particularly in data centers or servers. When submerged in dielectric liquid, the signal integrity performance of the electronics can be affected. Typically, full-wave simulation is employed to evaluate the signal integrity or power integrity of the system. However, conducting full-wave simulations for the entire digital system demands significant computational resources and time. The focus of this thesis is to develop models for signal integrity and power integrity assessment and optimization of high-speed digital systems, addressing the computational challenges associated with full-wave simulations.

1.1.1. Dielectric Liquid for the Immersion Cooling. The rise of high-performance data centers and cloud computing presents a significant cooling challenge for network servers. Immersion cooling, also known as liquid cooling, involves submerging electrical and electronic devices like data center servers and storage systems in a thermally conductive but non-electrically conductive liquid. This method eliminates the need for fans, thereby saving power. However, the use of coolant can have adverse effects on the

electrical performance of exposed connectors, components, and microstrip lines on the printed circuit board (PCB). It's crucial to extract the electrical properties of the coolant for early PCB design stages. Typically, coolants are chosen for their minimal impact on PCB loss, requiring careful consideration during selection and design phases.

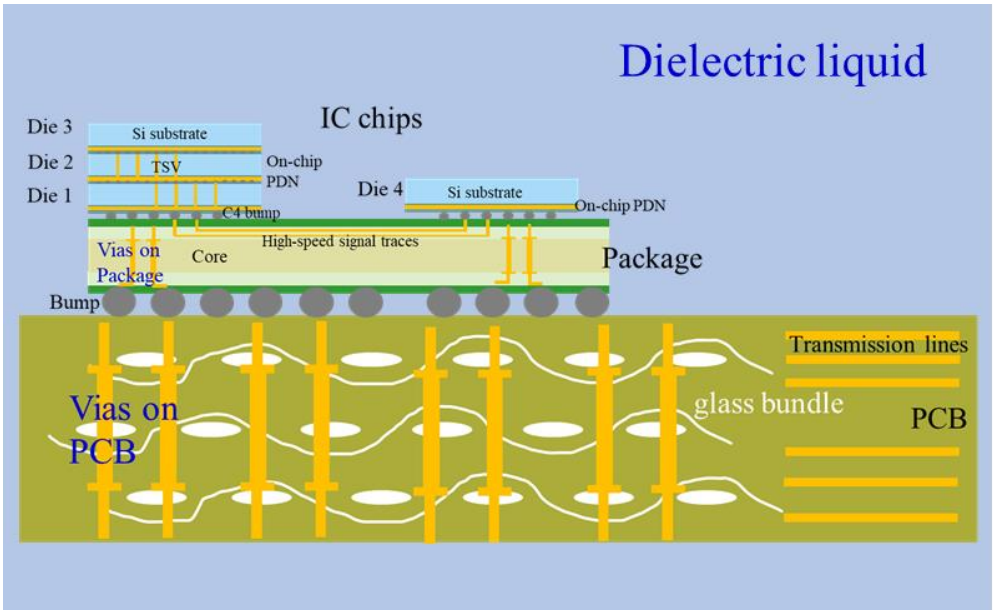


Figure 1.1 High-speed digital system submerged in dielectric liquid.

1.1.2. High-speed Interconnect. As technology continues to scale down and data rates rise, designing and optimizing high-speed channels has become increasingly challenging. Signal integrity maintenance is paramount for PCB designers working on high-speed products. In these channels, vias, or vertical interconnects, play a crucial role in routing signals across different layers. However, they often introduce impedance discontinuities, leading to significant signal integrity and power integrity issues. To address

these challenges, PCB vias must be designed for high electrical performance, meeting impedance, return loss, and insertion loss specifications.

Typically, designers utilize 3D full-wave simulation software like HFSS and CST for via optimization. These simulations help analyze via stub resonance and the impact of non-functional pads and ground via numbers. However, due to the structural complexity of via transitions and the multitude of design parameters, optimizing vias through 3D full-wave simulation is time-consuming. To mitigate this, many equivalent models for high-speed differential via pairs have been developed, reducing optimization time while maintaining design integrity.

1.1.3. On-chip PDN. Noise from the power delivery network (PDN) can lead to various issues such as timing jitter, skew in high-speed digital channels, electromagnetic interference, and noise coupling across different modules. Estimating impedance properties within the system PDN is crucial, as a high impedance level across a high-frequency bandwidth can result in significant power noise. The on-chip PDN forms a vital part of the system PDN, encompassing PDNs on the chip, package, and PCB. While full-wave simulation is commonly employed for PDN impedance evaluation, it faces limitations when applied to on-chip PDN impedance due to the substantial variation in geometric features within the on-chip PDN structure. To overcome these challenges, equivalent circuit models have been developed to accurately and efficiently predict PDN impedance. These models provide a valuable tool for assessing and optimizing the PDN to mitigate noise-related issues in high-speed digital systems.

1.2. CONTENTS AND CONTRIBUTIONS

This thesis presents several key contributions, outlined in the following summaries of each paper.

In the first paper, a cylindrical cavity resonator-based method was proposed to measure the dielectric constant and loss tangent of the dielectric liquid. A measurement apparatus of the dielectric cylindrical cavity resonator was designed and manufactured to verify the proposed method. The accuracy and effectiveness of the proposed method were verified based on full-wave simulations and measurements.

In the second paper, the equivalent circuit model of the high-speed via was developed to evaluate the performance of high-speed interconnects accurately and efficiently. The proposed high-speed via model was proposed based on the physics-based via model, which can work in a high bandwidth with a high accuracy. The proposed high-speed via model was verified based on full-wave simulations.

In the third paper, the on-chip PDN impedance model was proposed based on layer Green's function (LGF) and partial element equivalent circuit (PEEC) method. The partial resistance, inductance, and capacitance of the mesh-typed on-chip PDN can be extracted based on the physics of the on-chip PDN by the LGF and PEEC methods. The equivalent circuit model of the on-chip PDN can be used to evaluate the on-chip PDN performance and optimize the impedance of the on-chip PDN with de-capacitors.

These contributions collectively enable accurate and efficient evaluation and optimization of signal integrity and power integrity in high-speed digital systems. The proposed models provide valuable tools for designers to enhance system performance and mitigate potential issues effectively.

PAPER

I. ELECTRICAL CHARACTERIZATION OF DIELECTRIC LIQUID AT MULTIPLE FREQUENCIES BASED ON A CYLINDRICAL CAVITY RESONATOR

ABSTRACT

We propose a cylindrical cavity resonator (CCR)-based method to measure the dielectric constant (Dk) and the loss tangent (Df) of the dielectric liquid at multiple resonance frequencies. The proposed CCR-based method can be used to characterize the Dk and Df of the dielectric liquid based on the extent to which the dielectric affects the resonances and Q-factors of the cavity. In short, the resonance frequencies and Q-factors of the resonance modes of the CCR will be altered when a dielectric liquid fills the cavity. The Dk and Df of the dielectric liquid can therefore be determined based on the change of resonance frequencies and Q-factors at multiple resonance modes. Because the cavity is completely filled, the cavity resonances are extremely sensitive to the dielectric liquid in the cavity. Thus, the proposed method can measure the electrical properties of even low-loss dielectric liquids such as coolant. In this paper, we design and then evaluate a CCR apparatus using full-wave simulations. The relative error of Dk and Df extracted by the proposed CCR-based method were less than 1% and 10%, respectively, based on simulation results. The designed CCR apparatus was also manufactured for further validation, and empirical laboratory measurements confirmed the accuracy and effectiveness of the proposed CCR-based method.

Keywords: coolant, cavity resonator, resonator apparatus, dielectric constant, loss tangent, liquid characterization, measurement, resonance modes.

1. INTRODUCTION

The rapid development of cloud services, edge computing, artificial intelligence, and the internet of things has driven an increasing demand for high-performance data centers. However, high-performance data centers pose a significant challenge for thermal cooling systems. One cooling method for high-performance systems is immersion or liquid cooling, in which electrical and electronic devices, such as complete servers and storage systems, are submerged in a thermally but not electrically conductive liquid [1], as shown in Fig. 1. Immersion cooling systems cool electronics more efficiently than conventional air-cooling methods while requiring less power and space, and they are also easier to be managed. Despite these advantages, the coolant can negatively affect the electrical performance of the exposed components, connectors, and transmission lines on the printed circuit board (PCB). For example, previous studies have described the impacts of the conductor and the dielectric on the PCB [2, 3]. Another study used empirical measurements to quantify the effect of immersion cooling on the peripheral component interconnect express (PCIe) links [4]. In general, to evaluate the effects of immersion cooling on PCB channels, the electrical properties of the coolant must be adequately characterized. These properties can also be useful at the design stage of the PCB.

The coolant in an immersion cooling system is a typical dielectric liquid, which is sensitive to factors such as temperature, moisture, and air pressure, among others. To

reduce the effect of the coolant on the PCB, the coolant must be a low-loss dielectric liquid. Several methods have been developed to characterize dielectric liquids; these methods can be categorized as either non-resonant methods (e.g., the transmission line-based method, capacitance method, coaxial probe method, or free space method) or resonant methods (e.g., the cavity resonator method or resonator sensor).

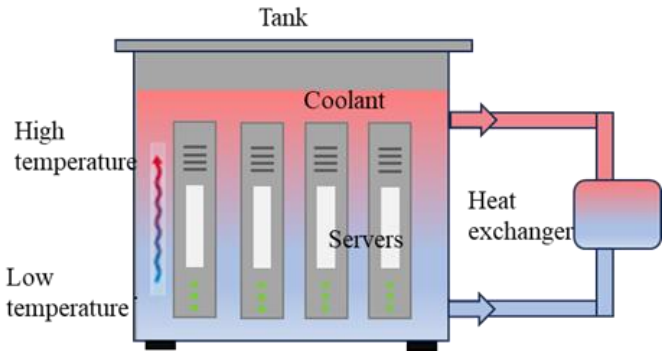


Figure 1. Immersion cooling for servers.

Non-resonant methods can generally characterize the dielectric liquid across a wide frequency bandwidth for the lossy material. For example, the transmission line-based method can measure the properties of a dielectric liquid from 10 MHz to 110 GHz [5]. However, accurate measurements from this method require the precise manufacture and model of the transmission line, especially when measuring low-permittivity dielectric liquids. One study recently proposed a cross-capacitance sensor to measure a dielectric liquid with low permittivity at low frequencies [6]. Conversely, the open-ended coaxial probe method has been widely used for high-permittivity liquids [7]. The free space method uses air as the transmission medium and is more suitable for high-lossy dielectric measurement in the millimeter wave range [8].

Compared with non-resonant methods, resonant methods are more sensitive to the dielectric liquid and are therefore highly accurate. Resonant methods can measure low-loss and low-permittivity dielectric liquids more accurately, and a multi-element complementary split-ring resonator has been proposed to measure high-loss and high-permittivity liquids [9]. The lossy liquid can also be measured using a multifrequency coupled-resonator sensor [10]. A stacked multi-ring resonator was developed to measure low-loss liquids, but this method only works at a specific frequency [11]. The cylindrical resonant cavity-based method, which works at TM_{0n0} modes, was likewise presented for low-loss liquids [12]. Overall, the available methods for characterizing dielectric liquids each have their advantages and limitations, and the best method for a specific application should therefore be selected on a case-by-case basis. The need for standardized measurements prompted the implementation of standard IEC 60247, which was proposed to improve measurement accuracy in dielectric liquid characterizations [13].

In this paper, we propose a cylindrical cavity resonator (CCR)-based method to accurately characterize the dielectric constant (Dk) and loss tangent (Df) of a low-loss dielectric liquid. Unlike other resonant methods, the method proposed here involves filling the cylindrical cavity with the dielectric liquid being tested, making the proposed method more sensitive to the dielectric permittivity. As a result, this method can accurately measure extremely low-loss dielectrics. Furthermore, the Dk and Df of the dielectric liquid can be extracted at multiple cavity resonance frequencies, which is meaningful for material characterization in practical applications. The following section introduces the design of the CCR apparatus and proposes the equivalent cavity model to calibrate H-probes and probing holes for cavity excitation. In Section III, we verify the proposed CCR-based

method and equivalent cavity model using full-wave simulations. The simulation results show that the relative error of Dk and Df extracted at five different resonance modes using the proposed CCR-based method could be less than 1% and 10%, respectively, when Dk is in the range of 2–10 and Df is in the range of 0.0003–0.002. We also manufacture the designed CCR apparatus and perform real lab measurements, which further verify the accuracy and effectiveness of the proposed method.

2. PROPOSED CCR-BASED METHOD

This section introduces our proposed CCR-based method. The CCR can work at different resonance modes (e.g., the transverse electric [TE] and transverse magnetic [TM] modes). Here, we use five different resonance modes as examples to demonstrate the proposed method for the characterization of a low-loss dielectric liquid.

2.1. CYLINDRICAL CAVITY RESONATOR

An electromagnetic wave can be confined inside a space, called a cavity, that is surrounded by conducting walls. A CCR is simply a cavity surrounded by a cylindrical-shaped conducting wall, which acts as a circular waveguide shorted at both ends. The cylindrical cavity can resonate at different transverse modes, such as the TE and TM modes. Fig. 2 shows the geometry of a typical cylindrical cavity. The resonance frequency of each resonance mode of the CCR can be calculated using Equations (1–2), which are based on the physics of the cavity [14]:

$$f_{mnp}^{TE} = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{x'_{mn}}{a}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \quad (1)$$

$$f_{mnp}^{TM} = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{x_{mn}}{a}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \quad (2)$$

In these equations, f_{mnp}^{TE} and f_{mnp}^{TM} are resonance frequencies of the TE_{mnp} modes and TM_{mnp} modes, respectively. M, n, and p represent the resonance mode numbers for the $\theta -$, $\rho -$, and $z -$directions, respectively, at the cylindrical coordinate. μ_r and ε_r are the relative permeability and the Dk of the dielectric in the cavity, respectively, and c is speed of light in the free space. x'_{mn} and x_{mn} are the n^{th} root of Bessel functions $J'_m(x')$ and $J_m(x)$, respectively [14], and a and h are the radius and the height of the cavity, respectively.

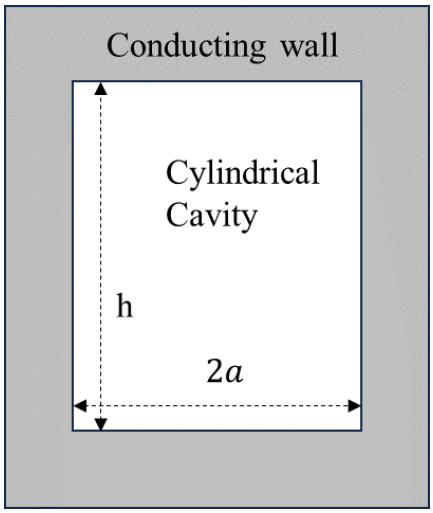


Figure 2. Cross-sectional view of a cylindrical cavity resonator.

The Q-factor of the ideal cylindrical cavity is associated with the properties of the material inside the cavity, the cavity size, and the conductivity of the cavity conductor. The cavity Q-factor can be calculated using the analytical formulas below.

For the TE modes,

$$Q_{mnp}^{TE} = 1/(\frac{2\pi\delta\left[(x'_{mn})^2+\left(\frac{p\pi}{2}\right)^2\left(\frac{2a}{h}\right)^3+\left(1-\frac{2a}{h}\right)\left(\frac{mp\pi a}{x'_{mn}h}\right)^2\right]}{\frac{c}{f_{mnp}^{TE}\sqrt{\mu_r\varepsilon_r}}\left[1-\left(\frac{m}{x'_{mn}}\right)^2\right]\left[(x'_{mn})^2+\left(\frac{p\pi a}{h}\right)^2\right]^{\frac{3}{2}}} + tan\delta) \quad (3)$$

For the TM modes,

$$Q_{mnp}^{TM} = 1/(\frac{\pi\delta\sqrt{\mu_r\varepsilon_r}f_{mnp}^{TM}(2+\frac{2a}{h})}{cx_{mn}} + tan\delta), \text{ when } p = 0 \quad (4)$$

$$Q_{mnp}^{TM} = 1/(\frac{2\pi\delta\sqrt{\mu_r\varepsilon_r}f_{mnp}^{TM}\left(1+\frac{2a}{h}\right)}{c\sqrt{(x_{mn})^2+\left(\frac{p\pi a}{h}\right)^2}} + tan\delta), \text{ when } p > 0 \quad (5)$$

where $\delta = \sqrt{\frac{1}{\pi\sigma\mu_0\mu_r f_{mnp}}}$ is the skin effect of the cavity conductor at the resonance frequency f_{mnp}, μ_0 is the permeability of the air, σ is the conductivity of the cavity conducting wall, and $tan\delta$ is the Df of the dielectric material inside the cavity.

Table 1. Verification of Equations (1–5).

Resonance modes	Ideal cylindrical cavity fully filled by dielectric. (a = 12 mm, h = 30 mm, $\sigma = 5 \times 10^8$), (Dk = 2, Df = 0.001)	
	HFSS Simulation Result	Equations (1 - 5)
TE_{111}	f = 6.267 GHz, Q = 913.83	f = 6.267 GHz, Q = 913.86
TM_{010}	f = 6.761 GHz, Q = 914.24	f = 6.761 GHz, Q = 914.27
TM_{011}	f = 7.629 GHz, Q = 898.04	f = 7.629 GHz, Q = 898.07
TE_{112}	f = 8.760 GHz, Q = 929.49	f = 8.759 GHz, Q = 929.53
TM_{012}	f = 9.781 GHz, Q = 908.87	f = 9.780 GHz, Q = 908.89

Equations (1–5) were verified using simulation results obtained from the high-frequency simulation simulator (HFSS) commercial software using the “solution” type of eigenmode. As shown in Table I, the simulated resonance frequencies f and Q-factors Q of an ideal cylindrical cavity perfectly match the results calculated using Equations (1–5) for five different example resonance modes. Equations (1–5) can therefore specify the relationship between dielectric properties and cavity resonance modes. If the cavity size and the cavity wall conductivity are known, these formulas can be used to extract the Dk and the Df of the dielectric filled in the cavity at different resonance frequencies when the cavity resonances are measured.

2.2. THE DESIGNED CCR APPARATUS

For laboratory measurements, the cavity must be excited using a probe or aperture. Fig. 3 shows the CCR apparatus that was designed for the laboratory measurements that were used to verify the CCR-based characterization method proposed here. This CCR apparatus consists of a cylindrical cavity and two PCB probes used to excite the cavity. The cavity has a lid that can be manually opened or closed for ease of filling or removing the dielectric. The PCB probes are magnetic field (H) probes typically used for near-field scanning [15]. Two small probing holes on the side wall of the cavity facilitate probe insertion and cavity excitation. The transmission loss between the H-probes can be measured using a vector network analyzer, and the resonance and Q-factor of the designed CCR apparatus can be calculated based on the measured transmission loss of the two H-probes.

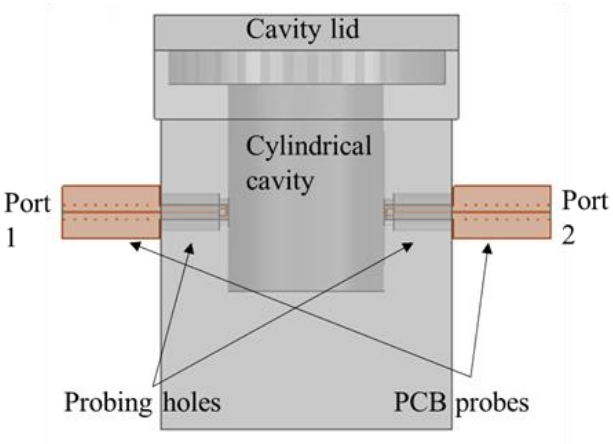


Figure 3. Cross-sectional view of the designed CCR apparatus.

Because the PCB probes and probing holes act as the external circuit to be connected by the dielectric in the cavity, the resonance frequencies and Q-factors of the cylindrical cavity are affected by the PCB probes and probing holes. The designed CCR apparatus is therefore not an ideal cylindrical cavity like the one shown in Fig. 2. Instead, the designed CCR apparatus is a loaded cavity resonator, and the resonances of this apparatus can be simulated using HFSS as shown in Fig. 3. In this simulation, the cavity is first excited by the PCB probes. The resonance frequencies and Q-factors are then calculated based on the simulated transmission loss of the PCB probes. The effect of the probes and probing holes on the resonance frequencies and Q-factors of the cavity are evaluated based on the simulation results. Table II shows the resonance frequencies and Q-factors at five different modes of the designed CCR apparatus as simulated by HFSS and calculated by Equations (1–5). The resonance frequency at each mode of the cylindrical cavity decreases by more than 100 MHz due to the effect of the probes and probing holes. Moreover, the Q-factor at each mode of the cylindrical cavity decreases by more than 700, which can cause a large error in the Df measurement for a low-loss dielectric. The effect

of probes and probing holes on the designed CCR apparatus therefore cannot be ignored. The comparisons shown in Table II further suggest that the probes and probing holes impact the TE modes of the cavity resonance much more than TM modes.

Table 2. Resonance frequencies and Q-factors at five different resonance modes of the designed CCR apparatus.

Resonance modes	Designed apparatus without dielectric inside. (a = 11.31 mm, h = 30 mm, $\sigma = 3.8 \times 10^7$)	
	HFSS Simulation Result	Equations (1 - 5)
TE_{111}	f = 9.3327 GHz, Q = 5185	f = 9.235 GHz, Q = 9886
TM_{010}	f = 10.2991 GHz, Q = 9363	f = 10.1452 GHz, Q = 10133
TM_{011}	f = 11.4666 GHz, Q = 7640	f = 11.3089 GHz, Q = 8399
TE_{112}	f = 12.768 GHz, Q = 10050	f = 12.6563 GHz, Q = 12318
TM_{012}	f = 14.3672 GHz, Q = 7562	f = 14.2403 GHz, Q = 9425

2.3. THE PROPOSED METHOD

It is difficult to derive the analytical model for the designed CCR apparatus given the probes and probing holes. Here, we use the equivalent theory to model the designed CCR apparatus. The designed CCR apparatus is assumed to be equivalent to an ideal cylindrical cavity that lacks the probes and probing holes. However, the size of this equivalent ideal cavity and the conductivity of its conductor would be different from the size and conductor conductivity of the real apparatus. In other words, the effect of the probes and probing holes in the designed CCR apparatus must be compensated for by the

equivalent size and the equivalent conductor conductivity of the corresponding ideal cylindrical cavity.

Before characterizing dielectric properties, we extract the equivalent radius of the designed resonator apparatus based on the measured resonance frequency when the resonator apparatus is empty. The equivalent radius of the designed CCR apparatus can be calculated as follows.

For TE_{mnp} modes,

$$a_{mnp}^{TE} = \frac{x'_{mn}}{\sqrt{\left(\frac{2\pi f_{mnp\_meas}^{TE}\sqrt{\mu_r\varepsilon_r}}{c}\right)^2 - \left(\frac{p\pi}{h}\right)^2}} \tag{6}$$

For TM_{mnp} modes,

$$a_{mnp}^{TM} = \frac{x_{mn}}{\sqrt{\left(\frac{2\pi f_{mnp\_meas}^{TM}\sqrt{\mu_r\varepsilon_r}}{c}\right)^2 - \left(\frac{p\pi}{h}\right)^2}} \tag{7}$$

where $f_{mnp\_meas\_e}^{TE}$ and $f_{mnp\_meas\_e}^{TM}$ are the resonance frequencies of the designed CCR apparatus measured for the corresponding resonance modes TE_{mnp} and TM_{mnp}, respectively, when the apparatus is empty. The effect of the H-probes and probing holes on the cavity resonance frequency is therefore compensated by the equivalent cavity radius. The Q-factor of the designed CCR apparatus is the loaded Q-factor Q_L, which accounts for the impact of H-probes and probing holes. The Q_L can be represented as:

$$Q_L = \frac{1}{\frac{1}{Q_c}+\frac{1}{Q_d}+\frac{1}{Q_{ext}}} \tag{8}$$

where Q_c and Q_d are the Q-factors of the apparatus related to the conductor loss and dielectric loss, respectively, inside the apparatus. Q_{ext} is the Q-factor related to the loss caused by the H-probes and probing holes on the side wall of the apparatus. However, it is

difficult to identify Q_{ext}. Instead, we use the equivalent conductivity of the cavity conductor to compensate for the impact of the H-probes and probing holes. The equivalent conductor conductivity should be extracted based on the measured Q-factor when the cavity is empty and can be calculated as shown below:

For TE_{mnp} modes,

$$\sigma_{mnp}^{TE} = \left\{ \frac{2\pi\sqrt{\mu_r\varepsilon_r}Q_{mnp_{meas}}^{TE} f_{mnp_{meas}}^{TE}\left[(x'_{mn})^2+\left(\frac{p\pi}{2}\right)^2\left(\frac{2a}{h}\right)^3+\left(1-\frac{2a}{h}\right)\left(\frac{mp\pi a}{x'_{mn}h}\right)^2\right]}{c\left[1-\left(\frac{m}{x'_{mn}}\right)^2\right]\left[(x'_{mn})^2+\left(\frac{p\pi a}{h}\right)^2\right]^{\frac{3}{2}}\sqrt{\pi\mu_0\mu_r f_{mnp_{meas}}^{TE}}} \right\}^2 \tag{9}$$

For TM_{mnp} modes,

$$\sigma_{mnp}^{TM} = \left(\frac{\pi\sqrt{\mu_r\varepsilon_r}\left(2+\frac{2a}{h}\right) f_{mnp\_meas}^{TM} Q_{mnp\_meas}^{TM}}{c x_{mn}\sqrt{\pi\mu_0\mu_r f_{mnp\_meas}^{TE}}} \right)^2, \text{ when } p = 0 \tag{10}$$

$$\sigma_{mnp}^{TM} = \left(\frac{2\pi\sqrt{\mu_r\varepsilon_r}\left(1+\frac{2a}{h}\right) f_{mnp\_meas}^{TM} Q_{mnp\_meas}^{TM}}{c\sqrt{(x_{mn})^2+\left(\frac{p\pi a}{h}\right)^2}\sqrt{\pi\mu_0\mu_r f_{mnp\_meas}^{TE}}} \right)^2, \text{ when } p > 0 \tag{11}$$

where $Q_{mnp\_meas}^{TE}$ and $Q_{mnp\_meas}^{TM}$ are the Q-factors of the designed CCR apparatus measured for the corresponding resonance modes TE_{mnp} and TM_{mnp}, respectively, when the apparatus is empty.

When the designed CCR apparatus is filled with the dielectric liquid being tested, the resonance frequency and Q-factor can be measured using a vector network analyzer. The Dk and the Df of the dielectric liquid can then be calculated based on these measured resonance frequencies and Q-factors:

For TE_{mnp} modes,

$$Dk_{mnp}^{TE} = \left(\frac{c}{2\pi f_{mnp\_meas\_f}^{TE}\sqrt{\mu_r}} \sqrt{\left(\frac{x'_{mn}}{a_{mnp}^{TE}}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \right)^2 \quad (12)$$

$$Df_{mnp}^{TE} = \frac{1}{Q_{mnp}^{TE}} - \frac{2\pi\delta_{mnp}^{TE}\left[\left(x'_{mn}\right)^2 + \left(\frac{p\pi}{2}\right)^2\left(\frac{2a_{mnp}^{TE}}{h}\right)^3 + \left(1 - \frac{2a_{mnp}^{TE}}{h}\right)\left(\frac{mp\pi a_{mnp}^{TE}}{x'_{mn}h}\right)^2\right]}{\frac{c}{f_{mnp\_meas\_f}^{TE}\sqrt{\mu_r Dk_{mnp}^{TE}}}\left[1 - \left(\frac{m}{x'_{mn}}\right)^2\right]\left[\left(x'_{mn}\right)^2 + \left(\frac{p\pi a_{mnp}^{TE}}{h}\right)^2\right]^{\frac{3}{2}}} \quad (13)$$

For TM_{mnp} modes,

$$Dk_{mnp}^{TM} = \left[\frac{c}{2\pi f_{mnp_{meas_f}}^{TM}\sqrt{\mu_r}} \sqrt{\left(\frac{x_{mn}}{a_{mnp}^{TM}}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \right]^2 \quad (14)$$

$$Df_{mnp}^{TM} = \frac{1}{Q_{mnp\_meas\_f}^{TM}} - \frac{\pi\delta_{mnp}^{TM}\sqrt{\mu_r Dk_{mnp}^{TM}}\left(2 + \frac{2a_{mnp}^{TM}}{h}\right)f_{mnp\_meas\_f}^{TM}}{cx_{mn}}, \quad \text{when } p = 0 \quad (15)$$

$$Df_{mnp}^{TM} = \frac{1}{Q_{mnp\_meas\_f}^{TM}} - \frac{2\pi\delta_{mnp}^{TM}\sqrt{\mu_r Dk_{mnp}^{TM}}\left(1 + \frac{2a_{mnp}^{TM}}{h}\right)f_{mnp\_meas\_f}^{TE}}{c\sqrt{(x_{mn})^2 + \left(\frac{p\pi a_{mnp}^{TM}}{h}\right)^2}}, \quad \text{when } p > 0 \quad (16)$$

where $\delta_{mnp} = \sqrt{\frac{1}{\pi\sigma_{mnp}\mu_0\mu_r f_{mnp}}}$ is the equivalent skin effect of the designed CCR apparatus conductor. $f_{mnp\_meas\_f}^{TE}$, $f_{mnp\_meas\_f}^{TM}$, $Q_{mnp\_meas\_f}^{TE}$, and $Q_{mnp\_meas\_f}^{TM}$ are the measured resonance frequencies and Q-factors for the corresponding resonance TE_{mnp} and TM_{mnp} modes of the apparatus when it is fully filled with the dielectric liquid being tested. The Dk and Df of a dielectric liquid can therefore be calculated using Equations (6–16), which rely on the measured resonance frequencies and Q-factors for (i) the empty apparatus and (ii) the apparatus fully filled by the dielectric liquid being tested.

2.4. DK AND DF EXTRACTION PROCEDURES

Based on Equations (6–16) above, our proposed CCR-based procedure for calculating the Dk and Df of a dielectric liquid is as follows:

i) Measure the empty cavity resonator apparatus to obtain the f_{mnp_meas} and Q_{mnp_meas}.

ii) Use Equations (6–11) to calculate the equivalent size a_{mnp} and the equivalent conductivity σ_{mnp} of the resonator apparatus based on the measured f_{mnp_meas} and Q_{mnp_meas}.

iii) Measure the cavity resonator apparatus fully filled by the dielectric liquid under test to obtain the $f_{mnp\_meas\_f}$ and $Q_{mnp\_meas\_f}$.

iv) Measure the cavity resonator apparatus fully filled by the dielectric liquid under test to obtain the $f_{mnp\_meas\_f}$ and $Q_{mnp\_meas\_f}$.

The first two steps of this procedure are calibration steps designed to compensate for the effect of the H-probes and probing holes on the resonance frequency and Q-factors of the real apparatus by extracting the equivalent cavity radius and conductivity of an idealized apparatus. In other words, this procedure ensures that the real apparatus is mathematically equivalent to an ideal cavity resonator without H-probes and probing holes. The second two steps of the measurement procedure extract the Dk and Df, at corresponding resonance frequencies, for the dielectric liquid filling the apparatus.

3. VERIFICATION AND ANALYSIS

In this section, we verify our proposed CCR-based method using full-wave simulations and measurements, and we use these results to confirm the accuracy and effectiveness of the proposed method.

3.1. FULL-WAVE SIMULATION VERIFICATION

Based on the simulated resonance frequencies and Q-factors for five different resonance modes of the designed CCR apparatus, as shown in Table II, the equivalent radius and the equivalent conductivity at each mode can be calculated using Equations (6–11). Table III shows these equivalent radii and conductivities for the equivalent ideal cavity model to clarify the effect of the H-probes and probing holes on the resonance frequencies for each resonance mode. The data in Table III suggest that the equivalent radius and the equivalent conductivity at each mode are all decreased relative to the designed CCR apparatus due to the effect of PCB probes and probing holes, though the magnitude of these decreases differ across the different resonance modes.

To verify our proposed method, we simulated the resonance frequencies and Q-factors for the designed CCR apparatus when filled with various simulated dielectric liquids outlined in Table IV. Based on the simulated resonance frequencies and Q-factors shown in Table IV, the Dk and Df of the dielectric used in the simulation can be accurately extracted using the CCR-based method proposed here. The "input Dk and Df" in Table IV are the dielectric properties used in the simulation, and the relative error σ, defined as $\sigma = \left|\frac{input - extracted}{input}\right| \times 100\%$, is used to quantify the accuracy of the proposed method. As

shown in Table IV, the relative errors of the calculated Dk and Df of the dielectric at TM modes are less than 1% and 5%, respectively, and the relative errors of the calculated Dk and Df at TE modes are less than 1% and 10%, respectively. Thus, the simulation results suggest that the CCR-based characterization method is sufficiently accurate for Dk and Df determination, though the relative error of Df extraction is larger at TE modes than TM modes due to the H-probe. H-probes are used to excite the cavity, and the probe is more sensitive to TM modes because it is vertically located in the apparatus.

Table 3. Equivalent sizes and conductivities of the equivalent ideal cavity model at five different resonance modes corresponding to the simulated apparatus. (Calculated based on equations (6-11)).

Designed apparatus	a = 11.31 mm, h = 30 mm, $\sigma = 3.8 \times 10^7$				
Resonance Modes	TE_{111}	TM_{010}	TM_{011}	TE_{112}	TM_{012}
Equivalent cavity radius (mm)	a_{111}^{TE}= 11.144	a_{010}^{TM} = 11.141	a_{011}^{TM} = 11.118	a_{112}^{TE} = 11.053	a_{012}^{TM} = 11.116
Equivalent conductivity (s/m)	σ_{111}^{TE} = 1.061e7	σ_{010}^{TM} = 3.266e7	σ_{011}^{TM} = 3.158e7	σ_{112}^{TE} = 2.590e7	σ_{012}^{TM} = 2.470e7

Table 4. Simulation-based verification of the proposed method performed by sweeping the Dk and Df of the dielectric.

(a)

	Input Dk and Df	Dk = 2 Df = 0.002	Dk = 4 Df = 0.001	Dk = 7 Df = 0.0005	Dk = 10 Df = 0.0003	Maximum relative error
TE_{111}	Simulated f (GHz) and Q	f = 6.5975 Q = 431	f = 4.6644 Q = 821	f = 3.526 Q = 1278	f = 2.9501 Q = 1611	-
	Extracted Dk and Df	Dk = 2.001 Df = 0.00209	Dk = 4.003 Df = 0.000945	Dk = 7.01 Df = 0.000469	Dk = 10.01 Df = 0.000278	-
	Relative error σ_{DK} and σ_{Df}	0.05% and 4.5%	0.08% and 5.5%	0.14% and 6.2%	0.1% and 7.3%	0.14% and 7.3%

Table 4. Simulation-based verification of the proposed method performed by sweeping the Dk and Df of the dielectric. (cont.)

(b)

	Input Dk and Df	Dk = 2 Df = 0.002	Dk = 4 Df = 0.001	Dk = 7 Df = 0.0005	Dk = 10 Df = 0.0003	Maximum relative error
TM_{010}	Simulated f (GHz) and Q	f = 7.2696 Q = 469	f = 5.1358 Q = 871	f = 3.8818 Q = 1490	f = 3.2476 Q = 2030	-
	Extracted Dk and Df	Dk = 2.007 Df = 0.00201	Dk = 4.021 Df = 0.00102	Dk = 7.04 Df = 0.000497	Dk = 10.06 Df = 0.000302	-
	Relative error σ_{DK} and σ_{Df}	0.35% and 0.5%	0.53% and 2%	0.57% and 0.6%	0.6% and 0.67%	0.57% and 2%
TM_{011}	Simulated f (GHz) and Q	f = 8.0881 Q = 459	f = 5.7141 Q = 838	f = 4.3189 Q = 1393	f = 3.6133 Q = 1888	-
	Extracted Dk and Df	Dk = 2.01 Df = 0.00202	Dk = 4.027 Df = 0.00101	Dk = 7.05 Df = 0.000505	Dk = 10.07 Df = 0.000296	-
	Relative error σ_{DK} and σ_{Df}	0.5% and 1%	0.67% and 1%	0.7% and 1%	0.7% and 1.3%	0.7% and 1.3%

Table 4. Simulation-based verification of the proposed method performed by sweeping the Dk and Df of the dielectric. (cont.)

(c)

	Input Dk and Df	Dk = 2 Df = 0.002	Dk = 4 Df = 0.001	Dk = 7 Df = 0.0005	Dk = 10 Df = 0.0003	Maximum relative error
TE_{112}	Simulated f (GHz) and Q	f = 9.0017 Q = 457	f = 6.3613 Q = 837	f = 4.8087 Q = 1500	f = 4.0233 Q = 2010	-
	Extracted Dk and Df	Dk = 2.012 Df = 0.00207	Dk = 4.029 Df = 0.00105	Dk = 7.05 Df = 0.000505	Dk = 10.07 Df = 0.000320	-
	Relative error σ_{DK} and σ_{Df}	0.6% and 3.5%	0.72% and 5%	0.71% and 2.6%	0.05% and 6.7%	0.72% and 6.7%
TM_{012}	Simulated f (GHz) and Q	f = 10.1417 Q = 461	f = 7.1659 Q = 778	f = 5.4164 Q = 1350	f = 4.5316 Q = 1888	-
	Extracted Dk and Df	Dk = 2.007 Df = 0.00201	Dk = 4.020 Df = 0.001	Dk = 7.04 Df = 0.000505	Dk = 10.05 Df = 0.000294	-
	Relative error σ_{DK} and σ_{Df}	0.35% and 0.5%	0.5% and 0%	0.57% and 1%	0.5% and 2%	0.57% and 2%

3.2. IMPACT OF CAVITY HEIGHT

The proposed CCR-based method for dielectric characterization involves modeling the designed CCR apparatus as an ideal CCR by extracting the equivalent cavity radius and conductivity. However, we assume that the cavity height of the designed CCR apparatus is equal to the height of the equivalent ideal CCR. In reality, the cavity height would vary due to manufacturing uncertainty or measurement inaccuracy. In other words, the cavity height used to calculate dielectric properties may not be the true, accurate value. Variation in the cavity height of the designed CCR apparatus would affect the accuracy of the calculated dielectric properties.

We used full-wave simulations to evaluate the effect of cavity height on the Dk and Df extraction accuracy for a dielectric. Here, we present the results for an example dielectric with $Dk = 2$ and $Df = 0.002$, for which the dielectric properties were calculated at the resonance of the TM_{010} mode. The true cavity height h_r was decreased or increased from the reference height h of 30 mm. Fig. 4 shows the relative error of the extracted Dk and Df as a function of the relative change in cavity height. Even when the cavity height is adjusted by $\pm 5\%$, the relative errors of the extracted Dk and Df are still less than 1% and 5%, respectively. In practice, cavity height variation can be controlled below 5 mils, which is less than 1% of the designed cavity height used here. Based on the analysis, we conclude that the effect of cavity height variation on Dk and Df determination for the designed CCR apparatus can be ignored.

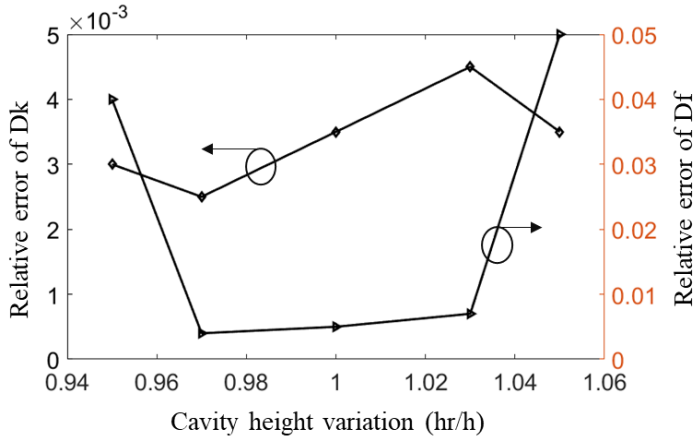
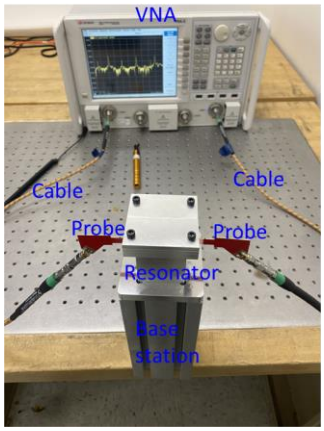


Figure 4. Effect of cavity height variation on the accuracy of calculated Dk and Df values.

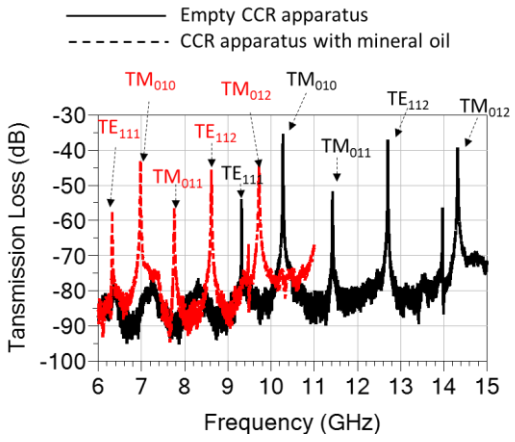
3.3. MEASUREMENT VERIFICATION

The designed CCR apparatus was then manufactured for measurement verification. The measurement setup for the manufactured CCR apparatus is shown in Fig. 5-(a). The vector network analyzer (VNA) is connected to the PCB probes, which are inserted into the manufactured CCR apparatus. With this setup, the resonance frequencies and Q-factors of the manufactured apparatus can be extracted at different resonance modes based on the transmission loss measured by the VNA. Before the measurement, the resonance frequencies of the manufactured apparatus at specific resonance modes can be roughly estimated using the designed CCR apparatus cavity size and Equations (1–2). The estimated resonance frequencies can then be used to help set up the measurement frequency bandwidth of the VNA. To obtain an accurate measurement of the Q-factor of the manufactured CCR apparatus, the internal frequency of the VNA is set at 1 KHz and the frequency step is 0.1 MHz. The measured transmission losses of the empty apparatus are plotted with a solid black line in Fig. 5-(b), and the transmission losses when the apparatus

is filled with mineral oil are shown with a dotted red line. Five different resonance modes are marked for both the empty and full apparatus. As shown in Fig. 5-(b), the resonance frequency decreased by more than 3 GHz when the manufactured CCR apparatus was filled with the dielectric, and the transmission loss obviously increased due to the dielectric loss of the mineral oil.



(a)



(b)

Figure 5. (a) Measurement setup. (b) Measured transmission loss when the manufactured CCR apparatus is empty or is filled with mineral oil.

To verify the proposed method, we measured the Dk and Df of a known material, mineral oil, at multiple resonance modes using the manufactured CCR apparatus at room temperature. Measurements were conducted six times at each resonance mode to evaluate the measurement uncertainty.

The average measured Dk and Df are listed in Table V, and the deviation shown in Table V represents the measurement uncertainty across the six measurements. The deviation of the extracted Dk was less than 0.5% at all resonance modes, indicating stable measurements for our proposed method of Dk extraction. The deviation of the extracted Df was below 5% except at resonance modes TM011 and TM012. The deviation for Df is larger than for Dk, but from an engineering perspective, these values are still acceptable for a very low-loss material. For comparison and further validation, Table V also lists the Dk and Df of mineral oil reported from other publications.

Overall, the Dk and Df that we measured using our CCR-based method were consistent with the results from previous studies [16, 17], thereby verifying the accuracy of our proposed method. This method will be further verified through future empirical tests of additional dielectric liquids.

Table 5. Dk and Df measurement of mineral oil using the proposed CCR-based method.

	Resonance modes	**Resonance frequency and Q-factor of empty CCR apparatus**	**Resonance frequency and Q-factor of CCR apparatus filled by mineral oil**	**Measured Dk and Df**	**Deviation**
Proposed method	TE_{111}	f = 9.3141 Q = 5360	f = 6.3182 Q = 1564.8	Dk = 2.1732 Df = 4.13e-4	± 0.1% ± 4%
	TM_{010}	f = 10.2759 Q = 4161	f = 6.9742 Q = 1425.8	Dk = 2.171 Df = 4.10 e-4	± 0.2% ± 4%
	TM_{011}	f = 11.4232 Q = 2750	f = 7.7577 Q = 1118	Dk = 2.1683 Df = 4.53e-4	± 0.3% ± 11%
	TE_{112}	f = 12.7026 Q = 5130	f = 8.6164 Q = 1667.2	Dk = 2.1734 Df = 3.63e-4	± 0.03% ± 5%
	TM_{012}	f = 14.3198 Q = 2440	f = 9.7204 Q = 1183.2	Dk = 2.1702 Df = 3.48e-4	± 0.03% ± 12%
Electrode method [16]	-	-	-	Dk = 2.2 Df = 0.32e-4 -- 3.35e-4	-
Electrode method [17]	-	-	-	Dk = 2.16 Df = 1e-5 – 4e-4	-

We also used the manufactured CCR apparatus to measure the Dk and Df of various coolants from different vendors. Table VI compares the measured results from our proposed method with the data reported by the respective datasheets. For all tested coolants, the measured Dk is very close to the data provided by the vendors, further verifying the effectiveness and accuracy of the proposed method for the Dk measurement. The discrepancy of measured Dks and the data from vendor is less than 2%.

The measured Df of coolants produced by vendor A were also well-correlated with the data from the vendor, with a discrepancy less than 15%. Vendor B and C cannot provide the Df of their coolants because they do not have a suitable method to determine the Df for such low-loss dielectric liquids. The coolant from D is a new product and the vendor was unable to provide the datasheet at the time of this study. In conclusion, measurements of the coolants by the manufactured CCR apparatus verify the accuracy and effectiveness of the proposed method for the low-loss dielectric liquid characterization.

Overall, the Dk and Df of a coolant, as determined by the CCR-based method proposed here, can be used to help evaluate the effect of the coolant on the electronics in an immersion cooling system. Furthermore, the measurements reported here may help guide engineers from electronics companies when selecting the appropriate coolant for their specific applications.

Table 6. Measurement of the Dk and Df of coolants from different vendors.

(a)

Vendor	Liquid name	Resonance modes	Resonance frequency f (GHz) and Q-factor	Measured Dk and Df with deviation	Dk and Df from datasheet
A	1	TE_{111}	f = 6.4672 Q = 713.7	Dk = 2.074 ± 0.01% Df = 1.24e-3 ± 7%	Dk = 2.07 Df = 0.0011
		TM_{010}	f = 7.1383 Q = 690.7	Dk = 2.072 ± 0.3% Df = 1.18e-3 ± 3%	
		TM_{011}	f = 7.9399 Q = 635.3	Dk = 2.07 ± 0.5% Df = 1.24e-3 ± 9%	
		TE_{112}	f = 8.8212 Q = 705	Dk = 2.074 ± 0.06% Df = 1.24e-3 ± 5%	
		TM_{012}	f = 9.948967 Q = 609	Dk = 2.072 ± 0.3% Df = 1.19e-3 ± 4%	

Table 6. Measurement of the Dk and Df of coolants from different vendors. (cont.)

(b)

Vendor	Liquid name	Resonance modes	Resonance frequency f (GHz) and Q-factor	Measured Dk and Df with deviation	Dk and Df from datasheet
A	2	TE_{111}	f = 6.4077 Q = 713.7	Dk = 2.113 ± 0.03% Df = 1.19e-3 ± 4%	Dk = 2.11 Df = 0.0011
		TM_{010}	f = 7.0988 Q = 708	Dk = 2.095 ± 0.03% Df = 1.15e-3 ± 1%	
		TM_{011}	f = 7.9196 Q = 652	Dk = 2.081 ± 0.03% Df = 1.14e-3 ± 1%	
		TE_{112}	f = 8.7444 Q = 726	Dk = 2.11 ± 0.03% Df = 1.16e-3 ± 1%	
		TM_{012}	f = 9.8919 Q = 593	Dk = 2.096 ± 0.03% Df = 1.23e-3 ± 5%	

Table 6. Measurement of the Dk and Df of coolants from different vendors. （cont.）

(c)

Vendor	Liquid name	Resonance modes	Resonance frequency f (GHz) and Q-factor	Measured Dk and Df with deviation	Dk and Df from datasheet
B	3	TE_{111}	f = 6.4279 Q = 1531.8	Dk = 2.10 ± 0.02% Df = 4.42e-4 ± 5%	Dk = 2.10 (vendor cannot provide Df)
		TM_{010}	f = 7.0931 Q = 1385	Dk = 2.099 ± 0.2% Df = 4.60e-4 ± 3%	
		TM_{011}	f = 7.8888 Q = 1101	Dk = 2.097 ± 0.2% Df = 4.13e-4 ± 10%	
		TE_{112}	f = 8.7661 Q = 1544	Dk = 2.10 ± 0.01% Df = 4.33e-4 ± 4%	
		TM_{012}	f = 9.8863 Q = 1137.5	Dk = 2.098 ± 0.02% Df = 4.19e-4 ± 1%	

Table 6. Measurement of the Dk and Df of coolants from different vendors. （cont.）

(d)

Vendor	Liquid name	Resonance modes	Resonance frequency f (GHz) and Q-factor	Measured Dk and Df with deviation	Dk and Df from datasheet
C	4	TE_{111}	f = 6.4254 Q = 1426.3	Dk = 2.101 ± 0.01% Df = 4.90e-4 ± 4%	Dk = 2.10 (vendor cannot provide Df))
		TM_{010}	f = 7.0973 Q = 1359	Dk = 2.096 ± 0.1% Df = 4.74e-4 ± 5%	
		TM_{011}	f = 7.903 Q = 1100	Dk = 2.089 ± 0.3% Df = 5.14e-4 ± 7%	
		TE_{112}	f = 7.903 Q = 1436.3	Dk = 2.101 ± 0.01% Df = 4.81 e-4 ± 4%	
		TM_{012}	f = 9.7204 Q = 1103	Dk = 2.096 ± 0.03% Df = 4.47e-4 ± 5%	

Table 6. Measurement of the Dk and Df of coolants from different vendors. （cont.）

(e)

Vendor	Liquid name	Resonance modes	Resonance frequency f (GHz) and Q-factor	Measured Dk and Df with deviation	Dk and Df from datasheet
D	5	TE_{111}	f = 6.4138 Q = 498.3	Dk = 2.109 ± 0.03% Df = 1.80e-3 ± 10%	(vendor cannot provide data)
		TM_{010}	f = 7.0769 Q = 495	Dk = 2.108 ± 0.1% Df = 1.76e-3 ± 1%	
		TM_{011}	f = 7.87095 Q = 479.3	Dk = 2.106 ± 0.2% Df = 1.69e-3 ± 8%	
		TE_{112}	f = 8.747 Q = 512.8	Dk = 2.109 ± 0.02% Df = 1.73e-3 ± 3%	
		TM_{012}	f = 9.8641 Q = 465.8	Dk = 2.108 ± 0.1% Df = 1.69e-3 ± 2%	

4. CONCLUSION

In this paper, we proposed a new CCR-based method for characterizing low-loss dielectric liquids, and we verified this method using full-wave simulations and empirical measurements. The methodology underlying the proposed method was first introduced and described. We then derived the analytical equations to calculate the resonance frequencies and Q-factors of the CCR, and we verified these equations using simulation results from HFSS. To measure the resonance frequency and Q-factor of the CCR in the real world, we designed H-probes and probing holes to excite the cavity of the apparatus. The H-probes and probing holes were calibrated using the equivalent cavity model of the designed CCR apparatus, such that the effect of the H-probes and probing holes on the cavity resonances of the designed apparatus can be compensated for by the equivalent cavity radius and the equivalent cavity conductivity.

The accuracy of the proposed CCR-based method was investigated at five different resonance modes using full-wave simulations. Although we only considered five different modes, the proposed method can theoretically work at any resonance mode. Based on the full-wave simulations, the relative errors of the Dk and Df extracted by the proposed method for the tested dielectric were less than 1% and 10%, respectively, at the five different modes. The designed CCR apparatus was then manufactured to verify the proposed CCR-based method. The manufactured CCR apparatus was used to measure the Dk and Df of mineral oil; the laboratory measurements were well-correlated with data from other publications, thus verifying the proposed method. The proposed method will be further verified with different dielectric liquids in the future. We additionally used the

manufactured CCR apparatus to determine the Dk and Df of coolants from different vendors, and the measured Dk of the coolants were close to the Dk provided by the vendors. The measured Dk and Df of the coolants reported here can help PCB designers select the appropriate coolant when designing the PCB or other electronics that require immersion cooling.

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II. MODE-DECOMPOSITION-BASED EQUIVALENT MODEL OF HIGH-SPEED VIAS UP TO 100 GHZ

ABSTRACT

Via transitions in high-speed channels critically influence the signal integrity and power integrity of high-speed systems. In this work, a mode-decomposition-based equivalent model of a high-speed via that can be applied at frequencies up to 100 GHz is proposed for the first time. The equivalent model for modeling the via transition consists of upper and lower via-to-plate capacitances and equivalent parallel-plate impedances, owing to the fundamental mode and higher-order modes for parallel-plate, all of which can be calculated from physical geometrical parameters. The via-to-plate capacitances are calculated by using the domain decomposition method in the anti-pad domain and via domain. The parallel-plate impedances representing via and parallel-plate coupling are calculated with the mode decomposition method for different parallel-plate modes (fundamental and higher-order modes) in the parallel-plate domain. The proposed equivalent via model provides more accurate results in the high-frequency range than previously proposed methods. Because the impact of higher-order modes on parallel-plate impedance is considered in the proposed mode-decomposition-based via model, and the effects of higher-order modes are prominent at high frequencies for printed circuit board vias with typical dimensions. The proposed model is validated with numerical examples, which show good correlation at frequencies as high as 100 GHz. The proposed model can be applied to high-speed via transitions in printed circuit boards and packages.

Keywords: Mode-decomposition equivalent model, high-speed channel, via, parallel plate, higher-order mode.

1. INTRODUCTION

Vertical interconnectors, more commonly known as vias, play essential roles in modern high-speed digital systems for connecting signals in multiplayer printed circuit boards (PCBs) and packages [1]. With increases in the number of integrated devices and the requirement for higher densities, vias have become ubiquitous in multilayer PCBs. Vias are used to route signals on different layers for different channels, which are typical discontinuous components in high-speed channels and can lead to severe signal integrity and power integrity problems. Therefore, accurate modeling of these interconnect components is necessary for high-speed channel design and optimization.

Various methods of via modeling have been developed in recent decades, including full-wave solvers based on the finite-difference time-domain method, finite-element method [2], [3], multiple scattering methods [4], [8], analytical and semi-analytical approaches [9], [10], and equivalent circuit methods [16]. Full-wave solvers can provide accurate simulation results, but they require substantial computational power and time to simulate a multilayer board with many vias. Multiple scattering methods based on the Foldy-Lax approach have been used to model dense vias with rectangular ground plates [5], [6]. Improved multiple methods have been introduced for dense bias modeling with arbitrarily or irregularly shaped ground plates [7], [8]. In one study [8], the general multiple scattering method was proposed to model dense vias with axially anisotropic modes in an

arbitrarily shaped plate pair. But it was only validated up to 50 GHz. In addition, the separation between vias and the distance of vias to plate edges should be sufficiently large to neglect the coupling of them by the higher-order evanescent modes for saving the computational time. Analytical or semi-analytical approaches can also be used to model dense vias with arbitrarily shaped plate pairs [9], [10], [12]; however, their upper frequency is limited, and these approaches do not provide sufficient physical insight for channel designers at higher bandwidths. Equivalent modeling methods of differential vias based on the PEEC method have been introduced [13]-[15]. In the equivalent circuit method, a via with parallel plates is first modeled by a π-type circuit with lumped elements [16], [17]. The associated models enable highly efficient simulation because the circuit elements can be calculated from analytical formulas. The topology of an equivalent circuit model provides physics-based insight for guidance in designing vias. To improve the accuracy of equivalent circuits, physics-based equivalent models have been proposed [18], [19], which use the parallel-plate impedance, Z_{pp}, to model the interconnection between the via and plates, on the basis of the fundamental mode (propagating mode) in parallel plates. The physics-based via model has been verified with measurements [20], [21]. In [22], and the capacitance coupling between the via and the parallel plate is represented by the transmission model. The closed-form expression of the parallel-plate impedance, Z_{pp}, due to the fundamental mode, has been analyzed in multiple studies [23], [24]. The fundamental parallel-plate mode is considered only for parallel-plate impedance calculation [25]-[28]. On the basis of the parallel-plate impedance, the inductance interaction of the via to the parallel plate can be extracted for power-ground plane design [29], [30]. Via modeling with the lossy material in real applications has been analyzed in papers [31], [32]. To extend the

physics-based via model for high-frequency applications, the higher-order modes of the parallel plate have been introduced in [23], [24], and [33]. However, the physics-based via models still cannot work in the high-frequency range above 20 GHz for arbitrary types of vias, because an accurate consideration of higher-order modes (non-propagating/evanescent modes) in the vicinity of the via becomes critical with increasing cavity height and frequency [35], [37]. Williamson [24] and Zhang [23] have proposed more complex equivalent circuits for via structures by considering higher-order modes in the vicinity of the via domain. However, extracting the circuit elements for the two models is complex, and the circuit models are not accurate beyond 40 GHz for typical PCB via dimensions [36]. Hybrid two-dimensional/three-dimensional (3D) finite-element methods have also been proposed to model vias with differently shaped anti-pads, to maintain accuracy while improving computational efficiency [38]-[40]. However, these approaches remain more time-consuming than equivalent circuit methods.

Herein, we propose mode-decomposition-based equivalent model for the via structure, which considers higher-order modes in the parallel-plate domain, on the basis of mode decomposition. The mode decomposition method used herein differs from the previous use of modal decomposition [11] to separately model the parallel-plate mode and the strip-line mode. Our decomposition method separates the higher-order modes from the fundamental mode of the parallel-plate modes. The equivalent model includes via-plate capacitance and parallel-plate impedance, owing to different parallel-plate modes, corresponding to different domains of the via structure. In contrast to the conventional physics-based via model, the higher-order modes in the parallel-plate domain are also modeled by using a higher-order mode impedance, Z', herein. All elements of the proposed

equivalent model can be calculated from the physical parameters of the via structure. The key contributions of this work can be summarized as follows:

1) A mode-decomposition-based equivalent model for high-speed via is proposed. The equivalent model for higher-order modes in the parallel-plate domain is analyzed, and the higher-order mode impedance is used to model the interaction between the via and plates, for the first time. The higher-order mode impedance is calculated with the mode decomposition method.

2) The field distribution and modes are analyzed. The physical meaning for all elements of the via equivalent model is analyzed and explained on the basis of the electric field distribution, thus greatly facilitating via design and optimization.

3) Full-wave simulations are presented to verify the proposed mode-decomposition-based equivalent model of a high-speed via up to 100 GHz.

The proposed equivalent model can predict S-parameters of via structures in the high-frequency range, and the results are compared with those of previous methods [20], [24], [36]. The remainder of this article is organized as follows. Section II details the proposed equivalent model and the formulas for via-plate capacitances and parallel-plate impedances. Fields and mode analysis are described in Section III to show the physical meaning of the equivalent model and why higher-order modes should be considered. Higher-order modes are shown to exist in the vicinity of the via between parallel plates and may be prominent at high frequencies. Section IV presents simulation examples verifying the accuracy and applicability of the proposed equivalent model, and conclusions are presented in Section V.

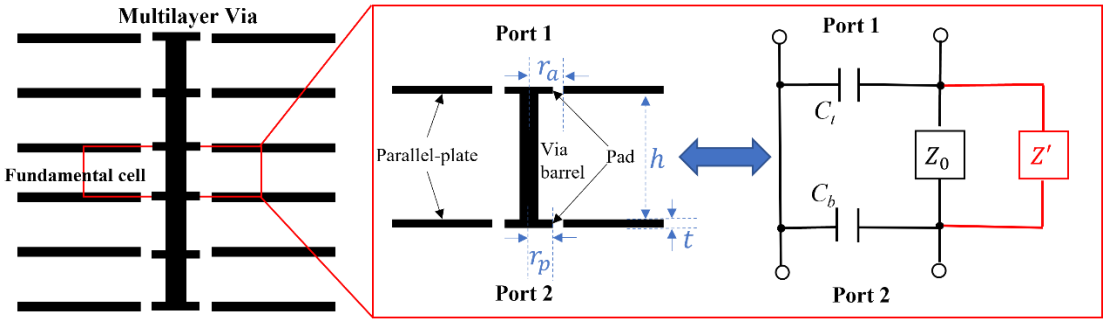


Figure 1. Proposed equivalent model of the via (fundamental cell).

2. PROPOSED MODELING METHOD

On the basis of the conventional physics-based method, a via can be modeled by using a π-type equivalent circuit with two capacitors and the parallel-plate impedance [20], [36]. Fig. 1 shows the proposed equivalent model for the fundamental cell of a via, which corresponds to via segments crossing a cavity enclosed by two reference plates. The equivalent model includes two capacitors and the parallel-plate impedance Z_{p0} and Z'. Z_{p0} and Z' arise from the fundamental mode and higher-order modes in the parallel-plate domain, respectively. Two capacitors represent the coupling between the via and the top or bottom plate. Unlike the conventional physics-based model, the proposed equivalent model considers the effects of higher-order modes, thereby allowing for more accurate modeling of the via at high frequencies.

2.1. VIA-PLATE CAPACITANCE

In Fig. 1, C_t and C_b are the via-top plate capacitance and via-bottom plate capacitance, respectively. The via-plate capacitance consists of the coaxial capacitance of

the anti-pad and the via barrel-plate capacitance, according to domain decomposition. Many methods have been developed for calculating the via-plate capacitance of a via structure [41]-[45]. Herein, the anti-pad capacitance and via barrel-plate capacitance are calculated as follows.

A transverse electromagnetic coaxial mode can be assumed in the anti-pad aperture [41]. The anti-pad capacitance can be calculated by

$$C_a = \frac{2\pi\varepsilon_0\varepsilon_r t}{ln(\frac{r_a}{r_p})} \tag{1}$$

where r_a and r_p are the anti-pad and pad radii, respectively; ε_0 and ε_r are the free space permittivity and relative permittivity, respectively; and t is the plate thickness.

The via barrel-plate capacitance can be calculated from the magnetic frill current [43] as

$$C'_b = \frac{j4\pi^2\varepsilon_0\varepsilon_r}{\left(ln\left(\frac{r_a}{r_p}\right)\right)^2 h}\sum_{n=1,3,5}^{\infty}\frac{\tilde{K}_n}{\tilde{k}_n} \tag{2}$$

where

$$\tilde{k}_n = -\frac{jn\pi}{h} \tag{3}$$

$$\tilde{K}_n = \frac{1}{\tilde{k}_n}\begin{pmatrix} \frac{2jln(r_a/r_p)}{\pi} - H_0^2(\tilde{k}_n r_a)J_0(\tilde{k}_n r_a) \\ -H_0^2(\tilde{k}_n r_p)J_0(\tilde{k}_n r_p) + 2H_0^2(\tilde{k}_n r_a)J_0(\tilde{k}_n r_p) \\ +\frac{J_0(\tilde{k}_n r_0)}{H_0^2(\tilde{k}_n r_0)}\left(H_0^2(\tilde{k}_n r_a) - H_0^2(\tilde{k}_n r_p)\right)^2 \end{pmatrix} \tag{4}$$

Here, h and r_0 are the dielectric height and via radius, respectively, and H_0^2 and J_0 are the zero-order Hankel function of the second kind and the zero-order Bessel function, respectively.

The via-top plate capacitance and via-bottom plate capacitance are represented as

$$C_t = C_b = C_a + C'_b \tag{5}$$

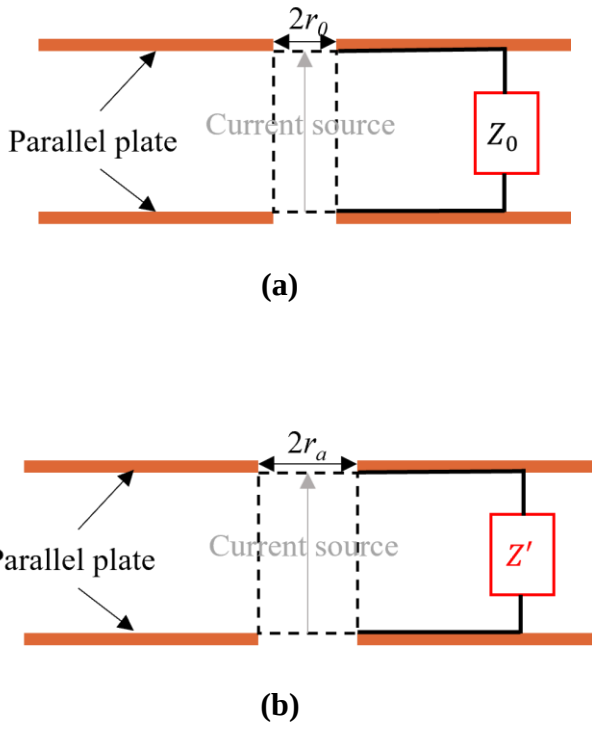


Figure 2. Equivalent mode of parallel plate impedance based on mode decomposition (r_0 and r_a are the via and anti-pad radii, respectively, and Z_0 and Z' are the parallel-plate impedance due to the fundamental mode and higher-order modes in the parallel-plate domain, respectively). (a) Equivalent model for the fundamental mode. (b) Equivalent model for higher-order modes.

2.2. PARALLEL-PLATE IMPEDANCE FOR FUNDAMENTAL MODE

In the conventional via modeling method, the parallel-plate impedance Z_{p0} represents coupling between the via and parallel-plate due to fundamental mode. As shown in Fig. 2 (a), the equivalent model for the fundamental mode consists of a current source

and a parallel plate. The radius of the current source is the same as the via radius; thus, the fundamental mode is excited at the via boundary. When the parallel plate is infinitely large, or the boundary condition of the plate consists of perfectly matched layers (PMLs), the parallel-plate impedance Z_{p0} can be calculated as [30]-[31]

$$Z_{p0} = \frac{V_0}{I_0} = \frac{-E_z^0 h}{2\pi r_0 H_\emptyset^0} \tag{6}$$

where V_0 and I_0 are the voltage and current at the via-barrel boundary due to the fundamental mode; h is the dielectric height in the parallel plate; and E_z^0 and $H_\emptyset^0$ represent the electric and magnetic fields at the via-barrel boundary due to the fundamental mode:

$$E_z^0(r_0) = k_0^2 a_0 H_0^2(k_0 r_0) \tag{7}$$

$$H_\emptyset^0(\mathrm{r}_0) = j\omega\varepsilon_0\varepsilon_r k_0 a_0 H_1^2(k_0 r_0) \tag{8}$$

Here, $k_0 = k' - jk''$, which is a complex wavenumber; $k' = \omega\sqrt{\mu_0\varepsilon_0\varepsilon_r}$; $k'' = \omega\sqrt{\mu_0\varepsilon_0\varepsilon_r}(tan\delta + \frac{d_s}{h})/2$; ω is the angular frequency; μ_0 is the permeability of free space; $tan\delta$ is the loss tangent of the material; $d_s = \sqrt{2/\omega\mu_0\sigma}$ is the skin depth of the conductor with conductivity of σ; a_0 is a constant coefficient that does not need to be determined; and H_1^2 is the first-order Hankel function of the second kind. The derivation of equation (7) and (8) is detailed in the appendix.

If the parallel plate is finite, or the boundary condition of the plate is a perfect electric or magnetic conductor (PEC or PMC) boundary, the parallel-plate impedance Z_{p0} can be calculated with the cavity method [34]. The closed-form expression for the parallel-plate impedance of a rectangular plate pair is given as

$$Z_{p0} = \frac{j\omega\mu_0 h}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{C_m^2 C_n^2 f_{bc} f_p}{k_{mn}^2 - k_0^2} \tag{9}$$

where a and b are the dimensions of the rectangular parallel plate; μ is the permeability of the dielectric material between the plates; $k_{mn} = \sqrt{(m\pi/a)^2 + (n\pi/b)^2}$; and m and n represent the mode number. In addition, C_m and C_n = 1 when m and n = 0; otherwise, C_m and $C_n = \sqrt{2}$. f_p and f_{bc} are terms correlated with the dimensions and shape of the via and the plate, respectively [33].

On the basis of the assumption that the via is circular, and the plate is rectangular, f_p and f_{bc} are expressed as follows:

$$f_p = J_0(k_{mn} r_0)^2 \tag{10}$$

$$f_{bc} = \begin{cases} cos^2\left(\frac{m\pi x}{a}\right) cos^2\left(\frac{n\pi y}{b}\right) & \text{PMC boundary} \\ sin^2\left(\frac{m\pi x}{a}\right) sin^2\left(\frac{n\pi y}{b}\right) & \text{PEC boundary} \end{cases} \tag{11}$$

where $x = a/2$, $y = b/2$, and f_{bc} differs when the boundary of the parallel plate is either a PMC or PEC boundary.

2.3. PARALLEL-PLATE IMPEDANCE FOR HIGH ORDER MODES

The parallel-plate impedance due to higher-order modes can be calculated with mode decomposition. When the waves enter the domain of the parallel plate, the higher-order modes can be excited at the anti-pad boundary, which is discontinuous. The equivalent model for higher-order modes is shown in Fig. 2 (b). The model contains an equivalent current source and a parallel plate, similarly to the equivalent model for the fundamental mode. The radius of this equivalent source is the same as the anti-pad radius; thus, the higher-order modes are excited at the anti-pad boundary. Similarly to the parallel-plate impedance of the fundamental mode, the higher-order mode impedance can

also be calculated by using the voltage and current at the anti-pad boundary due to the higher-order modes.

$$Z' = \frac{V_a}{I_a} \tag{12}$$

Here, V_a and I_a are the voltage and current at the anti-pad boundary due to the higher-order modes in the parallel-plate domain. These terms can be calculated according to the electric fields and magnetic fields at the anti-pad boundary. For the higher-order modes, only TM_{0n} modes are considered herein. Because the via structure considered is a circle, which is symmetric, and only TM_{0n} modes (higher-order modes/axially isotropic modes) are excited [7], [8]. The total electric and magnetic fields E_z^N and $H_\emptyset^N$ from TM_{0n} modes at the anti-pad boundary are expressed as

$$E_z^N(r_a, z) = \sum_{n=1}^{N} k_n^2 (a_0 H_0^2(k_n r_a)) cos\frac{n\pi z}{h} \tag{13}$$

$$H_\emptyset^N(r_a, z) = \sum_{n=1}^{N} j\omega\varepsilon_0\varepsilon_r k_n (a_0 H_1^2(k_n r_a))\ cos\frac{n\pi z}{h} \tag{14}$$

where $k_n = \sqrt{k_0^2 - (n\pi/h)^2}$; n represents the mode number; N is the total number of higher-order modes considered for the via modeling; and *z* is the coordinate in the vertical direction. The derivation of equations (13) and (14) is detailed in the appendix.

According to equations (13) and (14), electric fields and magnetic fields from higher-order modes vary along the z-axis. To accurately calculate the Z' at anti-pad boundary from higher-order modes, the discretization method is used herein. The current source is discretized into small parts, as shown in Fig. 3. For any small discretized current source, the corresponding impedance can be calculated as

$$\Delta Z' = \frac{\Delta V}{\Delta I} = \frac{\int_0^{\Delta z} E_z^N(r_a,z)dz}{\int_0^{2\pi} H_\emptyset^N(r_a,z)d\emptyset} = \frac{E_z^N(r_a,z)\times\Delta z}{2\pi r_a H_\emptyset^N(r_a,z)} \quad (15a)$$

When Δz is sufficiently small, e.g., Δz is less than 5% of the wavelength pertinent to the maximum frequency, the electric fields and the magnetic fields can be considered constant in the length of Δz. Thus, the integration equation (15a) can be rewritten as

$$\Delta Z' = \frac{E_z^N(r_a,z)\times\Delta z}{2\pi r_a H_\emptyset^N(r_a,z)} = \frac{\sum_{n=1}^N k_n^2(a_0 H_0^2(k_n r_a))\times\Delta z}{2\pi r_a \sum_{n=1}^N j\omega\varepsilon_0\varepsilon_r k_n(a_0 H_1^2(k_n r_a))} \quad (15b)$$

The variable of $cos\frac{n\pi z}{h}$ in the field expression of higher-order modes is eliminated in equation (15b). Then, for the total current source, the serialized impedance is calculated by integration as

$$Z' = \frac{h\sum_{n=1}^N k_n H_0^2(k_n r_a)}{j2\pi r_a\omega\varepsilon_0\varepsilon_r\sum_{n=1}^N H_1^2(k_n r_a)} \quad (16)$$

The fundamental cell of the via model, as illustrated in Fig. 1, is modeled by using the capacitance and parallel-plate impedance due to different parallel-plate modes, according to the domain decomposition method. From the mode decomposition method, the impedance due to different parallel-plate modes is modeled with different equivalent models. The proposed new mode-decomposition-based equivalent model is more accurate at high frequencies than the conventional physics-based circuit model, because it considers the effects of higher-order modes, which may be prominent in the high-frequency range.

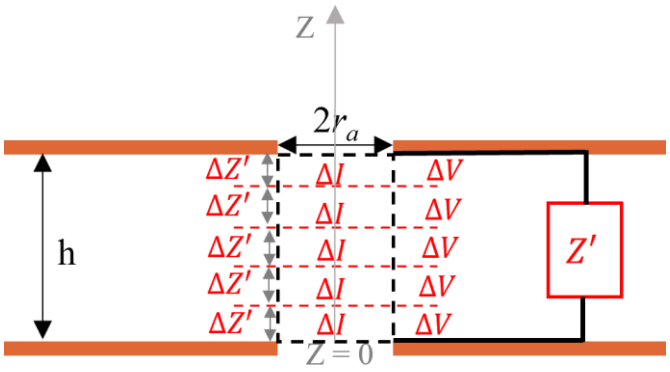


Figure 3. The current source of the equivalent model for high-order modes is discretized.

3. FIELD AND MODE ANALYSIS

An electric field distribution simulated by high-frequency simulation software (HFSS) at 100 GHz is shown in Fig. 4. As shown, a transverse electromagnetic mode arises in the anti-pad domains of the top and bottom parts, which can be represented by the via-to-plate capacitance C_a [41]. In the via-hole domain, the fields should be modeled by using the capacitance C'_b of the via barrel to the top and bottom plates [23], [41]. In the parallel-plate domain, the fundamental mode and higher-order modes of parallel-plate exist. The fundamental mode is a propagating mode, whereas the higher-order modes are evanescent modes that quickly vanish with propagating distance, thereby explaining why higher-order modes are observed only in the vicinity of the via domain. The parallel-plate impedance Z_0 represents the fundamental mode. Meanwhile, the parallel-plate impedance Z' is used to model higher-order modes. In Fig. 4, the fields are modeled with corresponding electrical elements. In the conventional physics-based equivalent model, only the

fundamental mode is considered for low-frequency modeling. However, higher-order modes may be dominant in the high-frequency range. Therefore, the proposed model is more accurate at high frequencies.

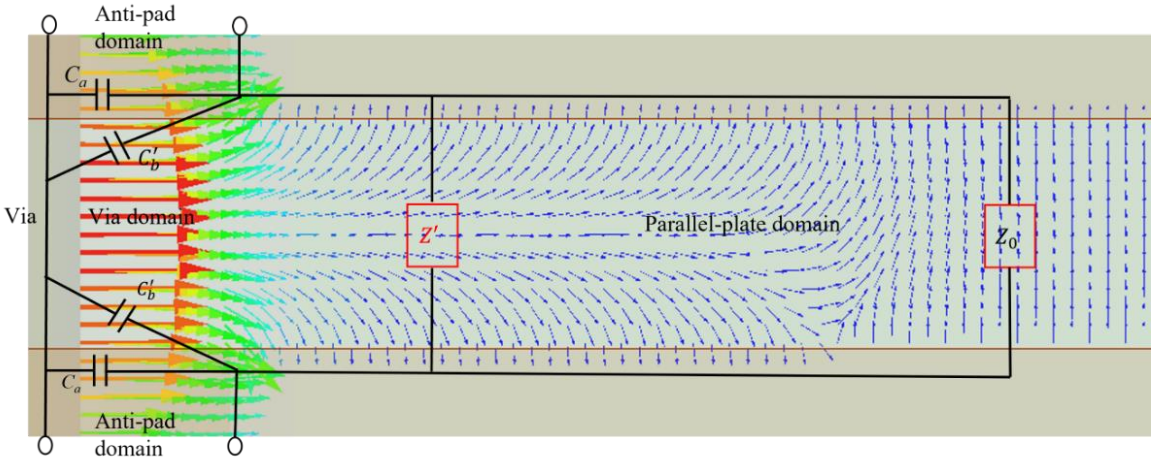


Figure 4. Simulated electric field distribution at 100 GHz in a via structure by HFSS and corresponding electrical elements, according to the domain decomposition method and mode decomposition method (r_0 = 4 mil, r_a = 15 mil, h = 15.3 mil, PML boundary for the parallel plate).

Fig. 5 shows the propagation constant in the ρ direction for some primary transverse magnetic (TM) modes. The cut-off frequency for higher-order modes (TM_{01}, TM_{02}, and TM_{03}) is very high. Even for the TM_{01} mode, the cut-off frequency is beyond 200 GHz. This result indicates that those higher-order modes are evanescent and cannot propagate in the ρ direction. This finding also explains why these modes are observed only in the vicinity of the via domain.

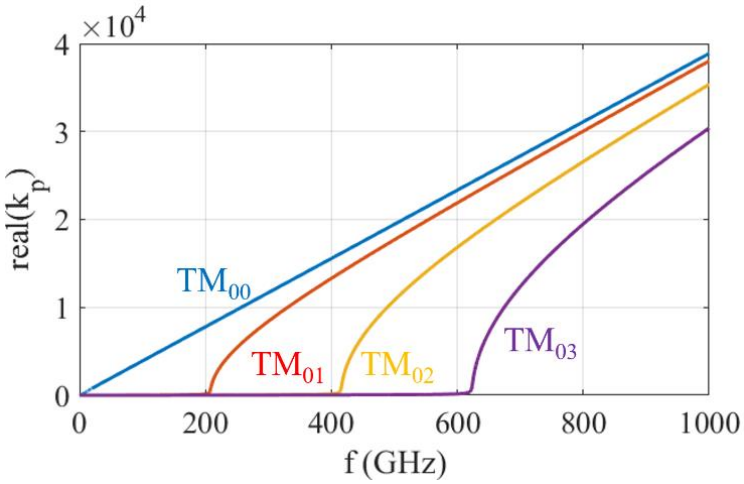


Figure 5. Cut-off frequencies of TM_{00}, TM_{01}, TM_{02}, and TM_{03} mode for a fundamental cell of a via with dielectric material of $\varepsilon_r = 3.68$, $tan\delta = 0.02$, r_0 = 4 mil, r_a = 15 mil, h = 15.3 mil, PML boundary for the parallel plate.

The admittance $Y = 1/Z$ from different parallel-plate modes for the via model of case 1 in the numerical examples section is compared in Fig. 6. The admittance Y is detailed in the appendix. The higher-order mode admittance is very small with respect to the fundamental mode admittance at frequencies below 20 GHz. However, the higher-order mode admittance can reach the same level as the fundamental mode admittance at high frequencies. This finding supports our analysis result showing that higher-order modes can be prominent in the high-frequency range. As shown in Fig. 6, the contribution to the parallel-plate admittance from the higher-order modes decreases as the mode order increases, in agreement with the properties of higher-order modes. Thus, equations (15) and (16) can converge very rapidly. For the via model considered in this work, the impedance due to the TM_{01} mode is dominant, and a parallel-plate mode coefficient N of 3 is chosen, which is sufficient.

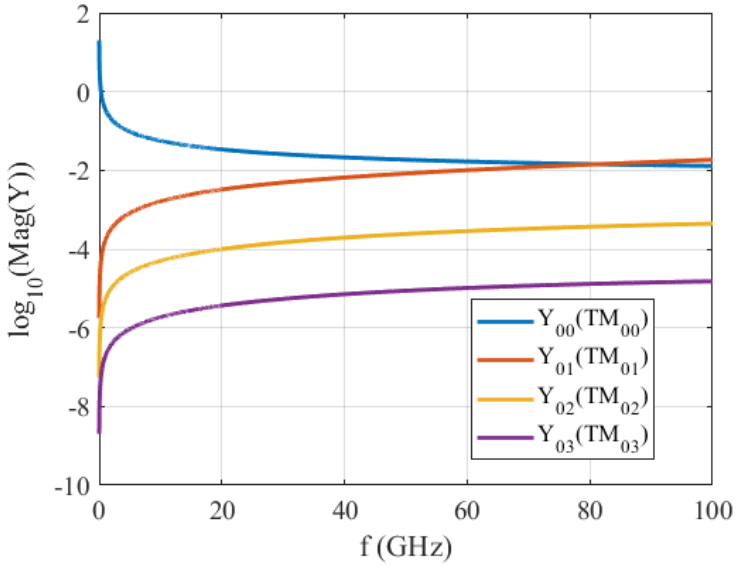
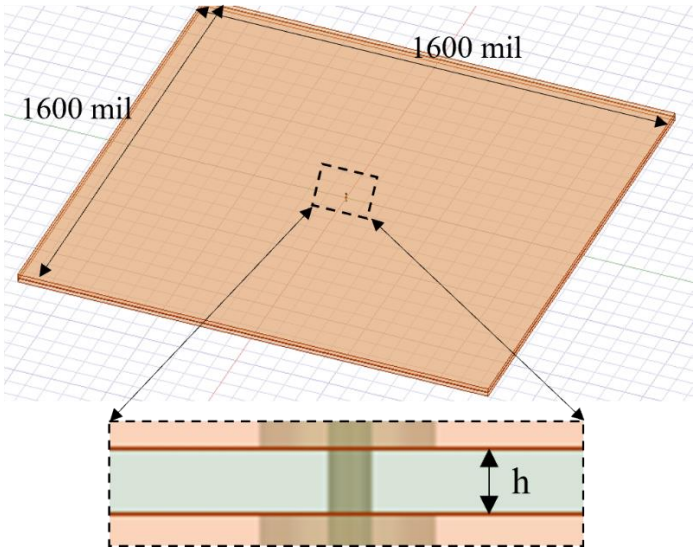


Figure 6. Comparison of admittance from different parallel-plate modes for the via model of case 1 ($Y_0 = 1/Z_0$ and $Y' = 1/Z'$): magnitude of Y_0 and Y' for different parallel-plate modes (r_0 = 4 mil, r_a = 15 mil, h = 15.3 mil, $\varepsilon_r = 3.68$, $tan\delta = 0.02$, PML boundary for the parallel plate).

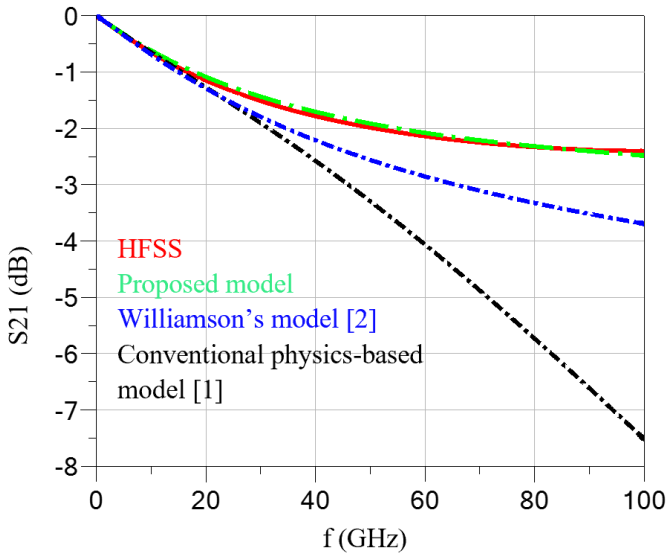
4. NUMERICAL EXAMPLES

In this section, the proposed equivalent model of a via is verified with numerical simulations. A simple case for a via with two plates is first examined. Subsequently, models with different anti-pad radii are shown to present the applicable range of the proposed model. Finally, a model with multiple plates is shown to present the efficiency of the proposed model. Comparisons of S-parameter results from different methods and simulations for different models indicate the accuracy of the proposed method, particularly at frequencies above 40 GHz.

Case 1 is a fundamental case consisting of a via with two layers. This model represents a fundamental cell for a via model with multiple plates. The insertion loss of the via for different boundary conditions is compared in Fig. 7. Fig. 7 (a) shows the cross-section of the via model for a rectangular plate with dimensions of 1600 mil by 1600 mil. The via radius r_0 is 4 mil, the anti-pad radius r_a is 15 mil, the plate thickness t is 1.3 mil, and the parallel-plate cavity height h is 15.3 mil. The relative permittivity ε_r and the loss tangent of material are 3.68 and 0.02 at 1 GHz with Djordjevic model. The conductivity of the copper plate is 5.8×10^7. Fig. 6 (b), (c), and (d) show insertion loss comparisons for a via with PML, PEC, and PMC boundaries, respectively, according to different methods and HFSS. A large difference is observed between the conventional physics-based model [20] and HFSS for all boundary cases at frequencies above 20 GHz. Williamson's model [24], as compared with the conventional physics-based model, improves the results but still cannot work in a high frequency range above 40 GHz. However, the results from the proposed model match the simulation results very well throughout the entire frequency range as high as 100 GHz for all three boundary cases. For the PEC and PMC boundary cases, the resonance of insertion loss due to a finite plate size is also accurately predicted throughout the entire frequency range.

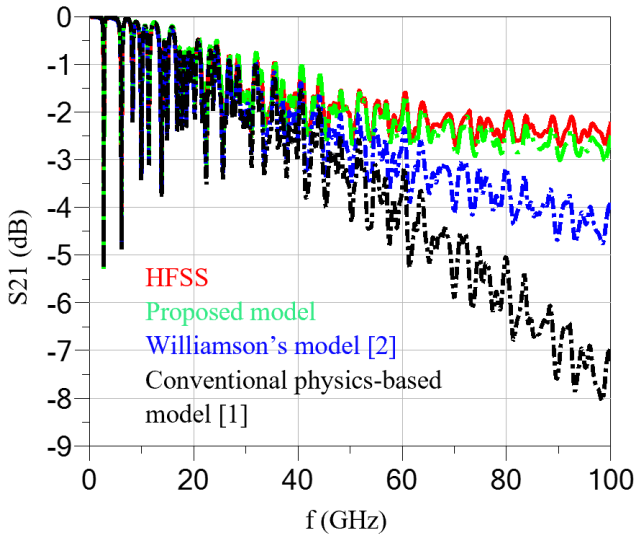


(a)

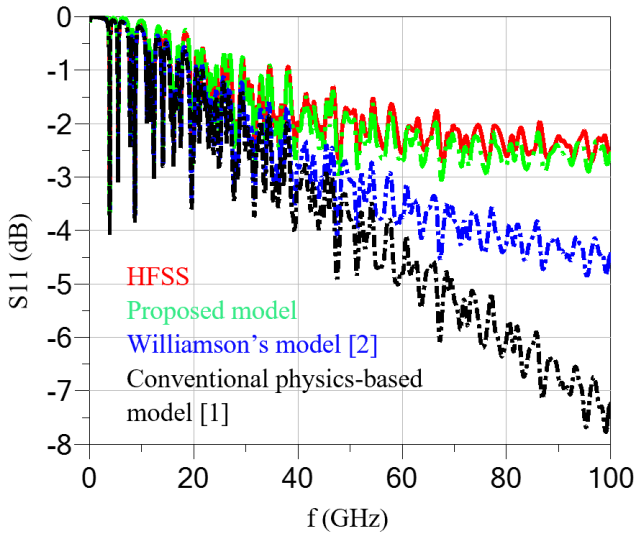


(b)

Figure 7. Case 1: via model with two plates. (a) Cross-sectional view of the via model. (b) Insertion loss comparison for a PML boundary.

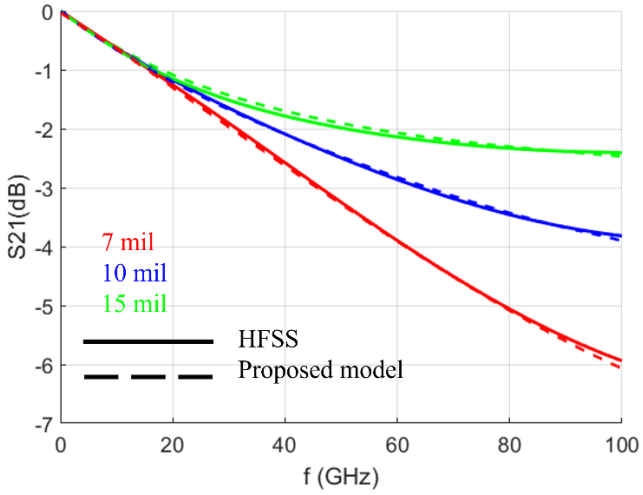


(c)

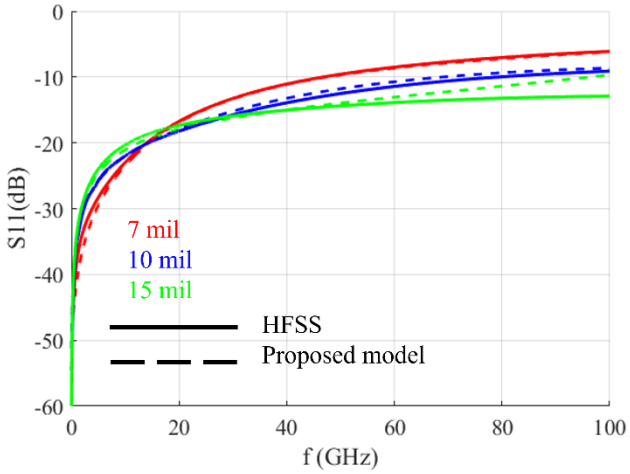


(d)

Figure 7. Case 1: via model with two plates. (c) Insertion loss comparison for a PEC boundary. (d) Insertion loss comparison for a PMC boundary. (cont.)



(a)

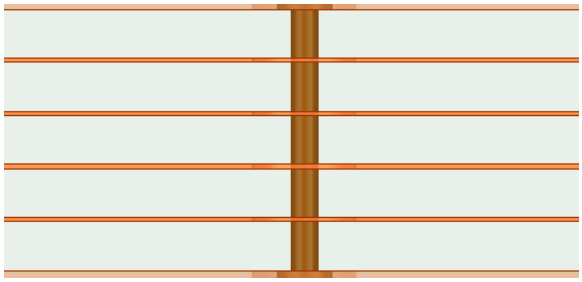


(b)

Figure 8. Case 2: S-parameter comparison for different anti-pad radii (PML boundary). (a) Insertion loss comparison. (b) Return loss comparison.

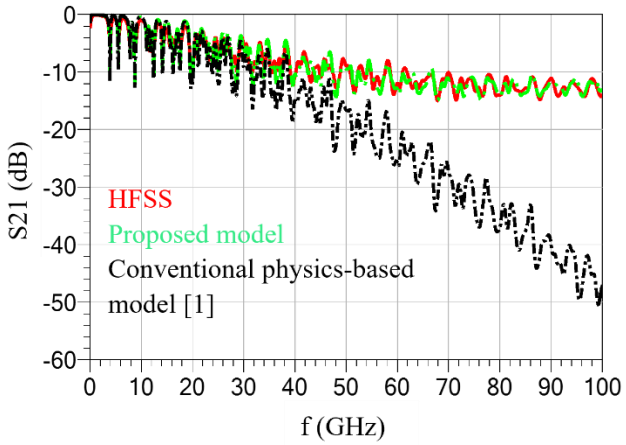
To further verify the applicable range of the proposed equivalent model, the anti-pad radius was swept from 7 mil to 15 mil in case 2, which is based on the model in case

1. Fig. 8 (a) shows insertion loss comparisons for HFSS and the proposed circuit model for different anti-pad radii. An excellent correlation is shown for all cases. For the return loss comparison shown in Fig. 8 (b), the results of the proposed circuit match well with the simulation results when the anti-pad radius is 7 mil or 10 mil. However, when the anti-pad radius increases to 15 mil, the return loss does not match well at frequencies above 70 GHz. However, the results from the proposed model remain better than the results from a conventional physics-based model. When the anti-pad radius is very large, mode conversion at the anti-pad boundary is more complex, and via self-inductance should be considered. We will focus on this situation in a future publication.

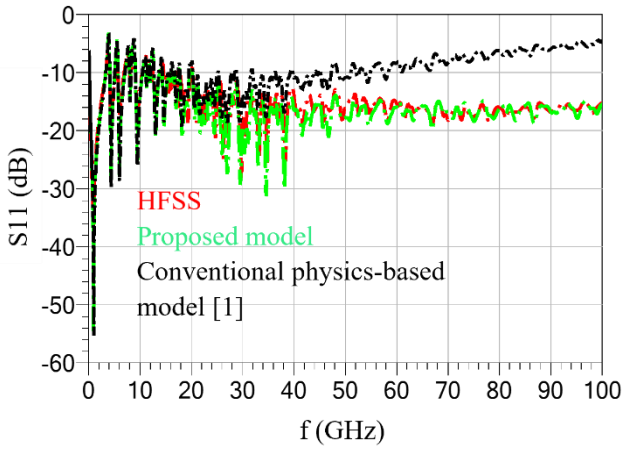


(a)

Figure 9. Case 3: via model with six layers (PMC boundary). (a) Cross-sectional view of the via model.

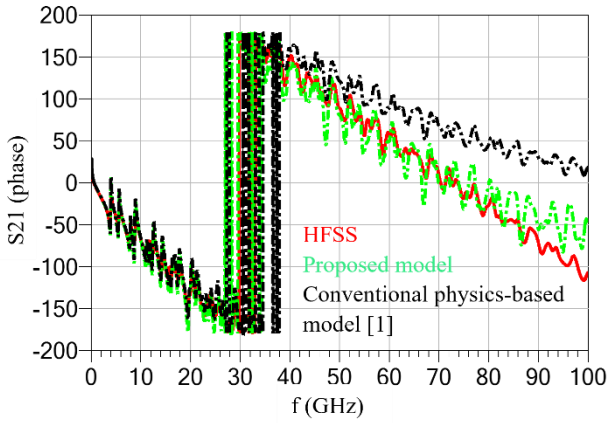


(b)

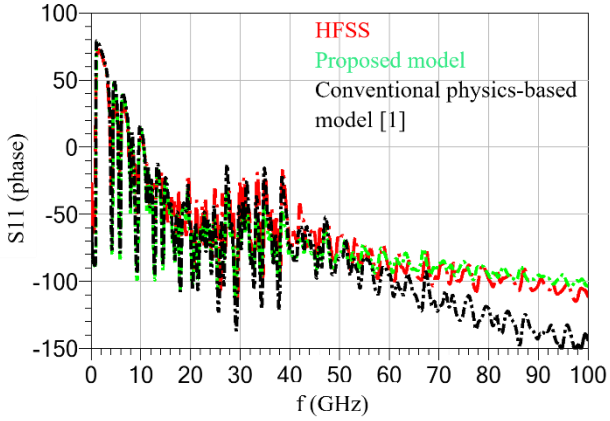


(c)

Figure 9. Case 3: via model with six layers (PMC boundary). (b) Comparison of insertion loss. (c) Comparison of return loss. (cont.)



(d)



(e)

Figure 9. Case 3: via model with six layers (PMC boundary). (d) Phase comparison of insertion loss. (e) Phase comparison of return loss. (cont.)

Case 3 is a via model with six layers. The geometry and dimensions of the via and plate in this model are the same as those in case 1. Thus, case 3 is a layered extension of case 1. On Layer 1 and 6, there are pads of radius with radius of 8 mil. The insertion loss and return loss of the via for the PMC boundary condition are compared in Fig. 9. A cross-

sectional view of the via with six layers is shown in Fig. 9 (a). Fig. 9 (b) and (c) compare the insertion loss and return loss, respectively. The conventional physics-based circuit method is accurate only up to 30 GHz, but the results from the proposed model match the full-wave simulation results throughout the entire frequency range, up to 100 GHz. The computational memory and time cost of case 3 are compared between the proposed model and the HFSS, run on a server with 3.45 GHz CPU speed and 512 GB memory. HFSS simulated the model of case 3 with 29.5 GB memory in 11.5 hours, whereas the proposed method required only 256 MB memory and 10.5 seconds. It validates that the proposed method is more efficient than full wave simulation.

5. CONCLUSION

A mode-decomposition-based equivalent model of a high-speed via is first proposed for the first time in this paper and is shown to provide accurate results up to 100 GHz. In our model, in contrast to the conventional physics-based via model [20], higher-order modes in the parallel-plate domain improve the accuracy of the model of the via at high frequencies. On the basis of the domain decomposition method, the via structure can be divided into an anti-pad domain, via domain, and parallel-plate domain. We use different equivalent electrical elements to model each domain. The capacitance values between the via and plates represent the fields in the anti-pad and via domain. A fundamental mode (propagating mode TM_{00}) and higher-order modes (evanescent modes TM_{0n}) are considered in the parallel-plate domain. The parallel-plate impedance Z and Z' for different parallel-plate modes is used to model the interactions between the via and

plates, which are calculated with the mode decomposition method. From the field distribution and mode analysis, we find that the higher-order modes in the parallel-plate domain can be dominant at high frequencies. This finding explains why the proposed equivalent model is more accurate than the conventional physics-based model, and also provides a physical meaning that should be useful in via design and optimization.

Numerical examples were used to verify the proposed model. Only cases of a single-via model were analyzed and verified to avoid the effects of other vias and traces. Full-wave simulation (HFSS) results validated the superior accuracy and applicability of the proposed equivalent model to those of the conventional physics-based model and Williamson's model, particularly at high frequencies. Meanwhile, the electrical elements in the proposed circuit can be easily extracted on the basis of the physical parameters of the via, in contrast to the equivalent circuits proposed by Williamson [24] and Zhang [23]. The applicable range of the proposed method was determined by sweeping of the anti-pad size. The insertion loss can be accurately predicted when the ratio of the anti-pad radius to the via radius is between 1.75 and 3.75. When the anti-pad radius is significantly larger than the via radius, the insertion loss can still be predicted accurately by the proposed model, whereas the return loss has a poor correlation above 70 GHz between the proposed model and HFSS simulation. In addition, the proposed method has better performance than the conventional physics-based method. We will investigate this situation in a future publication.

On the basis of the analysis herein, the proposed analytical model is useful up to 100 GHz, particularly for cases with a longer via length and smaller anti-pad radius to the via barrel radius ratio. The proposed parallel-plate impedance could also be applied to

model an arbitrary number of vias when the distance between vias is sufficiently large, such that the evanescent parallel-plate modes from one via do not affect neighboring vias. A mode-decomposition-based equivalent model for multiple vias that considers higher-order modes will be introduced in a future publication.

APPENDIX

The formulas below show general expressions of electric and magnetic fields in cylindrical coordinates for a radial parallel-plate waveguide. The details of their derivation have been described in the book [46].

For the TE_{mn}^{z} modes,

$$H_\rho = -jk_z k_\rho (a_0 H_m^{2\prime}(k_\rho\rho) + a_1 H_m^{1\prime}(k_\rho\rho))\, cos(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A1)}$$

$$H_\emptyset = jk_z \frac{m}{\rho}(a_0 H_m^2(k_\rho\rho) + a_1 H_m^1(k_\rho\rho))\, sin(m\emptyset)\, cos\frac{n\pi z}{h} \quad \text{(A2)}$$

$$H_z = -jk_\rho^2 (a_0 H_m^2(k_\rho\rho) - a_1 H_m^1(k_\rho\rho))\, cos(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A3)}$$

$$E_\rho = \omega\mu_0 \frac{m}{\rho}(a_0 H_m^2(k_\rho\rho) - a_1 H_m^1(k_\rho\rho))\, sin(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A4)}$$

$$E_\emptyset = \omega\mu_0 k_\rho (a_0 H_m^{2\prime}(k_\rho\rho) - a_1 H_m^{1\prime}(k_\rho\rho))\ cos(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A5)}$$

$$E_z = 0 \quad \text{(A6)}$$

For the TM_{mn}^{z} modes,

$$E_\rho = -k_z k_\rho (a_0 H_m^{2\prime}(k_\rho\rho) + a_1 H_m^{1\prime}(k_\rho\rho))\ cos(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A7)}$$

$$E_\emptyset = k_z \frac{m}{\rho}(a_0 H_m^2(k_\rho\rho) + a_1 H_m^1(k_\rho\rho))\, sin(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A8)}$$

$$E_z = k_\rho^2 (a_0 H_m^2(k_\rho\rho) + a_1 H_m^1(k_\rho\rho))\, cos(m\emptyset)\, cos\frac{n\pi z}{h} \quad \text{(A9)}$$

$$H_\rho = -j\omega\varepsilon_0\varepsilon_r \frac{m}{\rho}\left(a_0 H_m^2(k_\rho\rho) + a_1 H_m^1(k_\rho\rho)\right) sin(m\emptyset)\, cos\frac{n\pi z}{h} \quad \text{(A10)}$$

$$H_\emptyset = -j\omega\varepsilon_0\varepsilon_r k_\rho\left(a_0 H_m^{2\prime}(k_\rho\rho) + a_1 H_m^{1\prime}(k_\rho\rho)\right) cos(m\emptyset)\, cos\frac{n\pi z}{h} \quad \text{(A11)}$$

$$H_z = 0 \quad \text{(A12)}$$

where $k_\rho = \sqrt{k_0^2 - (n\pi/h)^2}$ is the wavenumber in the ρ-direction; $k_z = n\pi/h$ is the wavenumber in the z-direction; a_0 and a_1 are constant coefficients; the Hankel functions of the first kind H_m^1 represent radial waves propagating in the negative ρ-direction; and the Hankel functions of the second kind H_m^2 describe radial waves propagating in the positive ρ-direction.

On the basis of the assumption that the parallel plate is infinite, only radial waves propagate in the positive ρ-direction. Thus, the Hankel functions of the first kind H_m^1 should be eliminated, and consequently, $a_1 = 0$. For TM_{0n}^z modes, the expression of electric and magnetic fields can be simplified from equations (23)-(28) as

$$E_\rho = k_z k_\rho\left(a_0 H_0^2(k_\rho\rho)\right) cos(m\emptyset)\, sin\frac{n\pi z}{h} \quad \text{(A13)}$$

$$E_\emptyset = 0 \quad \text{(A14)}$$

$$E_z = k_\rho^2\left(a_0 H_0^2(k_\rho\rho)\right) cos\frac{n\pi z}{h} \quad \text{(A15)}$$

$$H_\rho = 0 \quad \text{(A16)}$$

$$H_\emptyset = j\omega\varepsilon_0\varepsilon_r k_\rho\left(a_0 H_1^2(k_\rho\rho)\right) cos\frac{n\pi z}{h} \quad \text{(A17)}$$

$$H_z = 0 \quad \text{(A18)}$$

For the case of a finite parallel plate, the waves of higher-order modes still propagate only in the positive ρ-direction. Because the higher-order modes are evanescent, they cannot reach the edge of the parallel plate to produce waves in the negative ρ-direction.

The equations of admittance for higher-order modes (TM_{01}, TM_{02}, and TM_{03}) are as follows:

$$Y' = \sum_{p=1}^{\infty} Y'_{0p} = \frac{1}{Z'} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \sum_{p=1}^{\infty}\left(H_1^2(k_p r_a)\right)}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))} \quad \text{(A19)}$$

$$Y'_{01} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \left(H_1^2(k_1 r_a)\right)}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))}, \qquad \text{for } TM_{01} \text{ mode} \quad \text{(A20)}$$

$$Y'_{02} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \left(H_1^2(k_2 r_a)\right)}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))}, \qquad \text{for } TM_{02} \text{ mode} \quad \text{(A21)}$$

$$Y'_{03} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \left(H_1^2(k_3 r_a)\right)}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))}, \qquad \text{for } TM_{03} \text{ mode} \quad \text{(A22)}$$

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III. PEEC-BASED ON-CHIP PDN IMPEDANCE MODELING USING LAYERED GREEN'S FUNCTION

ABSTRACT

This paper presents an impedance model of on-chip power distribution network (PDN), which is an efficient criterion for estimating simultaneous switching noises (SSNs) on 3-D integrated circuit (IC). The impedance of on-chip PDN, including the effect of silicon substrate, is accurately modeled based on partial element equivalent circuit (PEEC) and layered Green's function (LGF). The equivalent circuit model of PDN is extracted based on the physical dimensions and electrical material characteristic of PDN at first. And then the LGF is used to consider the effect of silicon substrate for improving the accuracy of on-chip PDN impedance model. The effectiveness of proposed model has been validated by full wave simulation. The high order resonance of PDN impedance can also be accurately predicted.

Keywords: Impedance modeling, PDN, PEEC, LGF, SSNs, Silicon substrate.

1. INTRODUCTION

Simultaneous switching noises (SSNs) on 3-D stacked memory Integrated Circuit (IC) in gigahertz range is becoming more and more serious challenge with the increase of bandwidth and power consumption, which obviously degrade the performance and reliability of the IC [1]-[2]. To estimate the SSNs generation and evaluate the Power Distribution Network (PDN) design for 3-D IC, calculation of PDN impedance is found to

be an efficient criterion because a high impedance level across a high bandwidth might generate a large amount of SSNs. In other words, it is really useful to accurately model the impedance of on-chip PDN for estimation of SSNs [3]-[6]. Because the dimension range of on-chip PDN is wide and the geometry and material are complex, it is difficult to obtain the impedance of on-chip PDN with separated power and ground current paths by full-wave simulation as mentioned in [6].

In recent years, many methods have been proposed to model the impedance of on-chip PDN based on partial element equivalent circuit (PEEC) method. In [3], an impedance modeling method of PDN based on resonant cavity model was proposed. But the method can only be applied to low frequency range that below gigahertz. A segmentation-based method of modeling on-chip PDN impedance was proposed in [4]-[6]. But they don't consider the effect of lossy silicon substrate which would introduce some deviations on modeling. The effect of silicon substrate was modeled as series capacitors between the substrate and power/ground (P/G) line in [7]-[12]. However, these methods still cannot predict the impedance of on-chip PDN accurately, especially near the resonance frequency.

In our proposed method, the impedance model of on-chip PDN is established based on PEEC method and layered Green's function (LGF). Firstly, the unit cell of PDN is extracted based on a segmentation method. Then the equivalent circuit of unit cell is modeled by PEEC method. The equivalent circuit of whole PDN is presented by connecting the equivalents circuits of all unit cells. Because the lossy silicon substrate right below on-chip PDN could affect the capacitive couplings between metal lines of on-chip PDN, the LGF was introduced to achieve the right capacitance between metal lines. By means of considering the effect of lossy silicon substrate, the accuracy of impedance

modeling of on-chip PDN is improved. Compared with the existing method, which added additional capacitors into equivalent circuit of PDN mentioned above, the proposed equivalent circuit would be more efficient. Because the capacitive coupling between P/G line is calculated by LGF including the effect of silicon substrate. Ultimately, some simulation results from HFSS are used to validate the effectiveness of the proposed method.

2. METHODOLOGY

The on-chip PDN is constructed by mesh-typed P/G PDN, insulator of silicon dioxide and silicon substrate, as shown in Fig. 1. In reality, the PDN is in silicon dioxide area above silicon substrate. The mesh typed PDN with silicon oxide medium can be modeled as equivalent *RLC* circuit based on PEEC method. The *RLC* parameters are extracted based on the physical dimensions and electrical material characteristic of PDN and silicon oxide medium.

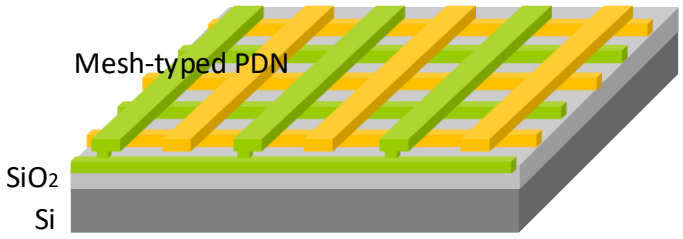

Figure 1. On-chip PDN structure.

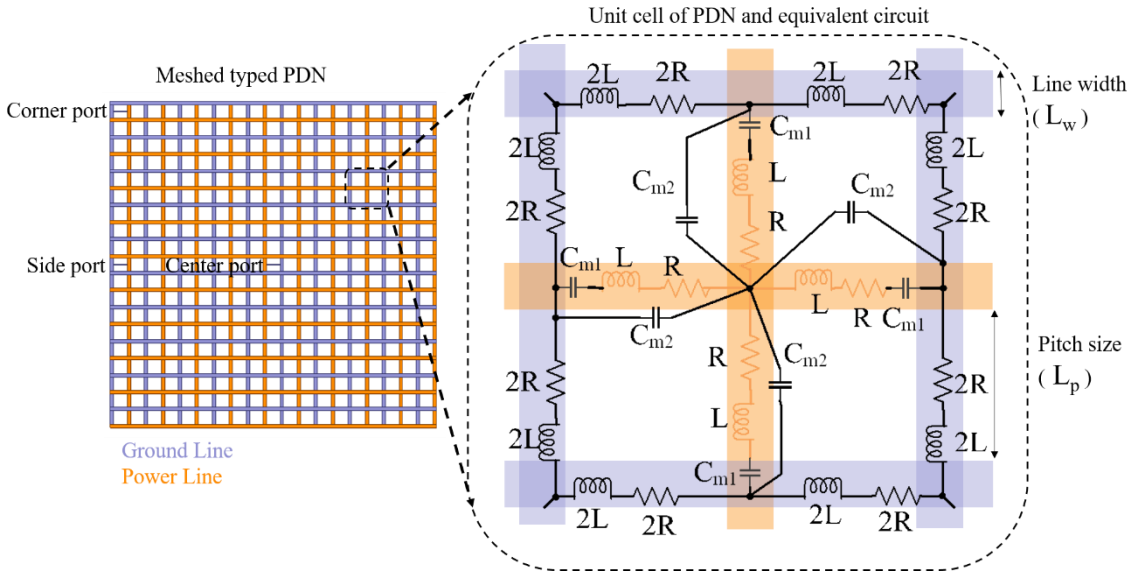

Figure 2. Top view of mesh-typed P/G PDN and the equivalent circuit of PDN unit cell.

On-chip PDN environment can be treated as multilayer structure. Then the LGF is used to take account into the effect of silicon substrate to guarantee an accurate impedance model of on-chip PDN.

2.1. PROPOSED PDN IMPEDANCE MODEL

The mesh-typed PDN can be separated into small unit cells as shown in right-top of Fig. 2. One unit cell can be represented as equivalent *RLC* circuit as shown in the right-bottom of Fig. 2. *R* and *L* are the partial resistances including the skin effect and the partial self-inductances of the P/G lines of PDN, respectively. To accurately model the PDN impedance, the mutual-inductance L_m between parallel P/G lines of PDN on same layer are considered. C_{m1} is the partial mutual capacitances between cross P/G lines on different layers while C_{m2} is the partial mutual capacitances between parallel P/G lines on same layer of PDN as shown in Fig. 2.

Resistance calculation here is defined as

$$R = \frac{L_p}{L_w \cdot t \cdot \sigma} \sqrt{1 + \alpha \cdot f} \tag{1}$$

where σ is the conductivity of P/G metal line. L_p is the pitch between power and ground line. L_w and t is the width and thickness of the P/G lines. α is the correction factors for skin effect, which is related to the thickness and conductivity of metal lines [9], [11]. For on-chip PDN where the P/G metal lines are very close to each other that means the current pass through in one metal line could be affected by the current in near metal line. Therefore, the skin effect in on-chip PDN is really important. f represents the frequency and indicates a high frequency portion for resistance.

The formulation for partial inductance calculation [13] here is

$$L = \frac{1}{t^2 \cdot L_w^{\,2}} \int_{V_i} \int_{V_j} G_A dV_i dV_j \tag{2}$$

where G_A is the corresponding vector potential Green's function for inductance calculation which relates to permeability of silicon oxide medium. $V_{i/j}$ is the volume of the mental line. When $i = j$, it represents the self-inductance L. When $i \neq j$, it is the mutual-inductance L_m.

The partial mutual capacitance between power line and ground line is calculated from sub-coefficients of capacitance c_s [14]. And c_s is calculated as $c_s = ps^{-1}$. Here ps is the coefficient of potential matrix and is defined as

$$ps = \frac{1}{S_p \cdot S_g} \int_{S_p} \int_{S_g} G_\phi dS_p dS_g \tag{3}$$

Here, G_ϕ is the corresponding scalar potential Green's function for capacitance calculation which relates to the permittivity of silicon oxide medium. In on-chip PDN impedance

modeling, G_ϕ should include the effect of silicon oxide medium where the PDN located in. S_p and S_g are the surface area of power line and ground line, respectively.

2.2. CONSIDERING EFFECT OF SILICON SUBSTRATE USING LGF

Because on-chip PDN structure can be treated as multilayer medium, LGF is used here to consider the effect of silicon substrate. From the LGF analysis of layered medium in [15]-[16] for 3-D IC/packaging systems, the vector potential G_A is dominated by the direct coupling, but the scalar potential G_ϕ is dominated by direct coupling and complex images due to the lossy silicon substrate. The complex image term of Green's function can be extracted by the discrete complex image method [14] as

$$G_{ci} = \sum_N \frac{1}{4\pi} a_i \frac{e^{-jkr_i}}{r_i} \tag{4}$$

where k is the wavenumber of the layer of metal line, N represents the number of complex images, a_i is the complex image coefficients and r_i relates to the complex image locations. Thus equation (3) is changed to (5).

$$ps = \frac{1}{S_p \cdot S_g} \int_{S_p} \int_{S_g} G_\phi + G_{ci} dS_p dS_g \tag{5}$$

The effect of silicon substrate is included in the capacitance of equivalent circuit of PDN. Because it doesn't add additional circuit component of capacitance, the equivalent circuit of PDN is simplified.

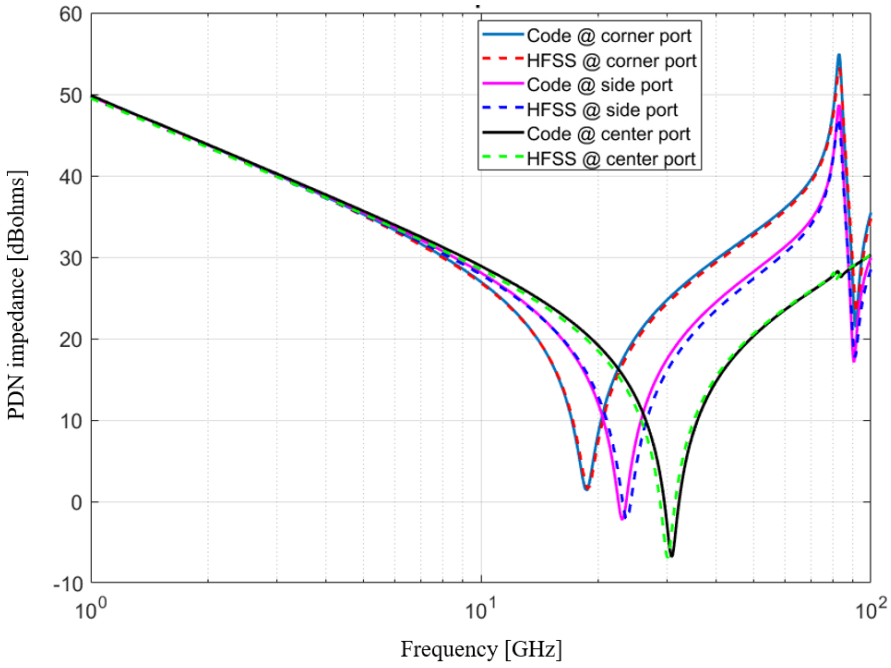

Figure 3. PDN impedance comparison from our code and HFSS for three port positions.

3. VERIFICATION

First, the impedance modeling of PDN in free space is validated. A mesh-typed P/G PDN as shown in Fig. 2 is modeled in HFSS-a commercial 3D full wave simulator. The width L_w of P/G line is 5um, the pitch L_p between power and ground line is 35um. The thickness t of P/G line is 1um. The length and the width of PDN are fixed as 985 um. The conductivity of metal line of PDN is 5.8×10^7 S/m. In the analysis of this PDN, the correction factors of α for skin effect is set as 0.54×10^8. Three ports are defined to check the input impedance of PDN, which is located at the corner, side and center of PDN respectively as shown in Fig. 2. Fig. 3 plots the input impedance curves from the code based on our method and HFSS simulation for three port positions within frequency range from 1 GHz to 100 GHz. The input impedances of PDN at three different positions from

our code are all correspond to simulation results. Even at resonance frequency points, the impedance of PDN can be predicted accurately. Obviously, it means the equivalent circuit of PDN is effective and accurate.

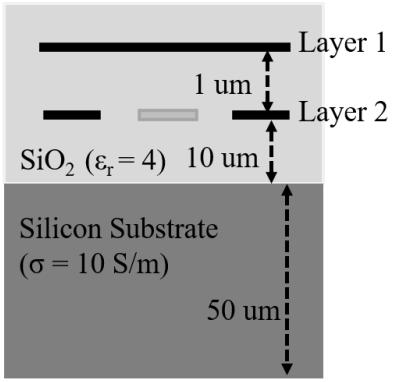

Figure 4. Cross section view of on-chip PDN.

Second, an on-chip PDN with lossy silicon substrate is modeled to validate the proposed model. Fig. 4 shows the cross-section view of the on-chip PDN. The geometrical parameters and conductivity of PDN are the same as the first example. The height of silicon substrate is assumed as 50 um. The distance between PDN and silicon substrate is 10 um. The relative permittivity of silicon oxide and the conductivity of silicon substrate are shown in Fig. 4. Three ports as described in previous example have also been analyzed, and the corner port is chosen as the representative case to check the impedance. The impedance curves of this on-chip PDN from the proposed model and HFSS are presented in Fig. 5. A good match can be observed in the whole frequency range from 1 GHz to 100 GHz. The differences between simulation and the proposed method are plotted in Fig. 6. We can

observe that the difference could be limited below 12% at high order resonance frequency points. The accurate of the proposed model is verified for a wideband frequency, up to 100 GHz.

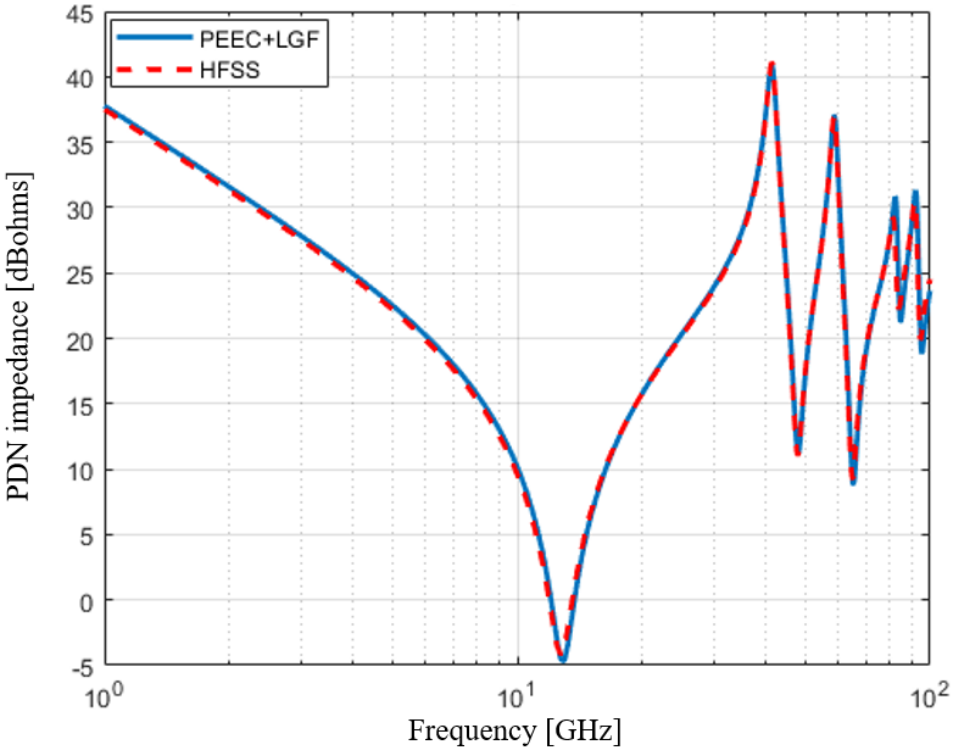

Figure 5. On-chip PDN impedance comparison from the proposed method and HFSS for corner port.

The simulation was conducted in a server with 3.45 GHz CPU speed and 512 GB memory. The cost of computational resources for simulation and the proposed method are compared in table I. It shows that the proposed method is more efficiency than full wave simulation.

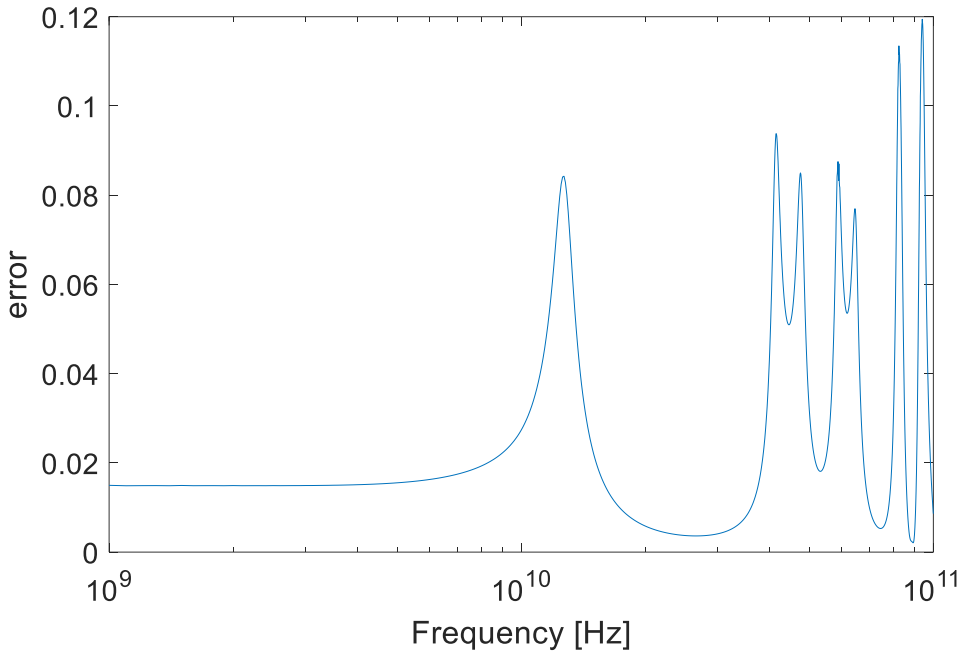

Figure 6. Difference between HFSS simulation and the proposed method (PEEC+LGF).

Table 1. Comparison of Computational Resources Cost.

Method	Memory Cost (GB)	CPU Time (hours)
Simulation	74	1.3
Proposed method	1.4	0.05

4. CONCLUSION

An on-chip PDN impedance modeling method based on PEEC and LGF is presented in the paper. The equivalent *RLC* circuit of unit cell of PDN is proposed at first. The *RLC* parameters are extracted with the known physical parameters of PDN based on

PEEC method. And then, the equivalent circuit of PDN can be modeled by connecting the equivalent circuits of all unit cells. Then LGF is applied to include the effect of lossy silicon substrate into the capacitance for the first time, which not only enhance the accuracy of the proposed impedance model but also simplify the impedance model compared with existing methods. A mesh-typed P/G PDN in free space is modeled firstly to validate the effectiveness of PEEC-based equivalent circuit of PDN. Then an on-chip PDN with silicon substrate is presented to verify the proposed method of modeling on-chip PDN impedance. The impedance of on-chip PDN from the proposed method matches with full wave simulation results at all resonance frequency points from 1 GHz to 100 GHz with tolerable errors. The efficiency of the proposed method is verified by comparison the computational resources cost in Table I. The proposed method could also be used to model the impedance of other complex 3-D package for performance analysis. In the future, some measurements will be conducted to validate the proposed method.

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SECTION

2. SUMMARY AND CONCLUSION

This thesis developed the dielectric liquid permittivity measurement method, equivalent circuit models for high-speed interconnect and on-chip PDN, which can help evaluate and optimize the signal integrity and power integrity of the high-speed digital system accurately and efficiently.

In the first paper, the proposed cylindrical cavity resonator-based method was verified by simulations and measurements of mineral oil. The measurement uncertainty was evaluated based on six different measurements, which can less than 1% for Dk extraction and less than 12% for Df extraction. Some cooling liquid from vendors were measured to verify the effectiveness of the proposed method. From measurements, the proposed method can measure the low permittivity dielectric liquid accurately and effectively.

In the second paper, the proposed high-speed via model was verified based on full-wave simulation for different cases. Compared with other methods, the proposed model can predict the s-parameter of the via accurately up to 100 GHz. The application range of the proposed model was evaluated based on full-wave simulations [80]. The proposed equivalent via model can also be used for multiple via modeling [81].

In the third paper, the proposed on-chip PDN impedance model was verified based on full-wave simulations for various cases with different port location. The effectiveness of the proposed model was evaluated by the comparison of the computational time cost

and the memory cost. It showed that the proposed equivalent circuit model can save a lot of computational resources than the full-wave simulation. The proposed equivalent circuit model of on-chip PDN can also be used to optimize the PDN impedance with de-capacitors.

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