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FAR-END CROSSTALK MODELING AND PREDICTION FOR HIGH-SPEED PCB DESIGN WITH INHOMOGENEOUS DIELECTRIC LAYERS (IDLS)

Yuanzhuo Liu
Missouri University of Science and Technology

Department: Electrical and Computer Engineering

FAR-END CROSSTALK MODELING AND PREDICTION FOR HIGH-SPEED PCB DESIGN WITH INHOMOGENEOUS DIELECTRIC LAYERS (IDLS)

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YUANZHUO LIU

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Approved by:

DongHyun Kim, Advisor
Jun Fan, Co-Advisor
Victor Khilkevich
Chulsoon Hwang
Xiaoning Ye

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ABSTRACT

Far-end crosstalk (FEXT) noise is a critical factor that affects signal integrity performance in high-speed systems. The FEXT level is sensitive to the inhomogeneity of the dielectric layers in fabricated printed circuit boards (PCB). The stripline is laminated by multiple inhomogeneous dielectric layers (IDL). The dielectric layers of the stripline are laminated with epoxy resin and glass bundles. The dielectric permittivity of the epoxy resin and glass bundles are different, which causes the inhomogeneity of the dielectric layers while also increasing the FEXT magnitude. The dielectric of the microstrip in printed circuit boards (PCB) fabrication usually consists of two layers: the solder mask layer and the substrate layer. In practice, the permittivity of the solder mask is generally higher than that of the substrate. Similarly, the inhomogeneity of the IDLs in the microstrip affects the FEXT and requires accurate characterization.

In this work, a practical FEXT modeling methodology for striplines and microstrips is proposed by introducing the extraction method for the permittivity of IDLs. The new stripline model is constructed with three IDLs comprised of core, prepreg, and resin pocket, to improve the model accuracy The microstrip is modeled with the air, solder mask, and substrate layers. To analyze the stripline and microstrip with IDLs, a practical superposition method is proposed. In addition, an analytical model to predict the FEXT polarity and magnitude of the stripline caused by the inhomogeneity is proposed and targeted for pre-layout application. The proposed models can provide useful analysis methodology and design guidelines to mitigate the FEXT level in high-speed systems, especially for high-volume PCB tests in the pre-layout and post-layout stages.

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1. INTRODUCTION

1.1. DIELECTRIC LAYERS IN PCB

Far-end crosstalk (FEXT) needs to be well-controlled in the high-speed system design to avoid system failure due to signal integrity issues. Therefore, during the pre-layout stage, it is important to model and reduce the FEXT of high-speed channels before fabrication to meet the high-speed system design margins. The inhomogeneity of the dielectric material is reported as a significant contributor to the FEXT. In the fabrication of the PCB, the dielectric material is laminated with different glass fiber and resin, which constructs the inhomogeneous dielectric layers.

Figure 1.1 shows the cross-section of a typical stripline. The dielectric layers of the stripline are laminated with epoxy resin and glass bundles. The dielectric permittivity (ε_r) of the epoxy resin and glass bundles are different, which causes the inhomogeneity of the dielectric layers. Stripline is typically modeled with a 2-layer (2L-IDL) model constructed with a core layer and prepreg layer which can only model the inhomogeneity between two layers. In this paper, a new model with multiple IDLs is proposed. A model with more than 3 IDLs can be generated if given enough information about the glass weaves and resin content. Each IDL has different dielectric permittivity, which is a closer model of the fabricated stripline to the real products. The additional third layer, sometimes also named “resin pocket”, is the layer that is only filled with resin between the core and prepreg layer, as is shown in Figure 1.1 with the red dotted boundary.

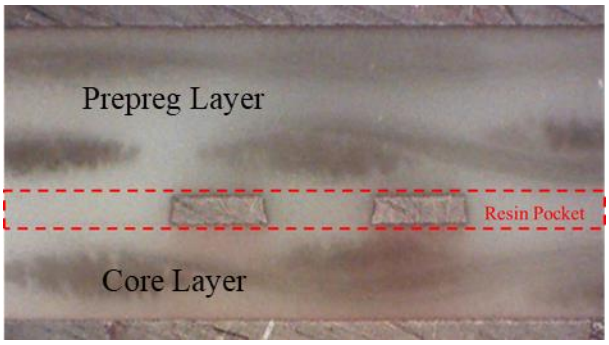

Figure 1.1. Cross-section of a pair of coupled stripline.

The dielectric of the microstrip in printed circuit boards (PCBs) fabrication usually consists of two layers: the solder mask layer and the substrate layer, as is shown in Figure 1.2. The samples of the traces are cut out from a fabricated PCB and encapsulated in an epoxy-based compound. The epoxy filled above the sample for fixation in the polishing procedure represent the air layer in PCB.

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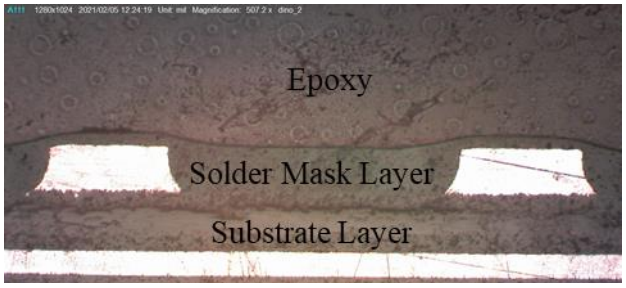


Figure 1.2. Cross-section of a pair of coupled microstrip.

1.2. EXTRACTION METHODOLOGY

FEXT noise is caused by the coupling between transmitting lines when the signal propagates from the transmit end to the receiving end. The modal analysis for the FEXT separates the aggressor signal into even and odd modes that propagate through the

coupled pair with different velocities. The odd and even phase velocities can be expressed using the per-unit length (PUL) model inductance and capacitance. To separate the contribution of each IDL, the capacitance is decomposed as is shown in Figure 1.3 and Figure 1.4 for stripline and microstrip pairs respectively. The capacitance is expressed by the product of the capacitances in the air-filled structure and the permittivity of the dielectric material. Then the relationship between the ε_r of the IDLs and the FEXT is expressed.

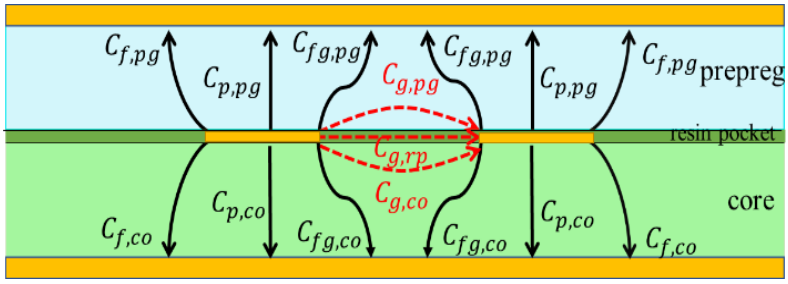


Figure 1.3. Illustration of the capacitance components for the coupled striplines.

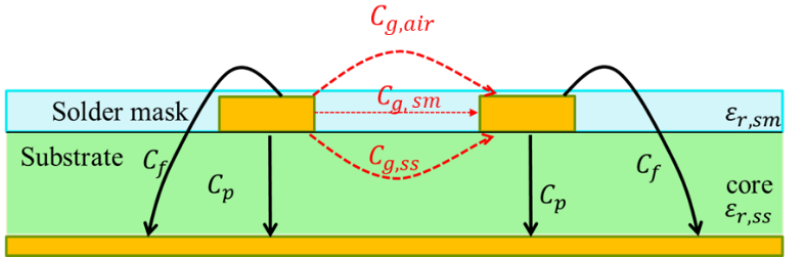


Figure 1.4. Illustration of the capacitance components for the coupled microstrip.

To extract the ε_r of each layer target function (T) is generated to evaluate the estimate of the error between the modeled result to the measured result. The function is defined with root mean squared error (RMSE), which is a general-purpose error metric

for numerical predictions. The difference of the ε_r has an obvious impact on the absolute value, which affects the FEXT level. While the differential mode per-unit-length (PUL) phase is quite sensitive to the sum of ε_r. The two unknowns can be solved with the two equations from the measurement results. The method is validated with measurement results using a test stripline structure with the extended unterminated line (EUL) and Delta-L structures. The EUL S-parameters provide the measured FEXT level and the Delta-L S-parameters after de-embedding provides β_{dd}. With the cross-section geometry, the simulation model is created by a 2D solver.

1.3. CONTENTS AND CONTRIBUTIONS

The outline and contributions of this dissertation are summarized.

In the first paper, a practical superposition method is proposed to analyze the PCB with three IDLs. A design guideline to mitigate the FEXT level in the stripline design is proposed based on the method.

In the following two papers, FEXT modeling methodologies for striplines and microstrip are proposed by introducing the extraction method for the $\boldsymbol{\varepsilon_r}$ of IDLs.

Based on the extraction methodology, a method to predict the FEXT polarity and peak level of the stripline caused by the inhomogeneity with an analytical expression is proposed. The prediction only needs the calculation by analytical expressions instead of with assistance from the 2D or 3D solvers. Compared to time-consuming full-wave simulation, the proposed method is time-efficient when optimizing a large number of designs with different geometry.

With the extracted properties, the FEXT and insertion loss of the microstrip can be characterized more accurately. In the design procedure of the microstrip, the design guideline for the key design parameters is of great use. Using the extracted model and the analysis of the FEXT of the microstrip, some general design guidelines are established based on the contribution of each parameter.

PAPER

I. FAR-END CROSSTALK ANALYSIS FOR STRIPLINE WITH INHOMOGENEOUS DIELECTRIC LAYERS (IDL)

Yuanzhuo Liu[#], Shaohui Yong[#], Yuandong Guo[#], Jiayi He[#], Liang Liu[#], Nick Kutheis*, Albert Sutono*, Vijay Kunda*, Amy Luoh*, Yunhui Chu*, Xiaoning Ye*, DongHyun Kim[#], Jun Fan[#]

[#]Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO, USA

*Datacenter Group, Intel Corporation, Portland, Oregon, USA

ABSTRACT

Far-end crosstalk (FEXT) noise is a critical factor that affects signal integrity performance in high-speed systems. The FEXT level is sensitive to the dielectric inhomogeneity of the stripline in fabricated printed circuit boards (PCB). Stripline is typically modeled as a 2-layer model with core and prepreg layers. However, in reality, the stripline is laminated by multiple inhomogeneous dielectric layers (IDL). The dielectric layers of the stripline are laminated with epoxy resin and glass bundles. The dielectric permittivity ($\boldsymbol{\varepsilon_r}$) of the epoxy resin and glass bundles are different, which causes the inhomogeneity of the dielectric layers while also increasing the FEXT magnitude. Therefore, typical 2-layer structure is inaccurate to model the FEXT. In this paper, the stripline model is constructed with the core, prepreg, and resin pocket layers. To analyze the stripline with three IDL, a practical superposition method is proposed. A

design guideline to mitigate the FEXT level in the stripline design is proposed based on the method.

Keywords: Far-end Crosstalk (FEXT), Stripline, Dielectric Material, Inhomogeneous Dielectric Layers (IDL).

1. INTRODUCTION

Far-end crosstalk (FEXT) noise is a critical factor that affects the signal integrity performance in high-speed systems with faster data transmission rates and a higher density of circuits [1-3].

In the fabrication procedure of the multilayer printed circuit boards (PCB), the dielectric layers are laminated with epoxy resin and glass bundles, as is shown in Figure 1. The dielectric permittivity (ε_r) of the epoxy resin and glass bundles are different. The inhomogeneity of the dielectric layers is caused by the different glass fiber weave/content in prepreg and core, prepreg melting during lamination, and epoxy resin property tolerances [4-6].

Stripline is typically modeled as a 2-layer model with core and prepreg layers [7-9]. FEXT between coupled stripline is the superposition of the received even and odd model signals [10]. With this analysis, FEXT is the superposition of the received even and odd model signals. Due to the difference between the dielectric constants (DK) in prepreg and core layers, the phase velocity for even and odd mode signals are not equal, which in return increases the FEXT magnitude [11].

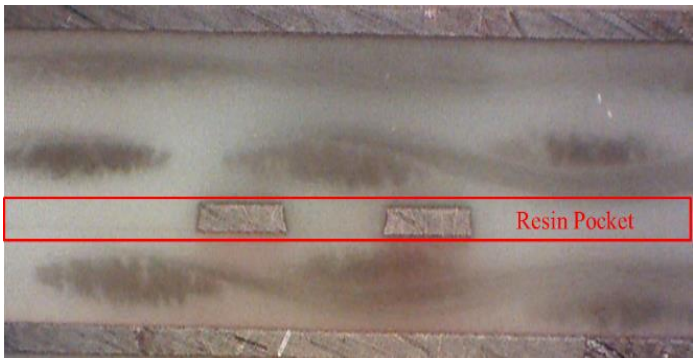


Figure 1. Cross-section of a pair of coupled stripline. The layer marked with red is the resin pocked.

The normal 2-layer model only takes the inhomogeneity between the core and prepreg layer into account. However, inhomogeneity caused by the epoxy resin and glass bundles inside the core and prepreg layers also affect the FEXT [12]. The 2-layer structure is then not accurate enough to model the stripline performance in frequency and time domain. The stripline model constructed with multiple inhomogeneous dielectric layers (IDL) with different dielectric permittivity is closer to the performance of the actual fabricated stripline. The resin pocket, which is a layer only filled with resin as shown in Figure 1, can be considered as a third layer different from the core and prepreg layers. During the lamination of the prepreg layer, some portion of resin melts and forms the resin pocket [13]. Since the resin pocket fills the area between the traces, it plays an important role in the stripline modeling. The model of the three IDL can provide a better description of the actual performance of the stripline [14].

To analyze the model with multiple IDL, a practical superposition method is proposed. To estimate the FEXT of multiple IDL models, the stripline can be

decomposed with 2-layer IDL models. The superposition of each 2-layer IDL model can provide a more accurate FEXT.

Section 2 introduces the impact of IDL on FEXT by a qualitative theory based on the transmission line theory and analytical expressions. The superposition method for analyzing the stripline model with multiple IDL is proposed and validated in Section 3. Section 4 analyzes the FEXT of the stripline with IDL. The proposed superposition method provides convenient analytical calculation of FEXT caused by the IDL. In addition, a guideline for the stripline with IDL is proposed as a reference for high speed PCB designers.

2. FEXT ANALYSIS METHODOLOGY FOR STRIPLINE WITH IDL

FEXT is the coupling between transmitting lines as the signal propagates from the transmit end of the pair to the receiving end. To describe the FEXT of coupled striplines, the methodology based on modal analysis is adopted [10]. In a pair of coupled striplines, the aggressor signal is separated into even and odd modes. The odd-mode signal and the even-mode signal propagate through the stripline with different velocities.

The odd and even phase velocities ($v_{p,odd}$, $v_{p,even}$) can be expressed using the per-unit length (PUL) model inductance (L_m) and capacitance (C_m):

$$v_{p,m} = \frac{1}{\sqrt{L_m C_m}} \tag{1}$$

Here, m represents even or odd mode. The FEXT is generated during the time interval between the arrival of the odd-mode signal and the arrival of the even-mode signal.

The differences between $v_{p,even}$ and $v_{p,odd}$ can be described as the variable Δ_{LC}, which is defined as:

$$\Delta_{LC} = L_{odd}C_{odd} - L_{even}C_{even} = 2(L_{11}|C_{21}| - C_{11}L_{21}) \quad (2)$$

To determine the influence of the IDL on Δ_{LC}, the capacitance can be decomposed [15]. In [15, Figure 2], the model with the core and prepreg layer is given. Based on the 2-layer model, the four categories of the per-unit-length capacitances in the 3-layer model shown in Table 1.

Table 1. The per-unit-length capacitances in the 3-layer model

Capacitance	Definition
C_f	Fringe capacitance on the outer side of the trace contributed by the prepreg ($C_{f,pg}$) and core ($C_{f,co}$) regions.
C_p	Parallel plate capacitance of the trace, contributed by the prepreg ($C_{p,pg}$) and core ($C_{p,co}$) regions.
C_{fg}	Fringe capacitance near the gap between traces, contributed by the prepreg ($C_{fg,pg}$) and core ($C_{fg,co}$) regions.
C_g	Mutual capacitance across the gap, contributed by the prepreg ($C_{g,pg}$), resin pocket ($C_{g,rp}$) and core ($C_{g,co}$) regions.

Notice that the thickness of the resin pocket is much smaller compared to the thickness of the core and prepreg layer. C_f, C_p, and C_{fg} are dominated by the prepreg and core regions. The mutual capacitance across the gap C_g can be expressed as:

$$C_g = C_{g,pg} + C_{g,co} + C_{g,rp} = \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \quad (3)$$

Here, α and β represent the potion of the flux that goes through prepreg and core.

The total capacitance in the prepreg ($C_{t,pg}$) is expressed using the capacitance components with subscript 'pg':

$$C_{t,pg} = C_{f,pg} + C_{p,pg} + C_{fg,pg} = \varepsilon_{r,pg} \cdot \left(C^a_{f,pg} + C^a_{p,pg} + C^a_{fg,pg}\right) = \varepsilon_{r,pg} \cdot C^a_{t,pg} \quad (3.a)$$

This capacitance can be estimated using the scaling of the capacitances in the air-filled line (denoted by the superscript 'a') by the permittivity of the dielectric media [16, Equ. (2.18)].

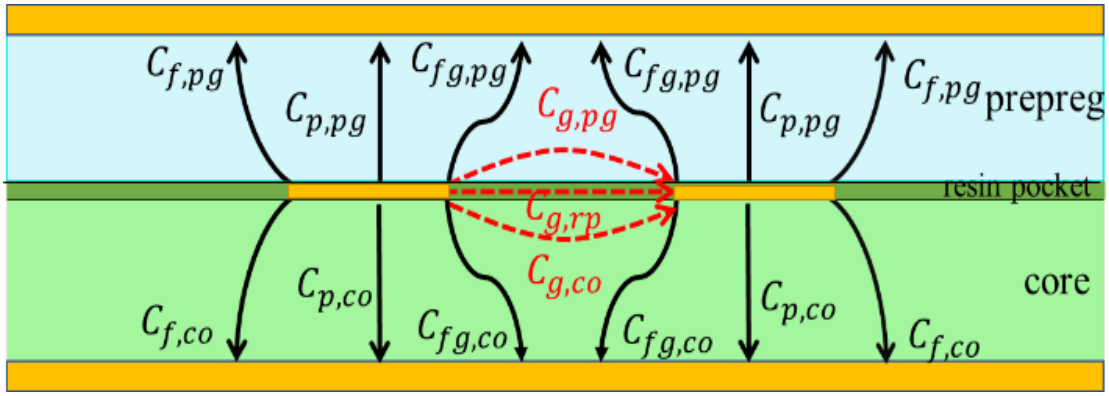


Figure 2. Illustration of the capacitance components for the coupled striplines. The dielectric permittivity in prepreg, resin pocket and core are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively.

Similarly, the total capacitance in the core ($C_{t,co}$) is expressed:

$$C_{t,co} = C_{f,co} + C_{p,co} + C_{fg,co} = \varepsilon_{r,co} \cdot \left(C^a_{f,co} + C^a_{p,co} + C^a_{fg,co}\right) = \varepsilon_{r,co} \cdot C^a_{t,co} \quad (3.b)$$

Thus, the self-capacitance in the nodal capacitance matrix can be expressed as:

$$C_{11} = C_{t,pg} + C_{t,co} + C_g$$

$$= \varepsilon_{r,pg} \cdot C^a_{t,pg} + \varepsilon_{r,co} \cdot C^a_{t,co} + \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \quad (4)$$

The mutual-capacitance in the nodal capacitance matrix:

$$|C_{21}| = C_g = \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \quad (5)$$

According to [12, Equ.14] [13, Equ. 14], the self-inductance and mutual-inductance can be estimated using capacitances of the air-filled line as:

$$L_{11}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10C^a_{11}}{9\Delta C^a} = \frac{10\left(C^a_{t,pg}+C^a_{t,co}+C^a_g\right)[\text{pF/cm}]}{9\Delta C^a\,[(\text{pF/cm})^2]} \quad (6)$$

$$L_{21}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10|C^a_{21}|}{9\Delta C^a} = \frac{10\left(C^a_{g,pg}+C^a_{g,co}+C^a_{g,rp}\right)[\text{pF/cm}]}{9\Delta C^a[(\text{pF/cm})^2]} \quad (7)$$

Where $\Delta C^a = (C^a_{11})^2 - (C^a_{21})^2$. For typical edge-coupled striplines $\Delta C^a > 0$. Then, Δ_{LC} is defined by (2) using the L and C given by (4)-(7) expressed as:

$$\Delta_{LC} = \frac{10}{9\Delta C^a} \cdot \left[\left(\varepsilon_{r,pg} - \varepsilon_{r,rp}\right) \cdot \left(C^a_{t,pg} C^a_{g,co} - C^a_{t,co} C^a_{g,pg} + C^a_{t,pg} C^a_{g,rp}\right) + \left(\varepsilon_{r,co} - \varepsilon_{r,rp}\right) \cdot \left(C^a_{t,co} C^a_{g,pg} - C^a_{t,pg} C^a_{g,co} + C^a_{t,co} C^a_{g,rp}\right)\right] \quad (8)$$

$C^a_{t,pg}$, $C^a_{t,co}$, $C^a_{g,pg}$, $C^a_{g,co}$, $C^a_{g,rp}$, ΔC^a are determined by the structure. From (8), it can be noted that Δ_{LC} is proportional to the dielectric permittivity difference between prepreg and resin pocket $\left(\varepsilon_{r,pg} - \varepsilon_{r,rp}\right)$ and the difference between the core and resin pocket $\left(\varepsilon_{r,co} - \varepsilon_{r,rp}\right)$. In other words, the FEXT caused by the 3-layer IDL can be separated into two parts: FEXT caused by the inhomogeneity of prepreg and resin pocket layers and FEXT caused by the inhomogeneity of core and resin pocket layers. Accordingly, the superposition method is introduced in Section 3.

3. SUPERPOSITION METHOD

To simplify the analysis of the stripline with IDL, the 3-layer model can be decomposed as two 2-layer models. As shown in Figure 3. Case 1 is the original 3-layer model. The dielectric permittivity in the prepreg, resin pocket, and core layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively. Two inhomogeneous boundaries exists in this model: the boundary between prepreg and resin pocket and the boundary between resin pocket and core. The basic idea is to decompose the two boundaries into two models individually.

In Case 2, the dielectric permittivity of the prepreg layer is set to be $\varepsilon_{r,rp}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 2 then becomes a 2-layer model with only one inhomogeneous boundary between the resin pocket and core. According to (8), Δ_{LC} of Case 2 is:

$$\Delta_{LC2}=\frac{10C_g^a}{9\Delta C^a}\cdot\left[\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right)\cdot\left(C_{t,pg}^aC_{g,co}^a-C_{t,co}^aC_{g,pg}^a+C_{t,pg}^aC_{g,rp}^a\right)\right] \quad (9)$$

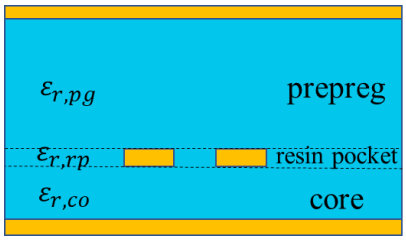
In Case 3, the dielectric permittivity of the core layer is set to be $\varepsilon_{r,rp}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 3 then becomes a 2-layer model with only one inhomogeneous boundary between the resin pocket and prepreg.

$$\Delta_{LC3}=\frac{10C_g^a}{9\Delta C^a}\cdot\left[\left(\varepsilon_{r,co}-\varepsilon_{r,rp}\right)\cdot\left(C_{t,co}^aC_{g,pg}^a-C_{t,pg}^aC_{g,co}^a+C_{t,co}^aC_{g,rp}^a\right)\right] \quad (10)$$

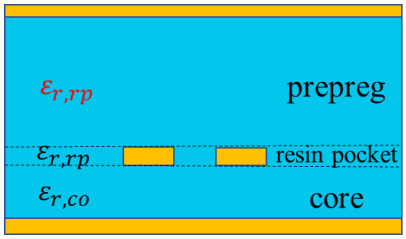
It can be assumed that the air-filled mutual capacitances across the gap contributed by each layer ($C_{g,pg}^a$, $C_{g,co}^a$, $C_{g,rp}^a$) remain the same when assigning different dielectric permittivity to the layers. Δ_{LC1} can be expressed by the superposition of Case 2 and Case 3:

$$\Delta_{LC1} = \Delta_{LC2} + \Delta_{LC3} \tag{11}$$

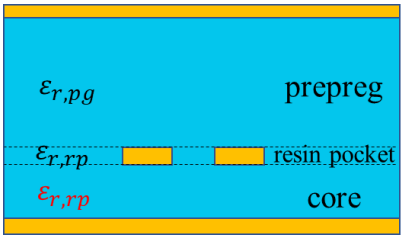
Then the FEXT caused by the inhomogeneity of the stripline with the 3 IDL model is equivalent to the superposition of the FEXT of two 2-layer models.



(a) Case 1



(b) Case 2



(c) Case 3

Figure 3. (a) Case 1: The dielectric permittivity in the prepreg, resin pocket, and core layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively. (b) Case 2: The dielectric permittivity in prepreg and resin pocket layers is $\varepsilon_{r,rp}$. (c) Case 3: The dielectric permittivity in core and resin pocket layers is $\varepsilon_{r,rp}$.

4. FEXT ANALYSIS FOR STRIPLINE WITH IDL

In this section, two examples are given of the FEXT analysis for the stripline with IDL and with different geometries.

4.1. EXAMPLE WITH SYMMETRIC GEOMETY

The stripline is normally considered as the combination of two layers: core and prepreg. In this way, only the inhomogeneous between the core and prepreg layer is taken into account for the FEXT analysis. However, inhomogeneous caused by the resin pocket will also affect the FEXT level.

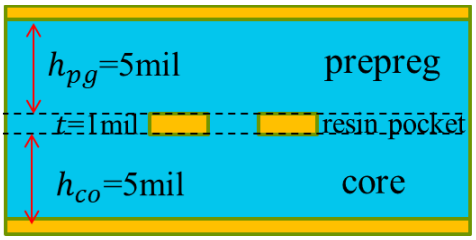


Figure 4. Cross-section geometry of two coupled symmetrical stripline traces. The trace width of the trace is 7.2mil. The spacing between the traces is 10mil.

For example, Figure 4 demonstrates a cross-section of the stripline. Both the thickness of the prepreg layer and the core layer is 5mil. Both the dielectric permittivity in core and prepreg is 4. The dielectric permittivity in the resin pocket is 2.8. The thickness of the trace, which is also the thickness of the resin pocket layer. The FEXT level of the example can be decomposed with two cases as Figure 3. All three cases are

simulated by ANSYS Q2D. The assignment of dielectric permittivity for the different cases are:

Case 1: $\varepsilon_{r,pg}$=4; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=4.

Case 2: $\varepsilon_{r,pg}$=2.8; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=4.

Case 3: $\varepsilon_{r,pg}$=4; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=2.8.

The transformed FEXT waveform result from the S-parameter of the Q2D simulation is shown in Figure5. Table 2 lists the peak value of the FEXT waveform of the three cases. The FEXT level of Case 1 is approximately equal to the sum of Case 2 and Case 3. The error is caused by the assumption during the derivation that the air-filled mutual capacitances across the gap contributed by each layer ($C^a_{g,pg}$, $C^a_{g,co}$, $C^a_{g,rp}$) are the same in different cases. The flux lines tend to get more concentrated in the region with higher dielectric permittivity. As a result, for different cases, the potion of the mutual capacitance contributed by different layers will be slightly different.

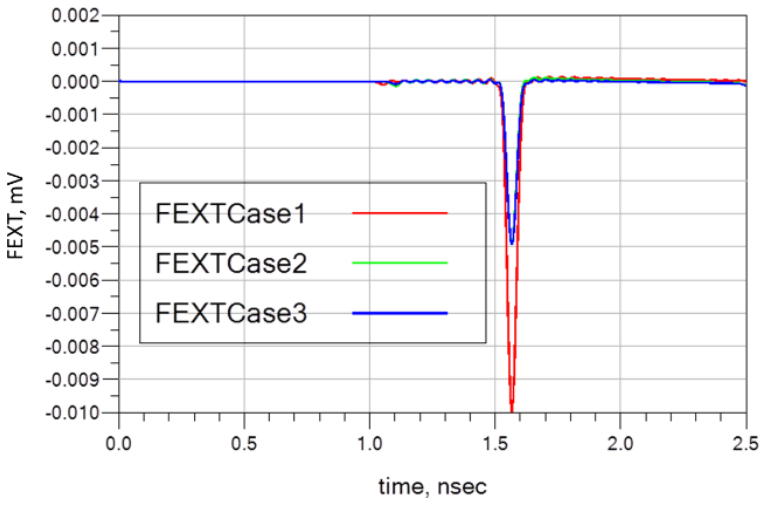


Figure 5. FEXT waveform for the stripline model with the geometry in Figure 4.

Table 2. Peak value of the FEXT waveform with the geometry in Figure 4

	Case 1	Case 2	Case 3
ε_{preg}	4	2.8	4
ε_{resin}	2.8	2.8	2.8
ε_{core}	4	4	2.8
FEXT Peak (mV)	-9.97	-4.96	-4.96

In this example, the core layer and the prepreg layer have the same thickness and dielectric. If the stripline is only modeled with core and prepreg layers, the mutual capacitance across the gap C_g can be expressed as:

$$C_g = C_{g,pg} + C_{g,co} = \varepsilon_{r,pg}{}' C^a_{g,pg}{}' + \varepsilon_{r,co}{}' C^a_{g,co}{}' \tag{12}$$

Then replace (3) by (9) for (4-7), the Δ_{LC} for the 2-layer model is:

$$\Delta'_{LC} = \frac{10}{9\Delta C^a} \cdot \left(\varepsilon_{r,pg}{}' - \varepsilon_{r,co}{}'\right) \cdot \left(C^a_{t,pg} C^a_{g,co}{}' - C^a_{t,co} C^a_{g,pg}{}'\right) \tag{13}$$

$\varepsilon_{r,pg}{}'$ are $\varepsilon_{r,co}{}'$ are effective dielectric permittivity for the prepreg and core layers in the 2-layer model. $C^a_{g,pg}{}'$, $C^a_{g,co}{}'$ are effective air-filled mutual capacitances across the gap contributed by prepreg and core layers. Thus, the FEXT level by this equivalent model is close to zero. Therefore, in this extreme symmetric example, the normal 2-layer model of the stripline can't perform accurately with multiple IDL.

4.2. EXAMPLE WITH ASYMMETRIC GEOMETY

An example with asymmetrical geometry, which is more common in actual PCB design, is simulated and analyzed. The cross-section geometry is shown in Figure 6. The

thickness of the prepreg layer is 7mil, while the thickness of the core layer is 3mil. The dielectric permittivity in the core is 3.5. The dielectric permittivity in the resin pocket is 2.8. In fabricated multi-layer PCB, due to the different glass fiber weave/content in prepreg and core, prepreg melting during lamination, and epoxy resin properties tolerances, etc. [4-6], the dielectric permittivity in the prepreg and core layer are different in this example. Where the dielectric permittivity prepreg is set to be 3.5, 4.5 and 5.5 for different series of the cases.

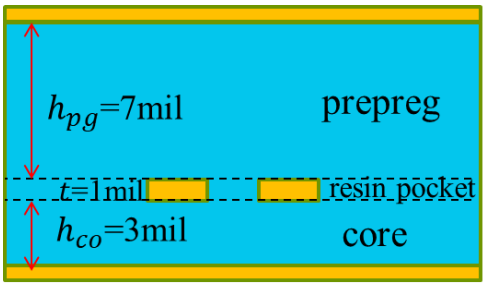


Figure 6. Cross-section geometry of two coupled stripline traces. The trace width of the trace is 7.2mil. The spacing between the traces is 10mil.

Table 3 lists the FEXT level of the cases. For the series of Case a, Case b, and Case c, the FEXT level of Case x.1 is approximately equal to the sum of Case x.2 and Case x.3 (x can be a, b or c), which provides the verification for the superposition method.

For this example, with asymmetrical geometry, it is difficult to analyze the FEXT directly from the 3-layer model. The superposition method can help by decomposing the total FEXT to two 2-layer cases. In (9) and (10), it can be noted that $\Delta_{LC}$is not only

related to the difference of the dielectric material, but also the capacitance. Then, (9) and (10) can be modified as:

$$\Delta_{LC2}=\frac{10C_g^a}{9\Delta C^a}\cdot\left\{\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right)\cdot\left(\left[C_{t,pg}^a\cdot\left(C_{g,co}^a+C_{g,rp}^a\right)-C_{t,co}^aC_{g,pg}^a\right]\right)\right\} \quad (14)$$

$$\Delta_{LC3}=\frac{10C_g^a}{9\Delta C^a}\cdot\left\{\left(\varepsilon_{r,co}-\varepsilon_{r,rp}\right)\cdot\left[C_{t,co}^a\cdot\left(C_{g,pg}^a+C_{g,rp}^a\right)-C_{t,pg}^aC_{g,co}^a\right]\right\} \quad (15)$$

In this example, the thickness of the prepreg layer is larger than that of the core layer. As the result, $C_{t,pg}^a$ will be smaller than $C_{t,co}^a$. Considering that the $C_{g,pg}^a+C_{g,rp}^a$ should be larger than $C_{g,co}^a$, Δ_{LC3} is expected to be a positive value. The value of the capacitance term in Δ_{LC2} is expected to be much smaller than that in Δ_{LC3}.

In practice, to improve the signal integrity performance in high-speed systems, the FEXT is always expected to be mitigated in the design procedure. In the design procedure of the stripline, the method to mitigate the FEXT level could help provide the value $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ as a guideline. From (11) and (12), both Δ_{LC2} and Δ_{LC3} are proportional to the difference of the dielectric permittivity while the capacitance term is mainly determined by the cross-section geometry. Therefore, the FEXT caused from Case 2 and Case 3 can be expressed approximately as:

$$FEXT_2\sim K_2\cdot\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right) \quad (16)$$

$$FEXT_3\sim K_3\cdot\left(\varepsilon_{r,co}-\varepsilon_{r,rp}\right) \quad (17)$$

K_2 and K_3 can be obtained by two simulations of 2-layer models. For example, from Case a.2 and Case a.3, K_2 is calculated as -9.3 and K_3 is calculated as 4.2. Then the prediction for the total FEXT caused by IDL is:

$$FEXT_{predict}=K_2\cdot\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right)+K_3\cdot\left(\varepsilon_{r,co}-\varepsilon_{r,rp}\right) \quad (18)$$

Table 3. Peak value of the FEXT waveform with the geometry in Figure 6

(a)

	Case a.1	Case a.2	Case a.3
ε_{preg}	3.5	2.8	3.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-3.65	-6.50	2.95

(b)

	Case b.1	Case b.2	Case b.3
ε_{preg}	4.5	2.8	4.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-0.30	-6.50	6.69

(c)

	Case a.1	Case a.2	Case a.3
ε_{preg}	5.5	2.8	5.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-3.91	-6.50	10.63

When the $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ is known as 2.8 and 3.5, to minimize the FEXT, the $\varepsilon_{r,pg}$ can be determined as 4.35. From Table 2(b), when $\varepsilon_{r,pg}$ is 4.5, the total FEXT is -0.3mV. The error between the solution of the prediction and the actual value is 3%. With the superposition method, only two simulations of 2-layer models are needed to predict the FEXT level with different dielectric materials that provide a solution to minimize the FEXT.

5. CONCLUSION

This paper proposes a practical method to analyze the FEXT for the stripline with IDL and provides a design guideline to mitigate the FEXT level. The 3-layer stripline model constructed with core, prepreg and resin pocket layers is investigated. The resin pocket is a critical layer with stable dielectric permittivity that locates surrounding traces. The FEXT for the stripline with multilayer IDL can be decomposed with the models that only with one inhomogeneity boundary.

For the stripline with fixed geometry, the FEXT level of the material with different dielectric constant can be expressed. Besides, the best solution of the dielectric constant assignment in the stripline with minimum FEXT can be calculated. This method can be further applied to the extraction of the stripline with IDL and the analysis of the FEXT for the microstrip model constructed with dielectric substrate and solder mask layers.

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II. FAR-END CROSSTALK MODELING AND PREDICTION FOR STRIPLINE WITH INHOMOGENEOUS DIELECTRIC LAYERS (IDLS)

Yuanzhuo Liu[#], Shaohui Yong[#], Yuandong Guo[#], Jiayi He[#], Chaofeng Li[#], Xiaoning Ye*, Jun Fan[#], DongHyun Kim[#]

[#]Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO, USA

*Datacenter Group, Intel Corporation, Portland, Oregon, USA

ABSTRACT

Far-end crosstalk (FEXT) is a critical factor that limits signal integrity performance in high-speed systems. The FEXT level is sensitive to the dielectric inhomogeneity of the stripline in fabricated printed circuit boards (PCB). The dielectric of the stripline is manufactured with multiple inhomogeneous dielectric layers (IDLs) of various resin and glass fiber bundles. A marginal difference in the dielectric permittivity of the IDLs can lead to a significant change FEXT level. In this paper, a practical FEXT modeling methodology for striplines is proposed by introducing the extraction method for the $\boldsymbol{\varepsilon_r}$of IDLs. The new stripline model is constructed with three IDLs comprised of core, prepreg, and resin pocket, to improve the model accuracy. With the cross-sectional geometry and measured S-parameters of the coupled striplines, the $\boldsymbol{\varepsilon_r}$ of IDLs can be extracted. In addition, an analytical model to predict the FEXT polarity and magnitude of the stripline caused by the inhomogeneity is proposed targeted for pre-layout application. The proposed models have been verified using measurement. The proposed models can provide useful analysis methodology and design guidelines to mitigate the FEXT level in

high-speed systems, especially for high-volume PCB tests in the pre-layout and post-layout stages.

Keywords: Far-end Crosstalk (FEXT), Delta-L, Extended unterminated line (EUL), Stripline, Dielectric material property, Far-end Crosstalk (FEXT), Stripline, Dielectric Material, Inhomogeneous Dielectric Layers (IDL).

1. INTRODUCTION

Far-end crosstalk (FEXT) needs to be well-controlled in the high-speed system design to avoid system failure due to signal integrity issues [1-3]. Therefore, during the pre-layout stage, it is important to model and reduce the FEXT of high-speed channels before fabrication to meet the high-speed system design margins [4-6].

The inhomogeneity of the dielectric material is reported as a significant contributor to the FEXT [5-7]. In the fabrication of the PCB, the dielectric material is laminated with different glass fiber and resin, which constructs the inhomogeneous dielectric layers [7-8]. The dielectric permittivity (ε_r) of the resin and glass bundles are different, typically around 3 (resin) and 5 to 7 (glass) respectively. The difference in phase velocities of even and odd mode signals caused by inhomogeneous dielectric layers (IDLs) results in non-zero FEXT noise in striplines. A marginal difference in dielectric permittivity can result in a significant FEXT level difference. For example, a difference of 0.1 between the permittivity of the core and prepreg layer could result in tens of millivolts crosstalk for a 3-inch stripline in the worst cases [7, Figure 4.].

Stripline is typically modeled with a 2-layer (2L-IDL) model constructed with a core layer and prepreg layer which can only model the inhomogeneity between two layers. In this paper, a new model with multiple IDLs (e.g., 3L-IDL model) is proposed. A model with more than 3 IDLs can be generated if given enough information about the glass weaves and resin content. Each IDL has different dielectric permittivity, which is a closer model of the fabricated stripline to the real products. The additional third layer, sometimes also named “resin pocket”, is the layer that is only filled with resin between the core and prepreg layer, as is shown in Figure 1. It is formed by resin flowing into metal gaps during the lamination process. Since the resin pocket fills the area between the two coupled traces and with a different dielectric constant, it has a critical influence on the SI performance of the stripline. The 3L-IDL model constructed with the resin pocket provides a more accurate representation of an actual fabricated stripline compared to a typical 2L-IDL model [9].

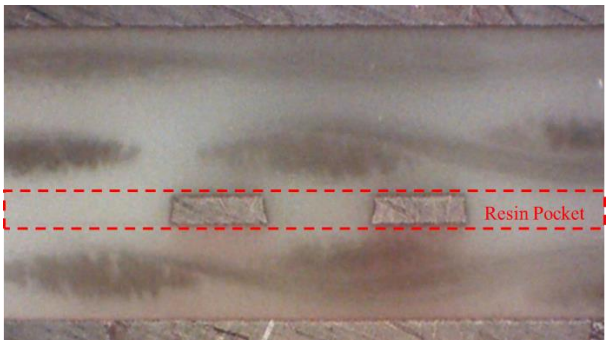


Figure 1. Cross-section of a pair of coupled stripline. the resin pocked is indicated with a dotted boundary

In order to characterize the FEXT due to the IDLs, the $\boldsymbol{\varepsilon_r}$ of each IDL in the new model needs to be determined. Previously reported models only extracted ε_r of prepreg

and core layers. In this paper, an approach to extract the ε_r of IDLs for the new 3-layer model is proposed.

The method is validated with measurement results using a test stripline structure with the extended unterminated line (EUL) and Delta-L structures, which is widely used for high-volume PCB tests [10-11]. The EUL structure is designed for convenient and accurate far-end crosstalk (FEXT) measurements, which allows only half the needed test ports while excluding the impact from FEXT due to mismatched terminals. Delta-L structures are differential striplines with different lengths [12]. With the de-embedding procedure [13-15], the vias and fixture effect can be removed so that S-parameters of the stripline is obtained. With the extracted ε_r of IDLs for the new 3-layer model, more accurate modeling of the FEXT waveform can be achieved.

The superposition method in [4] provides a practical way to analyze and model the FEXT of the stripline in multilayer IDLs. Using the same superposition principle, the FEXT caused by the inhomogeneity of 3 IDLs can be decomposed into the FEXT of two sets of 2L-IDL models. Furthermore, an analytical model is proposed to predict the polarity and magnitude of FEXT in striplines caused by the IDLs. The analytical model does not require any results from the 2D or 3D simulation tools. The analytical model can be applied for both the traditional 2L-IDL model and the newly proposed 3L-IDL model.

As part of the paper organization, in Section II, FEXT due to the IDLs are discussed. The FEXT analysis methodologies for the stripline with three IDLs are explained. Section III presents the extraction algorithm for the $\boldsymbol{\varepsilon_r}$ of IDLs using Delta-L and EUL design. Section IV provides an analytical model and verification using measurement results.

2. FEXT ANALYSIS METHODOLOGY

2.1. FEXT CAUSED BY IDLS

FEXT noise is caused by the coupling between transmitting lines when the signal propagates from the transmit end to the receiving end. The modal analysis for the FEXT [16] separates the aggressor signal into even and odd modes and propagates through the coupling pair with different velocities:

The odd and even phase velocities ($v_{p,odd}$, $v_{p,even}$) can be expressed using the per-unit length (PUL) model inductance (L_m) and capacitance (C_m):

$$v_{p,m} = \frac{1}{\sqrt{L_m C_m}} \tag{1}$$

Here, m represents even or odd mode. The FEXT is generated during the time interval between the arrival of the odd-mode signal and the arrival of the even-mode signal.

The differences between $v_{p,even}$ and $v_{p,odd}$ can be described as the variable Δ_{LC}[7], which is defined as:

$$\Delta_{LC} = L_{odd}C_{odd} - L_{even}C_{even} = 2(L_{11}|C_{21}| - C_{11}L_{21}) \tag{2}$$

To separate the contribution of each IDL on Δ_{LC}, the capacitance is decomposed [17]. In [17], the stripline is modeled with the core and prepreg layers. Based on that, the capacitance of the structure with 3 IDLs is decomposed in [4]. The four categories of the per-unit-length capacitances in the 3-layer model are explained in Table 1.

In reality, the thickness of the resin pocket may vary depending on the resin content of dielectrics used. In this study, since the main focus is to develop an equivalent model, we assume the thickness of the resin pocket is the same as the trace thickness. As

the result, C_f, C_p, and C_{fg} are mainly related to the flux that goes through the core and prepreg layers. The mutual capacitance across the gap C_g can be expressed as:

$$C_g = C_{g,pg} + C_{g,co} + C_{g,rp} = \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \quad (3)$$

Table 1. Definition of the decomposed capacitance.

Capacitance	Definition
C_f	Fringe capacitance on the outer side of the trace is contributed by the prepreg ($C_{f,pg}$) and core ($C_{f,co}$) regions.
C_p	Parallel plate capacitance of the trace, contributed by the prepreg ($C_{p,pg}$) and core ($C_{p,co}$) regions.
C_{fg}	Fringe capacitance near the gap between traces, contributed by the prepreg ($C_{fg,pg}$) and core ($C_{fg,co}$) regions.
C_g	Mutual capacitance across the gap, contributed by the prepreg ($C_{g,pg}$), resin pocket ($C_{g,rp}$) and core ($C_{g,co}$) regions.

The total capacitance in the prepreg ($C_{t,pg}$) is expressed using the capacitance components with subscript ‘pg’:

$$C_{t,pg} = C_{f,pg} + C_{p,pg} + C_{fg,pg} = \varepsilon_{r,pg} \cdot \left(C^a_{f,pg} + C^a_{p,pg} + C^a_{fg,pg}\right) = \varepsilon_{r,pg} \cdot C^a_{t,pg} \quad (3.a)$$

This capacitance is expressed by the product of the capacitances in the air-filled structure (denoted by the superscript ‘a’) and the permittivity of the dielectric material. The total capacitance in the core ($C_{t,co}$) is expressed similarly [18, Eq. (8.86)] as:

$$C_{t,co} = C_{f,co} + C_{p,co} + C_{fg,co} = \varepsilon_{r,co} \cdot \left(C^a_{f,co} + C^a_{p,co} + C^a_{fg,co}\right) = \varepsilon_{r,co} \cdot C^a_{t,co} \qquad (3.b)$$

Thus, the self-capacitance in the nodal capacitance matrix can be expressed as:

$$C_{11} = C_{t,pg} + C_{t,co} + C_g$$

$$= \varepsilon_{r,pg} \cdot C^a_{t,pg} + \varepsilon_{r,co} \cdot C^a_{t,co} + \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \qquad (4)$$

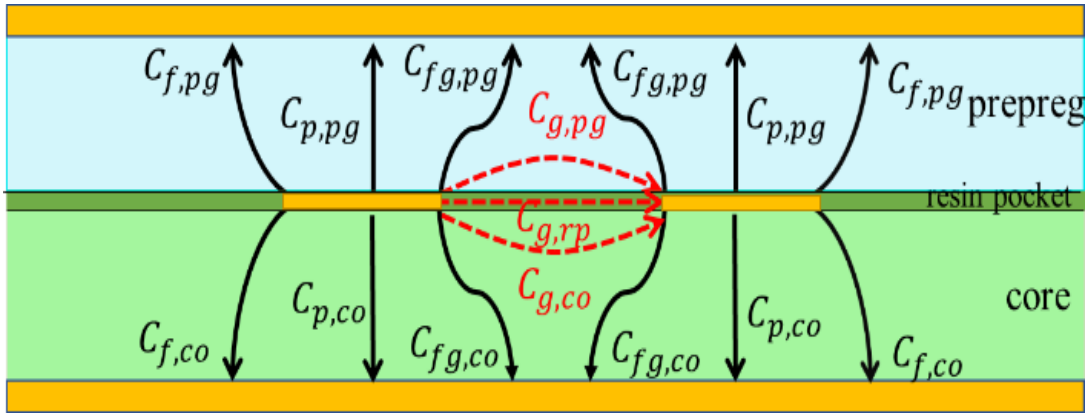


Figure 2. Illustration of the capacitance components for the coupled striplines. The dielectric permittivity in prepreg, resin pocket, and core are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively.

The mutual capacitance in the nodal capacitance matrix:

$$|C_{21}| = C_g = \varepsilon_{r,pg} C^a_{g,pg} + \varepsilon_{r,co} C^a_{g,co} + \varepsilon_{r,rp}\, C^a_{g,rp} \qquad (5)$$

According to [17, Eq. 14], the self-inductance and mutual inductance can be estimated using capacitances of the air-filled line as:

$$L_{11}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10 C^a_{11}}{9\Delta C^a} = \frac{10\left(C^a_{t,pg} + C^a_{t,co} + C^a_g\right)[\text{pF/cm}]}{9\Delta C^a\,[(\text{pF/cm})^2]} \qquad (6)$$

$$L_{21}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10|C^a_{21}|}{9\Delta C^a} = \frac{10\left(C^a_{g,pg} + C^a_{g,co} + C^a_{g,rp}\right)[\text{pF/cm}]}{9\Delta C^a[(\text{pF/cm})^2]} \qquad (7)$$

Here $\Delta C^a = (C^a_{11})^2 - (C^a_{21})^2$. For typical edge-coupled striplines $\Delta C^a > 0$.

Then, Δ_{LC} is defined by (2) using the L and C given by (4)-(7) expressed as:

$$\Delta_{LC}=\frac{10}{9\Delta C^{a}}\cdot[(\varepsilon_{r,pg}-\varepsilon_{r,rp})\cdot(C^{a}_{t,pg}C^{a}_{g,co}-C^{a}_{t,co}C^{a}_{g,pg}+C^{a}_{t,pg}C^{a}_{g,rp}) +(\varepsilon_{r,co}-\varepsilon_{r,rp})\cdot(C^{a}_{t,co}C^{a}_{g,pg}-C^{a}_{t,pg}C^{a}_{g,co}+C^{a}_{t,co}C^{a}_{g,rp})] \quad (8)$$

$C^{a}_{t,pg}$, $C^{a}_{t,co}$, $C^{a}_{g,pg}$, $C^{a}_{g,co}$, $C^{a}_{g,rp}$, ΔC^{a} are all the capacitance with the air-filled structure, which is only related to the geometry of the stripline.

From (8), it can be noted that Δ_{LC} is proportional to the dielectric permittivity difference between prepreg and resin pocket $(\varepsilon_{r,pg}-\varepsilon_{r,rp})$ and the difference between the core and resin pocket $(\varepsilon_{r,co}-\varepsilon_{r,rp})$. In other words, the FEXT caused by the 3L-IDL can be separated into two parts: FEXT caused by the inhomogeneity of prepreg and resin pocket layers and FEXT caused by the inhomogeneity of core and resin pocket layers. Accordingly, the superposition method is introduced.

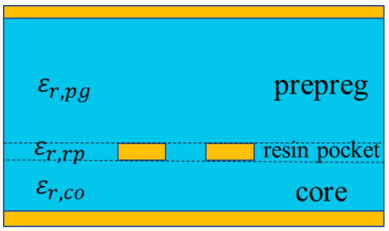
2.2. SUPERPOSITION METHOD

The 3L-IDL model with three different dielectric materials is not easy to analyze directly. Therefore, decomposing it into typical 2L-IDL models can help to simplify the complex structure.

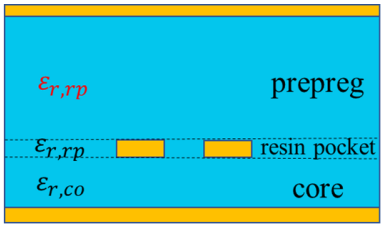
As shown in Figure 3, Case 1 is the original 3L-IDL model. The dielectric permittivity in the prepreg, resin pocket, and core layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively. Two inhomogeneous boundaries are formed in this model: the boundary between prepreg and resin pocket and the boundary between resin pocket and core, to decompose the two boundaries into two sets of relatively simple 2L-IDL models.

In Case 2, the dielectric permittivity of the prepreg layer is denoted by $\varepsilon_{r,rp}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 2 then becomes a 2-layer model with only one inhomogeneous boundary between the resin pocket and core. According to (8), Δ_{LC} of Case 2 is:

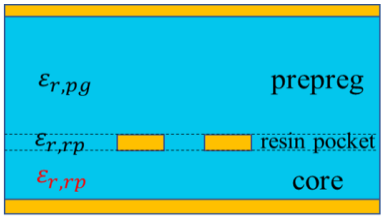
$$\Delta_{LC2}=\frac{10C_g^a}{9\Delta C^a}\cdot\left[\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right)\cdot\left(C_{t,pg}^a C_{g,co}^a - C_{t,co}^a C_{g,pg}^a + C_{t,pg}^a C_{g,rp}^a\right)\right] \quad (9)$$



(a) Case 1



(b) Case 2



(c) Case 2

Figure 3. (a) Case 1: The dielectric permittivity in the prepreg, resin pocket, and core layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$ and $\varepsilon_{r,co}$ respectively. (b) Case 2: The dielectric permittivity in prepreg and resin pocket layers is $\varepsilon_{r,rp}$. (c) Case 3: The dielectric permittivity in core and resin pocket layers is $\varepsilon_{r,rp}$.

In Case 3, the dielectric permittivity of the core layer is denoted by $\varepsilon_{r,rp}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 3 then becomes a 2-layer model with only one inhomogeneous boundary between the resin pocket and prepreg.

$$\Delta_{LC3} = \frac{10C_g^a}{9\Delta C^a} \cdot \left[\left(\varepsilon_{r,co} - \varepsilon_{r,rp}\right) \cdot \left(C_{t,co}^a C_{g,pg}^a - C_{t,pg}^a C_{g,co}^a + C_{t,co}^a C_{g,rp}^a\right)\right] \quad (10)$$

It can be assumed that the air-filled mutual capacitances across the gap contributed by each layer ($C_{g,pg}^a$, $C_{g,co}^a$, $C_{g,rp}^a$) remain the same when assigning different dielectric permittivity to the layers.

Δ_{LC1} can be expressed by the superposition of Case 2 and Case 3:

$$\Delta_{LC1} = \Delta_{LC2} + \Delta_{LC3} \quad (11)$$

Then the FEXT caused by the inhomogeneity of the stripline with the 3L-IDL model is equivalent to the superposition of the FEXT of two 2-layer models.

2.3. FEXT ANALYSIS FOR STRIPLINE WITH IDLS

As the validation of the FEXT analysis methodology, two examples are given for the stripline with IDL and with different geometries. One of the single-ended traces is considered the aggressor and the other trace is the victim. The FEXT caused by the coupling between the two traces is discussed. The work can be easily extended to differential signaling as well.

2.3.1. Stripline with Symmetric Prepreg and Core Dimension. Figure 4 demonstrates a cross-section of an equivalent model of the stripline. For simplicity, the cross-section of the stripline is set as rectangular instead of a typical trapezoidal shape. Both the thickness of the prepreg layer and the core layer is 5mil. Both the dielectric

permittivity in core and prepreg is 4. The dielectric permittivity in the resin pocket is set to be 2.8 as an example. The thickness of the trace is also set to be the same as the thickness of the resin pocket layer. In this example, the stripline is symmetric in that the core layer and the prepreg layer share the same thickness and material property. The FEXT level of the example can be decomposed into two cases as Figure 3.

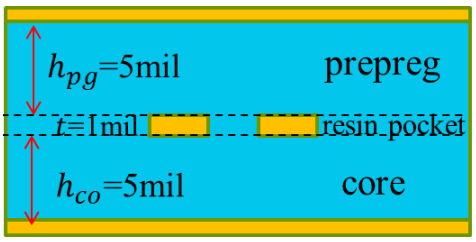


Figure 4. Cross-section geometry of two coupled symmetrical stripline traces. The trace width of the trace is 7.2mil. The spacing between the traces is 10mil.

All three cases are simulated by ANSYS Q2D. The assignment of dielectric permittivity for the different cases are:

Case 1: $\varepsilon_{r,pg}$=4; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=4.

Case 2: $\varepsilon_{r,pg}$=2.8; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=4.

Case 3: $\varepsilon_{r,pg}$=4; $\varepsilon_{r,rp}$=2.8, $\varepsilon_{r,co}$=2.8.

The transformed FEXT waveform result from the S-parameter of the Q2D simulation is shown in Figure 5. Table 2 lists the peak value of the FEXT waveform of the three cases. The FEXT level of Case 1 is approximately equal to the sum of Case 2 and Case 3. The error is caused by the assumption during the derivation that the air-filled mutual capacitances across the gap contributed by each layer ($C^a_{g,pg}$, $C^a_{g,co}$, $C^a_{g,rp}$) are the same in different cases. The flux lines tend to get more concentrated in the region with

higher dielectric permittivity. As a result, for different cases, the portion of the mutual capacitance contributed by different layers will be slightly different.

In this example, the core layer and the prepreg layer have the same thickness and dielectric. If the stripline is only modeled with core and prepreg layers, the mutual capacitance across the gap C_g can be expressed as:

$$C_g = C_{g,pg} + C_{g,co} = \varepsilon_{r,pg}{}' C^a_{g,pg}{}' + \varepsilon_{r,co}{}' C^a_{g,co}{}' \quad (12)$$

Then replace (3) by (9) for (4-7), the Δ_{LC} for the 2-layer model is:

$$\Delta'_{LC} = \frac{10}{9\Delta C^a} \cdot \left(\varepsilon_{r,pg}{}' - \varepsilon_{r,co}{}'\right) \cdot \left(C^a_{t,pg} C^a_{g,co}{}' - C^a_{t,co} C^a_{g,pg}{}'\right) \quad (13)$$

$\varepsilon_{r,pg}{}'$ are $\varepsilon_{r,co}{}'$ are effective dielectric permittivity for the prepreg and core layers in the 2-layer model. $C^a_{g,pg}{}'$, $C^a_{g,co}{}'$ are effective air-filled mutual capacitances across the gap contributed by prepreg and core layers. The FEXT level of this 2L-IDL model turns out to be close to zero, indicating that for this extreme symmetric example, the former 2L-IDL model cannot describe the performance of the multiple IDLs structures accurately.

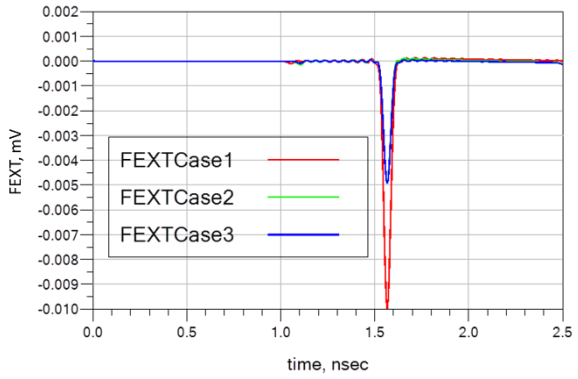


Figure 5. FEXT waveform for the stripline model with the geometry in Figure 4.

Table 2. The peak value of the FEXT waveform with the geometry in Figure 4

	Case 1	Case 2	Case 3
ε_{preg}	4	2.8	4
ε_{resin}	2.8	2.8	2.8
ε_{core}	4	4	2.8
FEXT Peak (mV)	-9.97	-4.96	-4.96

2.3.2. Stripline with Asymmetric Prepreg and Core Dimension. Another example is the stripline with asymmetrical prepreg and core dimensions. The trace is not in the middle between the reference plane and the dielectric constant is different for different layers. The structure is more frequently used in fabricated PCB design.

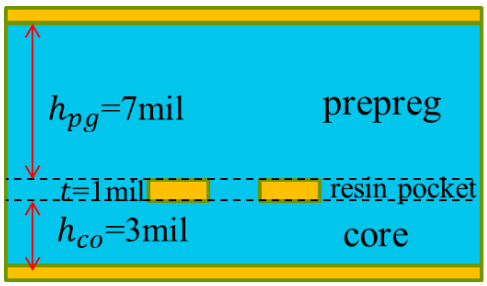


Figure 6. Cross-section geometry of two coupled stripline traces. The trace width of the trace is 7.2mil. The spacing between the traces is 10mil.

The cross-section geometry is shown in Figure 6. In this case, the thickness of the prepreg layer is 7mil, while the thickness of the core layer is 3mil. The dielectric permittivity in the core is 3.5. The dielectric permittivity in the resin pocket is 2.8. In fabricated multi-layer PCB, due to the different glass fiber weave/content in prepreg and

core, prepreg melting during lamination, and resin properties tolerances, etc [4-6]. The dielectric permittivity in the prepreg and core layer are different in this example, where the dielectric permittivity prepreg is defined as 3.5, 4.5, and 5.5 for different series of cases.

Table 3 lists the FEXT magnitude of the different cases. For the series of Case a, Case b, and Case c, the FEXT level of Case x.1 is approximately equal to the sum of Case x.2 and Case x.3 (x refers to a, b, or c), which validates the superposition method for asymmetric stack up as well.

For this asymmetrical example, the FEXT performance cannot be simply predicted from the 3L-IDL model. With the help of the superposition method, the problem is decomposed into two 2L-IDL cases and the total FEXT level can be predicted. In (9) and (10), it can be noted that $\Delta_{LC}$is not only related to the difference of the dielectric material but also the capacitance. Then, (9) and (10) can be modified as:

$$\Delta_{LC2}=\frac{10C_g^a}{9\Delta C^a}\cdot\left\{\left(\varepsilon_{r,pg}-\varepsilon_{r,rp}\right)\cdot\left(\left[C_{t,pg}^a\cdot\left(C_{g,co}^a+C_{g,rp}^a\right)-C_{t,co}^aC_{g,pg}^a\right]\right)\right\} \quad (14)$$

$$\Delta_{LC3}=\frac{10C_g^a}{9\Delta C^a}\cdot\left\{\left(\varepsilon_{r,co}-\varepsilon_{r,rp}\right)\cdot\left[C_{t,co}^a\cdot\left(C_{g,pg}^a+C_{g,rp}^a\right)-C_{t,pg}^aC_{g,co}^a\right]\right\} \quad (15)$$

In this example, the thickness of the prepreg layer is larger than that of the core layer. As the result, $C_{t,pg}^a$ will be smaller than $C_{t,co}^a$. Considering that the $C_{g,pg}^a+C_{g,rp}^a$ should be larger than $C_{g,co}^a$, Δ_{LC3} is expected to be a positive value. The value of the capacitance term in Δ_{LC2} is expected to be much smaller than that in Δ_{LC3}.

Table 3. Peak value of the FEXT waveform with the geometry in Figure 6

(a)

	Case a.1	Case a.2	Case a.3
ε_{preg}	3.5	2.8	3.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-3.65	-6.50	2.95

(b)

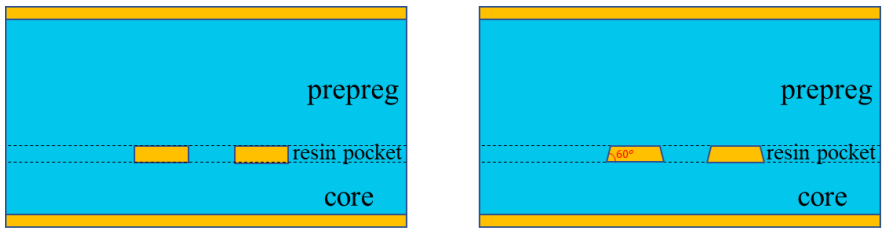
	Case b.1	Case b.2	Case b.3
ε_{preg}	4.5	2.8	4.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-0.30	-6.50	6.69

(c)

	Case a.1	Case a.2	Case a.3
ε_{preg}	5.5	2.8	5.5
ε_{resin}	2.8	2.8	2.8
ε_{core}	3.5	3.5	2.8
FEXT Peak (mV)	-3.91	-6.50	10.63

In all the cases, the traces are assumed to be rectangular. While in reality, due to the time-controlled etching process in the PCB fabrication, the copper area is actually dissolved from the top down, which results in the trapezoid trace shape [19].

Comparisons between the rectangle trace and trapezoid trace are shown in Table 4. The base angle of the trapezoid shape is 60^o. The average of the upper and lower edge of the trapezoid is the same as the width of the rectangle. The geometry of the Symmetric Case is the same as Figure 4, while the geometry of the asymmetric case is the same as Figure 6. The error caused by the approximation on the trace shape is within 6%.



(a) (b)

Figure 7. Cross-section geometry of two coupled stripline traces. The trace width of the trace is 7.2mil. The spacing between the traces is 10mil.

Table 4. Peak value of the FEXT waveform

	Symmetric Case	Asymmetric Case
ε_{preg}	4	3.5
ε_{resin}	2.8	2.8
ε_{core}	4	3.5
FEXT Peak of rectangle traces (mV)	-9.97	-3.65
FEXT Peak of trapezoid traces (mV)	-10.01	-3.87

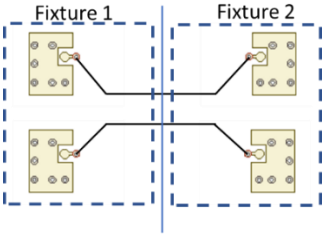
3. DIELECTRIC PERMITTIVITY EXTRACTION ALGORITHM

In this section, the ε_r of IDLs extraction methodology using measured S-parameters of Delta-L and EUL structures within the same layer of a PCB is introduced. A two-parameter optimization problem is formulated based on the investigations of the sensitivity of FEXT peak voltage and phase.

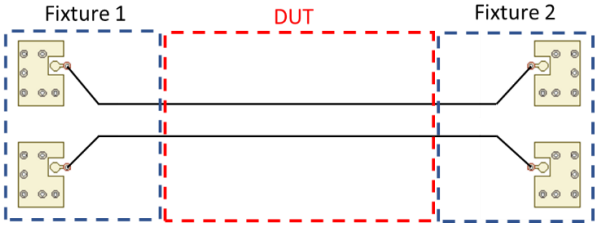
3.1. MEASUREMENT SETUP

To investigate the FEXT and insertion loss of the PCB, boards with multiple striplines with EUL structure and Delta-L lines are fabricated. We use the Delta-L and EUL structures since both of them are readily available in a typical PCB electrical characterization board, Delta-L is used to characterize the insertion loss of differential interconnect (such as PCIe, etc.), and EUL is used to characterize the crosstalk of single-ended interconnect (such as DDR, etc.).

The Delta-L structures are differential striplines with different lengths, as shown in Figure 8. The “Thru” is with a shorter length, and the “Total” is with a longer length. The test fixtures consist of connectors, pads, vias, transitions, etc. Using IPC test method 2.5.5.14, the insertion loss of “DUT” is obtained. The measurement is performed with D-probes [20]. Compared to the traditional measurement methods based on SMA connectors, more efficient tests can be performed with smaller landing space for the high-volume PCB manufacturing validation.



(a) Thru



(b) Total

Figure 8. Conceptual illustration of a Delta-L structure.

The striplines with EUL structures are illustrated in Figure 9. The device under test (DUT) is a pair of coupled single-ended striplines, and the striplines are intentionally extended. The extended parts are unterminated (open) without any coupling to the other pair. With a matched long transmission line termination, the impact from FEXT due to mismatched termination can be gated in the time domain [9]. Additionally, only half the test ports are needed, therefore it eliminates the requirement for costly test equipment with additional ports.

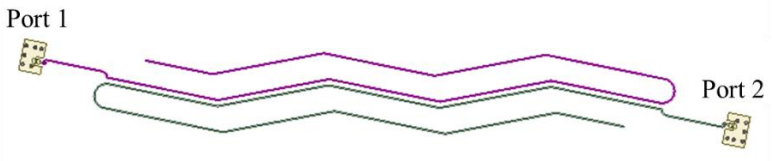


Figure 9. Conceptual illustration of striplines with EUL structures.

The S-parameters measurement is performed using Keysight N5244A 4-port Network Analyzer. Two 3-inch striplines with EUL structures are measured. The amplitude of the incident step signal on the aggressor line is set to +1V. The rise time is 50ps and the widow width is 1.5ns. In this study, the Intel IMLC tool [21] is used for fast calculation and batch mode. The Delta-L and EUL structures within the same layer of a PCB are assumed to share the same ε_r of each IDL.

3.2. EXTRACTION METHODOLOGY

In [22], a set of simulations are performed to investigate the FEXT's sensitivity to $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ of the 2L-IDL modeled. The difference of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ has an obvious impact on the absolute value of $v_{p,odd}$ and $v_{p,even}$, leading to shorter or longer modal time-of-flight, which in turn affects the FEXT level. On the other hand, the differential mode per-unit-length (PUL) phase (β_{dd}) is quite sensitive to the sum of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$.

As of the 3L-IDL model, the resin pocket layer is only filled with resin. The dielectric constant of the resin is provided by the PCB vendor as 2.8 in this test coupon. With the superposition method, the FEXT peak value can still be expressed as a function of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$:

$$v_{fext}{}' = \mathrm{K}_{FEXT}(\varepsilon_{r,pg}, \varepsilon_{r,co}) \tag{16}$$

According to [14], the differential propagation constant of a transmission line is related to the PUL RLGC parameters for differential mode:

$$\gamma_{dd} = \sqrt{(R_{dd} + j\omega L_{dd})(G_{dd} + j\omega C_{dd})} \tag{17}$$

Since all practical lines are low-loss, that is $R \ll \omega L$ and $G \ll \omega C$, (3) can be approximated using the Taylor series expansion, and the phase (β_{dd}) can be estimated [23, (2-85b)] as:

$$\beta_{dd} = \text{imag}(\gamma_{dd}) \approx \omega \cdot \sqrt{L_{dd} \cdot C_{dd}} \tag{18}$$

Since C_{dd} is contributed by the capacitance components distributed in prepreg ($C_{dd,pg}$), resin pocket ($C_{dd,rp}$), and core ($C_{dd,co}$) for differential mode. For a stripline, the capacitances in prepreg and core are in parallel [17]:

$$C_{dd} = C_{dd,pg} + C_{dd,rp} + C_{dd,co} \tag{19}$$

Thus, the β_{dd} should have a strong sensitivity to the sum of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$, since $C_{dd,pg}$ and $C_{dd,co}$ in (5) are scaled by $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$.

Then, the modeled β_{dd} is expressed as ${\beta_{dd}}'$ and ${v_{fext}}'$:

$${\beta_{dd}}' = \text{K}_\beta\left(\varepsilon_{r,pg}, \varepsilon_{r,co}\right) \tag{20}$$

To extract the inhomogeneous dielectric permittivity ($\varepsilon_{r,pg}$, $\varepsilon_{r,co}$), a target function (T) is generated to evaluate the estimate of the error between the modeled result to the measured result. The function is defined with root mean squared error (RMSE), which is a general-purpose error metric for numerical predictions as:

$$T = \sqrt{\left({v_{fext}}' - v_{fext0}\right)^2 + \left[\left(\frac{{\beta_{dd}}'}{\omega} - \frac{\beta_{dd0}}{\omega}\right) \cdot 10^8\right]^2} \tag{21}$$

Here, the unit for ${v_{fext}}' - v_{fext0}$ is mV, which is usually in the order of 10^{-1} while the ${\beta_{dd}}'/\omega - \beta_{dd0}/\omega$ is in the order of 10^{-9}. As the result, '1e8' is introduced for normalization -so that $({\beta_{dd}}'/\omega - \beta_{dd0}/\omega)$ and $\left({v_{fext}}' - v_{fext0}\right)$ can have a comparable impact on the target function (T).

The entire extraction procedure is illustrated in the flow chart in Figure 10. The EUL S-parameters provide the measured FEXT level and the Delta-L S-parameters after de-embedding provides β_{dd}. With the cross-section geometry, the simulation model is created by a 2D solver (Intel IMLC is the 2D tool we used for this study).

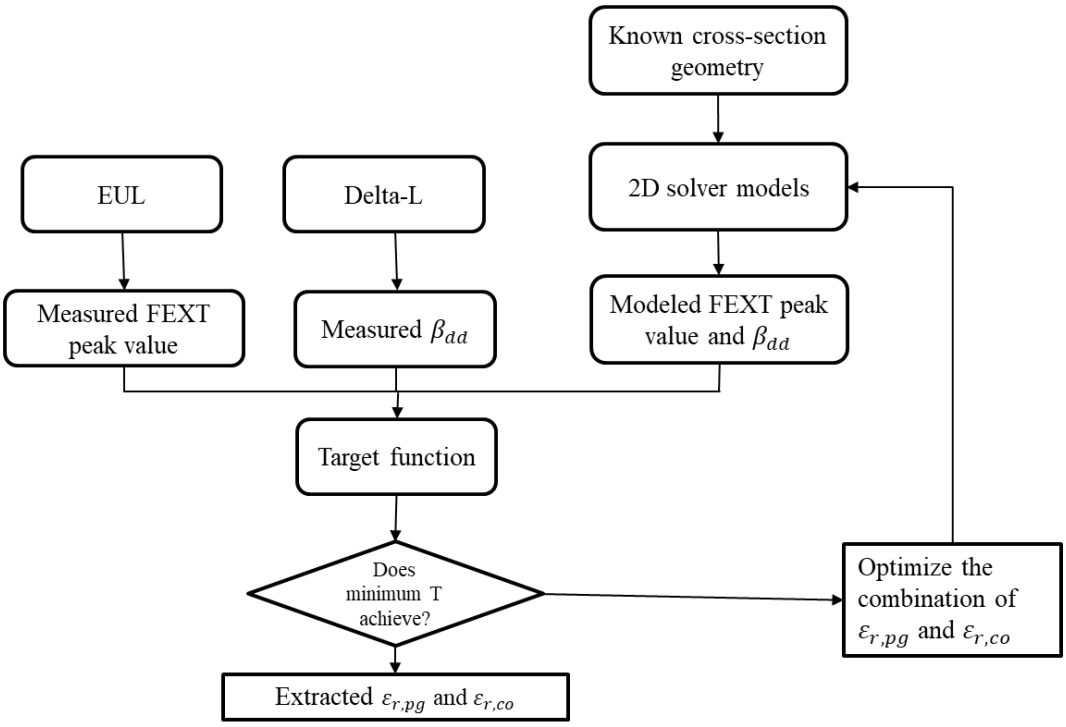


Figure 10. The flow chart of the proposed $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ extraction method

Table 5 shows the comparison of the extraction result with a different model. Case 1 and Case 2 are the striplines on the same layer of the same board but designed with different spacing. The extraction results of the $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ are expected to be quite close. Compared with the 3L-IDL model result, the difference of the 2L-IDL extraction results between Case 1 and Case 2 are larger. The 3L-IDL model with resin pocket model is more accurate to model the stripline behavior.

Table 5. Extraction result comparison of 2L-IDL model and 3L-IDL model.

	Spacing [mil]	2-IDL$\boldsymbol{\varepsilon_{r,pg}}$	2-IDL$\boldsymbol{\varepsilon_{r,co}}$	3-IDL$\boldsymbol{\varepsilon_{r,pg}}$	3-IDL$\boldsymbol{\varepsilon_{r,co}}$
Case 1	6.3	3.65	4.28	4.68	4.04
Case 2	7.3	3.77	4.22	4.65	4.04

Another validation is shown in Figure 11, which indicates the FEXT of the wide spacing model with narrow spacing extracted $\boldsymbol{\varepsilon_r}$, compared with the result from the measured S-parameters. As the spacing increases, the trace will see more glass and less resin ineffective the prepreg layer of the 2L-IDL model, which results in a larger difference between the modeled result and the measured result. Meanwhile, the 3L-IDL model can improve the accuracy of the FEXT prediction.

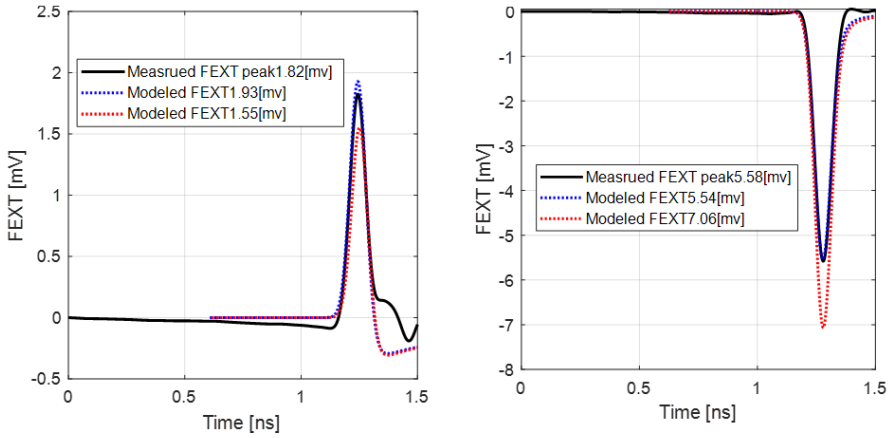
3.3. EXTRACTION ALGORISM OPTIMIZATION

The initial extraction procedure used the nominal value from the PCB vendor as the starting value, which is usually the effective value of the typical stripline model with 2 IDLs. As a result, the procedure requires a large amount of simulations

when applying gradient descent optimization. The superposition method can help to simplify the optimization procedure and reduce extraction time. The FEXT level of the decomposed Case 2 and Case 3 is simplified from Eq. (9) and (10) as:

$$FEXT_{case2} = \lambda_2(\varepsilon_{r,pg} - \varepsilon_{r,rp}) \tag{22}$$

$$FEXT_{case3} = \lambda_3(\varepsilon_{r,co} - \varepsilon_{r,rp}) \tag{23}$$



(a) (b)

Figure 11. The FEXT of the wide spacing model with narrow spacing extracted DK. (a) Example 1; (b) Example 2. Black solid lines: FEXT result from the measured S-parameters; Blue dash lines: FEXT result from the simulated S-parameters of 3-IDL model; Red dash lines: FEXT result from the simulated S-parameters of 3L-IDL model.

Here λ_2 and λ_3 are constant when the geometry is fixed. λ_2 and λ_3 can be achieved from the 2D solver with known geometry. The superposition method can approximate the FEXT of the stripline with IDLs. Accordingly, the FEXT level of the 3L-IDL stripline is:

$$FEXT_{case1} = FEXT_{case2} + FEXT_{case3}$$
$$= \lambda_2(\varepsilon_{r,pg} - \varepsilon_{r,rp}) + \lambda_3\,(\varepsilon_{r,co} - \varepsilon_{r,rp}) \quad (24)$$

The FEXT level can be expressed with $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ with known $\varepsilon_{r,rp}$ and two simulation cases. Since the definition of the core layers of the 2L-IDL model and 3L-IDL model remain the same, the nominate value of the core layer can be used as the initial value of $\varepsilon_{r,co}$. The initial value of $\varepsilon_{r,pg}$ can be solved from (20). Besides, the polarity of the λ_2 and λ_3 helps determine how to adjust the optimization of the combination of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$.

As an example, a pair of Delta-L and EUL structures is under test. The cross-sectional geometry is shown in Table 6.

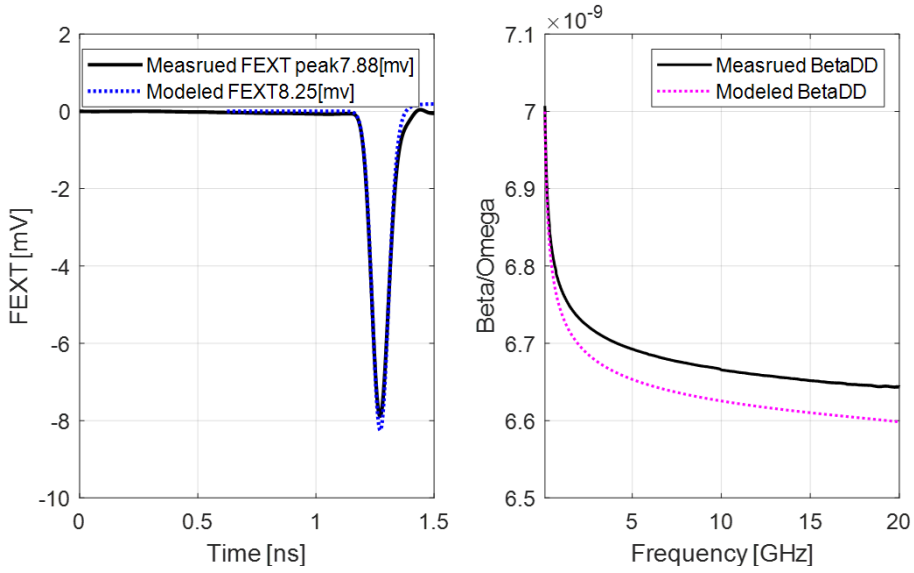
Table 6. Cross-sectional geometry of the Delta-L and EUL structure

Parameter	[mil]
Prepreg thickness	8.9
Core thickness	4.0
Trace thickness	1.2
Delta-L trace spacing	12.5
Delta-L trace width	5.4
EUL trace spacing	6.3
EUL trace width	7.1

The FEXT peak value of Case 2 is 26.38mV; the FEXT peak value of Case 3 is -35.9mV. From (18) and (19), the λ_2 is solved to be 15.51 and λ_3 is solved to be -29.92. With $\varepsilon_{r,rp}$ assigned to be 2.8 in (20), the FEXT level of the 3L-IDL model is:

$$FEXT_{case1} = 15.51\varepsilon_{r,pg} - 29.92 \cdot \varepsilon_{r,\mathrm{co}} + 40.35 \quad (25)$$

From the EUL measurement, the peak value of the measured FEXT is -7.88mV. The nominate $\varepsilon_{r,co}$ provided by the vendor is 4.0. Then the initial $\varepsilon_{r,pg}$ is solved to be 4.61.



(a) (b)

Figure 12. Comparison between measured result and modeled result with the initial value. (a) FEXT waveform; (b) β_{dd} waveform.

The simulation result of the initial value is shown in Figure 12. Modeled $\beta_{dd}$is lower than the measured result. Since the β_{dd} is related to the sum of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$, $\varepsilon_{r,pg}$ or $\varepsilon_{r,co}$ should be increased to match the measurement result. The peak value of modeled FEXT is lower than the measured result. According to (21), to increase the FEXT value, $\varepsilon_{r,pg}$ should be increased or $\varepsilon_{r,co}$ should be decreased. Therefore, considering both the FEXT and β_{dd} result, the $\varepsilon_{r,pg}$ needs to be increased. Figure 13 shows the comparison between the modeled result and the measured result after the optimization when $\varepsilon_{r,pg}$ is defined as 4.7. The modeled result matched the measured result much better. In addition to IMLC simulation results, we also performed simulation with Q2D tool commercially available. Q2D simulation result with the same material properties also validates the extraction result as shown in Figure 13.

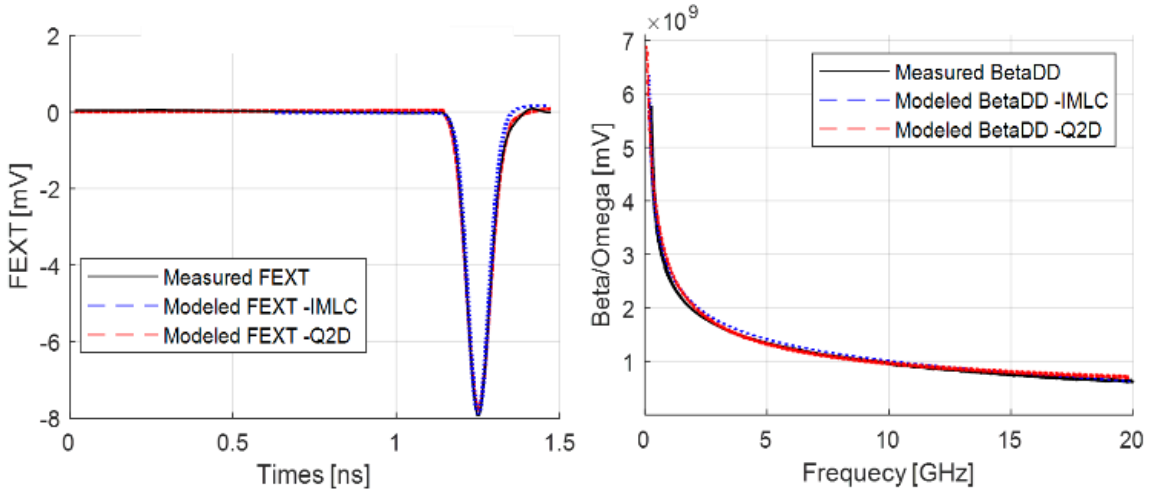


Figure 13. Comparison between measured result and modeled result with optimized value. (a) FEXT waveform; (b) β_{dd} waveform.

4. FEXT PREDICTION FOR STRIPLINE WITH IDLS

In practice, to improve the signal integrity performance in high-speed systems, the FEXT needs to be mitigated. The design of the stripline can be improved with the help of modeling various combinations of materials and geometry.

A method to predict the FEXT polarity and peak level of the stripline caused by the inhomogeneity with an analytical expression is proposed. The prediction only needs the calculation by analytical expressions instead of with assistance from the 2D or 3D solvers. Compared to time-consuming full-wave simulation, the proposed method is time-efficient when optimizing a large number of designs with different geometry.

Analytical expression of the FEXT peak level is derived based on the capacitance decomposing. For the model with multiple IDLs including resin pocket, the FEXT can be

expressed with the superposition of two cases with only 2 IDLs. The FEXT can be simplified as:

$$FEXT{\sim}\Delta LC \approx K\frac{C_{21}^{a}}{(C_{11}^{a})^{2}-(C_{21}^{a})^{2}}\cdot\left(\varepsilon_{r,pg}-\varepsilon_{r,co}\right)\cdot\left(\frac{1}{h_{pg}}-\frac{1}{h_{co}}\right) \tag{26}$$

For the typical stripline model with 2 IDLs with the symmetric structure in which the thickness of the core layer and the prepreg layer is the same as h, [18, Eq. (8.60-8.62)] proposed expression for the capacitance of air-filled case:

$$C_{m}^{a}=\frac{1}{cZ_{m}} \tag{27}$$

$$Z_{m}=\frac{30\pi}{\sqrt{\varepsilon_{r}}}\frac{K(k_{m}')}{K(k_{m})} \tag{28}$$

$$\frac{K(k_{m}')}{K(k_{m})}=\begin{cases}\dfrac{\ln\left(2\frac{1+\sqrt{k_{m}'}}{1-\sqrt{k_{m}'}}\right)}{\pi} & \text{if } 0\le k<\frac{1}{\sqrt{2}}\\ \dfrac{\pi}{\ln\left(2\frac{1+\sqrt{k_{m}'}}{1-\sqrt{k_{m}'}}\right)} & \text{if } \frac{1}{\sqrt{2}}\le k<1\end{cases} \tag{29}$$

$$\begin{cases}k_{o}=\tanh\left(\frac{\pi w}{4h}\right)\coth\left[\frac{\pi}{4}\left(\frac{w+s}{h}\right)\right], & k_{o}'=\sqrt{1-k_{o}^{2}}\\ k_{e}=\tanh\left(\frac{\pi w}{4h}\right)\tanh\left[\frac{\pi}{4}\left(\frac{w+s}{h}\right)\right], & k_{e}'=\sqrt{1-k_{e}^{2}}\end{cases} \tag{30}$$

Here, m represents even or odd mode. w is the trace width. s is the spacing between the traces.

The mutual capacitance and self-capacitance in (22) are expressed with the modal capacitance as:

$$\begin{cases}C_{11h}^{a}=C_{e}^{a}\\ C_{12h}^{a}=0.5(C_{o}^{a}-C_{e}^{a})\end{cases} \tag{31}$$

For the asymmetric structure in which the thickness of the core layer is h_{co} and the prepreg layer is h_{pg}, the capacitance is approximately expressed as:

$$\begin{cases} C_{11}^{a} = 0.5(C_{11\,h_{co}}^{a} + C_{11\,h_{pg}}^{a}) \\ C_{12}^{a} = 0.5(C_{12\,h_{co}}^{a} + C_{12\,h_{pg}}^{a}) \end{cases} \tag{32}$$

Here $C_{11\,h_{co}}^{a}$, $C_{11\,h_{pg}}^{a}$, $C_{12\,h_{co}}^{a}$, $C_{12\,h_{pg}}^{a}$ are the capacitance of the symmetric air-filled structure when the $h = h_{pg}$ or $h = h_{co}$.

Then the FEXT level of the stripline can be expressed as

$$FEXT_{2-IDL} = Kf'(\varepsilon_{co}, \varepsilon_{pg}, h_{co}, h_{pg}, s, w, t) \tag{33}$$

f' is solved from the above Eq. (23-29). K is decided from the simulation result based on the geometry in coupon design.

For the 3L-IDL stripline, the FEXT level is predicted with the superposition method as:

$$FEXT_{3-IDL} = FEXT_{2-IDL\,case2} + FEXT_{2-IDL\,case3} \tag{34}$$

As demonstrated in Figure 3, Case 2 is the same structure as the typical stripline, which considers the resin pocket layer and the prepreg layer filled with the homogenous material. While in Case 3, the core layer and the resin pocket layer are filled with the same material, which means the thickness of the core layer should be increased by t and the thickness of the equivalent prepreg layer used for the 2L-IDL model should be decreased by t. Therefore, the FEXT expression for the decomposed cases is

$$FEXT_{case2} = Kf'(\varepsilon_{co}, \varepsilon_{rp}, h_{co}, h_{pg}, s, w, t) \tag{35}$$

$$FEXT_{case3} = Kf'(\varepsilon_{rp}, \varepsilon_{co}, (h_{co} + t), (h_{pg} - t), s, w, t) \tag{36}$$

With Eq. (29) and (30), the polarity and the FEXT level of the stripline with 2 IDLs and 3 IDLs can be predicted. Based on over 351 measured cases with a different set of boards from 3 different vendors, the correct rate for the polarity prediction of the 2L-IDL model is 99.43% and that of the 3L-IDL model is 98.58%.

For the FEXT peak level prediction, the passing criteria are defined as the following: When the absolute FEXT peak value of the measurement is larger than 2mV if the difference prediction and the measurement is less than 30%, the case is passed.; when the absolute FEXT peak value is less than 2mV if the predicted FEXT level is less than 2mV and polarity of the is correctly predicted, the case is passed. The passing ratio of the 2-IDL model is 90.03% and that of the 3-layer model: 80.63%.

The prediction error is introduced from the following process: the analytical expressions for the capacitance and inductance; the assumption for the superposition method; the inaccuracy of the geometry information.

With the prediction expression for the stripline, the following design guidelines are summarized to mitigate the FEXT.

4.1.1. The Thickness of the Core and Prepreg Layer Needs Identical, if not as Similar as Possible. Table 7 shows 3 cases of measurement with different core and prepreg thicknesses, while with the same trace spacing and manufactured with the same material by the same vendor. According to Eq. (22), when the thickness of the core and prepreg are designed to be closer, the FEXT level will be smaller. The measured result matches the expectation.

4.1.2. The Spacing Between the Traces Should be Maximized. The following shows two cases of measurement in the same layer of the same board with different spacing. The FEXT level of the larger spacing case is smaller.

4.1.3. Using the 2L-IDL Model, a Combination of Core and Prepreg Should be Chosen with the Least Difference Between the Two Dielectric Constants. Table 9 demonstrates 3 cases of measurement with different boards while with the same

geometry. According to Eq. (22), when the DK of core and prepreg are designed to be closer, the FEXT level will be smaller. The measured result matches the expectation as expected.

Table 7. FEXT comparison with different thicknesses of core and prepreg

	$\boldsymbol{h_{co}}$ [mil]	$\boldsymbol{h_{pg}}$ [mil]	FEXT [mV]
Structure #1	3	7	1.68
Structure #2	4	7	0.98
Structure #3	5	6	-0.15

Table 8. Measured FEXT comparison with different spacing of test coupon

	Spacing [mil]	FEXT [mV]
Set #1	4.5	-7.68
	6.0	-4.84
	9.0	-2.90
Set #2	7.2	-0.96
	9.3	-0.47
	18.0	-0.15
	20.3	-0.03
	21.0	-0.02

Table 9. FEXT comparison with DK of core and prepreg

	$\boldsymbol{\varepsilon_{preg}}$	$\boldsymbol{\varepsilon_{core}}$	FEXT [mV]
Board #1	4.08	3.46	-3.74
Board #2	3.96	3.87	-0.55

4.1.4. Using the 3L-IDL model, Core and Prepreg Combinations Should be Chosen to Match the DK Value to Minimize FEXT, Using the Proposed Analytical Model, as Much as Possible. To get the optimized design for the dielectric material, the expression for the FEXT of a certain stripline can be generated and the permittivity can be solved. The process is as follows:

With known geometry information and the initial value of the permittivity, solve the FEXT level for Case 2 and Case 3 by a 2D solver or Equ. (23-30)

Generate the FEXT expression of 3L-IDL with the superposition method

Solve the equation when the FEXT is equal to zero and find the best solution for the permittivity

For example, the structure in Figure 6 is designed with $\varepsilon_{r,rp}$=2.8 and $\varepsilon_{r,co} = 3.5$. The $\varepsilon_{r,pg}$ need to be determined. can be designed for minimum FEXT. The initial value for $\varepsilon_{r,pg}$ is 3.5. The FEXT for Case 2 is solved as -6.5mV and the FEXT for Case 2 is solved as 2.95mV. Then the FEXT can be predicted as:

$$FEXT_{predict} = 4.2\left(\varepsilon_{r,pg} - \varepsilon_{r,rp}\right) - 9.3\left(\varepsilon_{r,co} - \varepsilon_{r,rp}\right) \quad (37)$$

Then the $\varepsilon_{r,pg}$ is solved as 4.35 when the $FEXT_{predict}$ is 0. The simulated FEXT is -0.3mV. The simulated best solution of $\varepsilon_{r,pg}$ is 4.5 The error between the solution of the prediction and the simulation value is 3%. Only with the superposition method and analytical prediction, the best minimizes the FEXT can be achieved.

5. CONCLUSIONS

In this paper, the stripline model of 3L-IDL is proposed with improved FEXT prediction accuracy compared to the 2L-IDL model by separating the resin pocket from the traditional stripline model and using the superposition principle. A summary table is shown in Table 10.

To better model the FEXT, the ε_r of IDLs is extracted using measured S-parameters of Delta-L and EUL structures. The extraction algorism is optimized with the superposition principle. Moreover, the prediction for the FEXT polarity and magnitude of the stripline caused by the inhomogeneity can be predicted using the proposed analytical model and is verified with the measurement data. With the stack up information, the polarity can be predicted with over 98% accuracy and the FEXT level can be predicted with over 80% accuracy. This paper also provides a design guide to minimize FEXT induced by IDLs for PCB material designers.

Table 10. Summary of the comparison between 2L-IDL and 3L-IDL model

	Pros	Cons
2L-IDL Model	Easy to control the permittivity in the manufacturing procedure for material selection	Inaccurate to modeling and predicting the FEXT, especially when the trace spacing is varied.
3L-IDL Model	1. Accurate characterization for the dielectric property 2. Accurate modeling and prediction of the FEXT 3. Effective FEXT mitigation for the inhomogeneous design can be generated.	More complicated modeling and extraction of material property process. Requires the superposition method for the FEXT analysis

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III. AN EMPIRICAL MODELING OF FAR-END CROSSTALK AND INSERTION LOSS IN MICROSTRIP LINES

Yuanzhuo Liu[#], Shaohui Yong[#], Yuandong Guo[#], Jiayi He[#], Chaofeng Li[#], Xiaoning Ye*, Jun Fan[#], Victor Khilkevich[#], DongHyun Kim[#]

[#]Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO, USA

*Datacenter Group, Intel Corporation, Portland, Oregon, USA

ABSTRACT

The difference in the dielectric permittivity of the different dielectric layers (including air) surrounding the microstrip is one of the major contributors to the far-end crosstalk (FEXT) in microstrip lines. The dielectric of the microstrip in printed circuit boards (PCBs) fabrication usually consists of two layers: the solder mask layer and the substrate layer. The characterization of the relative permittivity (ε_r), dielectric dissipation factor (tanδ) for the dielectric layers of the microstrip are important parameters for board-level electronic system designs. In addition, the foil surface roughness cannot be ignored for the conductor loss modeling. In this work, an extraction method with high accuracy is proposed to characterize the dielectric material and foil surface roughness properties from the measured S-parameters with known cross-sectional geometry up to 20GHz. With the extracted properties, the FEXT and insertion loss of the microstrip can be estimated more accurately, providing design guidelines for PCB design and the material selection of the microstrip.

Keywords: Far-end Crosstalk (FEXT), Delta-L, Extended unterminated line (EUL), Dielectric material characterization.

1. INTRODUCTION

The microstrip line is a commonly used transmission line structure in RF and microwave designs for its low fabrication cost and high layer utilization. However, compared with striplines, microstrip lines suffer from relatively higher FEXT compared to stripline because of the air dielectric which surrounds the microstrip line [1-3]. Hence, it is important to accurately control and predict the FEXT of the microstrip. Therefore, an accurate estimation of the parameters of the microstrip line is critical for circuit performance modeling, including the loss and the FEXT.

Many techniques were developed to characterize the material properties of PCBs, such as the new rapid plane solver [4], the short-pulse propagation technique based on time-domain reflectometry measurements [5], and the ring resonator method [6]. However, these methods require a special design or additional measurement to extract the dielectric material properties. S-parameters, which describe the electrical behavior of electrical networks, are widely used in electronics, communication systems design, and microwave engineering. Meanwhile, the material properties may vary from the raw material after fabrication. Therefore, the extraction based on S-parameters measured on fabricated microstrip is more accurate and practical in actual design.

A new approach to the extraction process is proposed in the previous paper [7]. The per-unit-length inductance and capacitance of the air-filled line are obtained using an

accurate 2D solution of the transmission line cross-section, and the approximated analytical expression is used only to relate the effective permittivity of the transmission line to the actual permittivity of the dielectric layer. However, this proposed method is limited to a simplified microstrip structure as shown in Figure 1, without considering the effects of the solder mask.

The dielectric of the microstrip in printed circuit boards (PCBs) fabrication usually consists of two layers: the solder mask layer and the substrate layer. [8] and [9] proves that the inhomogeneity between the dielectric layers is a critical reason for the FEXT. In practice, the permittivity of the solder mask is generally higher than that of the substrate [2]. As a result, aside from the inhomogeneity between the air and the substrate in the simplified microstrip structure, the solder mask layer will help reduce the FEXT by introducing additional (with opposite effects on crosstalk polarity) inhomogeneity between the dielectric layers [2,3]. Previous models use only provide one effective dielectric constant value for surrounding dielectric layers, neglecting the impact of a thin solder mask between the air dielectric layer and substrate dielectric layer. As the result, an accurate estimation of the permittivity of each dielectric layer is critical for FEXT modeling. The comparison between the existing microstrip characterization methods to the proposed method is shown in Table 1.

The extended unterminated line (EUL) structure was proposed in [10] and [11] to achieve convenient and accurate FEXT measurements. It is widely used for high-volume PCB tests because the EUL structure reduces the required ports by half while eliminating the requirement for expensive test equipment with additional ports. In addition, the structure is proven to eliminate the impact from FEXT due to mismatched terminals in

the time domain [10]. Delta-L structures are differential transmission lines with different lengths [12]. With the de-embedding procedure [13-14], the vias and fixture effect can be removed so that S-parameters of the transmission line is obtained. To accurately characterize the inhomogeneous dielectric material of microstrip, the dielectric permittivity (ε_r) is extracted for solder mask and substrate using measured S-parameters and cross-sectional geometry of both Delta-L and EUL structures.

Table 1. Summary of the microstrip characterization methods.

Method	**Cons**	**Pros**
Rapid Plane Solver	Requires special test fixture design and/or multiple measurements	Extraction of the pure dielectric properties without de-embedding error
Short-pulse Propagation		
Ring Resonator		
Insertion Loss Measurement only	Only effective permittivity dielectric substrate can be extracted, resulting in low FEXT prediction accuracy	Minimal Number of Measurement
Insertion Loss and FEXT Measurement (Proposed)	Requires one additional EUL structure for accurate FEXT measurement	Permittivity of the substrate and solder mask layer can be separated from S-parameter measurement

To accurately model the loss, the dielectric dissipation factor and the surface roughness are critical factors. To model additional conductor loss due to foil surface roughness various empirical or physical models have been brought up to provide surface roughness correction factors for the per-unit-Length (PUL) resistance assuming certain roughness of foil conductors. The dielectric dissipation factor can be also extracted with the measured S-parameters. With all the extracted parameters: the dielectric permittivity (ε_r) of the dielectric layers, the dissipation factor, and the foil surface roughness the performance characteristics like the FEXT and the loss of the microstrip can be estimated.

As part of the paper organization, in Section 2, the algorithm of the ε_r extraction for different layers is introduced. Both the simplified microstrip that only contains the substrate layer and the practical microstrip model with solder mask layer is extracted. Section 3 provides the extraction of the foil surface roughness and the correction factor for the resistance caused by that. Section 4 shows the dissipation factor extraction for the insertion loss modeling. In section 5, the design guideline to mitigate the FEXT of the microstrip is provided.

2. PERMITTIVITY EXTRACTION METHODOLOGY

2.1. HOMOGENEOUS MODEL EXTRACTION

The simplified cross-sectional geometry of the microstrip line is shown in Figure 1. A conductor of thickness t and width w is fabricated on a dielectric substrate of thickness h above a ground plane The dielectric constant of the homogeneous medium

that equivalently replaces the air and dielectric regions of the microstrip is defined as the effective permittivity (dielectric constant) [15].

The propagation constant γ of a single-ended transmission line can be expressed through the per-unit-length (PUL) parameters as:

$$\gamma = \sqrt{(R + j\omega L)(G + jwC)} \tag{1}$$

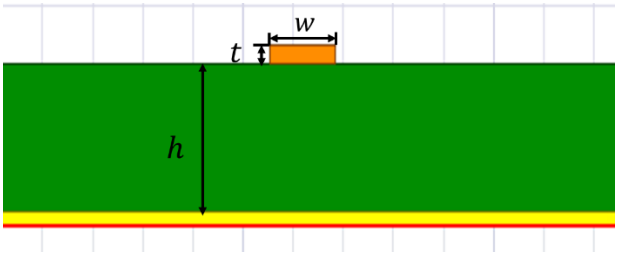


Figure 1. The cross-sectional geometry of a simplified microstrip

Here R, L, G, and C represent the per-unit length resistance, inductance, conductance, and capacitance of the transmission line. For practical low-loss transmission lines, the following conditions are true: $R \ll j\omega L$ and $G \ll j\omega C$. Using Taylor series expansion, the attenuation factor α and phase constant β, in this case, can be approximated as [15]:

$$\alpha = \text{real}(\gamma) \approx \frac{1}{2} R \sqrt{\frac{C}{L}} + \frac{1}{2} G \sqrt{\frac{L}{C}} \tag{2}$$

$$\beta = \text{imag}(\gamma) \approx \omega\sqrt{CL} \tag{3}$$

Due to the definition of the effective dielectric constant, the capacitance C can be calculated by scaling the capacitance of the air-filled transmission line C_{air} (i.e. the capacitance calculated from the geometry only) by the effective dielectric relative permittivity (ε_{r_eff}) in (4.36) of [16]:

$$C = C_{air}\varepsilon_{r\_eff} \tag{4}$$

Considering that the inductance L is not affected by the dielectric material (its relative permeability is assumed to be equal to 1), the inductance of the air-filled transmission line L_{air} is the same as L. Then the phase constant β can be expressed as:

$$\beta \approx \omega\sqrt{C_{air}\varepsilon_{r_{eff}}L_{air}} \tag{5}$$

If the cross-sectional dimensions of the transmission line are known, C_{air} and L_{air} can be calculated by solving the 2-D cross-sectional problem using an appropriate solver (Ansys Q2D in our case).

When the S-parameters of the line are measured with the impedance of the ports perfectly matched to the characteristic impedance of the line, the phase constant can be expressed as:

$$\beta = \left|\frac{\arg(S_{21})}{l}\right| \tag{6}$$

In the practical measurement by a Vector Network Analyzer (VNA), the de-embedding procedure (such as TRL, 2X-Thru, etc.) is essential to eliminate the impedance mismatch.

In [17], Inder Bahl proposed an analytical expression for the effective dielectric constant of a microstrip line as:

$$\varepsilon_{r\_eff} = \begin{cases} \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} + 0.04\left(1-\frac{w}{h}\right)^2\right] - \frac{\varepsilon_r-1}{4.6}\frac{\frac{t}{h}}{\sqrt{\frac{w}{h}}} & \frac{w}{h} \le 1 \\ \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} - \frac{\varepsilon_r-1}{4.6}\frac{\frac{t}{h}}{\sqrt{\frac{w}{h}}} & \frac{w}{h} > 1 \end{cases} \quad (7)$$

By inverting (7) and combining it with (5) and (6) the dielectric constant of the substrate ε_r can be extracted from the S-parameter and the cross-sectional geometry. The final formula of ε_r expressed with measured S-parameter and 2-D solver result is:

$$\varepsilon_r = \begin{cases} \frac{\frac{2}{C_{air}L_{air}}\left(\frac{\arg(S_{21})}{l\omega}\right)^2 - 2}{1+\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} + 0.04\left(1-\frac{w}{h}\right)^2 - \frac{\frac{t}{h}}{2.3\sqrt{\frac{w}{h}}}} + 1 & \frac{w}{h} \le 1 \\ \frac{\frac{2}{C_{air}L_{air}}\left(\frac{\arg(S_{21})}{l\omega}\right)^2 - 2}{1+\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} - \frac{\frac{t}{h}}{2.3\sqrt{\frac{w}{h}}}} + 1 & \frac{w}{h} > 1 \end{cases} \quad (8)$$

A microstrip test coupon designed with FR4 as a substrate is shown in Figure 2. There is no solder mask over the microstrip. Four microstrips traces on the PCB have different lengths. The SMA connectors are attached to the backside of the PCB.

To obtain the S-parameter, the transmission coefficients of the microstrips are measured with a VNA. The following 5 pairs are created for de-embedding by the 2X-Thru SFD method [13].

1. Total: 4.25cm; Thru: 2.25cm.
2. Total: 4.25cm; Thru: 2cm.
3. Total: 8cm; Thru: 4.25cm.
4. Total: 8cm; Thru: 2.25cm.
5. Total: 8cm; Thru: 2cm.

The attenuation factor for all 5 pairs calculated from the de-embedded s-parameters as (2) is shown in Figure 3. The differences between the curves are due to the de-embedding errors because of the non-identical coaxial-to-microstrip transitions of the lines in the pairs (the reasons are mainly manufacturing and connector tolerances).

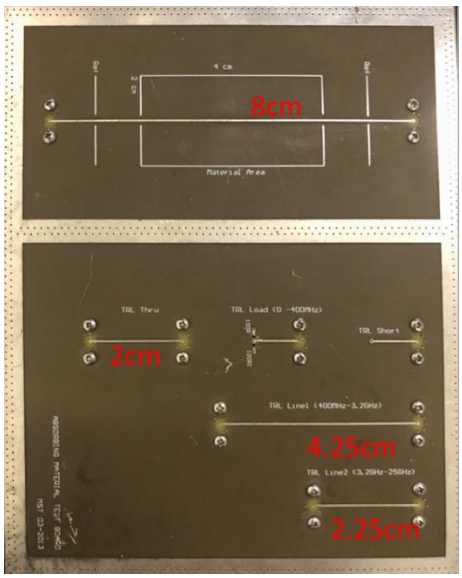


Figure 2. Microstrip test coupon. The trace thickness t is 0.046 mm. The trace width w is 0.4318 mm. The thickness of the dielectric h is 0.24 mm.

As demonstrated in [18], selecting standards with the largest length difference allows for reducing the de-embedding error. As can be seen in Figure 3, the green line which corresponds to the pair with the largest length differences (Total: 8cm; Thru: 2cm) is the smoothest one and is expected to provide more accurate extraction results up to 20GHz. The extracted permittivity for different combinations is shown in Figure 4 and has similar values. The difference between the results is mostly due to the de-embedding

errors. At the same time, as can be seen, the green line (Total: 8cm, Thru: 2cm) is the smoothest of all five as expected.

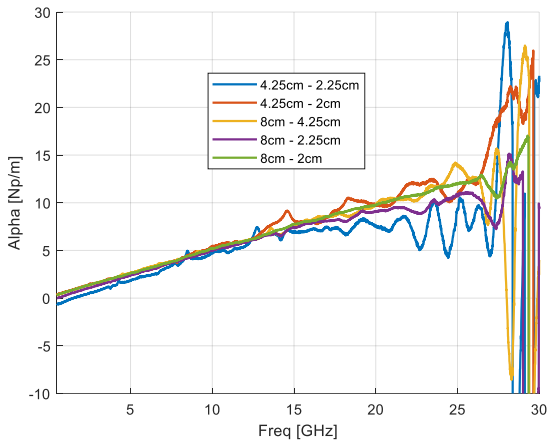


Figure 3. Measured attenuation factor

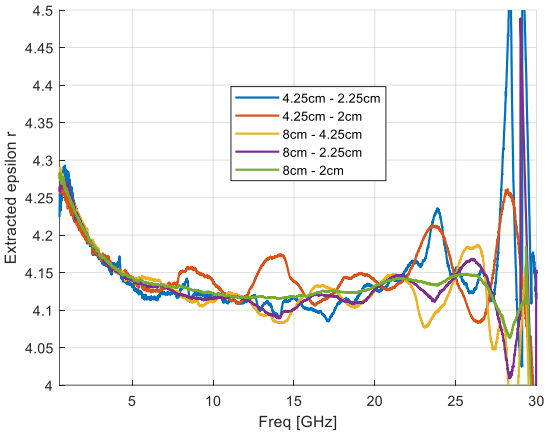


Figure 4. The extracted permittivity of the test coupon substrate

2.2. INHOMOGENEOUS MODEL EXTRACTION

2.2.1. Extraction Algorithm. In the fabrication of the microstrip in PCB, the solder mask is a crucial layer to protect the traces against corrosion and oxidation. A simplified structure of microstrip in fabricated PCB is shown in Figure 5. For the insertion loss modeling, the dielectric layer of the microstrip can be considered a homogeneous layer with the equivalent primitivity. However, due to the that the solder mask will affect the FEXT level of the microstrip, the homogeneous model cannot describe the FEXT caused by the material inhomogeneity between the solder mask and the substrate. To better model the microstrip in PCB, the extraction for the permittivity of both the solder mask and the substrate layer is essential.

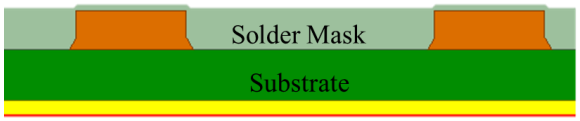


Figure 5. The cross-sectional geometry of microstrip with solder mask

FEXT noise is caused by the coupling between transmitting lines when the signal propagates from the transmit end to the receiving end. The modal analysis for the FEXT [8] separates the aggressor signal into even and odd modes that propagate through the coupled pair with different velocities:

$$V_{fext}(t) = V_{even}(t) + V_{odd}(t) \tag{9}$$

The odd and even phase velocities ($v_{p,odd}$, $v_{p,even}$) can be expressed using the per-unit length (PUL) modal inductance (L_m) and capacitance (C_m):

$$v_{p,m} = \frac{1}{\sqrt{L_m C_m}} \tag{10}$$

Here, m represents the even or odd mode. The FEXT is generated during the time interval between the arrival of the odd-mode signal and the arrival of the even-mode signal [8, Eq. (3)] as:

$$V_{fext} = \frac{V_1 l}{2t_r}\left(\frac{1}{v_{p,odd}} - \frac{1}{v_{p,even}}\right) \tag{11}$$

Here V_1 is the magnitude of the aggressor signal with the rise time of t_r. To describe the difference between different modes, the FEXT is expressed with variable Δ_{LC} as (11), which is the dominant contributor compared to the parameters with lower-order terms.

$$V_{fext} = \frac{V_1 l}{2t_r(\sqrt{L_{odd}C_{odd}}+\sqrt{L_{even}C_{even}})}\Delta_{LC} \tag{12}$$

Δ_{LC} is defined in [9] as:

$$\Delta_{LC} = L_{odd}C_{odd} - L_{even}C_{even} = 2(L_{11}|C_{21}| - C_{11}L_{21}) \tag{13}$$

To separate the contribution of solder mask and substrate layers to the Δ_{LC}, the capacitance is decomposed according to [19]. Based on the decomposition of a simplified model in [19], the capacitance of the structure with 3 dielectric layers (air, solder mask, and substrate) is decomposed as is shown in Figure 6. The four categories of the per-unit-length capacitances in the 3-layer model are explained in Table 2.

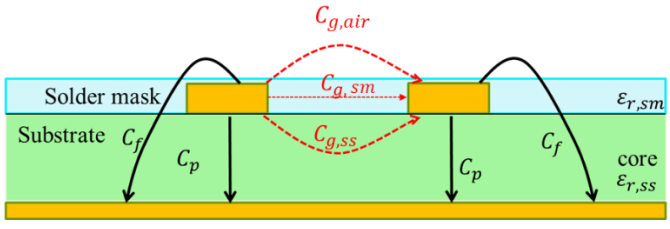


Figure 6. Illustration of the capacitance components for the coupled microstrip pair.

The mutual capacitance across the gap C_g can be expressed as:

$$C_g = C_{g,air} + C_{g,sm} + C_{g,ss}$$
$$= C_{g,air} + \varepsilon_{r,sm} C^a_{g,sm} + \varepsilon_{r,ss}\, C^a_{g,ss} \quad (14)$$

Table 2. Definition of the decomposed capacitance.

Capacitance	**Definition**
C_f	Fringe capacitance on the outer side of the trace, including the top, side, and bottom of the trace, is contributed by the air ($C_{f,air}$), solder mask ($C_{f,sm}$) and substrate ($C_{f,ss}$) regions.
C_p	Parallel plate capacitance of the trace, contributed by the substrate region.
C_g	Mutual capacitance across the gap, contributed by the air ($C_{g,air}$), solder mask ($C_{g,sm}$) and substrate ($C_{g,ss}$) regions.

This capacitance is expressed by the product of the capacitances in the air-filled structure (denoted by the superscript 'a') and the permittivity of the dielectric material [16].

The self-capacitance in the nodal capacitance matrix can be expressed as:

$$C_{11} = C^a_{f,air} + \varepsilon_{r,sm} \cdot C^a_{f,sm} + \varepsilon_{r,ss} \cdot C^a_{f,ss} + \varepsilon_{r,ss} \cdot C^a_p + + C_g \quad (15)$$

The mutual capacitance in the nodal capacitance matrix:

$$|C_{21}| = C_g = C_{g,air} + \varepsilon_{r,sm} C^a_{g,sm} + \varepsilon_{r,ss}\, C^a_{g,ss} \quad (16)$$

According to [18, Eq. 14], the self-inductance and mutual inductance can be estimated using capacitances of the air-filled line as:

$$L_{11}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10C_{11}^{a}}{9\Delta C^{a}}$$

$$= \frac{10\left(C_{f,air}^{a}+C_{f,sm}^{a}+C_{f,ss}^{a}+C_{p}^{a}+C_{g}\right)[\text{pF/cm}]}{9\Delta C^{a}\,[(\text{pF/cm})^2]} \quad (17)$$

$$L_{21}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10|C_{21}^{a}|}{9\Delta C^{a}}$$

$$= \frac{10\left(C_{g,pg}^{a}+C_{g,co}^{a}+C_{g,sm}\right)[\text{pF/cm}]}{9\Delta C^{a}[(\text{pF/cm})^2]} \quad (18)$$

Here $\Delta C^{a} = (C_{11}^{a})^2 - (C_{21}^{a})^2$. Then, Δ_{LC} as defined by (13) and using the L and C given by (14)-(18) is expressed as:

$$\Delta_{LC} = C_{11}L_{21} - L_{11}|C_{21}|$$

$$= \frac{10}{9\Delta C^{a}} \cdot [(\varepsilon_{r,sm}-1)(C_{g,air}\cdot C_{f,sm}^{a} - C_{g,ss}^{a}\cdot C_{f,air} + C_{g,ss}^{a}C_{f,sm}^{a} - C_{g,sm}^{a}C_{f,ss}^{a} - C_{g,sm}^{a}C_{p,ss}^{a}) + (\varepsilon_{r,ss}-1)(C_{g,air}\cdot C_{f,ss}^{a} - C_{g,sm}^{a}\cdot C_{f,air} + C_{g,air}\cdot C_{p,ss}^{a} - C_{g,ss}^{a}C_{f,sm}^{a} + C_{g,sm}^{a}C_{f,ss}^{a} + C_{g,sm}^{a}C_{p,ss}^{a})] = k_1\varepsilon_{r,sm} + k_2\varepsilon_{r,ss} + b \quad (19)$$

The coefficients k_1, k_2, and b are related to the air-filled structure, which can be determined by solving 3 simulation cases with a fixed structure to achieve the 3 unknowns. Then, the FEXT peak value in (12) can be expressed as a function of $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$:

$$V_{fext} = K_{FEXT}\Delta_{LC} \sim k_1\varepsilon_{r,sm} + k_2\varepsilon_{r,ss} + b \quad (20)$$

where $K_{FEXT} = \frac{V_1}{2t_r(\sqrt{L_{odd}C_{odd}}+\sqrt{L_{even}C_{even}})}$.

The effect of dielectric changes on K_{FEXT} is assumed to be minor compared to that on Δ_{LC}. Since the FEXT level of the modeled microstrip is achieved by the 2D solver, the error caused by the assumption can be compensated in the extraction procedure.

For a microstrip, the capacitances in prepreg and core are in parallel [19]:

$$C_{dd} = C_{dd,air} + C_{dd,sm} + C_{dd,ss} \tag{21}$$

Thus, the β_{dd} should have a strong sensitivity to the sum of $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$, since $C_{dd,ss}$ and $C_{dd,sm}$ in (5) are scaled by $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$. Then, the β_{dd} is expressed as:

$$\beta_{dd} = f\left(\varepsilon_{r,ss}, \varepsilon_{r,sm}\right) \tag{22}$$

To extract the inhomogeneous dielectric permittivity ($\varepsilon_{r,pg}$, $\varepsilon_{r,co}$), a target function (T) is defined as:

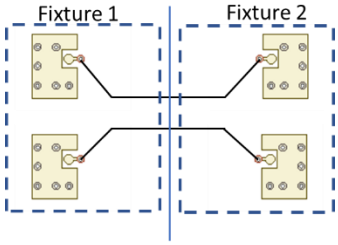
$$T = \sqrt{\left(v_{fext}{}' - v_{fext0}\right)^2 + weight\left[\left(\frac{\beta_{dd}{}'}{\omega} - \frac{\beta_{dd0}}{\omega}\right)\right]^2} \tag{23}$$

Here, $v_{fext}{}'$ and $\beta_{dd}{}'$ are the FEXT peak value in the time domain waveform and phase of the modeled result. The parameter $weigtht$ is introduced to make $(\beta_{dd}{}'/\omega - \beta_{dd0}/\omega)$ and $\left(v_{fext}{}' - v_{fext0}\right)$ have a comparable impact to the target function (T). Normally, the PUL inductance of the microstrip is in the order 100nH and the PUL capacitance is in the order of pF, $(\beta_{dd}{}'/\omega - \beta_{dd0}/\omega)$ is in the order of $1e^{-16}$ according to (5). As a result, the value of the $weigtht$ is assigned as $1e^{16}$.

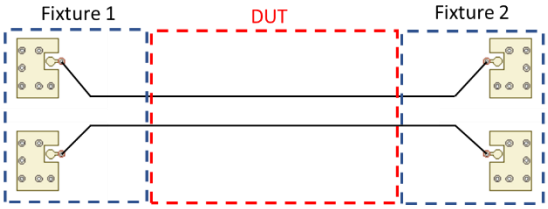
2.2.2. Application on Test Coupon. To investigate the FEXT and insertion loss of the PCB, boards with multiple striplines with EUL structure and Delta-L lines are fabricated. The test coupon used in the measurement is designed with Delta-L and EUL structures.

The Delta-L structures are differential striplines with different lengths, as shown in Figure 7. The “Thru” is with a shorter length, and the “Total” is with a longer length.

The unwanted fixtures are composed of connectors, pads, vias, and transition sections. After 2X-thru de-embedding [13], the S-parameters of "DUT" is obtained.



(a) Thru



(b) Total

Figure 7. The illustration of a Delta-L structure.

The microstrip with EUL structures is illustrated in Figure 8. The device under test (DUT) is a pair of coupled striplines, and the striplines are intentionally extended. The extended parts are unterminated (open) without any coupling to the other pair. With a matched long transmission line termination, the impact from FEXT due to mismatched terminals can be excluded in the time domain [8]. The measurement is performed with differential microprobes (D-probes) [20]. Compared to the traditional measurement methods based on SMA connectors, more efficient tests can be performed with smaller landing space for the high-volume PCB manufacturing validation.

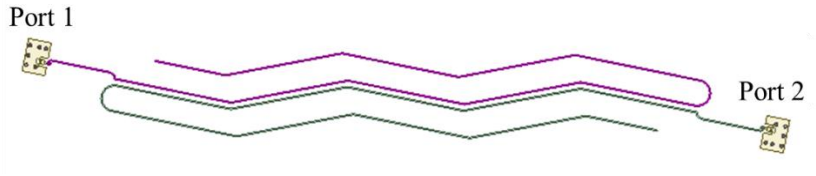


Figure 8. Illustration of striplines with EUL structures.

The S-parameters measurement is performed using Keysight N5244A 4-port Network Analyzer. Using the measured S-parameters, with the amplitude and rise time of the incident step signal on the aggressor line set to +1V and 50ps, the FEXT waveform was calculated by Keysight ADS [21] as shown in Figure 9.

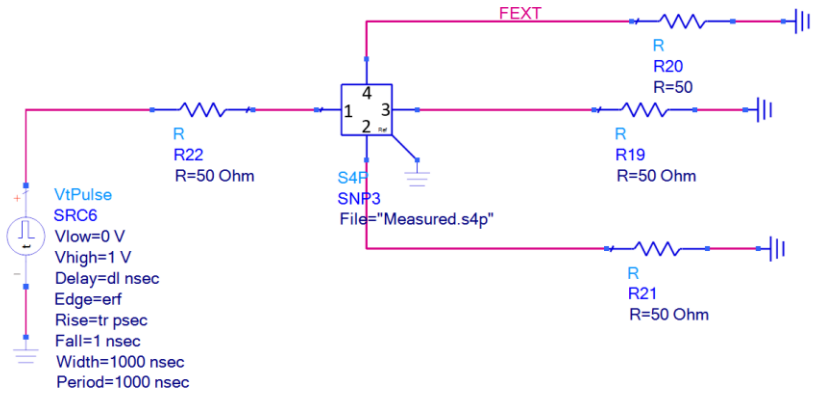


Figure 9. Schematic for FEXT calculation in ADS.

The entire extraction procedure is illustrated in the flow chart in Figure 11. In the extraction procedure, the measurements result of Delta-L and EUL are acquired first from the traces on the same layer of the same board. As a result, the dielectric properties of the same layer are assumed to be the same. The EUL S-parameters provide the measured FEXT level and the Delta-L S-parameters after de-embedding provides β_{dd}. With the

cross-section geometry, the simulation models of both EUL and Delta-L structures are created by a 2D solver. Intel IMLC [22] (a 2-D field solver) is the tool used to model the EUL and Delta-L lines.

After the S-parameters are measured, the samples of the traces are cut out from a fabricated PCB and encapsulated in an epoxy-based compound. Then the cross-section of the copper layer of interest is polished so that the profile perpendicular to the plane of view can be achieved. Figure 10 shows an example of the cross-section geometry for the microstrip case with solder mask and substrate layers. The epoxy is filled above the sample for fixation in the polishing procedure. The extraction procedure is shown in Figure 11. The initial value of the combination of $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$ is set based on datasheets from the vendor. Then the gradient descent is applied as the optimization with 0.1 sweeping steps After the iterations, the value is optimized and the $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$ are updated as the final extracted results.

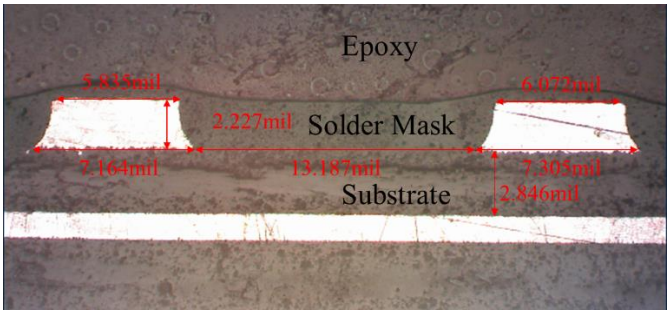


Figure 10. The cross-sectional geometry information for the microstrip. The epoxy is filled above the sample for fixation in the polishing procedure.

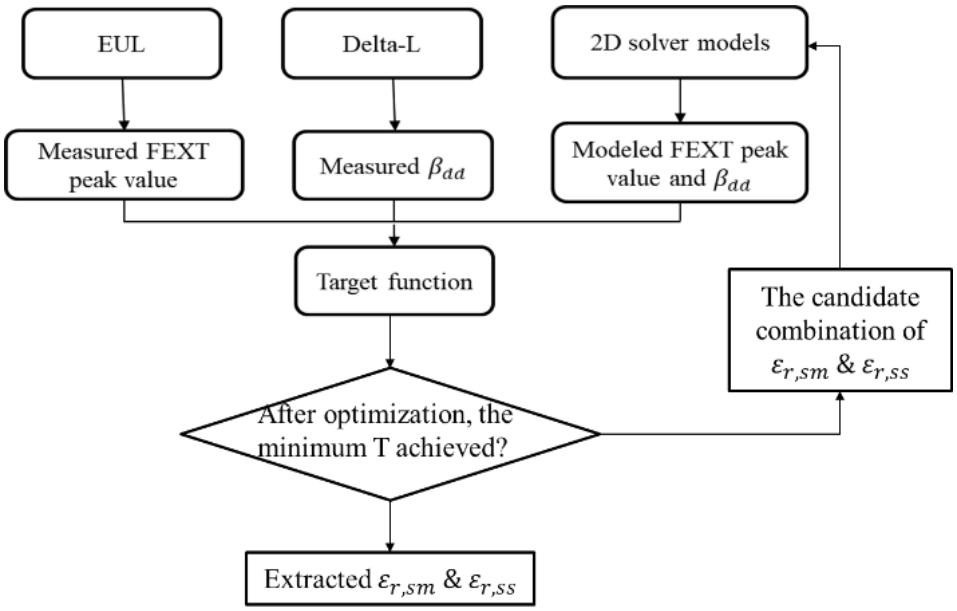
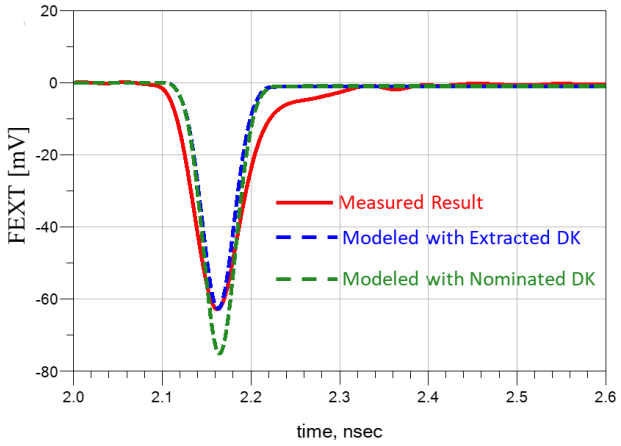


Figure 11. The flow chart of the proposed $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$ extraction method

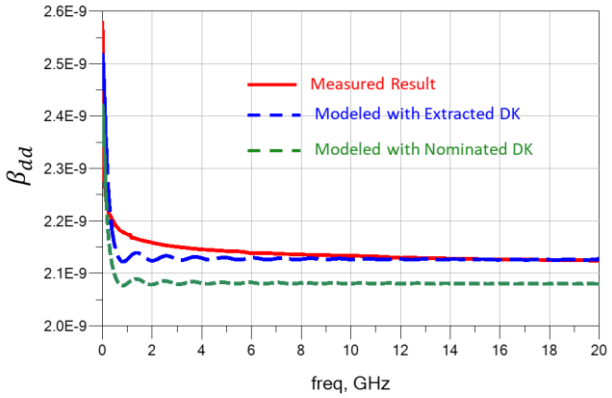
Table 3 lists the nominal permittivity value provided by the PCB vendor and the extracted values. Figure 12 demonstrates the comparison between the measured, the modeled result with the extracted value, and the modeled result with the nominal value. The extracted model result matches the measured result well and improves the accuracy of the nominal model.

Table 3. Permittivity of solder mask and substrate layers at 1GHz.

	DK Nominal	DK Extracted
Solder Mask	4.25	4.0
Substrate	3.6	3.3



(a)



(b)

Figure 12. The comparison between the measured and modeled FEXT (a) and β_{dd} (b).

3. SURFACE ROUGHNESS EXTRACTION

For the Delta-L structure, after de-embedding, the α_{dd}, which is the real part of the differential propagation constant that can be calculated from the measured S-parameters. Information about the dielectric loss is contained in the PUL conductance G [23]. Then the other differential parameters are determined from the previous sections.

$$\alpha_{dd} = \frac{-\ln\left[|S_{dd21}|\right]}{l} \tag{24}$$

l is the length of the transmission line after de-embedding.

$$\alpha_{dd} = \frac{1}{2}\left(R_{dd}\sqrt{\frac{C_{dd}}{L_{dd}}} + G_{dd}\sqrt{\frac{L_{dd}}{C_{dd}}}\right) \tag{25}$$

To model the total insertion loss of the microstrip, conductor loss caused by the surface roughness needs to be extracted accurately[24]. Various approaches have been proposed to calculate the frequency-dependent surface roughness correction factor using the cross-sectional profile [25,26] or the root-mean-square (RMS) roughness levels [27]. The surface roughness correction factor (K) can be expressed with the PUL resistance as:

$$K = \frac{R_{dd_{rough}}}{R_{dd_{smooth}}} \tag{26}$$

The surface of the microstrip does not have the same roughness level for each edge. As is shown in Figure 13, the bottom edge of the trace is much rougher than the upper edge of the trace and the top side of the reference plane beneath the trace. It is no longer accurate if one considers all the surface roughness to be at the same level [27]. As the result, the edges of the microstrip should be assigned with different roughness to ensure the accuracy of the model.

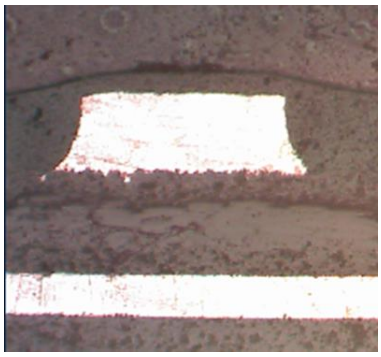


Figure 13. The cross-sectional geometry for the microstrip.

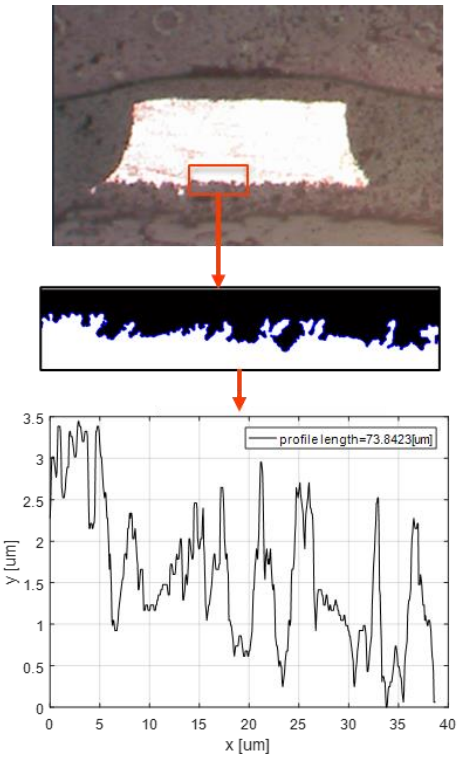


Figure 14. The roughness level extraction for one area. The contrast of the cross-section image is optimized for each area. Then the profile of the surface roughness is extracted, and RMS value is calculated for all the areas along the surface.

After achieving the SEM picture of the traces, the contrast of the image is optimized so that the roughness profile can be extracted. The procedure is shown in Figure 14. Then, the RMS value of the surface can be calculated for each zoomed-in area. The RMS surface roughness level of the lower edge is extracted as 0.6um in the RMS value. The other surface is assumed to be smooth. The conductor edges in the model created in Q2D with the geometry is assigned with different roughness level. In Q2D, the roughness level is added as the finite conductivity boundary of Hammerstad model. Figure 15 shows the resistance solved from the simulation. The equivalent correction factor is calculated by (26), shown in Figure 16.

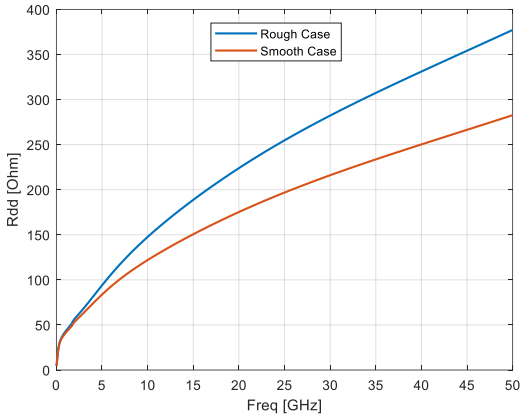


Figure 15. PUL resistance of the rough and smooth cases, solved by Q2D microstrip model.

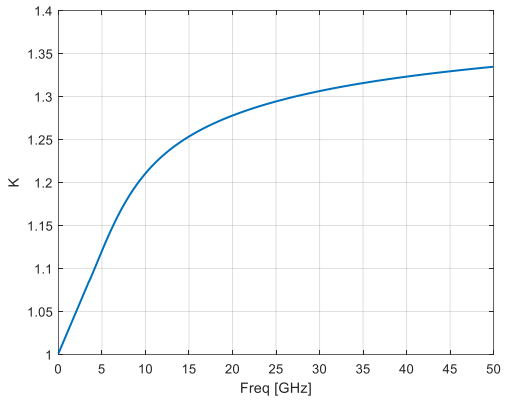


Figure 16. A correction factor of the surface roughness calculated from the Q2D microstrip model.

4. DIELECTRIC DISSIPATION FACTOR EXTRACTION

Then by solving the equation for each frequency point in (27), the dielectric loss tangent can be achieved. The loss tangent can only affect the insertion loss. As a result, the effective value can represent the performance of the two dielectric layers. Table 4

shows the extraction result of the example in Figure 10. The extracted value is between the nominal tangent delta of the solder mask and substrate layers as expected. Figure 17 demonstrates the attenuation factor comparison between the measured result and the modeled result with the extracted value. The error is introduced from the S-parameter measurement by the instrument, per-unit-length parameters calculation by the 2D solver, and the manufacturing variations of the fixture which affects the de-embedding procedure to obtain attenuation factors [14]. Besides, the sensitivity of the surface roughness in (26) is shown in Table 5.

$$G_{dd} = \omega \cdot C_{dd} \cdot tan\delta \tag{27}$$

Table 4. Tangent delta of solder mask and substrate layers at 1GHz.

	Tangent delta Nominal	Tangent delta Extracted
Solder Mask	0.0267	0.0170
Substrate	0.004	

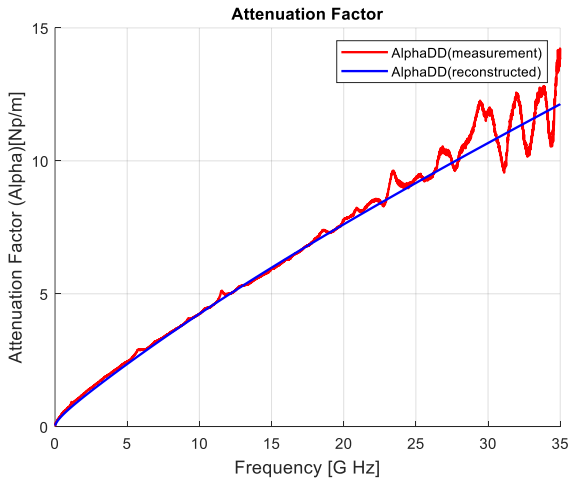


Figure 17. The comparison between the measured and modeled attenuation factor.

Table 5. Tangent delta sensitivity to the surface roughness

DF without roughness error	DF with 5% error in K	DF with 10% error in K
0.0170	0.0174	0.0178

5. DESIGN GUIDELINE

In practice, to improve the signal integrity performance in high-speed systems, FEXT mitigation is always a key design factor. As the frequency of the system gets higher, the difference of the phase velocity increases, which in turn results in higher FEXT. In the design procedure of the microstrip, the design guideline for the key design parameters is of great use. Using the extracted model and the analysis of the FEXT of the microstrip, some general design guidelines are established based on the contribution of each parameter, which is validated by sweeping the parameters.

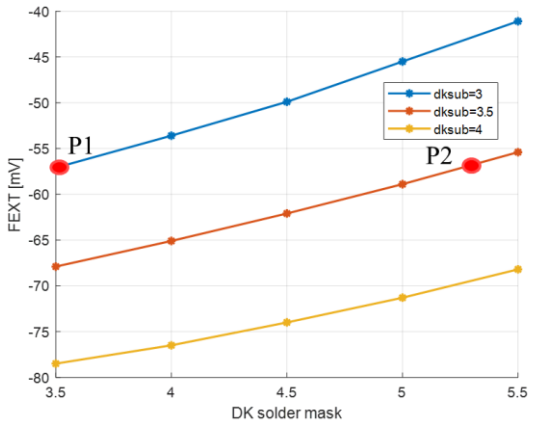


Figure 18 Relationship between the dielectric constant and the FEXT

For the simplified microstrip model in Figure 1, The FEXT of the simplified microstrip is mainly caused by the inhomogeneity between the dielectric layer and the air. In order to reduce the FEXT level, it is well known that we can either decrease the thickness of the substrate or decrease $\varepsilon_{r,ss}$.

For the microstrip model with both the solder mask and the substrate layers in Figure 5, Figure 18 shows the FEXT level with the geometry in Figure 10 with different $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$ from commercial 2D field solver (Ansys Q2D) simulation. The higher the negative FEXT peak value shows, the better the design will be. The decrease of the $\varepsilon_{r,ss}$ and the increase of the $\varepsilon_{r,sm}$ help improve the FEXT result. To compensate for the FEXT caused by the change of $\varepsilon_{r,ss}$, $\varepsilon_{r,sm}$ needs larger change. For example, in Figure 18, P1 and P2 share the same FEXT value. P1 represents the case that $\varepsilon_{r,sm}$ is 3.5 and $\varepsilon_{r,ss}$is 3, while P2 represents the case that $\varepsilon_{r,sm}$ is 5.3 and $\varepsilon_{r,ss}$ is 3.5. The 0.5 increase of the $\varepsilon_{r,ss}$ needs 1.7 increase of the $\varepsilon_{r,sm}$ to compensate.

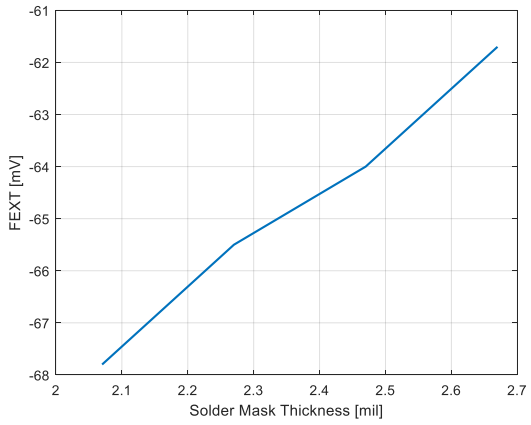


Figure. 19. Relationship between solder mask thickness and FEXT

Besides, the increase of the solder mask thickness will help reduce the inhomogeneity between the substrate and the solder mask, and in turn helps immigrate the FEXT, validated by the simulation as is shown in Figure 19.

In a summary, in order to mitigate the FEXT of the practical microstrip model, one can:

- Decrease $\varepsilon_{r,ss}$
- Increase $\varepsilon_{r,sm}$
- Increase dielectric constant of the solder mask should be to compensate the FEXT increasing due to increased dielectric constant of the substrate
- Decrease the thickness of the substrate.
- Increase the thickness of the solder mask.
- Increase the number of solder mask to two or grater to reduce FEXT by increasing the thickness of the total solder mask.

6. CONCLUSTIONS

An empirical modeling approach to microstrip FEXT and insertion loss is proposed in this paper. Both the simplified model with one dielectric layer and the practical model with solder mask and the substrate layers are studied. To model the FEXT and insertion loss, the relative permittivity (ε_r), dielectric dissipation factor (tanδ), and the surface roughness are extracted and verified up to 20GHz. With the extracted properties, the FEXT and insertion loss of the microstrip can be characterized more accurately, which can guide the PCB design and the material selection of the microstrip.

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SECTION

2. SUMMARY AND CONCLUSIONS

This work proposes practical methods to analyze the FEXT for the stripline and microstrips in the high-speed PCB design with IDL and provides design guidelines to mitigate the FEXT level.

The stripline model of 3L-IDL is proposed with improved FEXT prediction accuracy compared to the 2L-IDL model by separating the resin pocket from the traditional stripline model and using the superposition principle. The ε_r of IDLs is extracted using measured S-parameters of Delta-L and EUL structures. The extraction algorism is optimized with the superposition principle. Moreover, the prediction for the FEXT polarity and magnitude of the stripline caused by the inhomogeneity can be predicted using the proposed analytical model and is verified with the measurement data. With the stack up information, the polarity can be predicted with over 98% accuracy and the FEXT level can be predicted with over 80% accuracy. This paper also provides a design guide to minimize FEXT induced by IDLs for PCB material designers.

The modeling approach for microstrip FEXT and insertion loss is also proposed in this paper. Both the simplified model with one dielectric layer and the practical model with solder mask and the substrate layers are studied. To model the FEXT and insertion loss, the relative permittivity (ε_r), dielectric dissipation factor (tanδ), and the surface roughness are extracted and verified up to 20GHz. With the extracted properties, the FEXT and insertion loss of the microstrip can be characterized more accurately, which can guide the PCB design and the material selection of the microstrip.

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VITA

Yuanzhuo Liu was born in Mishan, Heilongjiang, China. She received a Bachelor of Science Degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China in June 2017. She then joined the EMC Laboratory in the Missouri University of Science and Technology, Rolla, MO, USA. She received a Master of Science and a Doctor of Philosophy in Electrical Engineering from Missouri University of Science and Technology in December 2019 and December 2022, respectively.

Her research interests included signal integrity, electromagnetic interference, radio frequency desense, noise, and jitter analysis in high-speed digital systems. She received 2022 President's Memorial Award of IEEE EMC Society.