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PI AND EMI ANALYSIS OF 3D IC SYSTEM WITH TSVS AND CO-PACKAGED OPTICS

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PI AND EMI ANALYSIS OF 3D IC SYSTEM WITH TSVS AND CO-PACKAGED OPTICS

by

WEI ZHANG

A DISSERTATION

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Paper I, found on pages 3–35, is intended for submission in IEEE Transactions on Signal and Power Integrity.

Paper II, found on pages 36–64, has been published in IEEE Transactions on Electromagnetic Compatibility.

ABSTRACT

With the demand for developing high-capacity, high-density, high-power optical links for data center communications, co-packaged optics is a promising solution. When the three-dimensional (3D) IC and optic engines are integrated into the same package, the design of such systems in terms of signal integrity, power integrity, and electromagnetic interference will be more challenging.

This first paper mainly focuses on modeling the bias-voltage-dependent, temperature-dependent, and light-intensity-dependent hysteresis behavior of a through-silicon-vias (TSV) structure in 3D IC, and analyzing its effect on the power integrity of a system with 3D IC.

This second paper investigates the scaled tendency of the emissions in a router system loaded with hundreds of optical modules, which can be applied for both traditional and future router systems with co-packaged optics. An artificial router mimicking the real system was built to investigate this tendency. Theoretical analysis, a statistical prediction method, and measurement have predicted and verified that the average of the maximal electric field radiated will increase following a 10 log10 N (dB) tendency, where N is the number of optical modules.

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1. INTRODUCTION

With the demand for developing high-capacity, high-density, high-power optical links for data center communications, co-packaged optics is a promising solution to meet the development requirement of the optical links, which brings the optical engine much closer to the main switching ASIC. In this scenario, the 3D IC with TSVs and co-packaged optic engines are embedded together in one package, which increases the challenges in terms of signal integrity, power integrity, and EMI.

Through-silicon-via (TSV) technology is widely used in 2.5D and 3D ICs such as high bandwidth memory (HBM) and CMOS image sensor (CIS) to increase integration density and shorten the interconnect length and reduce the power consumption. Since it is a metal-oxide-semiconductor (MOS) structure, the electrical performance of a single TSV can be affected by conditions such as bias voltage and temperature in 2.5D/3D ICs with HBM, and light intensity in 2.5D/3D ICs with CIS. Since a large number of TSVs are embedded in a 2.5D/3D IC system, several external factors such as bias voltage, temperature, and light intensity have a significant impact in evaluating the risk of signal integrity (SI) and power integrity (PI) issues of a system in a pre-design stage. Based on the low-frequency (several hundred MHz) capacitances measured on a single TSV structure, the first paper characterized and modeled the behavior of the dependency of low-frequency TSV capacitance under conditions of bias voltages, temperatures, and light intensities. Based on the bias voltage-dependent power/ground (P/G) TSVs, the power integrity of a system with 3D HBM IC and P/G TSVs is analyzed with and without considering the bias effect on the P/G TSVs. In addition, the importance of considering the bias-dependency of P/G TSVs during the system power integrity design is emphasized.

In a multi-modular system, an increase in the number of radiating optical modules will increase the electromagnetic emissions. Similar to traditional router systems/network switches with a large number of optical modules, the risk of electromagnetic interference (EMI) related to high-speed and high-power electrical-to-optical transceivers in co-packaged optics needs to be identified to ensure electromagnetic compatibility. The second paper investigates the scaled tendency of the emissions in a router system loaded with hundreds of optical modules, which can be applied for both traditional router systems and future router systems with co-packaged optics. An artificial router mimicking the real system was built to investigate this tendency. Based on statistical simulation and measurement, it is proved that the average of the maximal radiated electric field from a multi-modular system will follow a tendency of around 10 log10 N (dB), where N is the number of modules/radiators.

PAPER

I. MODELING ON HYSTERESIS OF 3D IC TSV AND PI ANALYSIS OF 3D IC SYSTEM WITH TSVS AND CO-PACKAGED OPTICS

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ABSTRACT

Through-silicon vias (TSVs) are commonly used in the vertical interconnect of 2.5D and 3D IC systems. Since TSVs are metal-oxide-semiconductor (MOS) structures, aspects such as bias voltage, temperature, and light density will affect the electrical performance of TSVs. In a 2.5D/3D IC system with TSVs such as high bandwidth memory (HBM) or CMOS imager sensors, the large number of TSVs with bias-voltage-dependency, temperature-dependency, and light-intensity-dependency will have a non-negligible impact on the power integrity and signal integrity of the 3D IC system, which increases the difficulty of accurately estimating the risk of power integrity or signal integrity in the design stage.

This paper mainly focuses on understanding, characterizing, and modeling the depletion effect and hysteresis behavior of a single TSV structure as a function of bias voltage, temperature, and light intensity. In addition, the influence of bias voltage-dependent power/ground TSVs on the power integrity of a system with 3D HBM IC and power/ground TSVs is analyzed based on a hierarchical power distribution network

(PDN) model of a 3D IC system, in which the importance of considering the depletion effect of TSVs during the system power integrity design are emphasized.

1. INTRODUCTION

The JEDEC standards [1] [2] have specified the details of high bandwidth memory (HBM) systems. In HBM systems, through-silicon vias (TSVs) provide short vertical interconnections between stacks of dynamic random-access memory (DRAM) chips. Under DC bias conditions, the metal-oxide-semiconductor (MOS) structure of the TSV can form a depletion region between silicon oxide (SiO2) and silicon (Si), resulting in a bias-dependent capacitance of the depletion layer [3] – [8].

The hysteresis effect of the low-frequency capacitance of a TSV vs. bias voltage has been studied in [4]. A simplified bias-dependent model for TSV capacitance was proposed and validated.

However, the proposed model is not accurate enough for the transition region between the accumulation and depletion region, which has a difference of 8%. Besides, when sweeping the bias voltage with different ranges, very few papers have analyzed the corresponded change in hysteresis curves. Moreover, the existing study about the temperature effect on TSV performance is mainly focused on capacitance in the accumulation and inversion region, which is lacking comprehensive investigations on the depletion region and the hysteresis behaviors. In addition, discussions about the light intensity effect on the TSV hysteresis behavior of a 3D IC with a CMOS imager sensor (CIS) have not been studied.

The modeling of the system PDN has been extensively investigated. In [9], a physics-based approach to extract the equivalent circuit of the system PDN from PCB to the chip was discussed. For 3D ICs and packaging, Green's function-based method in [10] can be used to extract the PDN impedance with multi-dielectric layers. For the P/G grids of the interposer and on-chip PDN of 3D ICs with TSVs, the calculation of the capacitance, inductance, and resistance on the unit cell of the P/G grid and TSVs has been discussed and equivalent circuit models have been proposed for fast prediction of PDN impedance [11] – [15].

In power distribution networks (PDNs), this bias-dependent capacitance will significantly affect the low-frequency behavior (below 1 GHz) of the PDN impedance when the number of power/ground (P/G) TSVs is sufficiently large. This situation may become worse when the power supply voltage decreases and the power consumption of the chip increases. Therefore, voltage-dependent PDN modeling and evaluation of various P/G TSV patterns or quantities are necessary during the design stage of the PDN in HBM systems to predict the accurate PDN impedance and reduce the PDN impedance below the target impedance. However, traditional PDN modeling with power/ground (P/G) TSVs fails to consider the depletion effect caused by the bias voltage.

Therefore, an accurate model of the hysteresis behavior of a single TSV under different sweeping ranges of the bias voltage, temperatures, and light intensities is needed to better understand the mechanism of the TSV behavior and provide an estimation on it when designing a 3D IC with TSVs, especially for the PDN design.

In this work, an improved model of the bias-dependent effect and hysteresis on the low-frequency capacitive behavior of a single TSV is proposed. The model can predict the hysteresis behavior of a low-frequency TSV capacitance under different bias voltage sweeping ranges, temperatures, and light intensities with better accuracy than the previous models. Based on the hysteresis measurement of a single TSV sample, the relationship between the interfacial traps and the starting value of the bias voltage during the hysteresis sweep is extracted. Besides, the parameters affected by temperature and light intensity in the hysteresis model are discussed and modeled.

Furthermore, the total bias-dependent capacitance of P/G TSV arrays with different patterns and quantities is investigated. Then, to investigate the effect of the voltage-dependent capacitance of P/G TSVs on PDN impedance of HBM systems, a hierarchical PDN model is developed including PCB and package, Si interposer, and on-chip PDN with voltage-dependent P/G TSV array. Based on the system PDN model, the influence of bias voltage on the system PDN is analyzed in both frequency and time domains.

Finally, the low-frequency capacitance of a TSV in the inversion region is discussed and a mitigation method is proposed.

2. THEORETICAL MODEL FOR HYSTERESIS OF SINGLE TSV

2.1. TSV EQUIVALENT CAPACITANCE WITH BIAS VOLTAGE

Figure 1 shows a TSV structure with a silicon (Si) substrate and its equivalent circuit [4]. Since the TSV is a MOS structure, it should be noted that when a bias voltage is applied to the power (PWR) TSV, a depletion region could be formed between the SiO2 layer and Si layer. The width of the depletion region depends on the bias voltage and thus the capacitance formed in the depletion region depends on the bias voltage. The total capacitance caused by the SiO2 layer and depletion layer dominates the low-frequency behavior of the coupling between TSV and other structures.

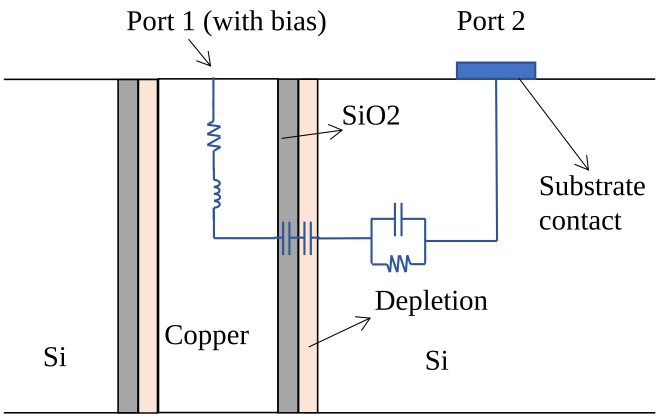


Figure 1. TSV structure and depletion region.

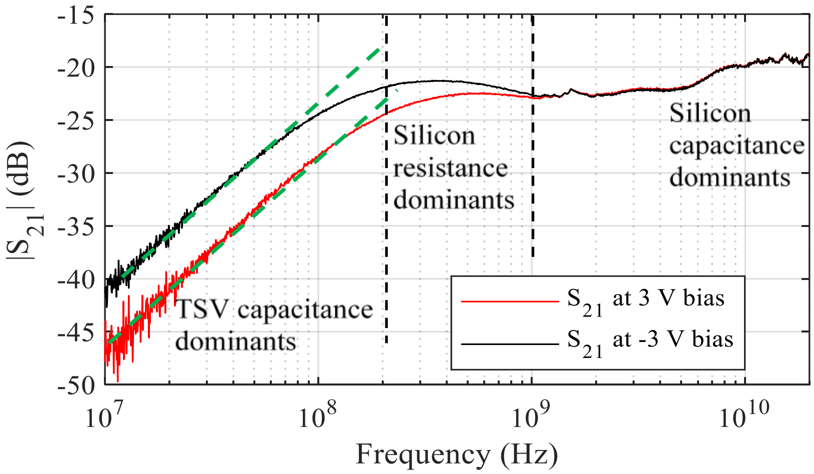


Figure 2. Measured coupling ($|S_{21}|$) between a single TSV and Si substrate contact under +3 V and – 3 V bias voltages.

For the coupling between a TSV structure and the Si substrate contact, Figure 2 shows the measured S_{21} under the bias voltage of +3 V and -3 V applied to the TSV. The dimensions of the TSV structure are shown in Table 1. Due to the short length of TSV (80 um), the equivalent resistance and inductance show a negligible effect on S_{21} in the frequency below 200 MHz. According to the equivalent circuit model of the TSV-substrate structure in Figure 1, the TSV equivalent capacitance caused by the series connection of the capacitance between the SiO2 layer and depletion layer dominates the total coupling below 200 MHz. The resistance caused by the Si substrate dominates the total coupling in 200 MHz – 1 GHz. And the capacitance of the Si substrate dominates the total coupling above 1 GHz.

Table 1. Dimensions of the TSV structure.

Parameters	Description	Value
H_{TSV}	Height of TSV	80 μm
tox	Thickness of the SiO2 layer	0.23 μm
R_{TSV}	Radius of the TSV copper	14.65 μm
ε_{SiO2}	Relative permittivity of SiO2	4.1
ε_{Si}	Relative permittivity of Si	11.9
σ_{Si}	Conductivity of Si	10 S/m

The hysteresis curve of the low-frequency equivalent TSV capacitance vs. bias voltage is shown in Figure 3 [4]. For the TSV structure studied in this paper, the equivalent TSV capacitance varies between 1280 fF and 677 fF with the bias voltage changes between + 3 V and -3 V. The low-frequency equivalent TSV capacitance is also affected by the thickness of the SiO2 layer since it is a series connection of the SiO2 layer and the depletion layer capacitance. The bias-dependency effect is only caused by different widths of the depletion layer corresponding to the varying bias voltages.

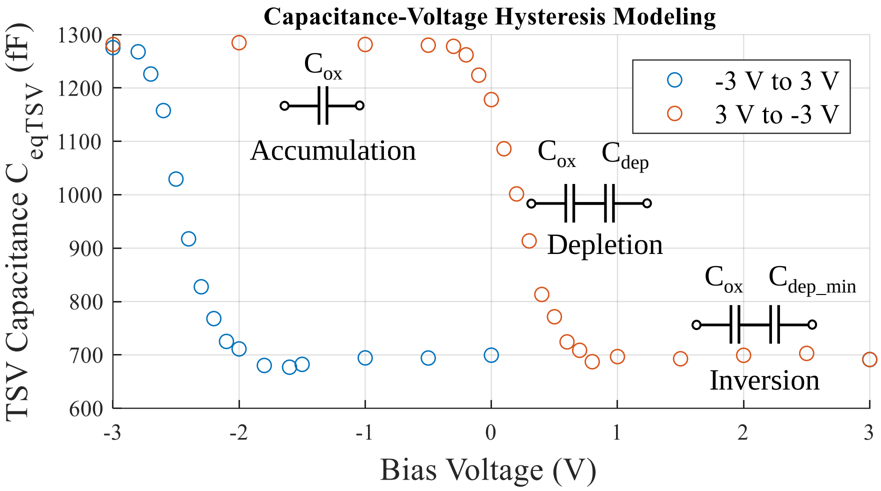


Figure 3. Hysteresis of low-frequency equivalent TSV capacitance vs. bias voltage.

Since the voltage-dependent effect of equivalent TSV capacitance affects the low-frequency electrical characteristics, it needs to be considered during the pre-design of an HBM system in terms of power integrity (PI) analysis when a large number of power TSVs are present. Therefore, a model to characterize the depletion behavior or hysteresis behavior under different conditions such as bias voltage, temperature or light intensity is needed to help engineers in PI or signal integrity (SI) design on 3D ICs with TSVs and gain an understanding of this behavior.

2.2. MODELING ON TSV HYSTERESIS BEHAVIOR

As TSV is also a MOS structure, its behavior can be explained by a simple MOS Capacitor (MOS CAP). The fundamental theory of MOS CAP has already been derived comprehensively in [16]. Therefore, the TSV structure solved in this paper refers to the derivation for MOS CAP in [16].

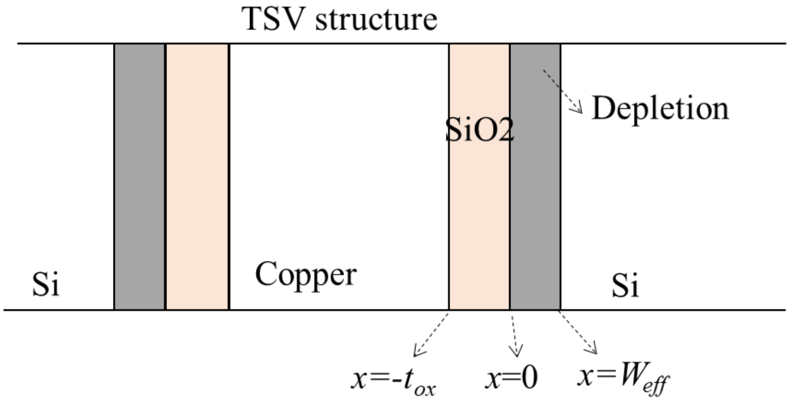


Figure 4. TSV structure and coordinates for field calculation.

Figure 4 shows the typical TSV structure. The Poisson's equation in one-dimensional structure can be expressed by (1) [16]:

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_{si}\varepsilon_0} = \frac{q}{\varepsilon_{si}\varepsilon_0}\left(p - n + N_D - N_A\right) \tag{1}$$

where E, x, and ρ are the electric field, distance, and charge density from the surface between the SiO2 and Si substrate to inside the Si substrate; p and n are the carrier charge densities/carrier concentration for holes and electrons inside the Si substrate; N_D and N_A are the doping (donor and acceptor) concentrations inside Si; q is the elementary charge; ε_{si} is the relative permittivity of Si; ε_0 is the vacuum permittivity.

Besides, the E field can be expressed as (2) [16].

$$E = \frac{1}{q}\frac{d\mathrm{E}_i(x)}{dx} = \frac{1}{q}\frac{kT}{q}\frac{dU}{dx} \tag{2}$$

where E$_i$ is the intrinsic Fermi level; *k* is Boltzmann constant; T is the temperature in kelvin; *U* is the electrostatic potential inside the semiconductor, which can be expressed as [16]:

$$U\left(x\right)=\frac{\phi\left(x\right)}{kT/q}=\frac{\mathrm{E}_i(bulk)-\mathrm{E}_i(x)}{kT} \tag{3}$$

where ϕ(x) is the electrostatic potential inside the MOS structure; E$_i$(bulk) is the Fermi energy of the bulk semiconductor, which has the following characteristics:

$$\frac{d\mathrm{E}_i(bulk)}{dx}=0 \tag{4}$$

Besides, the concentration for holes (*p*) and electrons (*n*) inside the Si substrate can be written as (5) and (6) [16].

$$p=n_ie^{[\mathrm{E}_i(x)-\mathrm{E}_F]/kT}=n_ie^{U_F-U(\mathrm{x})} \tag{5}$$

$$n=n_ie^{[\mathrm{E}_F-\mathrm{E}_i(x)]/kT}=n_ie^{U(\mathrm{x})\text{-}U_F} \tag{6}$$

where n_i is the intrinsic carrier concentration of the Si substrate; E$_F$ is the Fermi level of the semiconductor; U_S is the normalized surface potential with $\phi_S=\phi(x=0)$; U_F is the normalized surface potential with $\phi_S(x=0)=\phi_F$, which is the middle depletion point. For p-type semiconductor, it is:

$$\phi_F=\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{7}$$

Inside the semiconductor bulk, there is ρ=0 and U= 0 [16]. From (1), (5) and (6), there will be:

$$0=p_{bulk}-n_{bulk}+N_D-N_A=n_ie^{U_F}-n_ie^{-U_F}+N_D-N_A \tag{8}$$

Therefore, from (1), (5), (6) and (8), the charge density can be rewritten as:

$$\rho = qn_i\left(e^{U_F-U} - e^{U-U_F} + e^{-U_F} - e^{U_F}\right) \tag{9}$$

Furthermore, Possion’s equation can be rearranged as:

$$\frac{d^2U}{dx^2} = \frac{-1}{2L_D^2}\left(e^{U_F-U} - e^{U-U_F} + e^{-U_F} - e^{U_F}\right) \tag{10}$$

where L_D is the intrinsic Debye length [16], which is calculated as:

$$L_D = \left[\frac{\varepsilon_S\varepsilon_0 kT}{2q^2 n_i}\right]^{1/2} \tag{11}$$

Given the boundary conditions for U as (12), the exact solution for the electrical field inside the semiconductor can be derived as (13), where $F(U, U_F)$ and $\hat{U}_S$ are expressed as (14) and (15) [16].

$$\begin{cases} \dfrac{dU}{dx} = 0 & \text{at } x = \infty \\ U = U_S & \text{at } x = 0 \end{cases} \tag{12}$$

$$E = -\frac{kT}{q}\frac{dU}{dx} = \hat{U}_S\frac{kT}{q}\frac{F\left(U,U_F\right)}{L_D} \tag{13}$$

$$F\left(U,U_F\right) = \left[e^{U_F}(e^{-U} + U - 1) + e^{-U_F}(e^{U} - U - 1)\right]^{1/2} \tag{14}$$

$$\hat{U}_S = \begin{cases} +1 & \text{if } U_S > 0 \\ -1 & \text{if } U_S < 0 \end{cases} \tag{15}$$

From (13), one can solve the $U(x)$ for a given U_S.

Furthermore, the total capacitance of a MOS TSV structure (C_{TSV}) can be expressed as a series connection between oxide layer capacitance and depletion layer capacitance in (16)-(18), with the effective depletion width in different regions shown in (19) [16]. Therefore, the relationship between U_S and TSV capacitance is established.

$$C_{TSV} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_S}} \tag{16}$$

$$C_S = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{R_{TSV} + t_{oxide} + W_{eff}}{R_{TSV} + t_{oxide}}\right)} h_{TSV} \tag{17}$$

$$C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{R_{TSV} + t_{oxide}}{R_{TSV}}\right)} h_{TSV} \cdot surface\_constant \tag{18}$$

$$W_{eff} = \begin{cases} \hat{U}_S L_D \left[\frac{2F(U_S, U_F)}{e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right)} \right] & \text{Accumulation} \\ \frac{\sqrt{2} L_D}{\left(e^{U_F} + e^{-U_F}\right)^{1/2}} & \text{Flat band} \\ \hat{U}_S L_D \left[\frac{2F(U_S, U_F)}{e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right) / \left(1 + \Delta\right)} \right] & \text{Depletion and Inversion} \end{cases} \tag{19}$$

Besides, the relationship of the applied bias voltage (V_G) and U_S can be expressed as (20) [16]:

$$V_G = V_{FB} + \phi_s + V_{ox} + V_{trap} = V_{FB} + \frac{kT}{q} U_S + \hat{U}_S \frac{kT}{q} \frac{\varepsilon_S t_{ox}}{\varepsilon_o L_D} F\left(U_S, U_F\right) + \frac{Q_{trap}}{C_{ox}} \tag{20}$$

$$V_{trap} = -\frac{Q_{trap}}{C_{ox}} \tag{21}$$

Finally, by identifying the unique U_S, one can solve the corresponded C_{TSV} and V_G. Therefore, the one-one relationship between C_{TSV} and the applied bias voltage V_G can be determined, which is called *C-V* curve. As is shown in (20) and (21), the different number of donor-like and acceptor-like traps at the surface between the SiO2 and Si layer will cause the *C-V* curve shifts with the starting status of the TSV structure when sweeping the V_G, e.g., accumulation region or inversion region.

Since the derivations are all based on the rigorous field calculation from MOS CAP theory, no approximations of the charge densities are made. Therefore, the *C-V* curve extracted is expected to be an accurate solution.

3. MODEL AND VALIDATION OF TSV WITH BIAS VOLTAGE, TEMPERATURE, AND LIGHT INTENSITY

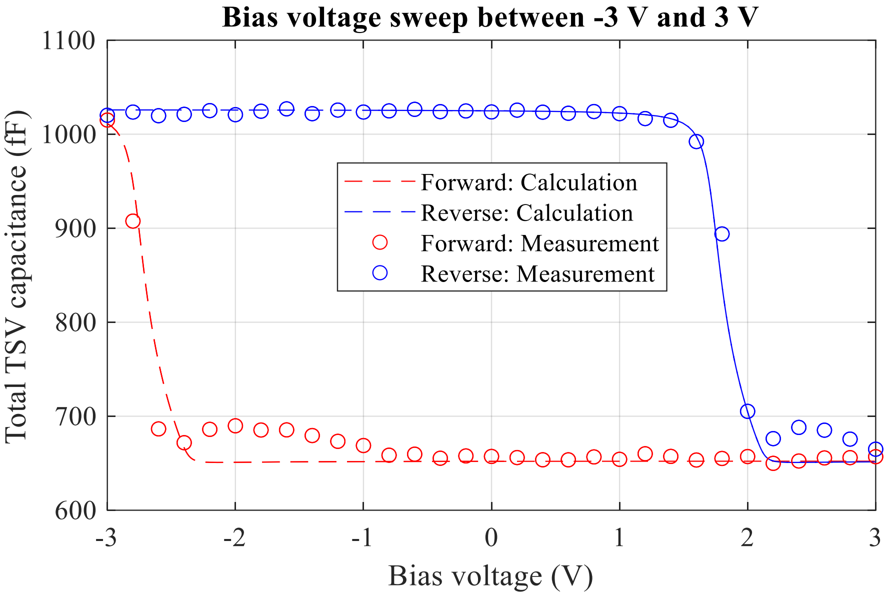
Based on the analytical model discussed in Section 2, the TSV hysteresis curve with different bias voltages, temperature, and light intensity conditions are measured, modeled, and discussed.

3.1. TSV HYSTERESIS WITH BIAS VOLTAGE

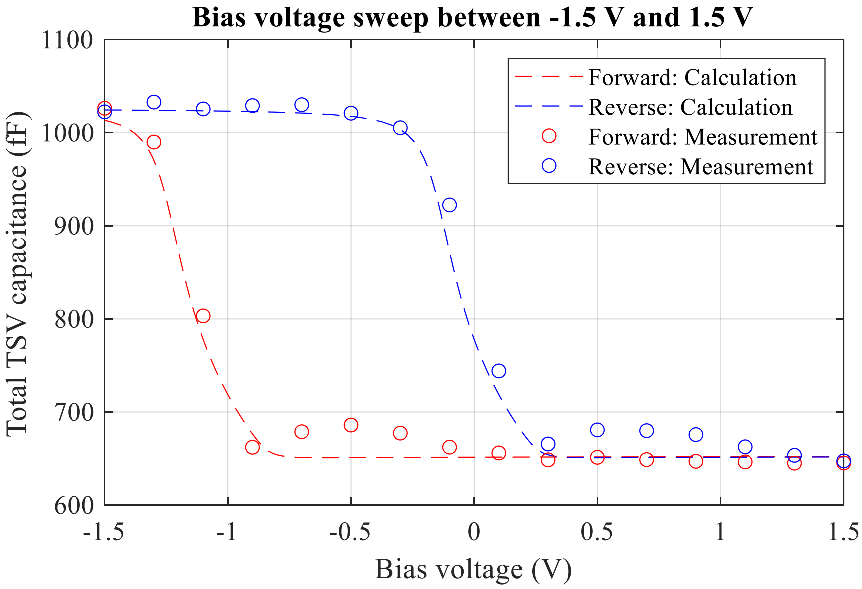
Based on the analytical model for characterizing the hysteresis behavior of a TSV sample, when sweeping the bias voltage between ±3 V, ±1.5 V, and ±1 V in the “Forward” and “Reverse” directions, the simulated hysteresis curves of a TSV sample under some assumed donor-like and acceptor-like interfacial traps are compared with the measurement results in Figure 5.

The “Forward” sweep direction intends for the bias voltage to be swept from negative voltage to positive voltage, and the “Reverse” sweep direction intends for the bias voltage to be swept from positive voltage to negative voltage.

According to (20) and (21), by tuning the number of donor-like interfacial traps in the accumulation region during the forward sweep and acceptor-like interfacial traps in the inversion region during the reverse sweep, good agreements between the measured and calculated hysteresis can be achieved. The extracted trap density is listed in Table 2.

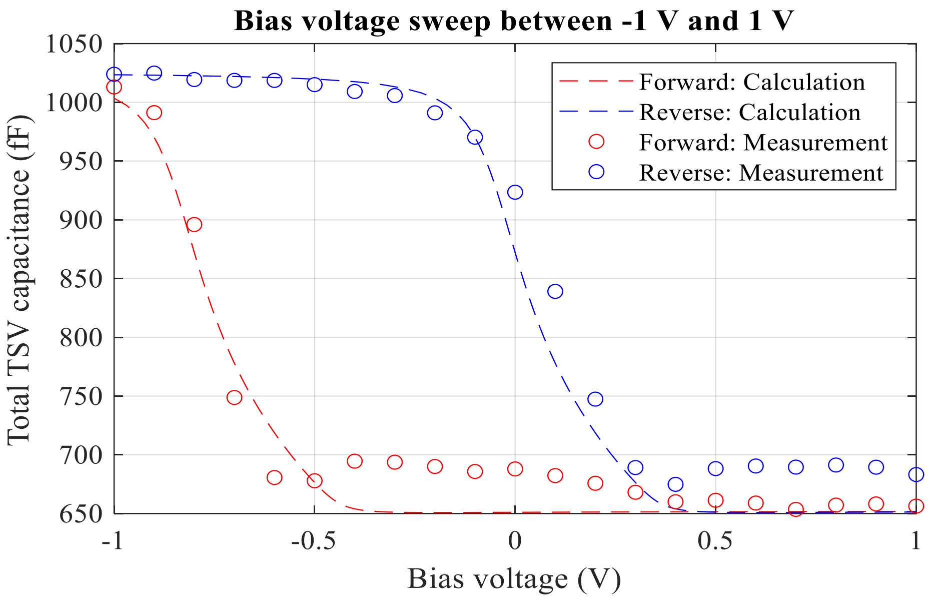


(a)



(b)

Figure 5. Hysteresis when the applied bias voltage is swept between ±3 V, ±1.5 V, and ±1 V.



(c)

Figure 5. Hysteresis when the applied bias voltage is swept between ±3 V, ±1.5 V, and ±1 V. (a) Bias voltage swept between ±3 V; (b) Bias voltage swept between ±1.5 V; (c) Bias voltage swept between ±1 V (cont.).

Table 2. Extracted trap density.

Trap density / Bias range	Forward sweep (min → max) $\rho_{t\ donor\text{-}like\ trap}$	Reverse sweep (max → min) $\rho_{t\ acceptor\text{-}like\ trap}$
±3 V	-2.1439e11 /cm^2	1.6693e11 /cm^2
±1.5 V	-0.8474e11 /cm^2	0.1356e11 /cm^2
±1 V	-0.5593e11 /cm^2	-0.3051e11 /cm^2

Furthermore, the trap density vs. the starting value of bias voltage in the forward and reverse sweep direction is shown in Figure 6.

In the forward bias sweep where the bias voltage starts from a negative value and the TSV is in the accumulation region first, the smaller the initial negative bias voltage is applied, the larger the number of donor-like trap density will be. In the reverse bias sweep where the bias voltage starts from a positive value and the TSV is in the inversion region first, the larger the initial positive bias voltage is applied, the larger the number of acceptor-like trap densities will be.

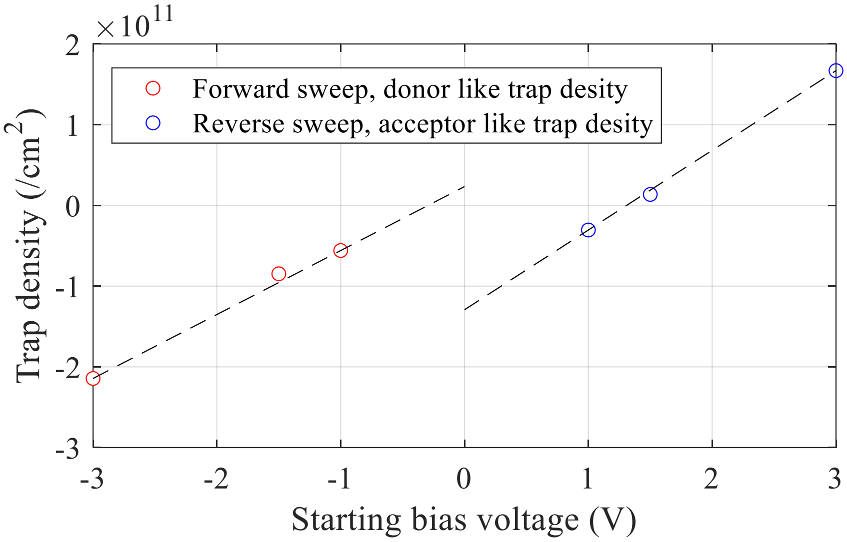


Figure 6. Trap densities vs. starting value of the swept bias voltage in forward and reverse directions.

3.2. TSV HYSTERESIS WITH TEMPERATURE

In a 3D IC system with large power consumption, the temperature inside the chip can be much higher than room temperature even with the heatsinks. Therefore, the effect of temperature on the performance of the TSVs needs to be characterized.

Based on the analytical model in Section 2, the main affecting parameters by the temperature during the C_{TSV} calculation are the intrinsic carrier concentration (n_i), the permittivity of SiO2 and Si (ε_{SiO2}, ε_{Si}), and the interfacial traps (Q_{trap}). (22) shows the equation for calculating the intrinsic carrier concentration with temperature.

$$n_i = \sqrt{N_c(T)N_v(T)}e^{-E_g/2kT} = 3.9\times 10^{16} T^{3/2} e^{\left(-\frac{1.21eV}{2kT}\right)} \text{ cm}^{-3} \tag{22}$$

where the parameters in (22) are defined in Table 3.

Table 3. Definition of parameters.

Parameter	Description	Value
k	Bolzman constant	1.3806488e-23 (J/K)
N_c	Effective density of states in the conduction band	$N_c = 2\left[\frac{2\pi m_n kT}{h^2}\right]^{3/2}$
N_v	Effective density of states of the valence band	$N_v = 2\left[\frac{2\pi m_p kT}{h^2}\right]^{3/2}$
E_g	Band/energy gap of Si	1.21 eV
T	temperature	300 K, 330 K, and 360 K measured

According to [17] and [18], the permittivity of SiO2 and Si are increasing with an increase in temperature:

$$\varepsilon_{SiO2} = 4.1 + k_{SiO2}\left(T - 300\right) \tag{23}$$

$$\varepsilon_{Si} = 11.55 + k_{Si}\left(T - 300\right) \tag{24}$$

According to [19], the surface interfacial trap density also shows a linear relationship with the temperature, as is shown in (25). Figure 7 shows the measured hysteresis of C_{TSV} vs. bias voltage at 300 K, 330 K, and 360 K. And the quantitative parameters extracted from the measured hysteresis are listed in Table 4.

$$\frac{Q_{trap}}{q}(T_0)=\frac{Q_{trap}}{q}T_0+k_{trap}\cdot(T-T_0) \tag{25}$$

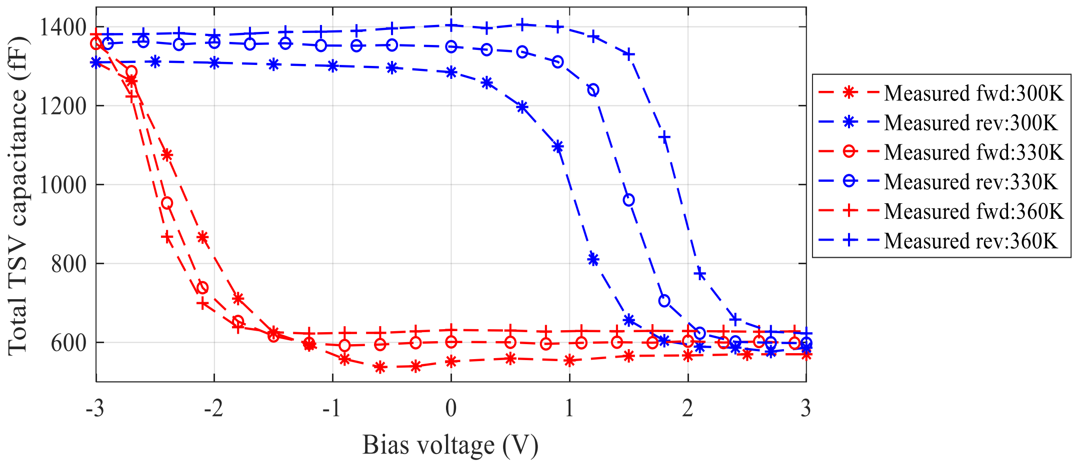


Figure 7. Measured *C-V* hysteresis under 300 K, 330 K and 360 K.

Table 4. Parameters extracted from the measured hysteresis at 300 K, 330 K, and 360 K.

T	300 K	330 K	360 K
C_{accu} (fF)	1312	1355	1384
C_{inv} (fF)	570	599	622
ΔC (fF)	742	756	762
V_{FB_fwd} (V)	-2.7	-2.8	-3
V_{TH_fwd} (V)	-0.9	-1.3	-1.6
V_{FB_rev} (V)	0.3	0.9	1.2
V_{TH_rev} (V)	2.1	2.4	2.6
Hysteresis opening (V)	3	3.7	4.2

In the accumulation region, the capacitance of the SiO2 layer is approximately the same as the C_{TSV}, assuming the charges are only distributed on the surface between the SiO2 layer and Si layer, as is shown in (26). Therefore, the C_{TSV} increases with the increasing temperature, which is due to the permittivity of SiO2 (ε_{SiO2}) increasing with temperature.

$$C_{TSV} \approx C_{ox} = \frac{2\pi\varepsilon_{SiO2}}{\ln\left(\frac{R_{TSV}+t_{oxide}}{R_{TSV}}\right)} h_{TSV} \cdot surface\_constant \tag{26}$$

In the inversion region, the C_{TSV} is calculated as the series connection between the SiO2 layer and the maximum depletion layer, as is shown in (27). With the increasing temperature, the permittivity of SiO2 increases, leading to an increase in C_{ox}. Meanwhile, the permittivity of Si also increases with time. Besides, from (28) and (29), the maximum depletion width W_{dep_max} vs. temperature is shown in Figure 8, which indicates a reducing tendency of W_{dep_max} when the temperature increases no more than 440 K.

$$\begin{aligned} C_{TSV} &= \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{dep\_\max}}} \\ &= \frac{1}{\frac{1}{\frac{2\pi\varepsilon_{SiO2}}{\ln\left(\frac{R_{TSV}+t_{oxide}}{R_{TSV}}\right)} h_{TSV} \cdot surface\_constant} + \frac{1}{\frac{2\pi\varepsilon_{si}}{\ln\left(\frac{R_{TSV}+t_{oxide}+W_{dep\_\max}}{R_{TSV}+t_{oxide}}\right)} h_{TSV}}} \end{aligned} \tag{27}$$

$$W_{dep\_\max} = \sqrt{\frac{4\varepsilon_{Si}\ \phi_F}{qNa}} \tag{28}$$

$$\phi_F = \frac{kT}{q}\ln\frac{Na}{n_i} = \frac{1}{q}\left(\frac{1.21eV}{2} - 3.3T - T\ln T^{3/2}\right) \tag{29}$$

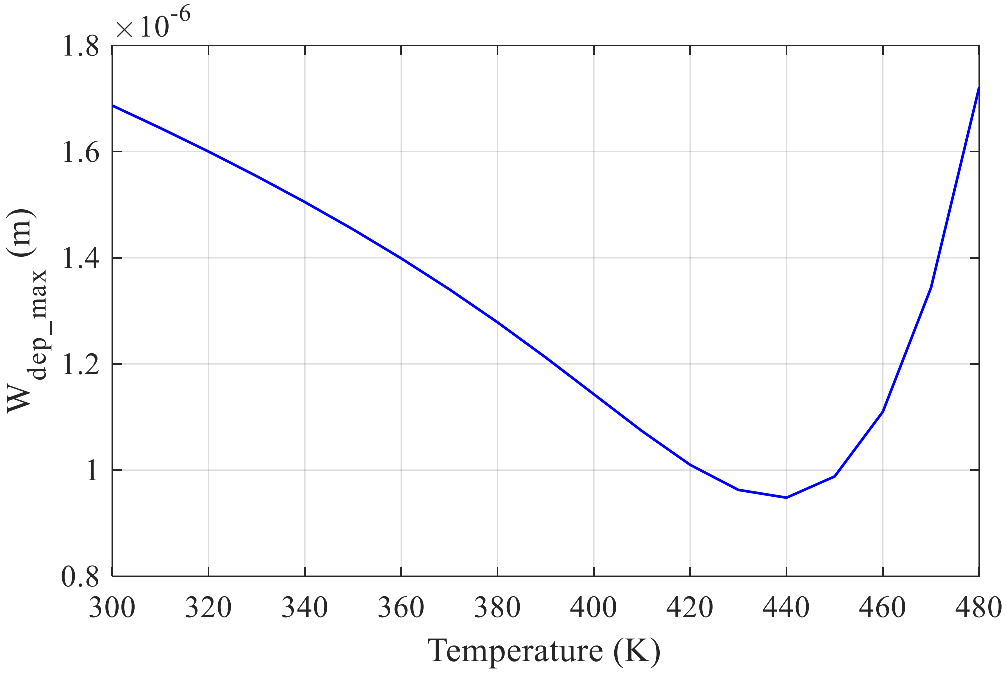


Figure 8. W_{dep_max} with temperature.

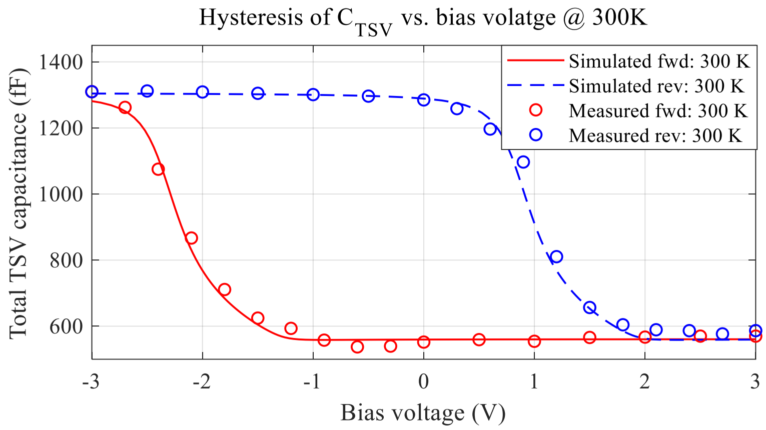
By tuning the coefficient k_{SiO2}, k_{Si} and Q_{trap} for donor-like and acceptor-like traps in (23) – (25), the calculated and measured hysteresis can be matched well, as is shown in Figure 9. The empirical equation for ε_{SiO2}, ε_{Si}, $\frac{Q_{trap\_donor\_like}}{q}$, $\frac{Q_{trap\_accecptor\_like}}{q}$ are shown in (30) – (33).

$$\varepsilon_{SiO2} = 4.1 + 0.145 \times (T - 300) \tag{30}$$

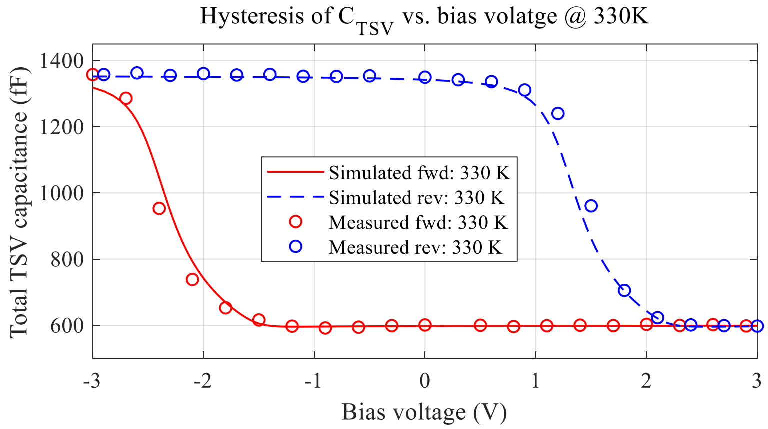
$$\varepsilon_{Si} = 11.9 + 0.0015 \times (T - 300) \tag{31}$$

$$\frac{Q_{trap\_donor\_like}}{q}(T) = \frac{Q_{trap\_donor\_like}}{q}(T_0) + 0.006e11 \cdot (T - T_0) \tag{32}$$

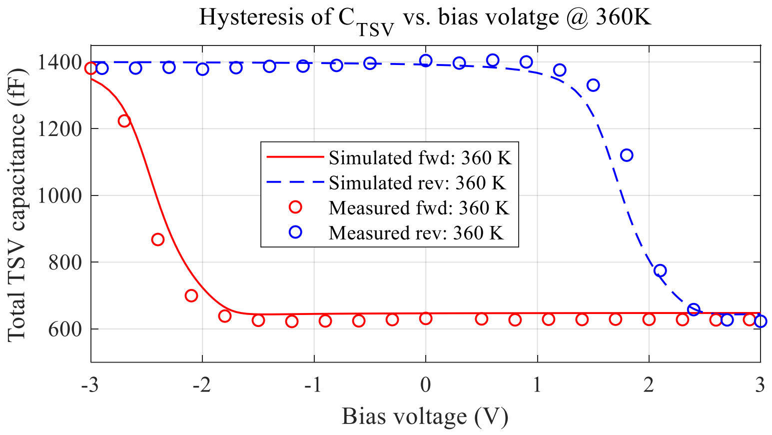
$$\frac{Q_{trap\_accecptor\_like}}{q}(T) = \frac{Q_{trap\_accecptor\_like}}{q}(T_0) + 0.017e11 \cdot (T - T_0) \tag{33}$$



(a)



(b)



(c)

Figure 9. Hysteresis comparison between measurement and calculation. (a) 300 K; (b) 330 K; (c) 360 K.

3.3. TSV HYSTERESIS WITH LIGHT INTENSITY

In 3D ICs embedded with CMOS image sensors (CIS), there will be TSVs connecting the photodiodes in the top layer and the circuits or DRAMs in the middle layers [20]. However, when light/image interacts with such 3D IC, the Si substrate will also be affected by light, which will also detune the performance of the TSV structures. Therefore, the effect of light intensity on the TSV hysteresis curve is studied.

The mechanism of light absorption by the semiconductor is the energy in the incident photons (E_{ph}) to create electron-hole pairs in the semiconductor [21]. When the energy of the photon (E_{ph}) is smaller than the bandgap (E_G) between the valence and conductance band of Si, i.e., $E_{ph} < E_G$, no electron and hole pairs can be created. When $E_{ph} \geq E_G$, the photons will be absorbed, and electron-hole pairs will be created. Due to a large number of majority carriers in the doped Si, the increase in the number of majority carriers due to the absorbed photon can be neglected. However, due to the very small amount of minority carriers in the doped Si, the increase in the number of minority carriers due to the absorbed photon is significant. From the semiconductor fundamental theory, there is:

$$n \cdot p = n_i^2 \tag{34}$$

where n and p are the concentrations of electrons and holes in the Si.

Therefore, the intrinsic carrier concentration will increase due to the increase of the minority carriers when the incident photons with enough energy are absorbed by the semiconductor.

Figure 10 shows the measured *C-V* curve in the forward bias sweeping under different light intensities. The C_{TSV} in the inversion region increases with the increasing light intensity, which is caused by the reduced W_{dep_max} due to the increasing intrinsic carrier concentration, as is shown in (27) - (29). The quantitative C_{TSV} in the accumulation and inversion region under different light intensities are listed in Table 5.

Based on the measured C_{TSV} in the inversion region under different light intensities, the n_i is calculated and plotted in Figure 11, which is approximately a linear relationship.

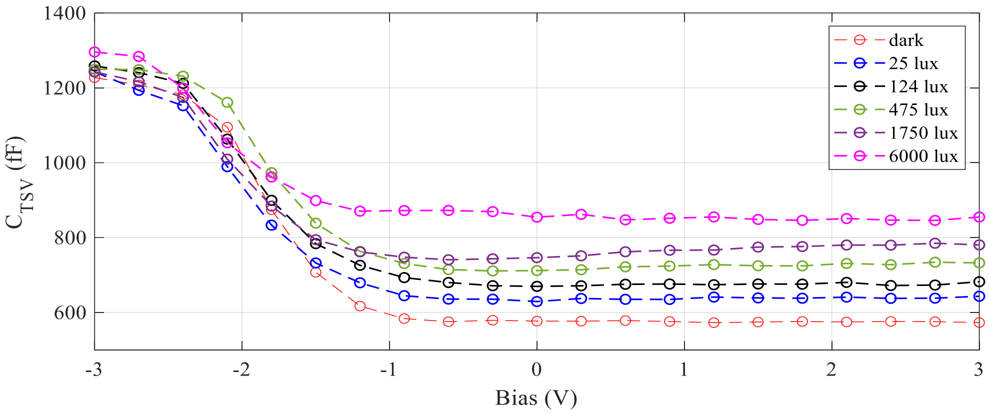


Figure 10. *C-V* curve in the forward bias sweeping under different light intensities.

Table 5. C_{TSV} in accumulation and inversion regions under different light intensities.

Light intensity (lux)	Cap accumulation (fF)	Cap inversion (fF)
1	~1265	570
25	~1269	643
124	~1265	680
470	~1265	730
1750	~1267	780
6000	~1271	855

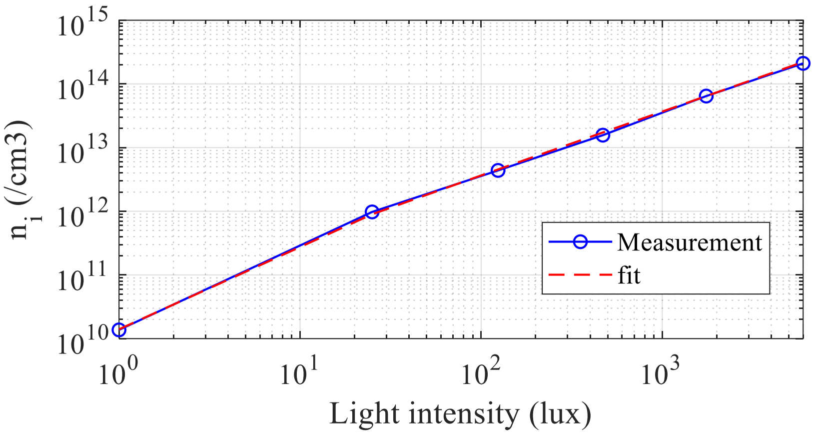


Figure 11. Intrinsic carrier concentration vs. light intensity.

Furthermore, an empirical equation for n_i vs. light intensity is extracted as (35).

$$n_i \approx 1.4e10 + 3.6799e10 \cdot Light\ intensity \quad \mathrm{cm}^{-3} \tag{35}$$

4. PI ANALYSIS OF SYSTEM PDN WITH TSVS

In JEDEC standards such as JESD235B, the core supply voltage (VDDC) of an HBM IC is recommended in the range of 1.14 V – 1.26 V with a typical value of 1.2 V. The maximum rated DC voltage of VDDC is -0.3 V – 1.5 V. Therefore, when the HBM system is powered up or down, the TSV capacitance will change accordingly. According to the specification in the JESD235B, 2 – 12 layers of DRAM dies/chips can be stacked in the 3D IC. From the recommended micro-bump array and the ball map of the VDDC net, it is roughly estimated that the number of P/G TSV pairs in one DRAM die can be greater than 880. The large number of TSVs will cause a non-negligible capacitance effect on the power distribution network of a system. However, during the traditional power integrity (PI) evaluation of the 3D IC or a system with 3D IC, engineers always use the C_{ox} as the C_{TSV} without considering the depletion/inversion effect of the TSV when applying a bias voltage, which increases the risk of over/under-estimating the potential PI issues in the system. Therefore, in this section, a hierarchical PDN model from PCB to on-die PDN is built to show the importance of considering the depletion effect of the power/ground (P/G) TSVs.

4.1. PDN MODEL WITH TSVS

The assumptions of the hierarchical PDN model are shown as follows:

a) The DRAM dies are four-layer stacked.

b) The on-chip decoupling capacitance in each DRAM die is 2 nF.

c) There are 1200 P/G TSV pairs in each interconnect layer.

d) When the power is on, the P/G TSVs are in the inversion region with a capacitance (C_{TSV}) of 580 fF each; When the power is off, the P/G TSVs are in the accumulation region, with a capacitance (C_{TSV}) of 1250 fF each.

e) The Z_{11} is simulated looking from the top DRAM die to the PDN of the PCB.

f) The size of the on-chip PDN is assumed as 5.5 mm by 7.3 mm [22].

g) The size of the Si interposer PDN is assumed as 28 mm by 36 mm [22].

The hierarchical PDN model is shown in Figure 12. Under power on and off conditions, the simulated PDN impedance will have different resonances in the frequency range of around several hundreds of MHz due to different values of the P/G TSV capacitances used, as is shown in Figure 13.

If applied a switching current of 2.75 A at 233 MHz and 265 MHz, the ripple noise in VDD can be simulated under power on and off conditions. As is shown in Figure

14 and Figure 15, the ripple noise simulated in the power-off case is around 370 mV higher than the power-on case at 233 MHz and around 580 mV lower than the power-on case. Therefore, the TSV capacitance when powered on should be considered individually and can’t be assumed as the capacitance when powered off.

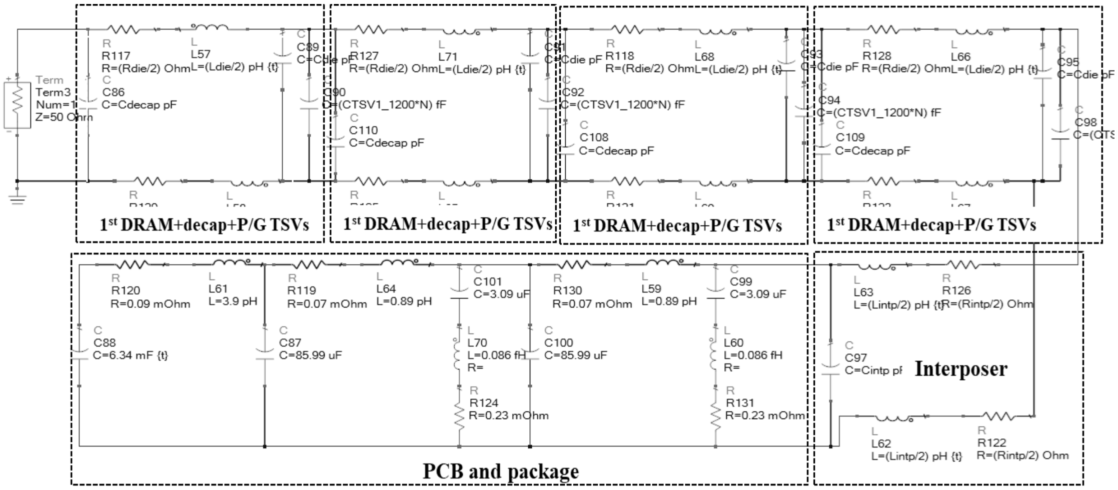


Figure 12. Hierarchical PDN model.

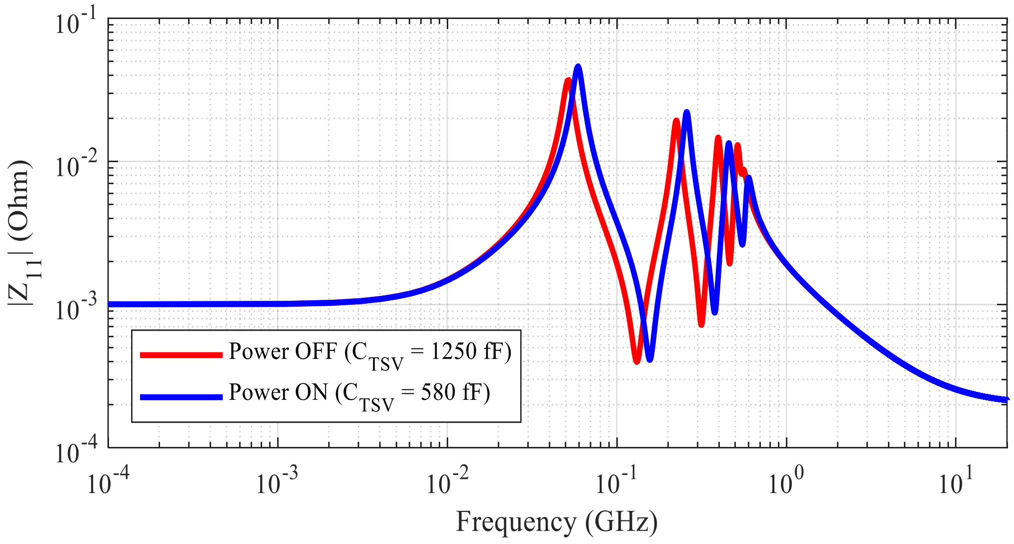


Figure 13. Z_{11} simulated from the hierarchical PDN model.

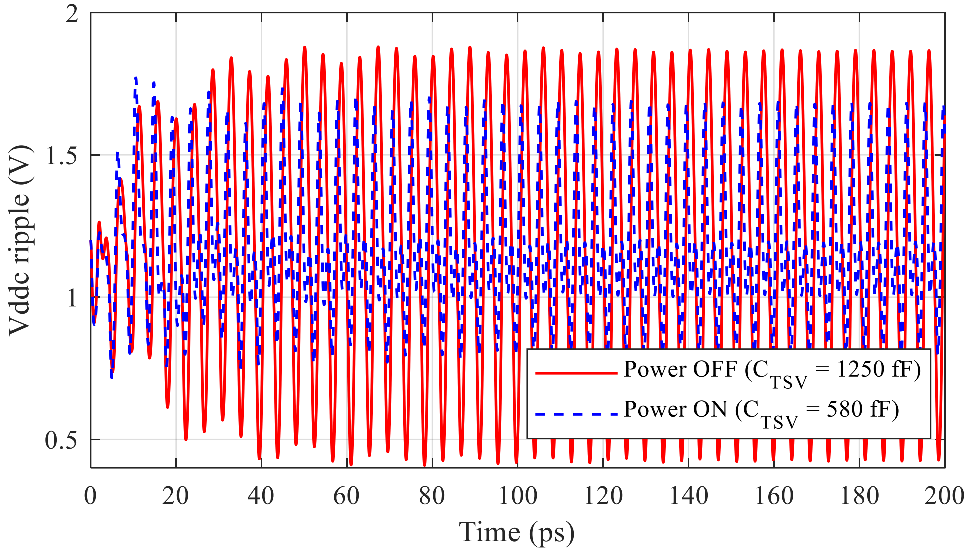


Figure 14. Ripple noise in VDD at 233 MHz.

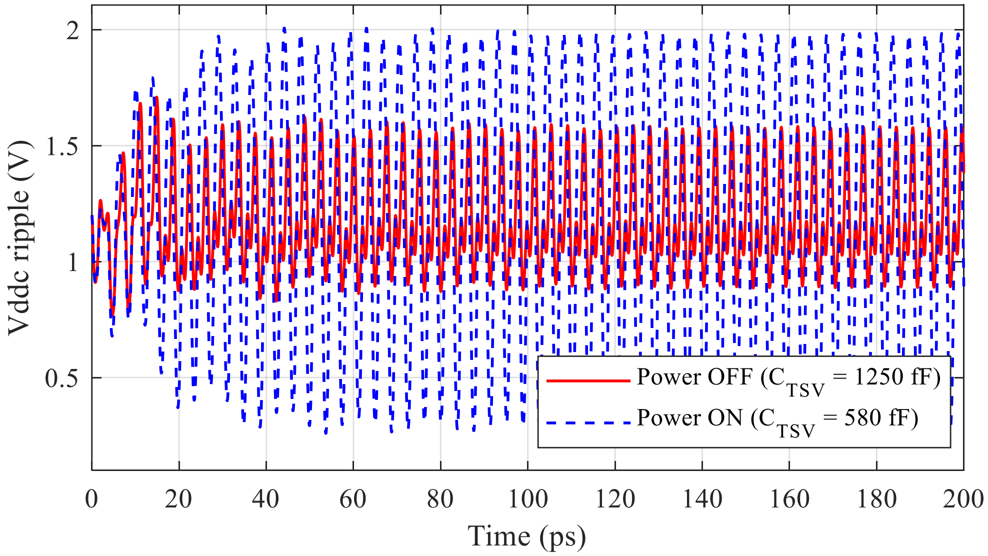


Figure 15. Ripple noise in VDD at 265 MHz.

Furthermore, the power-supply-induced jitter is also evaluated by adding the noisy power supply signals in Figure 15 to a DDR model I/O buffer [23]. The circuit model is shown in Figure 16.

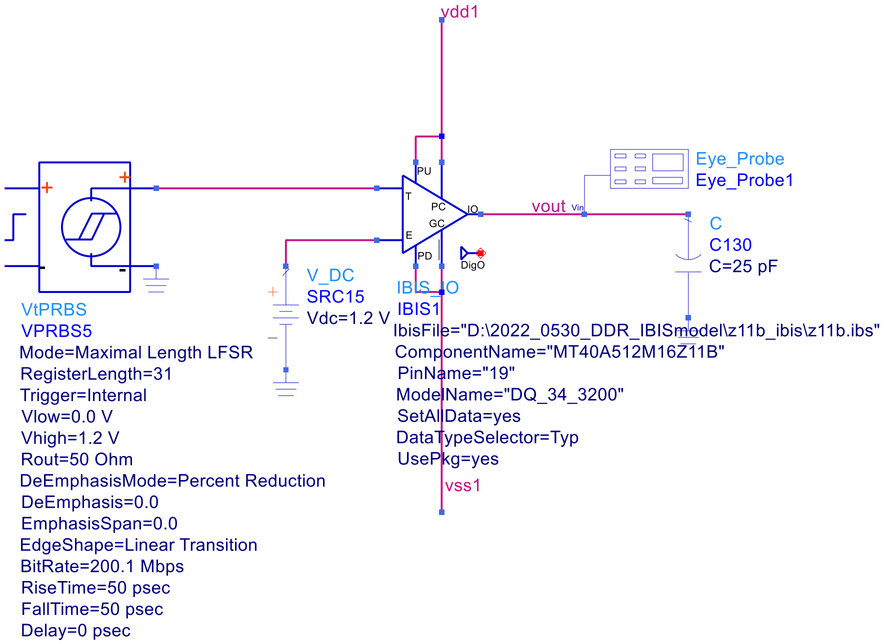
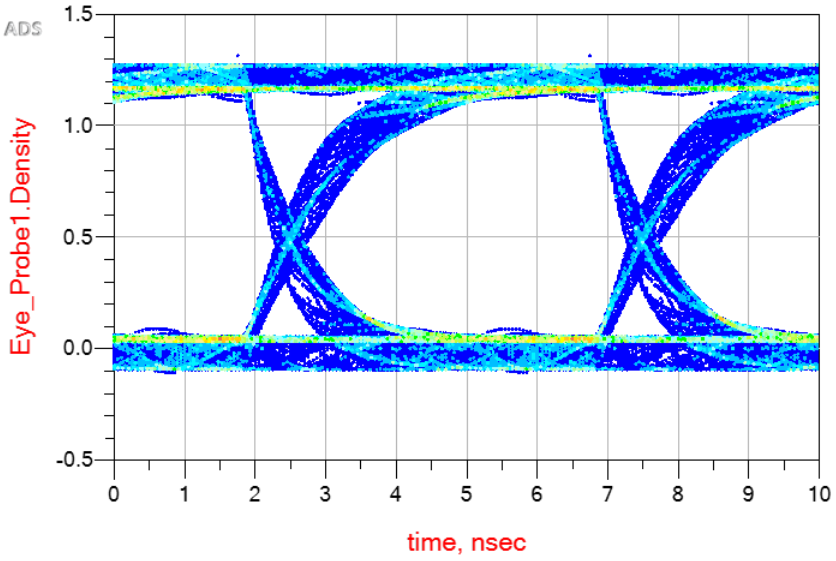


Figure 16. Circuit model for power-supply-induced jitter simulation.

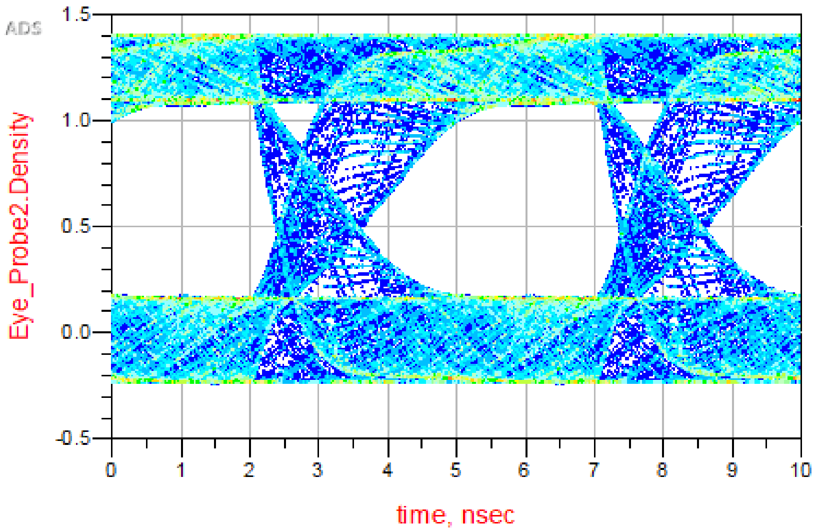
Table 6. Eye diagram information.

Trap density Bias range	Eye Height	Eye Width	Peak-peak jitter
Not consider the TSV bias effect	0.965 V	4.648 ns	450 ps
Consider the TSV bias effect	0.827 V	3.773 ns	1.274 ns

The simulated eye diagram caused by the PDN noise with and without considering the bias effect on the P/G TSVs is shown in Figure 17. The detailed parameters extracted from the eye diagram simulated with and without considering the bias effect of the P/G TSVs are compared in Table 6. It is shown that at 265 MHz, when considering the bias effect of the P/G TSVs, the larger power noise will cause the eye diagram of the output data signals to become worse, with smaller eye openings and larger peak-peak jitter. However, when not considering the bias effect of the P/G TSVs, the estimated eye diagram of the output data signal will be underestimated at this frequency.



(a)



(b)

Figure 17. Simulated eye diagram with/without the bias effect on TSV structure. (a) Case1: PDN noise added, not consider the bias effect; (b) Case 2: PDN noise added, consider the bias effect.

4.2. MITIGATION ON C_{TSV} IN THE INVERSION REGION

From the discussion in Section 4.1, the current bias voltage such as 1.2 V of a 3D IC system could make the P/G TSVs in the inversion region, which will reduce the total TSV low-frequency capacitance almost by half and cause discrepancies in evaluating the PI risk of the system with 3D IC if one fails to consider the bias effect on the P/G TSVs.

As the C_{TSV} in the inversion region is complicated to estimate and with a relatively low value, in practice the large SiO2 capacitance of TSV is preferred to be used for PI estimation if possible. Therefore, a method to keep the C_{TSV} in the inversion region still the same as C_{ox} is proposed even under a certain bias voltage.

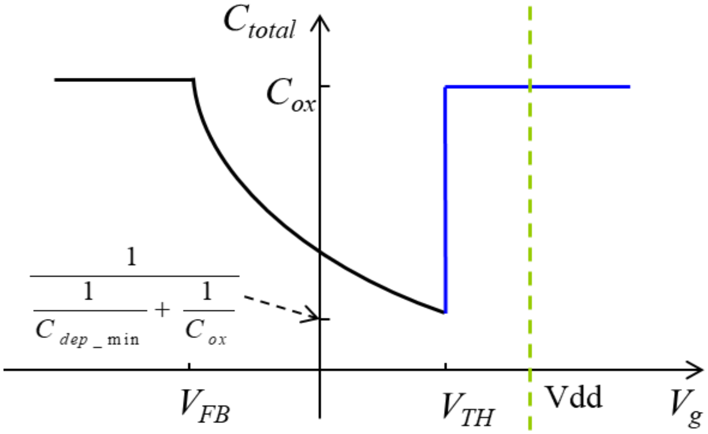


Figure 18. C-V curve of MOS transistor.

From a MOS transistor with a P-type Si, an N-doped region is created at the surface between the SiO2 and Si, which can offer electrons immediately (in an order of 1e-10 ~ 1e-13s) to respond to the AC small-signal change at the DC bias voltage [16]. The ionized acceptors in the maximum depletion region will not play a role in responding to the AC small signal. Therefore, the capacitance of the MOS transistor will recover to

C_{ox} without any capacitive effect caused by the maximum depletion region. Figure 18 shows a *C-V* curve of the MOS transistor.

Similarly, as is shown in Figure 19, if an N-doped area is formed nearby the SiO2 layer and the Si layer, the C_{TSV} in the inversion region will also recover to C_{ox}. Therefore, although a bias voltage is applied to such P/G TSVs, the C_{TSV} under a certain bias voltage will show the same capacitance as the power-off case as long as the bias voltage is large enough to make it in the inversion region. A similar idea was also proposed in [24].

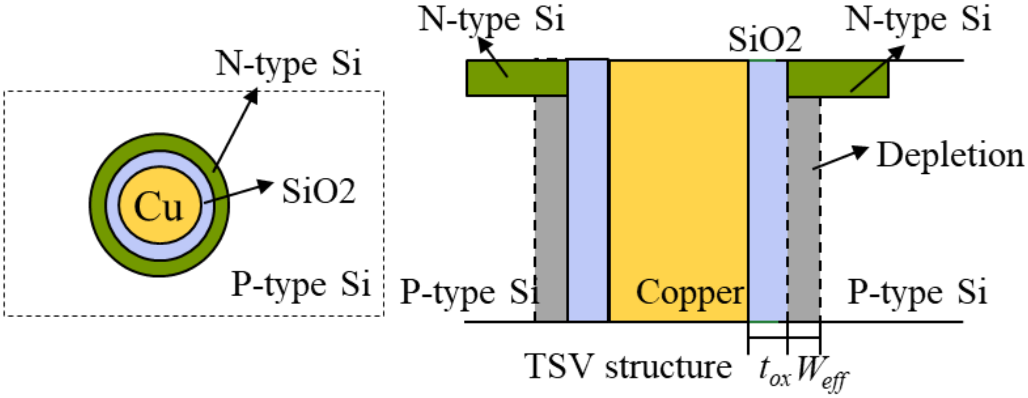


Figure 19. New TSV structure with N-doped region.

The limitation of this new TSV structure is that the bias voltage is large enough to make the TSV in the inversion region. However, with the development of the 3D ICs, the VDD tends to be reduced year by year. In the future, the VDD could be lower than 0.6 V. Therefore, the assumption of the inversion region may not hold for the future bias voltage condition. The C_{TSV} will fall into the depletion region instead of the inversion region, which the model proposed in Section 2 will be needed to predict the accurate TSV capacitance to be used for PI evaluation.

5. CONCLUSION

This paper proposed an improved analytical model for predicting the hysteresis behavior of the TSV with different bias voltages, temperatures, and light intensities. The model could offer good accuracy compared to the measurement results with the assumption of certain interfacial traps. Besides, the relationship of interfacial traps with the starting value of the bias voltage and temperature is also extracted and discussed. Moreover, the relationship of the intrinsic carrier concentration with the light intensity is extracted and discussed. Based on the bias effect on the TSV electrical performance, the potential PI issue in 3/2.5 D IC systems with a large amount of bias- and temperature-dependent P/G TSVs are discussed. The importance of considering the bias effect of the P/G TSVs during PI estimation is emphasized. Finally, a method to mitigate the low C_{TSV} in the inversion regions is discussed.

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II. SYSTEM-LEVEL EMI OF AN ARTIFICIAL ROUTER SYSTEM WITH MULTIPLE RADIATORS: PREDICTION AND VALIDATION

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ABSTRACT

In a multi-modular system, an increase in the number of radiating optical modules will increase the electromagnetic emissions. This paper investigates the scaled tendency of the emissions in a router system loaded with hundreds of optical modules. An artificial router mimicking the real system was built to investigate this tendency. A patch antenna array mimics the radiation of the optical modules. It can be excited in in-phase and random-phase configurations. The measurement data verifies the theoretical analysis and the prediction from a statistical method without performing hundreds of different experiments on a real router. Assuming that all radiators are radiating at the same frequency and have similar radiation patterns with random phases, the average of the maximal directivity of the system will saturate if the number of radiators (N) is larger than 14. Furthermore, the average of the maximal electric field radiated will increase following a 10 log10 N (dB) tendency.

1. INTRODUCTION

In a backbone internet router, the optical modules are the dominating radiating sources [1]. Standards such as CISPR 32 [2] and FCC part 15 [3] have specified the emission limits of electronic devices when operating. However, they do not specify a detailed guideline for handling the devices that are comprised of a large number of radiators. As a result, it is difficult to always test and debug a fully populated system reaching such complexity. In such cases, the goal is to estimate the radiation of the fully populated system as well as the uncertainty of this estimation by testing a partially populated system. To achieve this, the scaling tendency needs to be known from theory/prediction, and it must be verified by experiments. As experiments on such very complex routers are difficult to perform, alternately a radiating structure that mimics the actual router system could be created and used for hundreds of experiments to obtain statistical data.

Mechanisms that cause the radiation of the optical modules are: 1) common mode noise caused by the unbalanced differential pairs [4], [5]; 2) imperfect contact between the optical module and cage; 3) imperfect contact between the cage and chassis [6]-[8]. Furthermore, fiber-weave-effects in the PCB can cause common mode in the driving signal [9].

With an increased number of optical modules, the system always has the potential to fail EMC regulations [10]. Early in a project phase, it is difficult to obtain sufficient hardware for a full test. Early EMC evaluations can only be done based on the characterization of the optical modules in a mock-up system or on systems that are sparsely populated. To avoid debugging in a late project phase, it is helpful to know the scaling tendency of emissions. For systems with numbers of similar emission sources, the International Telecommunication Union (ITU) recommended a statistical approach to estimate the system-level radiated emissions (RE) compliance in terms of probability [11]. Based on the individual emission of each radiator, the total emission was estimated with the assumption that the radiators have a random-phase distribution. In [12], a statistical analysis method was used to estimate the maximal increase of the radiated and conducted emissions from a multi-radiator system. However, no specified tendency of the Emax with the number of radiators was derived. In [13], a model of a dipole antenna array excited by random phases was used to mimic the radiation performance of the sources. The estimation of Emax was calculated statistically from 1 000 000 cases. However, the emission prediction methods in [11]-[13] were not verified by measurement.

In [14], the Emax from an electrically large radiation source with multiple sub-radiators was determined by considering the relationship between total radiated power (TRP), the maximal directivity (Dmax), and the maximal electric field (Emax). The Dmax was derived theoretically from the electrical size of the radiator and statistically from the simulation model. However, no physical explanation was provided to explain the tendency of Emax with the increasing number of radiators. Reference [15] discusses the factors to be considered for predicting the emission growth with the number of radiators. However, the growth tendency was extracted without a systematic measurement approach for validation. In [16], a statistical model based on the actual radiation characteristics of the optical modules was proposed. Possible reasons for the observed discrepancies between the measured and predicted Emax of the actual system are discussed in [17]. The authors of [18] discussed the correlation between different RE test methods and mathematically addressed the uncertainties in the conversion between the results from different test sites. However, for achieving the goal of basing regulatory compliance on combining limited measurements with a prediction of the full system, a more comprehensive validation is needed from measurement.

The main contribution of this paper lies in providing a well-controlled artificial system that allows for varying different EMC-related parameters. This allows validating our statistical analysis model of the tendency of radiation increase which is observed when the number of radiators increases. The advantage of the artificial system is its flexibility to operate in different controlled configurations. It allows for the selection of in-phase or random phase radiation of the different antennas, and they can be driven at the same frequency or slightly different frequencies.

This paper expands upon the information provided by the authors in [17]. Using experimental methods, it studied the increase of system-level EMI when adding radiators, and it validates the theoretical analysis and prediction provided in [17]. This is achieved by: 1) designing an artificial with similar radiation characteristics as the actual router system; 2) analyzing measurement data on the EMI tendency with an increasing number of radiators for different phase configurations; 3) and using measurement data to validate the simulation model and analysis provided in [17].

This paper is organized as follows. Section 2 uses the antenna array theorem and statistical simulation model to discuss the scaling tendency of the averaged maximal directivity ($<D_{\max}>$) and the averaged maximal electric field ($<E_{\max}>$) with the increasing number of radiators. Section 3 introduces the design of the artificial system. A comparison of the radiation characteristics between the single patch antenna and the optical module is provided. Section 4 is devoted to the validation of the scaling tendency of $<E_{\max}>$ under different system configurations. Section 5 concludes the paper.

2. SCALED EMI TENDENCY: THEORY AND PREDICTION

2.1. THEORETICAL ANALYSIS OF THE SCALED EMI TENDENCY

Figure 1 presents the router system. It was loaded with 15 line cards (LCs), each of which houses 30 to 36 plug-in optical modules.

The unintentional radiation is mainly around 10.31 GHz. The fully loaded system contains 16 LCs with more than 400 optical modules. Therefore, it is assumed that the leakage emission from the optical modules dominates the total radiation of the whole system at 10.31 GHz.

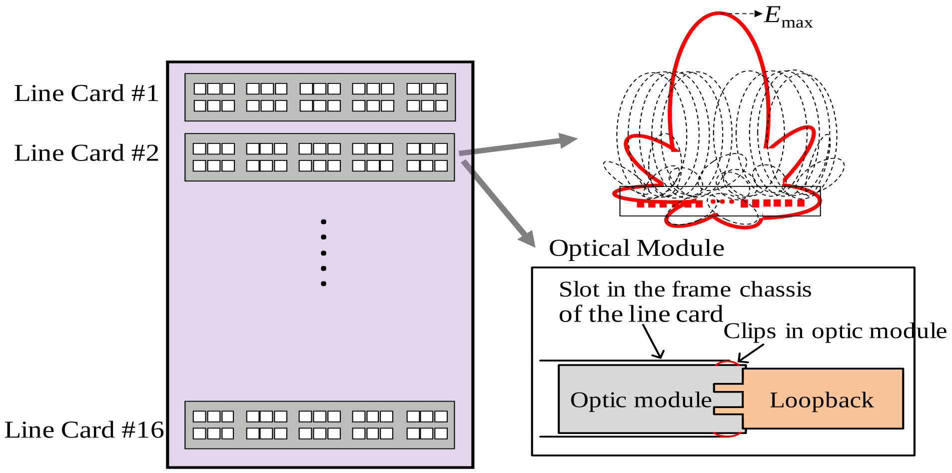


Figure 1. Router system description.

Normally, most optical modules in the system are from the same vendor and have similar mechanical structures. It is reasonable to assume that they also have similar radiation characteristics. Other radiation sources, such as cooling vents, are well controlled. Therefore, the loaded system can be considered to be an antenna array of radiating optical modules.

As unintentional radiators, the radiation efficiency of each optical module is very low. Therefore, the mutual coupling between the optical modules can be neglected. For an array of N-element antennas in the location (X_n, Y_n, Z_n), the far-field strength can be expressed as [19]:

$$E(\theta,\varphi) = E_0(\theta,\varphi)\sum_{n=1}^{N} A_n \exp(jk\Psi_n) \tag{1}$$

where $E_0(\theta,\varphi)$ is the radiation pattern of a single element along the θ axis and φ axis; A_n describes the excitation strength; Ψ_n is the phase relationship for adjacent elements:

$$\Psi_n = \Phi_n + X_n \sin(\varphi)\cos(\theta) + Y_n \sin(\varphi)\sin(\theta) + Z_n \cos(\varphi) \tag{2}$$

where Φ_n is the initial phase of each element.

Not only are the phase relationships between the optical modules within one LC important, but in addition, one also needs to consider the phase relationship between the LCs.

Theoretically, if all optical modules radiate in phase, a high gain antenna radiating into the frontal direction will be formed [20]. As the number of radiators increases, the value of Dmax will increase with 10 log10 N (dB) and the same does the TRP. Therefore, Emax will increase following a 20 log10 N (dB) tendency, with N being the number of radiators.

The system considered in this study had fixed, random-phase relationships between the optical modules within each LC, which is discussed in detail in Section III, part B. However, each LC used its own crystal (XTAL) source. Thus, frequencies between LCs differed by a few kHz. Within one LC, the radiation frequency between each optical module is the same. There are no time-invariant phase differences between LCs. In this case, the frequency differences are small enough to capture the total power of all the signals within one standard resolution bandwidth of the receiver during EMI testing (1 MHz). However, if each element is fed by a random-phase signal, it is unlikely that the array forms a high-gain antenna radiating in one specific direction. If many different phase realizations are analyzed statistically and $D_{\max}$ and $E_{\max}$ are determined for each realization, at a certain angle, waves from some radiators will add constructively and waves from other radiators will add destructively. After a certain number of radiators are added, it is very unlikely that the addition of more radiators will add constructively in one direction, and hence, the directivity ($\langle D_{\max} \rangle$) saturates, which is observed in [16] and [17]. The saturation of the $\langle D_{\max} \rangle$ was also observed in [18]. The value of the $\langle E_{\max} \rangle$ does not follow the 20 log10 N (dB) tendency.

Figure. 2 shows an example of the $\langle D_{\max} \rangle$ tendency for an array of radiators having the same radiation pattern and frequency as well as random-phase distribution. $\langle D_{\max} \rangle$ shows a saturation phenomenon when the number of radiators is larger than 14. As is shown in (3), the value of $E_{\max}$ in the far field can be related to the total radiated power and $D_{\max}$ by [17] - [21], where η_0 is the wave impedance in the free space. The total power radiated by the device under test (DUT) is TRP. The observation distance from the source is R.

$$E_{\max} = \frac{1}{R}\sqrt{\frac{\eta_0}{4\pi}\mathrm{TRP}\times D_{\max}} \tag{3}$$

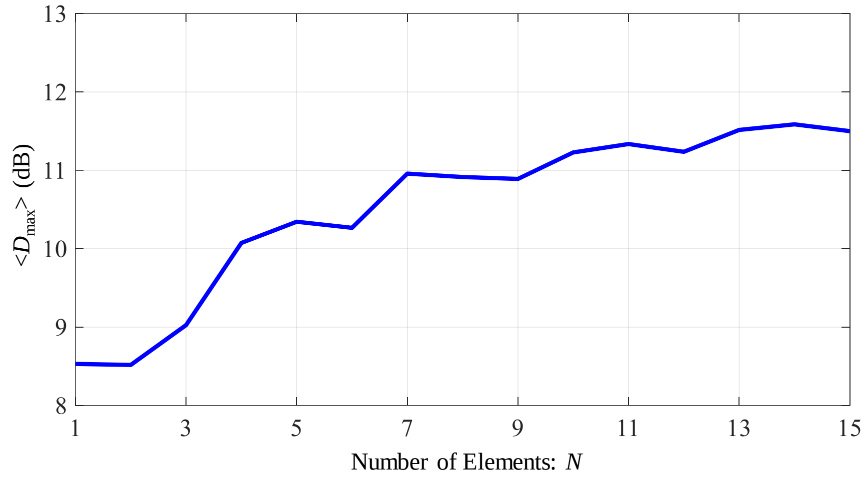


Figure 2. $D_{\max}$ tendency with an increasing number of radiators using the model provided in [16].

From (3), if <$D_{\max}$> saturates, <$E_{\max}$> will follow the tendency of TRP. The TRP is calculated as the spherical integral of the effective radiated power P(θ, φ). Numerically, it can be calculated by adding the sampled values of the power at N locations along the θ axis and M locations along the φ axis, shown in (4):

$$\mathrm{TRP} = \frac{1}{4\pi}\int_0^{2\pi}\int_0^{\pi} P(\theta,\varphi)\sin\theta\,\mathrm{d}\theta\mathrm{d}\varphi \approx \frac{\pi}{2NM}\sum_{n=1}^{N}\sum_{m=1}^{M} P(\theta_n,\varphi_m)\sin\theta_n \tag{4}$$

Therefore, for the random-phase distribution of an antenna array with similar radiating elements, the far-field <Emax> under many phase configurations of the elements was expected to follow a 10 log10 N (dB) tendency. As the TRP of the array increases linearly with the number of elements, the corresponding <Dmax> will saturate when the number of elements is larger than 14.

2.2. STATISTICAL SIMULATION MODEL

By measuring the emissions loaded with one optical module in one LC, the emission of a fully loaded system (16 LCs, each with 30 optical modules) can be predicted using the statistical simulation model proposed in [16] and [17]. The statistical model is based on the phase array antenna theorem and Monte Carlo simulation (MCS). The input of the model is the 3D radiation pattern of the single radiator, the number of the radiators, the distance between each radiator, and the distance of the observation point. The output of this model is a cumulative distribution function (CDF) describing the probability P(x) that the variable takes a value less than or equal to x, i.e., $P(x) \leq x$. This function gives a reliable prediction of the averaged total electric field emission (<Emax>) from the DUT, which helps compare the emissions to the standard limit.

The prediction assumes that the dominant radiating sources are the optical modules. The phase distribution is discussed in Section III, subpart B, and in [15, 16]. The phase shift between each module was random but repeatable. Each line card had different phase distributions. Therefore, it is reasonable to consider a random phase distribution for the radiators in the prediction procedure for each line card. The phase distribution of the radiators forms an independent random variable with uniform distribution. This makes the phased array antenna model an orthogonal model with all the independent variables in the model are uncorrelated. Since we ran the predictive model for thousands of iterations, we can get a cumulative distribution function (CDF) of <Emax> and predict <Emax> lower than a certain value with a certain probability.

All the radiators are under the following assumptions: 1) the same radiation frequency; 2) the same radiation pattern; 3) radiation observed in the far-field region.

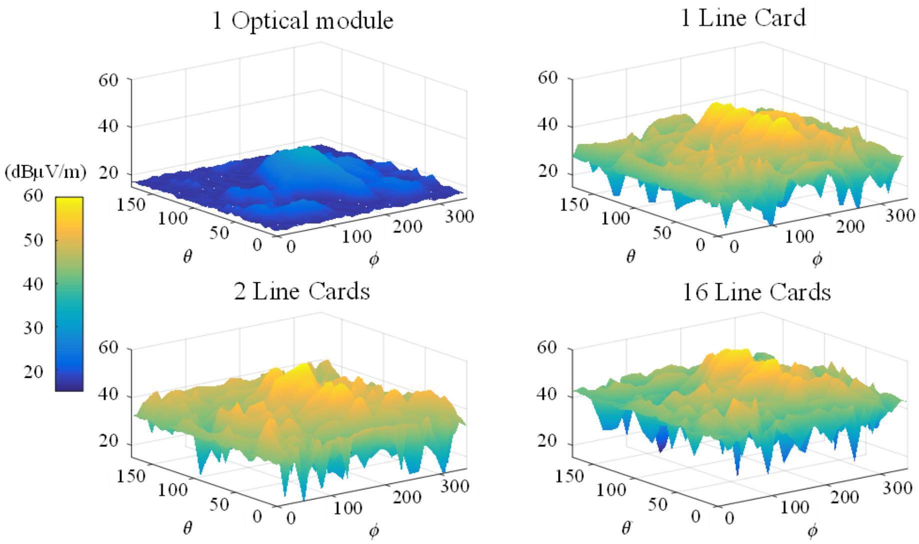


Figure 3. *E* field pattern of 1 optical module, 1 LC, 2 LCs, and 16 LCs in 1 random-phase realization in simulation [17].

Figure. 3 shows the radiation pattern of 1 optical module, one LC (16 optical modules), two LCs, and sixteen LCs under a certain random-phase distribution. The total radiation energy of the subsystems is randomly distributed to the front direction due to the random-phase distribution.

When the LCs are at slightly different frequencies (several kHz), the <Emax> was expected to follow a tendency slower than 10 log10 N (dB), i.e., 8 log10 N (dB). The total radiation measured by the instrument is added by power intensities instead of complex fields, which is discussed in detail in [17].

3. ARTIFICIAL SYSTEM DESIGN

Analyzing the emissions of an actual system for the effect of EMC relevant parameter variations such as the phasing of the radiators is difficult. These systems have no built-in function to vary such parameters. Therefore, a simplified artificial system is built to not only mimic the radiation but also to allow the analysis via repeated measurements under different phase excitations of the radiators. Once the behavior of the artificial system is validated against simulation, the statistical method can be applied to predict the emissions of a fully loaded system.

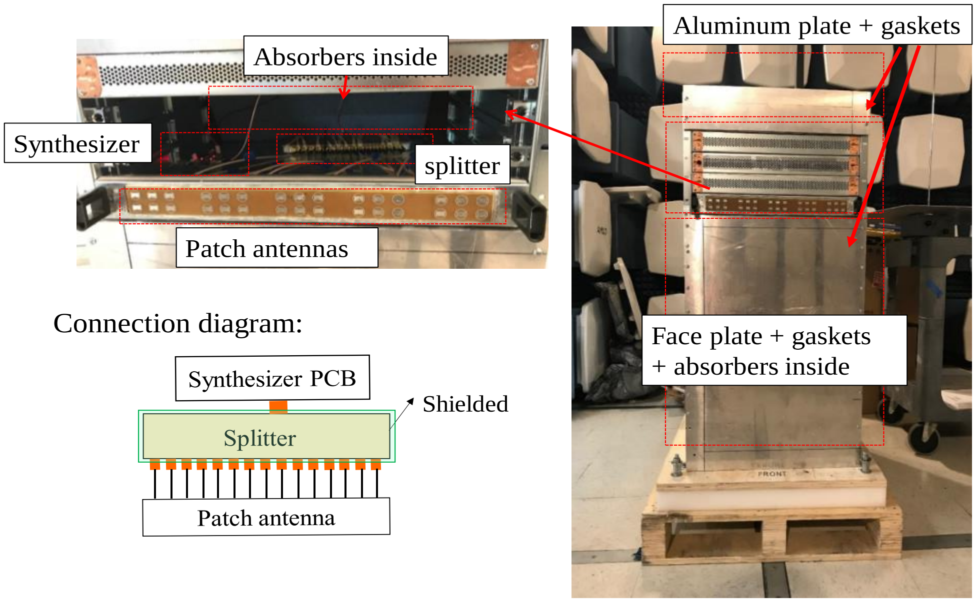


Figure 4. Artificial system description.

To avoid the complexity and cost of experiments on a real router system, an artificial system was built to mimic the real router system. It provides the RF excitation and allows control of the power, pattern, and phase at each radiating element. As shown in Figure. 4, the artificial system consists of five parts: a high-frequency synthesized source, power divider, patch antenna array, varying-length cables, and the chassis. The high-frequency synthesized source is set to 10.31 GHz. The power divider splits the signal with equal amplitude and phase. Cables of varying lengths are connected to feed the patches. By controlling the cable lengths and the number of patches used, the radiation of the actual router is reproduced. For each realization of different phases, the cables with different lengths are randomly exchanged.

3.1. HIGH-FREQUENCY SYNTHESIZED SOURCE

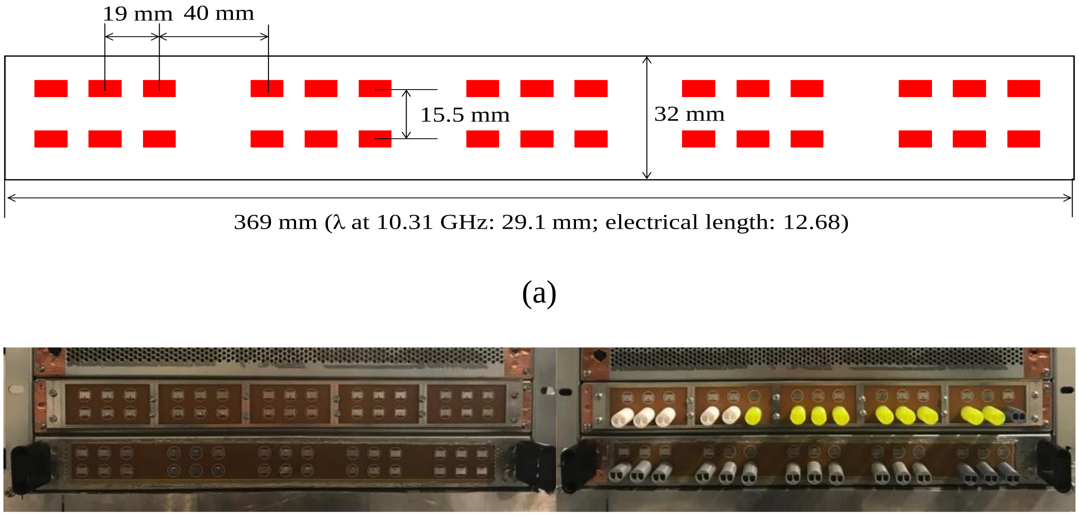
An ADF3555-based synthesizer provides -5 dBm at 10.31 GHz. Two Wilkinson power splitters (1 input and 16 outputs) feed the patches. The insertion loss was measured to be around 17 dB, which is 5 dB more than the value a lossless system would show.

3.2. PHASE CONTROL

For the actual router system under study, the relative phase of the radiation from each optical module was measured by near-field scanning using a measurement probe and a reference probe [15], [16]. The measured phase distribution for each optical module showed a random, stable distribution between - 180° and 180°. Rebooting did not change the phase, but each LC showed a different phase distribution. To mimic this random behavior, repeated measurements used different cable lengths to feed the patches.

3.3. PATCH ANTENNA ARRAY

A patch antenna array was designed initially to mimic an LC. Similar to the arrangement of the optical modules in the LC, two rows (each having 15 patch antennas) are used. However, unlike the radiation pattern of an optical module, a single patch antenna has a wide 3 dB beam width (≈ 96°). To narrow the beam width, a dielectric rod made of 3D printed polylactic acid (PLA, relative permittivity $\approx$ 3.5) material was mounted in front of the patch antenna. Figure. 5 shows the patch antenna array with and without rods. The rod bundles the beam of each patch antenna as it acts as a dielectric antenna. In the end, the single patch antenna has a dominating polarization in vertical polarization similar to a single optical module [15].



(a)

(b)

Figure 5. Patch antenna array and the system with different source configurations. (a) Dimensions of patch antenna array; (b) Patch antenna array; (c) Patch antenna array with optical fiber cables.

The reflection coefficient ($|S_{11}|$) of a single patch antenna with and without the rod is shown in Figure. 6. The holes on the rods are designed for the option of plugging in the fiber cables, similar to the optical modules. The resonant frequency for the designed patch antenna with the rod was around 10.31 GHz. The simulation was done in CST Microwave Studio [21]. Compared with the single patch antenna without the rod, the 3 dB beam width is reduced to 56°. For the single patch antenna with/without rod, most of the energy in these 2 cases radiates at 10.31 GHz. Therefore, in this study, using the patch antenna array either with or without the rod as the source does not affect the conclusion of the EMI tendency with the increasing number of radiators in this paper. This will be further shown in the measurement results in Section 4.

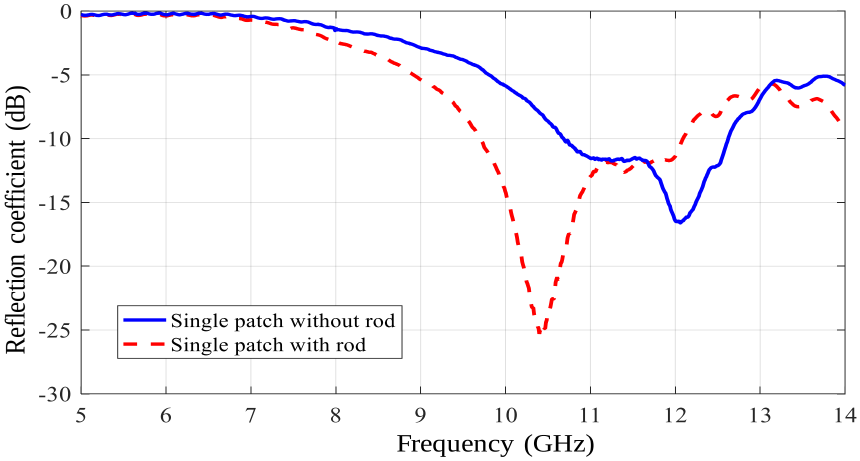
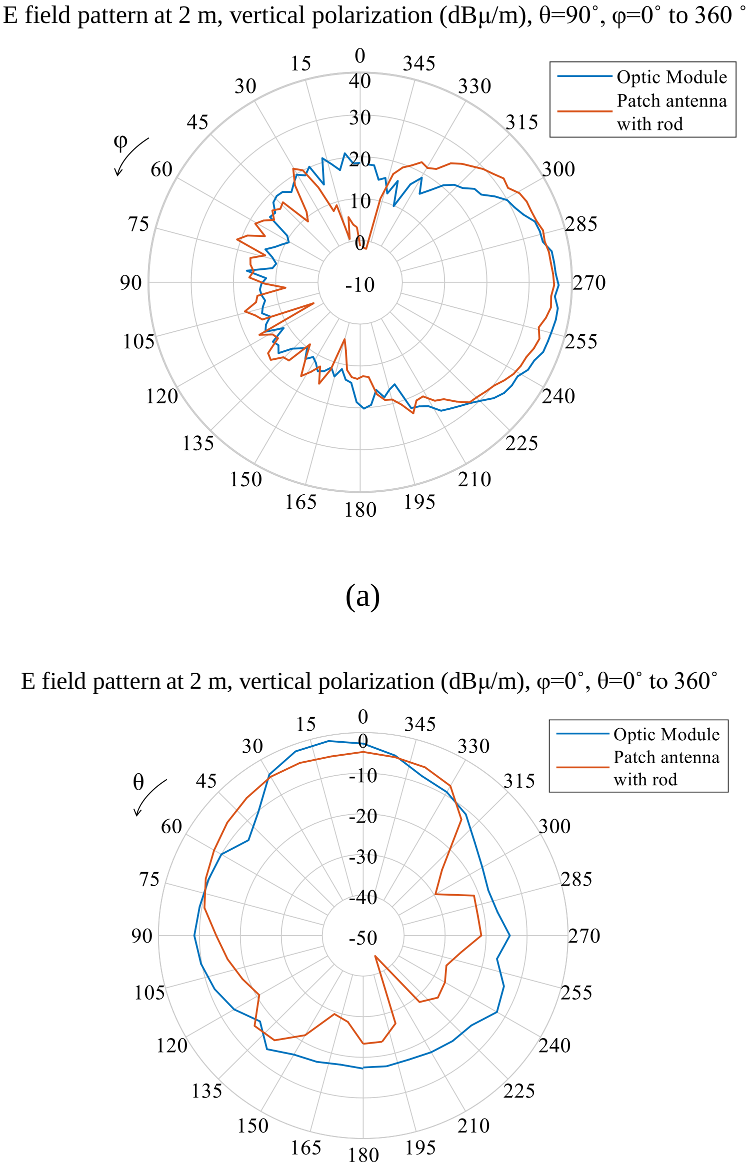


Figure 6. Reflection coefficient of a single patch in different configurations.

Adding 3D printed structures to the patches allows mimicking of the radiation pattern of other optical modules without having to change the PCB or feed structure. It further allows changing the radiated power of individual patch antennas by partially printing carbon-loaded filaments that add loss to the dielectric extension.

3.4. COMPARISON OF THE RADIATION CHARACTERISTICS BETWEEN A SINGLE OPTICAL MODULE AND PATCH ANTENNA WITH ROD

The radiation pattern of a single patch antenna with a rod and a single optical module was measured in an anechoic chamber at 2 m [15], [23]. The 3 dB beam width, dominating polarization, directivity, TRP, and Emax at 2 m could all be derived from the measured radiation pattern [19].



(a)

(b)

Figure 7. Comparison of 2D radiation pattern between patch antenna and optical module. (a) θ = 0˚, φ = 0 ˚ to 360˚; (b) φ = 0˚, θ = 0 ˚ to 360˚.

Figure. 7 shows the comparison of the E field pattern between the single patch antenna with rod and the single optical module in the θ = 90° and φ = 0° planes, vertical polarization. The radiation pattern of the patch antenna with rod matches the single optical module in the main radiation direction and polarization. Table 1 compares the single optical module and the patch antenna with rod for: 1) 3 dB beam width; 2) dominating polarization; 3) directivity; 4) TRP; 5) $E_{\max}$ at a distance of 2 m. The similarity between the single optical module and a single patch antenna allows the use of the artificial system to mimic the real router.

Table 1. Comparison of radiation characteristics between single optical module and patch antenna with the rod.

Parameters	Single optical module	Patch antenna (fed with -69 dBm)
Frequency (GHz)	10.31	10.31
3 dB beam width	45°	56°
Dominating polarization [16]	Vertical	Vertical
Directivity (dB)	7.7	8.5
TRP from radiation pattern (dBm)	-69.2	-68.7
$E_{\max}$ measured at 2 m (dBμV/m)	37.2	38.5

4. E_{MAX} SCALING VALIDATION AND DISCUSSIONS

Based on the artificial router system, the scaling tendency for TRP, $D_{\max}$, and Emax was measured under different configurations. The measurement was done to validate the prediction on the scaling tendency of $\langle D_{\max}\rangle$ and $\langle E_{\max}\rangle$ from theoretical analysis and the statistical model-based prediction given in Section 2.

4.1. TRP TENDENCY USING 1 TO 30 ELEMENTS ON RANDOM PHASE

It is expected that the TRP will increases linearly as more radiators are added to the system. Therefore, TRP will follow the 10 log10 N (dB) tendency if each radiator emits the same power.

To verify the behavior of the whole system, the TRP was measured for 1 to 30 patch antenna excitations in a reverberation chamber tent [24]-[27]. TRP was measured by averaging the received signal 500 times while shaking the tent to stir the modes. Each patch was fed with the power of -25.5 dBm at 10.31 GHz. By exciting different numbers of patch antennas and terminating the unused outputs of the power splitter, the TRP from 1 to 30 patch antennas was measured and compared in Figure. 8. When only one antenna was excited, the received TRP was 2.7 dB larger than expected as the radiated power of the synthesizer PCB itself was already -25 dBm. Measurement results showed that the TRP of multiple patch antennas added up linearly indicating a reliable test system.

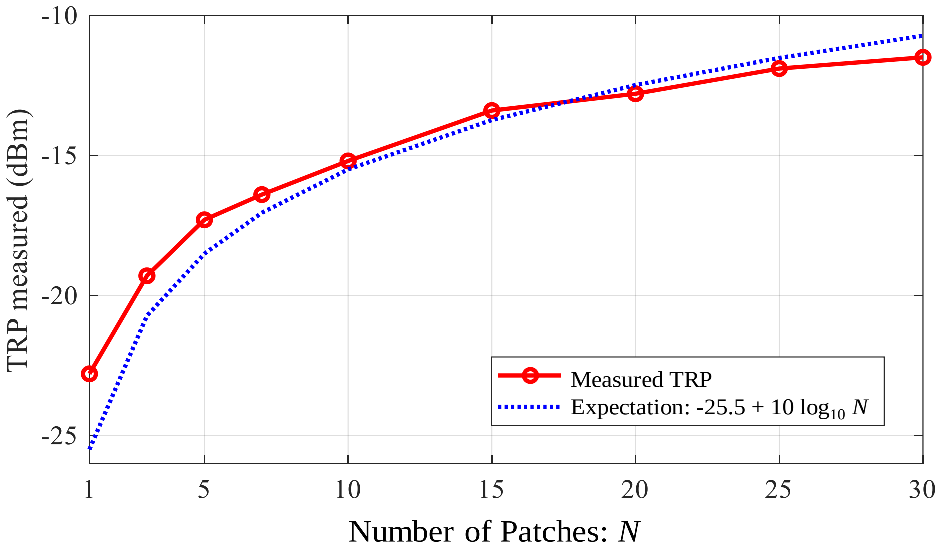


Figure 8. Comparison between measured TRP and expectation for 1 – 30 patch antennas.

4.2. SCALED *E*MAX FOR 1, 2, AND 4 PATCH ANTENNAS WITH IN-PHASE EXCITATIONS

For the in-phase configuration, the scaling tendency of $E_{\max}$ was analyzed with one, two, and four patch antenna elements. As the initial excitation phase of each patch is the same, the spacing between each patch antenna will determine the beamforming of the antenna array. In this configuration, the comparison between the measurement and theoretical expectation provided validation for the whole radiation emission (RE) set-up with the system under test. In the RE test set-up, a horn antenna (ETS-Lindgren 3115) was mounted on the antenna tower to perform a 1.5 m height scan with a step of 0.15 m. Absorbers were put on the floor to prevent the reflection from the ground. The $E_{\max}$ radiated from the artificial system at a 3 m distance was measured during the RE height scan. As the measurement configuration is only valid for an antenna array with 2 and 4 elements radiating at 10.31 GHz, the measured Emax at 3 m is in the far-field region considering the electric size of the array. Under in-phase configuration, Emax is expected to follow the 20 log10 N (dB) tendency with the number of radiators.

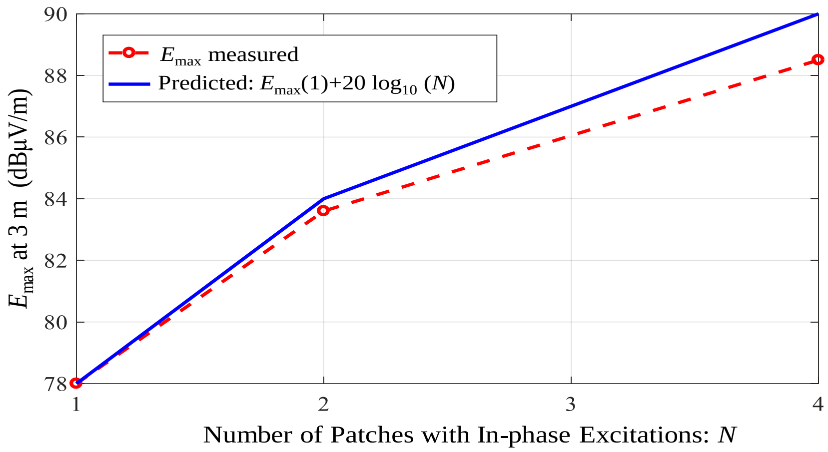


Figure 9. E_{max} tendency with the number of patches under in-phase excitations.

Figure 9 shows the measured E_{max} tendency for in-phase excitation at 3 m distance at 10.31 GHz. The Emax of the in-phase antenna array shows a tendency close to 20 log10 N (dB) with the increasing number of radiators. This matches with the theoretical analysis for the in-phase antenna array. Besides, this observation offers validation on the performance of the RE test set-up with the artificial system.

4.3. <E_{MAX}> TENDENCY FOR 15, 20, 25, AND 30 ELEMENTS WITH RANDOM-PHASE EXCITATIONS

For the random-phase configuration, the scaling tendency of Emax was analyzed using 15, 20, 25, and 30 patch antenna elements. In this configuration, the spacing between each patch antenna is no longer important as the statistical term <D_{max}> and <E_{max}> are studied from thousands of different random-phase distributions for the initial excitation phase of each patch antenna. Each element was fed with an RF power of around -31 dBm with 3 dB variations.

As random-phase excitations will give different emissions, statistical analysis should be based on the measured data under different random-phase cases. Randomization was achieved by switching the feed cables with different lengths from the splitter to the antennas. This was repeated six times for each number of the patch antenna elements. The value of $<E_{\max}>$ gives the average of the six tests statistically.

By comparing the tendency of EMI with an increasing number of radiators in simulation and measurement of the artificial system, validation is made on the estimation from statistical analysis. Two cases were studied in the random-phase configuration in terms of different sources: 1) Patch antenna array; 2) Patch antenna array with dielectric rods.

For the patch antenna array as the radiation source, the comparison of the measured and theoretically expected $<E_{\max}>$ tendency, relative to the number of radiators, is shown in Figure 10. As is discussed in Section II, when the phase distribution of the radiators is random, statistically the $<E_{\max}>$ will only follow the tendency of TRP as the directivity saturates when the number of the radiators increases larger than 14. The tendency of the measured $<E_{\max}>$ with the increasing number of radiators is close to 10 log10 N (dB) tendency, which validates the theoretical analysis. The predicted $E_{\max}$ range for 15 and 30 patch antennas under random-phase configuration with different probabilities is shown in Figure 11. For the artificial system with a patch antenna array in random-phase distributions, the measured $<E_{\max}>$ under different phase randomizations fell into the 40% to 90% probability range. With a large number of samples, the measured $\langle E_{\max} \rangle$ can reach the minimum and maximum limit shown in the prediction.

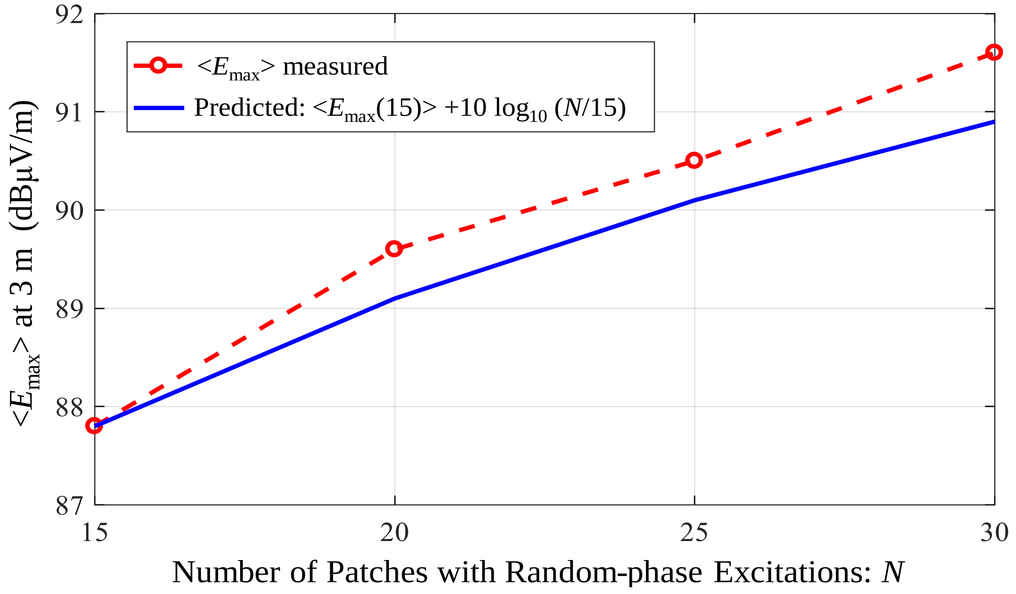


Figure 10. $\langle E_{\max} \rangle$ tendency in random phase excitations.

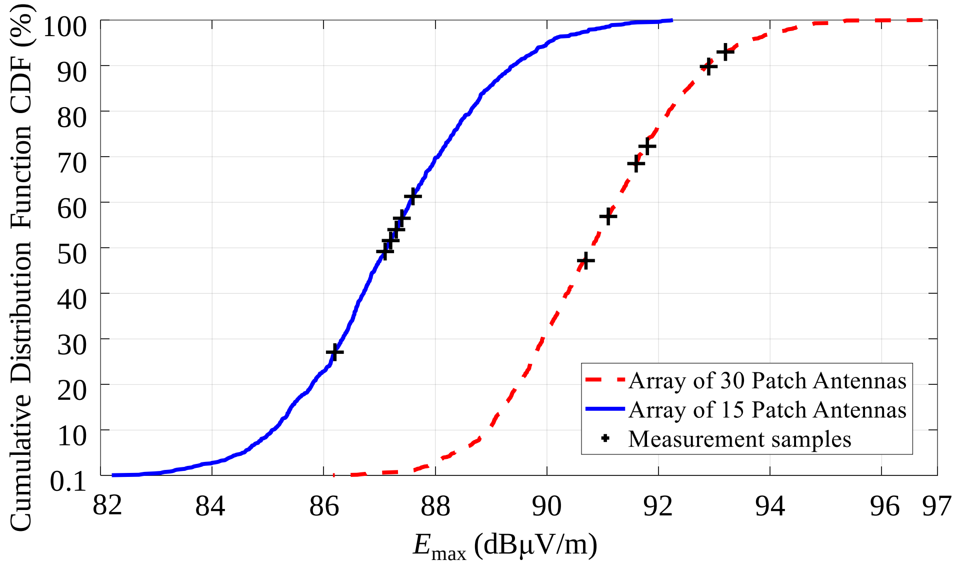


Figure 11. Measurement samples (black cross) and prediction (blue and red).

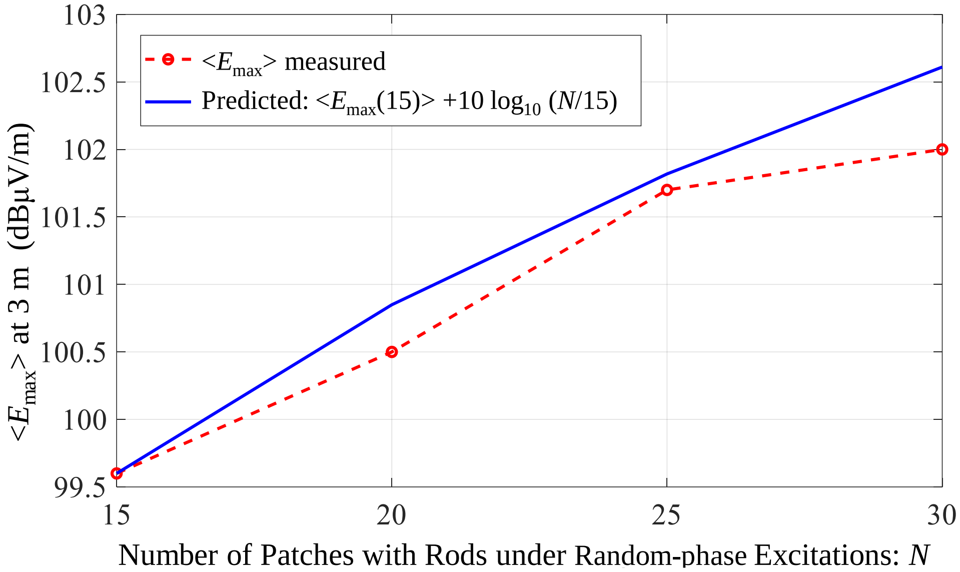


Figure 12. <E_{max}> tendency in random phase excitations.

Similarly, the measured and predicted <E_{max}> of the artificial system for 16 to 30 patch antennas with dielectric rods in random-phase excitation is shown in Figure 12 and Figure 13. For the excitation of 15 patch antennas with rods, the measured <E_{max}> under different phase randomizations fell into the 20% to 90% probability range. For the excitation of 30 patch antennas with dielectric rods under different random-phase distributions, the measured <E_{max}> under different phase randomizations fell into the 10% to 60% probability range.

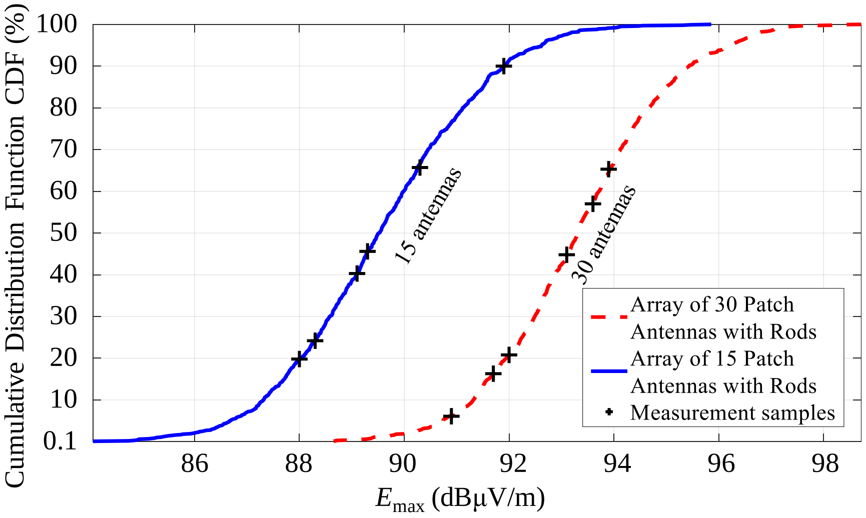


Figure 13. Measurement results and prediction.

In the two cases investigated with random-phase distributions, the $<E_{\max}>$ with an increasing number of radiators all follow the tendency close to 10 log10 N (dB). This validates the prediction from the simulation and theoretical analysis.

From the EMC point of view, the difference between simulation and measurement is within 2 dB. The possible reasons for the difference between measurement and simulation are: 1) the number of samples that we measure for random phase distribution may not be enough to get statistical $<E_{\max}>$, for example, $<E_{\max}>$ is obtained based on the measurement for 6 times random phase distribution; 2) possibilities to miss the $E_{\max}$ peak in the radiation emission measurement, such as receiving antenna height step and turntable rotation angle during the RE scan, which is discussed in [17]. To reduce the error, more samples measured in the random-phase distribution and finer scan steps in RE measurement are suggested.

4.4. EFFECT OF OPTICAL FIBER CABLES ON THE RADIATION

The rods in front of the patch antennas mimic the fiber connector (normally made from plastic material but may also contain a ceramic section and a metal ring). The structure can have waveguiding and beam forming effects, it may also introduce losses or scatter the signal to the sides.

In the real system, many optical fiber cables are in the path of radiation. The loss of the optical fiber cables was investigated by measuring TRP. The scattering was measured using $\langle E_{\max} \rangle$ with/without fiber cables. Comparing columns 2 and 3 of the measured TRP in Table 2, the optical fiber cables do not absorb at 10.31 GHz.

Table 2. TRP for 15 to 30 patch antennas.

Number of patches	TRP rods (dBm)	TRP rods + fibers (dBm)
15	-20.7	-21.0
20	-18.8	-19.0
25	-17.9	-18.0
30	-17.5	-17.5

The scattering effect of the optical fiber cables was also investigated by observing the $\langle E_{\max} \rangle$. For 15 and 30 antennas excited in random phases, Emax was measured with/without fiber cables for six times with the phase randomization. Figure 14 shows the $\langle E_{\max} \rangle$ tendency with the number of radiators with/without fiber cables. They are all close to the 10 log10 N (dB) tendency. Therefore, no significant effect on the lossy or scattering of the fiber cables was observed.

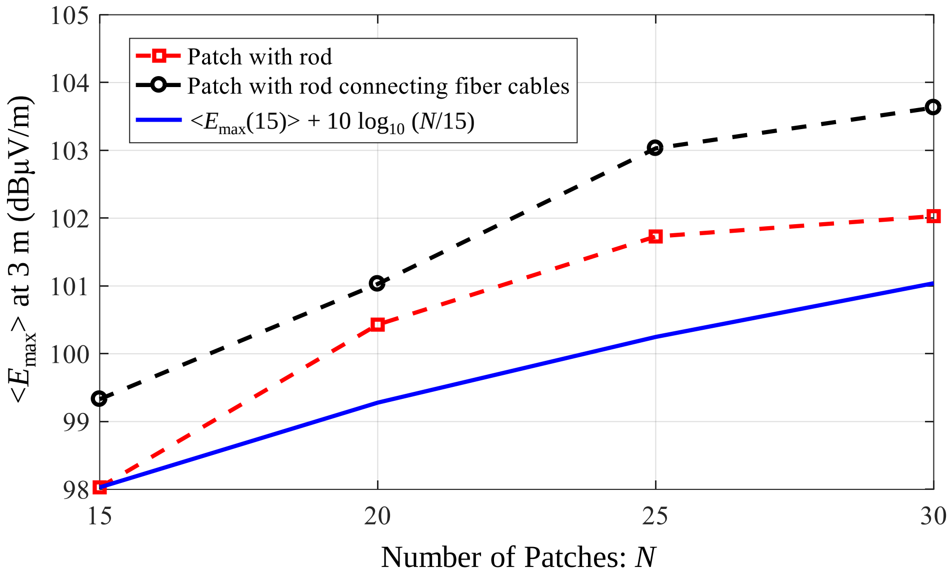


Figure 14. <$E_{\max}$> tendency for 15 to 30 patch antennas with rod/rod + fiber cables.

4.5. DISCUSSION OF E_{MAX} AND TRP CORRELATION

When there are large numbers of radiators in the system with random-phase distribution, the <$E_{\max}$> and TRP can be obtained from measurement. Thus the <$D_{\max}$> can be obtained from (3). According to the statistical model proposed in [16] and [17], a prediction on <$D_{\max}$> of the artificial system based on the radiation characteristics of a single radiator can be obtained statistically from random-phase realizations for 1 000 times. By comparing the <$D_{\max}$> obtained from (1) and the statistical simulation model, the validation of (1) and the saturation of <$D_{\max}$> in the random phase configuration can be proved.

From the statistical model, for a patch antenna array with 30 patch antennas fed by 30 random-phase excitations at the same frequency, the <$D_{\max}$> was saturated to

12 dB when the number of radiators is larger than 14. Similarly, for the antenna array with 30 patch antennas with rods, the <$D_{\max}$> was saturated to 12.5 dB. These are shown in Figure. 15. In both cases, <$D_{\max}$> was calculated using (1) based on the measured TRP and <$E_{\max}$>. Table 3 shows the measured TRP, measured <$E_{\max}$>, <$D_{\max}$> obtained from statistical simulation model, and the <$D_{\max}$> calculated from (1) with the measured TRP and <$E_{\max}$>. The error between the <$D_{\max}$> from (1) and the statistical model is within 1.5 dB, validating the simulated <$D_{\max}$> by measurement. These significant results confirmed that for the random-phase excitations in the system, the <$D_{\max}$> saturated when the number of radiators was larger than 14, and the <$E_{\max}$> trended to follow the 10 log10 N (dB) formula.

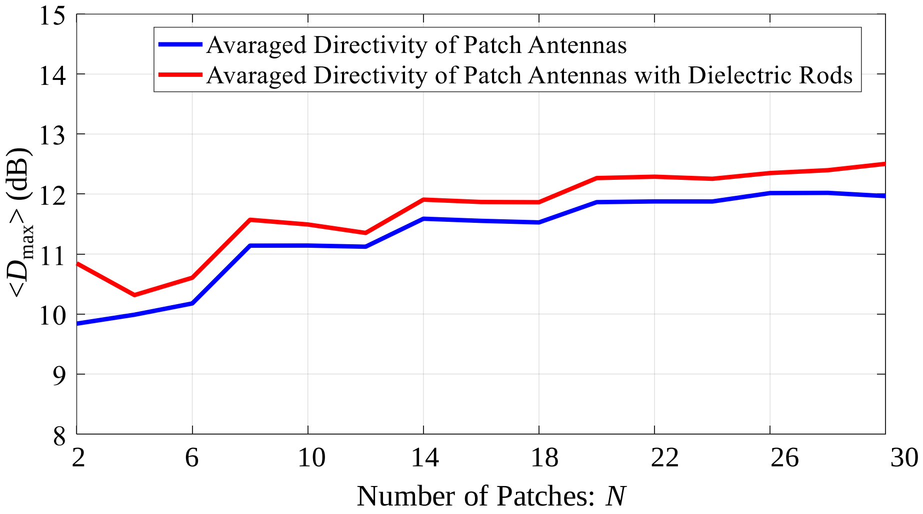


Figure 15. Saturation of directivity as the number of radiators increases.

Table 3. TRP, directivity, and E_{MAX} correlation.

Parameters to be compared	30 Patch antennas	30 Patch antennas with rods
TRP measured	-16.4 dBm	-17.5 dBm

$<E_{max}>$ measured at 3 m	91.6 dBμV/m	91.78 dBμV/m
$<D_{max}>$ predicted by the statistical model	12 dB	12.5 dB
D_{max} calculated from (3)	12.9 dB	13.9 dB

5. CONCLUSIONS

In this paper, the EMI tendency of a multi-radiator system with an increasing number of radiators is discussed with the theoretical and a statistical analysis model. A scalable artificial system was designed to mimic the actual radiation emissions from the real router for this study. By analyzing the emission behaviors of the single optical module in the actual router, the artificial system was designed to be able to generate similar element radiation performances based on a patch antenna array. Furthermore, the artificial system provided strong evidence of the Emax tendency with an increasing number of radiators under different controlled configurations, i.e., in-phase/random-phase excitations. When all the radiators are in phase, the system shows a 20 log10 N (dB) tendency in E_{max}. When all the radiators are in random phase and N is larger than 14, the system showed a 10 log10 N (dB) tendency in $<E_{max}>$, following the 10 log10 N (dB) tendency in TRP as the $<D_{max}>$ is proved to saturate. As the whole idea is based on antenna array theory, it can be applied to both single-mode and multi-mode optical transmission if the system can be assumed to act as an antenna array. Based on the study in this paper, the ways to reduce the emission of a router system are: 1) using optical modules with lower radiation; 2) controlling the phase of the channels such that the radiation is distributed in as many directions as possible; 3) adding EMI doors with absorbers in front of the system; 4) spreading the frequency of each LC over more than 1 MHz to create a spread spectrum. Furthermore, the artificial system can be improved to provide evidence of the predicted $<E_{\max}>$ tendency from a router system loaded with LCs operating at different frequencies (kHz range).

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SECTION

2. CONCLUSIONS AND RECOMMENDATIONS

In a system with 3D ICs and co-packaged optics, issues such as power integrity and electromagnetic interference could all occur. In the first paper, an improved model of characterizing the electrical performance of the P/G TSVs is proposed. It allows for accurate estimation of the hysteresis behavior of a TSV under a swept bias voltage condition in the forward and reverse directions. Furthermore, the model can provide an estimation of the hysteresis behavior for different ranges of the swept bias voltages, and under different temperature and light intensity conditions. Besides, the importance of considering the bias effect during the PI design with 3D ICs and P/G TSVs is emphasized through a hierarchical PDN model. Finally, a mitigation method to increase the low TSV capacitance in the inversion region when the system is powered on is discussed.

In the second paper, the scaled EMI is predicted and validated for a large router system with a large number of optical modules through an artificial router system, which can be used to guide the EMI estimation in future systems with co-packaged optics. The scaled EMI with the number of optics is analyzed and validated to follow a tendency of $10 \log(N)$ (dB), where N is the number of optical modules/radiators in the system.

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