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ADVANCED TOPOLOGIES OF HIGH STEP-UP DC-DC CONVERTERS FOR
RENEWABLE ENERGY APPLICATIONS

by

RAMIN RAHIMI

A DISSERTATION

Presented to the Graduate Faculty of the
MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

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Approved by:

Mehdi Ferdowsi, Advisor
Pourya Shamsi
Jonathan Kimball
Rui Bo
Ali Rownaghi

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PUBLICATION DISSERTATION OPTION

This dissertation consists of the following five articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I, found on pages 17–52 has been published in *IEEE Transactions on Power Electronics*.

Paper II, found on pages 53–87, has been published in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*.

Paper III, found on pages 88–126, has been published in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

Paper IV, found on pages 127–161, has been published in *IEEE Access*.

Paper V, found on pages 162–194, has been published in *IEEE Open Journal of Power Electronics*.

ABSTRACT

This research is focused on developing several advanced topologies of high step-up DC-DC converters to connect low-voltage renewable energy (RE) sources, such as photovoltaic (PV) panels and fuel cells (FCs), into a high-voltage DC bus in renewable energy applications. The proposed converters are based on the combinations of various voltage-boosting (VB) techniques, including interleaved and quadratic structures, switched-capacitor (SC)-based voltage multiplier (VM) cells, and magnetically coupled inductor (CI) and built-in-transformer (BIT). The proposed converters offer outstanding features, including high voltage gain with low or medium duty cycle, a small number of components, low current and voltage stresses on the components, continuous input current with low ripple, and high efficiency. This research includes five new advanced high step-up DC-DC converters with detailed analyses. First, an interleaved converter is presented, which is based on the integration of two three-winding CIs with SC-based VM cells. Second, a dual-switch converter is proposed, which is based on the integration of a single three-winding CI with SC-based VM cells. Third, the SC-based VM cells are utilized to present three new Z-source (ZS)-based converters. Fourth, two double-winding CIs and a three-winding BIT are combined with SC-based VM cells to develop another interleaved high step-up converter. Finally, two double-winding CIs and SC-based VM cells are adopted to devise an interleaved quadratic converter with high voltage gain. The operating and steady-state analyses, design considerations, and a comparison with similar converters in the literature are provided for each converter. In addition, hardware prototypes were fabricated to verify the performance of the proposed converters.

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I would like to dedicate this dissertation to my father's soul, who encouraged me to pursue my dreams but never lived to see this accomplishment. There are no words that can express my appreciation to him.

I present my sincere thankfulness to my dear mother for her great role in my life and her numerous sacrifices for me. Many thanks to my brothers and my sister for their support and for being truly siblings when needed. Finally, I owe my deepest gratitude to Roxana, who is my love. I am forever thankful for her unconditional love and support throughout my Ph.D. journey.

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SECTION

1. INTRODUCTION

1.1. RESEARCH BACKGROUND

Increasing consumption of fossil fuels, to meet the current energy demands, has generated a resurgence of interest in promoting renewable energy (RE) sources to meet the developing world's growing energy needs. RE sources, such as solar photovoltaic (PV) panels and fuel cells (FCs), are clean, globally available, and easy to use. Thus, they are promising solution to address environmental concerns and fossil fuel depletion issues. However, the voltage generated by the RE sources is usually less than 60 V, which is relatively low, which is a big challenge in their use. Accordingly, to integrate the RE sources into the existing AC utility grid or DC microgrid, their voltage must be increased to a high voltage, such as 380-400 V, to meet the DC bus voltage level. There are two main solutions to lift the voltage of the RE sources: connecting the RE sources in series and employing a high step-up DC-DC converter, which are explained below.

1.1.1. Series Connection of RE Sources. The first solution of lifting the low voltage of RE sources is to connect the PV panels or FCs in series to produce a high voltage. However, the series connection of the PV panels suffers from low reliability because any mismatch between the PV panels reduces the total output power of the PV panels' string; the reason is that the maximum current of the string is limited to the cell/panel with the

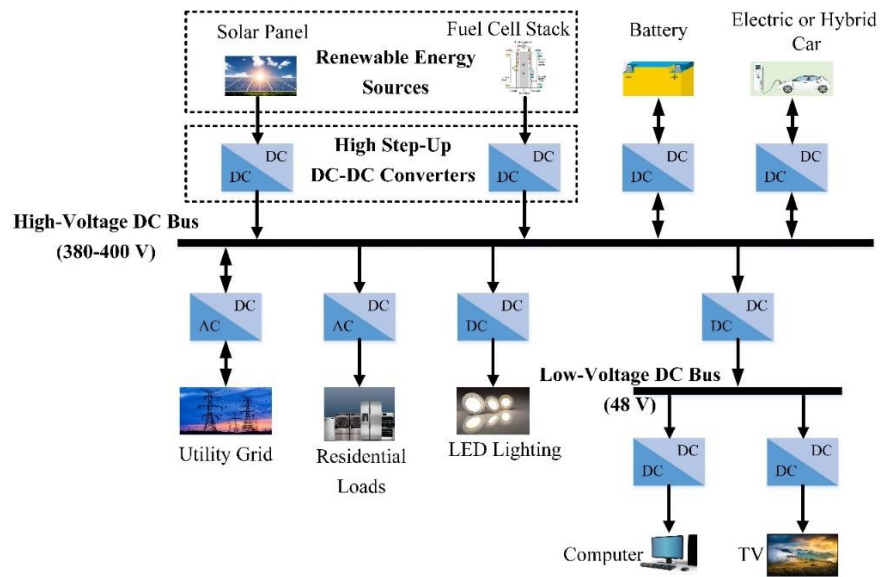


Figure 1.1. A typical configuration of a DC microgrid with the RE sources.

lowest current [1]. Also, due to the electrochemical reaction, it is difficult and expensive to manufacture a fuel cell stack with high output voltage [2].

1.1.2. High Step-Up DC-DC Converters. Since the series connection of RE sources is not a viable solution, it is essential to place a high step-up DC-DC converter at the output end of the RE sources to increase the voltage level [3]. Figure 1.1 illustrates a typical configuration of a DC microgrid with the RE sources and a common high-voltage DC bus of 380-400 V. As seen, the high step-up DC-DC converters interface the PV panel and FC stack with the common high-voltage DC bus. The conventional DC-DC boost converter, shown in Figure 1.2, is the most basic and simplest high step-up DC-DC converter. It consists of one normal boost inductor (L_B), one power switch (Q_B), one output diode (D_o), and one output capacitor (C_o). In Figure 1.2, the RE source is represented by the voltage source (V_{in}), and the load is denoted by a resistor (R). Diode D_o and capacitor C_o act together as the output filter and rectifier without providing any functionality of the

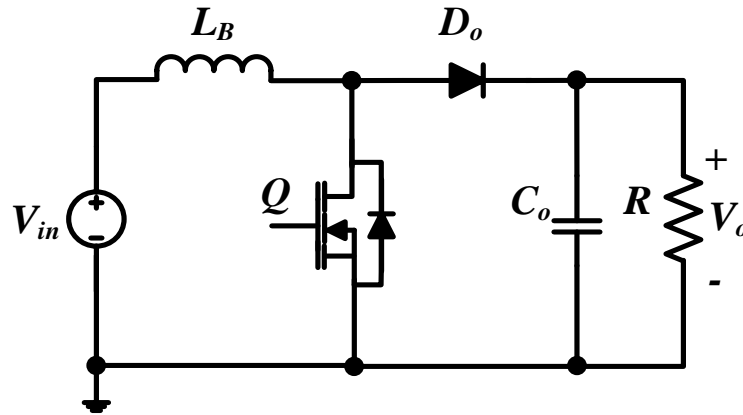


Figure 1.2. The conventional high step-up DC-DC boost converter.

voltage gain extension. The ideal voltage gain (M) of the conventional boost converter is as:

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-D} \quad (1.1)$$

where V_o is the output voltage and D is the duty cycle of switch Q_B , which is the amount of time that switch Q_B is in ON state relative to the switching period (T)—which is the reciprocal of the converter switching frequency (f_{sw}); that is, $T=1/f_{sw}$. As obvious, the conventional DC-DC boost converter is required to operate at an extreme duty cycle, close to 1, to achieve a high voltage gain. However, under this situation, the boost converter has large input current and output voltage ripples, which makes the boost inductor and output capacitor massive, meaning that the size and cost of the boost converter increases. In addition, under the extreme duty cycle, the boost converter has high voltage stresses on the power switch and output diode, which leads to increased conduction and switching losses, thus reducing the converter efficiency. Also, when the boost converter operates at an extreme duty cycle, the output diode suffers from the severe reverse-recovery problem,

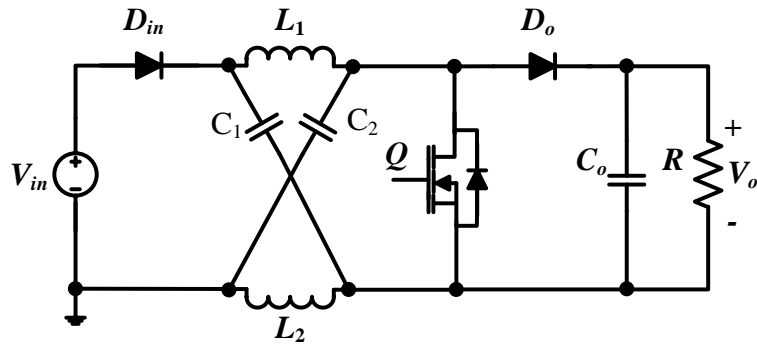


Figure 1.3. The conventional high step-up ZS DC-DC converter.

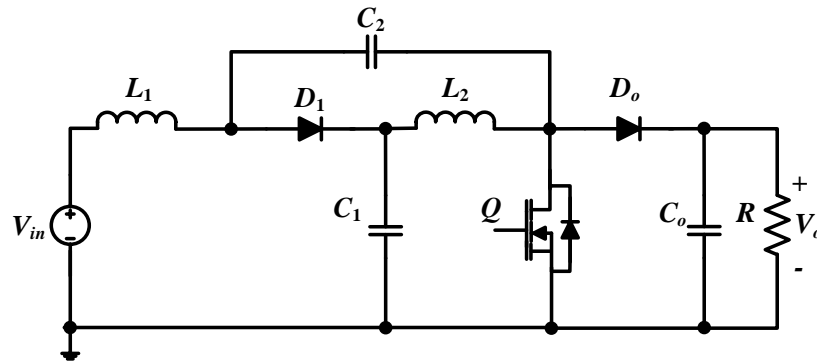


Figure 1.4. The conventional high step-up qZS DC-DC converter.

thus reducing the converter efficiency. Also, when the boost converter operates at an extreme duty cycle, the output diode suffers from the severe reverse-recovery problem because it conducts for a very short time. Furthermore, due to the parasitic elements of the components, the voltage gain of the boost converter is degraded under the extreme duty cycles [4, 5].

The conventional Z-source (ZS) converter [6], shown in Figure 1.3, and quasi-Z-source (qZS) converter [7], shown in Figure 1.4, are other basic high step-up DC-DC converters. The voltage gain expression of both ZS and qZS converters is as in (1.2)—their full operating duty cycle range is from 0 to 0.5. Therefore, they can provide high voltage

gains with duty cycles of less than 0.5, thus avoiding extreme duty cycles. However, their voltage gain is not significantly high; also, like the conventional boost converter, the voltage stresses on the power switch and output diode of the conventional ZS and qZS converters are high and the same as the output voltage.

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-2D} \quad (1.2)$$

The conventional buck-boost, cuk, zeta and sepic converters can also be used as the basic none-isolated high step-up DC-DC converters; however, they suffer from the same problems as the conventional boost, ZS, and qZS converters [8]. Another category of the high step-up DC-DC converters are isolated DC-DC converters such as flyback, forward, push-pull, half-bridge, and full-bridge converters. The voltage gains of these converters can be adjusted by the turns-ratio of the magnetically coupled inductor (CI) or transformer, in addition to the duty cycle of the power switches. Thus, the isolated converters can achieve high voltage gains through using larger turns-ratio of their CIs or transformers. However, an elevated turns-ratio necessitates an increase in the leakage inductance, thus increasing the switching losses and reducing the efficiency of the converter [9, 10]. In addition, for these isolated converters, the input current is pulsed, which leads to a reduced lifetime of the RE sources.

Thus, to overcome the problems of the conventional none-isolated and isolated high step-up DC-DC converters, advanced topologies of non-isolated high step-up DC-DC converters have been developed by the researchers to further increase the voltage gain while maintaining high efficiency. The high-efficiency advanced high step-up DC-DC converters employ different voltage-boosting (VB) techniques to achieve extreme voltage

gains. There are three main VB techniques: multi-stage, voltage multiplier (VM), and magnetic coupling. The multi-stage technique is realized using multiple identical modules; cascaded, quadratic boost, hybrid boost, multi-level, and interleaved converters are based on multi-stage technique. The VM technique is divided into two categories: the first one is switched-capacitor (SC) or charge pump and the second one is switched-inductor (SL). In the magnetic coupling technique, the CI and built-in-transformer (BIT) are used to transfer the energy from the input source side to the output load side of the converter [11]. The windings other than the primary one of the CI and BIT act as the dependent voltage sources that contribute to voltage gain extension in high step-up applications. Another advantage of the CI and BIT is that their leakage inductances limit the rising and falling rates of currents flowing through the components, thus eliminating the high current transitions of the converter.

Countless advanced topologies of high step-up DC-DC converters can be obtained with any combination of the three main VB techniques mentioned above. Therefore, researchers in the field have widely investigated how to combine the VB techniques and develop new advanced topologies with the following features: 1) high voltage gain with low or medium duty cycle, 2) low components count, 3) low input current ripple, 4) low voltage and current stresses on the components, especially semiconductor devices, and 5) high efficiency. It must be noted that in comparing the advanced high step-up DC-DC converters, it is fair to perform the comparison within the same combination categories of the VB techniques in terms of all aspects including voltage gain, input current ripple,

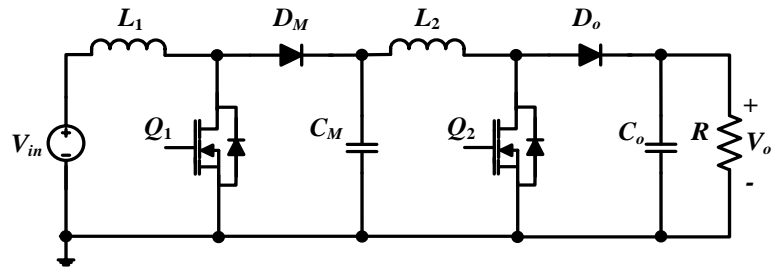


Figure 1.5. The cascaded high step-up DC-DC boost converter.

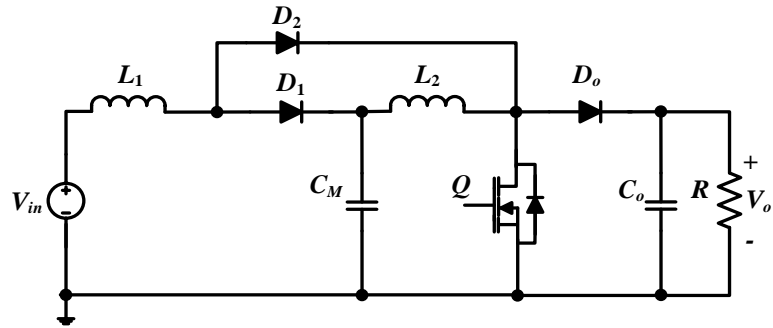


Figure 1.6. The quadratic high step-up DC-DC boost converter.

components count, voltage and current stresses of the components, and efficiency [12]. That is, the drawbacks—brought by the high voltage gain achieved—must also be considered to have a fair comparison. It is a tedious work to review all the advanced high step-up DC-DC converters in the literature. Therefore, this work briefly discusses some of the most promising ones below.

The cascaded and quadratic DC-DC boost converters are demonstrated in Figure 1.5 and Figure 1.6, respectively [13, 14]. Their voltage gains are equal, which is given by (1.3). As seen, compared to the basic high step-up DC-DC converters, the voltage gain of the cascaded and quadratic converters is further extended due to its quadratic dependency on the duty cycle. Nevertheless, output diode D_o in both converters and switches Q and Q_2

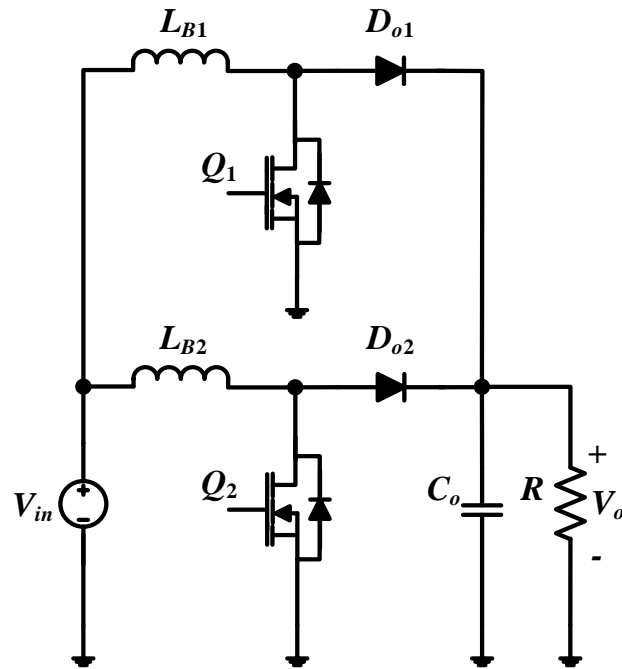


Figure 1.7. The two-phase interleaved high step-up DC-DC boost converter.

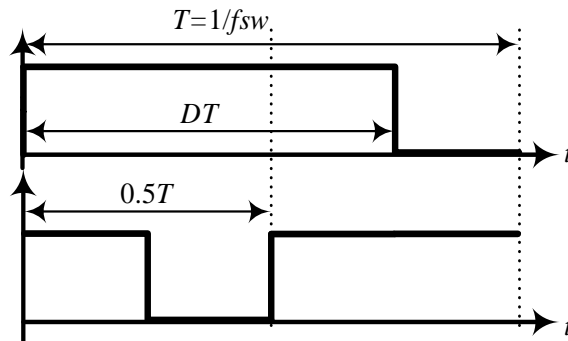


Figure 1.8. The gating pulses of the two-phase interleaved DC-DC boost converter.

in cascaded and quadratic converters, respectively, suffers from high voltage stress, which is equal to the output voltage.

$$M = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \quad (1.3)$$

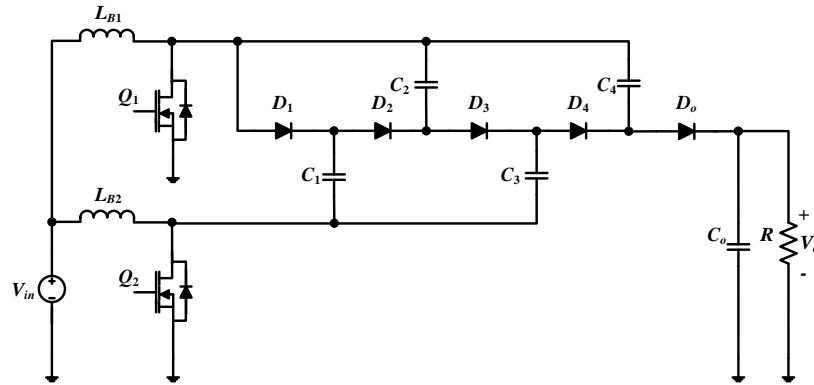


Figure 1.9. The interleaved high step-up DC-DC converter with SC-based VM cells.

Figure 1.7 depicts the two-phase interleaved DC-DC boost converter; as obvious from the gating signals (G_1 and G_2) shown in Figure 1.8, two power switches (Q_1 and Q_2) operate at 180° out of phase from each other [15]. Accordingly, in comparison with conventional boost converter, the two-phase interleaved converter has lower input current and output voltage ripples as well as lower current stresses on the components. However, the voltage gain and voltage stresses on the semiconductor devices of the two-phase interleaved boost converter are exactly the same as those of the conventional boost converter. To address these issues, in [16], the voltage gain of the interleaved DC-DC boost converter was extended by using the SC-based VM cells, which is depicted in Figure 1.9. Its voltage gain is as:

$$M = \frac{V_o}{V_{in}} = \frac{5}{1-D} \quad (1.4)$$

The voltage gain of the converter in [16] is higher than that of the interleaved converter shown in Figure 1.7. However, it suffers from high current transitions on the capacitors and low efficiency because it requires a large number of diode-capacitor cells to

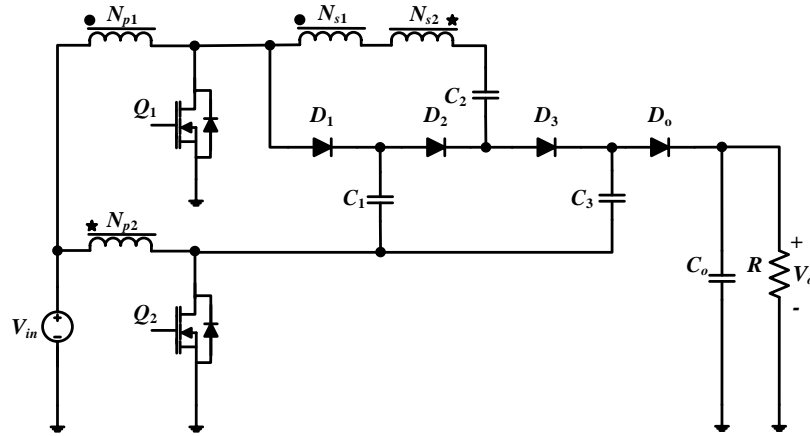


Figure 1.10. The interleaved high step-up DC-DC converter with double-winding CIs and SC-based VM cells.

achieve higher voltage gains. To successfully deal with these problems, the CI and BIT were integrated with the SC-based VM cells in [17] and [18], respectively. The converter in [17] is illustrated in Figure 1.10. As seen, there are two double-winding CIs; the primary windings act as the boost inductors and the secondary windings are integrated with the SC-based VM cells to act as the voltage sources, thus further increasing the voltage gain. The voltage gain of this converter is given as:

$$M = \frac{V_o}{V_{in}} = \frac{2N + 4}{1 - D} \quad (1.5)$$

where N is the turns-ratio of the CIs; that is, $N = N_{s1}/N_{p1} = N_{s2}/N_{p2}$. As obvious, the voltage gain can be adjusted by two different parameters: the duty cycle of the switches (D) and turns-ratio of the CIs (N), which makes the converter design more flexible. Obviously, the voltage gain increases significantly as either D or N increases; thus, the converter in [17] can reach high voltage gains without extreme duty cycles or high turns-ratios. Also, due to the existence of the leakage inductances of the CIs, there are no high current transitions in

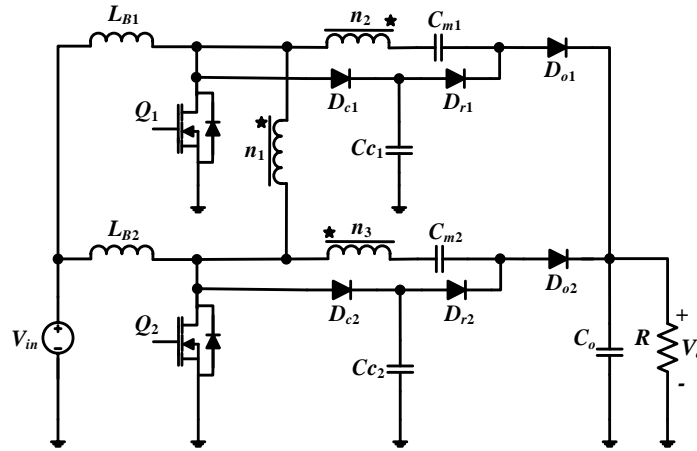


Figure 1.11. The interleaved high step-up DC-DC converter with three-winding BIT and SC-based VM cells.

the converter. In [18], a three-winding BIT was integrated with the SC-based VM cells to introduce an advanced high step-up DC-DC converter, which is depicted in Figure 1.11. Considering the turns-ratio of the BIT as $n=n_2/n_1=n_3/n_1$, the voltage gain of the converter in [18] is as:

$$M = \frac{V_o}{V_{in}} = \frac{2n+2}{1-D} \quad (1.6)$$

As seen from (1.6), the voltage gain is a function of two parameters, which are the duty cycle of the power switches and turns-ratio of the BIT. Thus, an extra control freedom is provided for extending the voltage gain without extreme duty cycles.

The advanced high step-up DC-DC converter in [19] is shown in Figure 1.12, which is based on the combination of the SC-based VM cells with both CIs and BIT. In comparison with the converters with only CIs [17] or only a BIT [18], the converter in [19] offers another degree of freedom for the adjustment of the voltage gain, which leads to

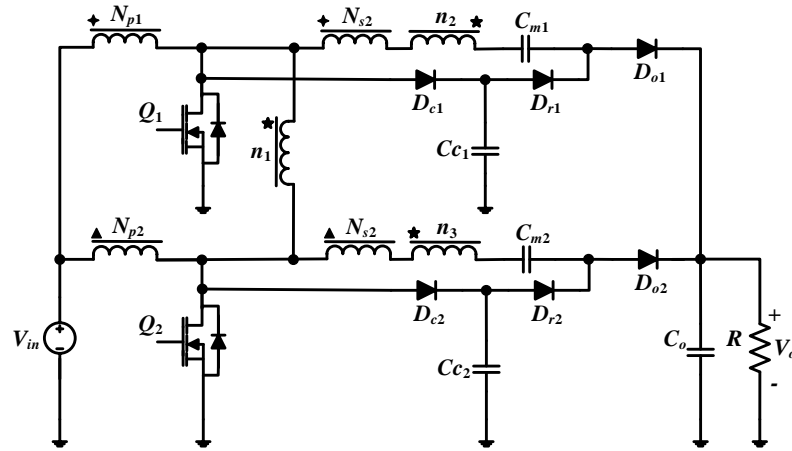


Figure 1.12. The interleaved high step-up DC-DC converter with double-winding CIs, three-winding BIT, and SC-based VM cells.

further extension of the voltage gain and further reduction of the voltage stresses on the power switches. In fact, from the voltage gain expression of the converter in [19] given by (1.7), it is seen that the voltage gain is controlled by the turns-ratio of the CIs (N) and turns-ratio of the BIT (n), in addition to the duty cycle of the power switches (D), thus increasing the design flexibility of the converter.

$$M = \frac{V_o}{V_{in}} = \frac{2n + N + 2}{1 - D} \quad (1.7)$$

1.2. RESEARCH CONTRIBUTION

The research in this dissertation is motivated by the drawbacks of the high step-up DC-DC converters in the literature. Therefore, several new advanced topologies of high step-up DC-DC converters with desirable features are proposed, which are suitable candidates for energy harvesting from the RE sources.

In Paper I, titled "*A Three-Winding Coupled Inductor-Based Interleaved High-Voltage Gain DC-DC Converter for Photovoltaic Systems*," an innovative advanced high

step-up DC-DC converter is proposed, which is capable of converting low voltage of a PV panel to a high voltage required by the DC bus in the PV applications. The proposed advanced high step-up DC-DC converter has an interleaved structure and is based on the integration of the SC-based VM cells with the secondary and tertiary windings of two three-winding CIs. The voltage gain of the proposed converter depends on the duty cycle of the switches and turns-ratio of the CIs, which helps to avoid operating at extreme duty cycle to achieve a high voltage gain; also, the two degrees of freedom—duty cycle and turns-ratio—make the converter design more flexible. The main advantage of the proposed converter is ultra-high voltage gain with medium duty cycle as well as the low voltage and current stresses on all components, which reduces the size and cost of the converter and increases the power conversion efficiency. Another advantage is that the input current has a small ripple due to the interleaved structure of the proposed converter, which leads to the increased lifetime of the solar PV panel. In addition, due to the presence of the leakage inductances of the CIs, the current-falling rates of the diodes are controlled, thus alleviating the reverse-recovery problems of the diodes. A detailed analysis of the proposed converter is given in the paper. Also, a thorough comparison with other similar converters, presented by other researchers in the field, is carried out to verify the superiority and merits of the proposed converter over its competitors. Additionally, the proposed converter's theoretical analysis and performance are confirmed through a 400-W prototype with the input and output voltages of 20 V and 400 V, respectively. In summary, the proposed advanced high step-up DC-DC converter can be replaced with the conventional high step-up DC-DC converters in solar PV systems to increase the total efficiency and to make the system more power-dense by decreasing its size.

A single three-winding CI is integrated into the SC-based VM cells in a dual-switch structure to derive another advanced high step-up DC-DC converter in Paper II, titled "*A Three-Winding Coupled Inductor-Based Dual-Switch High Step-Up DC-DC Converter for Photovoltaic Systems.*" Using only a single magnetic core, a high voltage gain with a low duty cycle of less than 0.5 is achieved. Other features of the proposed converter are low current and voltage stresses on the semiconductors, simple topological structure, continuous input current, and increased design flexibility. Furthermore, the current-falling rates of most diodes are controlled by the leakage inductances of the CI, thus leading to significant reduction of reverse-recovery losses. The operating modes, steady-state analyses, design considerations, comparison with other converters are presented in the paper. Moreover, to validate the theoretical calculations, the experimental results of a 200-W prototype with the output voltage of 400 V for two different voltage gains of 20 and 11.6 are presented.

In Paper III, titled "*Z-Source-Based High Step-Up DC-DC Converters for Photovoltaic Applications,*" three advanced ZS-based converters are proposed, which are suitable candidates for connecting a low-voltage solar PV panel to a high-voltage DC bus in PV applications. The main idea of this paper is to modify the conventional ZS network by integrating it with SC-based VM cells in three different ways, each of which leads to a new advanced high step-up DC-DC converter. The proposed ZS converters offer high voltage gains with a duty cycle of 0 to 0.5, which is the full operating duty cycle range for ZS-based converters. Other merits of the proposed converters are simple configuration, low voltage stress on the semiconductors, and smooth input current. The detailed operating principles are discussed in the paper, followed by the voltage and current

analyses for all three proposed converters. Furthermore, the design considerations, comparative study, and experimental results of a 400-W/400-V laboratory prototype are presented.

The advanced high step-up DC-DC converter proposed in Paper IV, titled "*An Interleaved High Step-Up DC-DC Converter Based on Integration of Coupled Inductor and Built-in-Transformer with Switched-Capacitor Cells for Renewable Energy Applications*," is topologically similar to the advanced interleaved converter in Paper I. However, the three-winding CIs are replaced by the double-winding CIs in Paper IV. Also, a three-winding BIT is added to the converter in Paper IV; thus, another degree of freedom—the turns-ratio of the BIT—is added to further control and increase of the converter voltage gain. Additionally, the voltage stresses on the power switches are further decreased, which contributes to the further reduction of converter power loss. The feasibility of the proposed converter in Paper IV is verified through a 200-W experimental prototype with a voltage gain of 25 and input voltage of 16 V.

In Paper V, titled "*An Interleaved Quadratic High Step-Up DC-DC Converter with Coupled Inductor*," an interleaved high step-up DC-DC converter is proposed whose voltage gain has a quadratic dependency on the duty cycle of the switches, which results in increased voltage gain. To further increase the voltage gain of the converter, the secondary windings of two double-windings CIs are combined with the SC-based VM cells. In addition to the ultra-high voltage gain, the continuous input current with low ripple, low voltage stresses on the switches, simple structure, and low component count are the primary merits of the proposed converter in Paper V. The operating principles, steady-state analysis, and design considerations are provided in the paper. Also, to justify the

merits of the proposed converter, it is compared with other converters in the literature. Furthermore, the experimental results of a 400-W setup with the input voltage of 25 V and output voltage of 400 V are presented to validate the feasibility and correctness of the proposed converter.

PAPER

I. A THREE-WINDING COUPLED INDUCTOR-BASED INTERLEAVED HIGH-VOLTAGE GAIN DC-DC CONVERTER FOR PHOTOVOLTAIC SYSTEMS

Ramin Rahimi, *Student Member, IEEE*, Saeed Habibi, *Student Member, IEEE*, Mehdi Ferdowsi, *Member, IEEE*, Pourya Shamsi, *Senior Member, IEEE*

ABSTRACT

In this paper, an interleaved high-voltage gain DC-DC converter is proposed for use with photovoltaic (PV) systems. By integrating two three-winding coupled inductors (CIs) with switched capacitor (SC) cells, the voltage gain is further extended. Through passive diode-capacitor clamp circuits, the energy stored in the leakage inductances is absorbed; additionally, the voltage stress of the power switches is clamped to a value far lower than the output voltage, which enables designers to select switches with low-voltage ratings. Due to the interleaved structure of the proposed converter, the input current has a small ripple, which leads to the increased lifespan of the PV panels. In addition, the current stress on the components is reduced. Thanks to the leakage inductances of the CIs, the zero-current switching (ZCS) condition is intrinsically provided for the diodes; accordingly, the adverse impact of the diodes' reverse-recovery is alleviated. The operating principles, steady-state analyses, and design considerations of the proposed converter are presented in this paper. A comparison with other similar converters is carried out to verify the merits of

the proposed converter. Finally, the theoretical analyses are confirmed through the experimental results of a 400 W prototype with an output voltage of 400 V.

Keywords: DC-DC converter, high-voltage gain, high step-up, coupled inductor (CI), photovoltaic (PV), switched-capacitor (SC) cell.

1. INTRODUCTION

With the growing interest in the field of DC micro-grids and integration of renewable energy sources—such as wind, fuel cell, and photovoltaic (PV)—in power generation, high step-up DC-DC converters have become one of the most viable options [1-3]. The conventional DC-DC boost converter is unable to support high-voltage gain PV applications because it can only achieve high gain with an extreme duty cycle that increases the power losses and reduces the efficiency [4-8]. Thus, researchers have developed different high gain DC-DC topologies to boost the low voltage (10-56 V) from the solar panel to high voltages of 200–400 V without an extreme duty cycle, and that makes it feasible for connecting it to DC micro-grids [9]. A general schematic of a PV system is depicted in Figure 1; as is presented, the high gain DC-DC converter is used to boost the low voltage of the PV panel to high voltage required by the high voltage DC bus.

There were many high gain DC-DC converters discovered in the review of literature, which had mixed voltage-boosting techniques including switching capacitor (SC), switching inductor (SL), cascade connection, and coupled inductor (CI) techniques with either conventional or interleaved boost converters to step up the voltage gain. A topology was proposed in [10]; it used CI and SC to achieve a high voltage gain. A passive

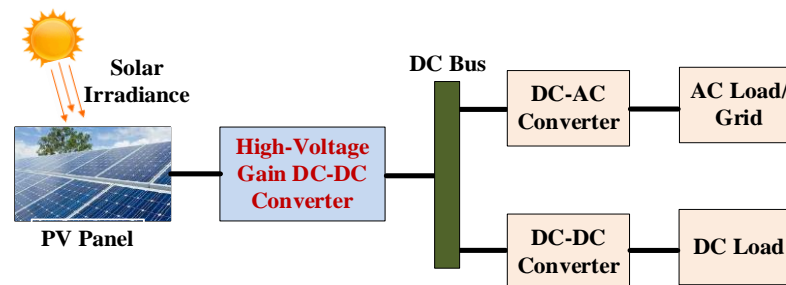


Figure 1. High-voltage gain DC-DC converter in a general PV system.

diode-capacitor clamp circuit was used to reduce the voltage stress and circulate the leakage energy of the CI; it helped to reduce the power loss and reach a high efficiency level. Two CI-based converters with large voltage gains were proposed in [11]; one was based on the combination of SC cells with a two-winding CI, and the other benefited from SC cells and a three-winding CI. A passive clamp circuit was used to recycle the leakage inductance energy in both topologies proposed in [11]. A single-switch high step-up CI-based converter was presented in [12], and the new converter proposed in [13] was based on the converter in [12]; in [13], the authors have added one capacitor and one diode and replaced the boost diode with an active switch. Their results indicated higher voltage gains and lower voltage stresses on the switches and diodes due to the series connection of the added capacitor with the secondary winding of the CI. Other high gain converters—based on the combination of CI and SC techniques—were proposed in [14-18]; they had high voltage gains and low voltage stresses on the semiconductor devices. The interleaved structure was employed by high gain converters to reduce the input current ripples and current stresses on the components. In [19], an interleaved converter with a two-winding CI for each phase and a passive clamp circuit was introduced; however, the voltage stresses across the power switches were high and equal to the output voltage. Other two-winding

CI-based interleaved high gain converters utilizing SC cells were proposed in [20-27]. In [28], a three-winding CI-based interleaved converter was introduced that could achieve zero-voltage switching (ZVS) condition for switches with active clamp circuits in each phase. However, the auxiliary switch required an extra gate driver increase the control complexity and the cost. Moreover, due to the active clamp structure, the ZVS condition was lost at light loads. The voltage gain was not high enough, and the voltage stress on the switches was still high. In [29], a three-winding CI was employed in each phase of an interleaved converter by applying passive clamp circuits to eliminate the leakage effect of the coupled inductor and to reduce the voltage stress on the power switches, thereby deriving a high-voltage gain DC-DC converter. Nevertheless, the voltage gain was not high enough. The concept of integrating the three-winding CIs and SC cells was also employed in [30-35] to generate interleaved converters with extended voltage gains and reduced voltage stresses on the switches. Generally, the interleaved high-voltage gain converters with CIs have the following advantages: reduced current stresses on the components and continuous input current with lower ripple; increased design flexibility of adjusting the voltage gain through two degrees of freedom: turns-ratio of the CI and duty cycle of the switches; reduced reverse-recovery losses of the diodes due to the leakage inductance of the CI providing turn-off zero-current switching (ZCS); reduced voltage stresses on the power switches; extended voltage gain due to recycling the leakage inductance energy into the output. In contrast, there are some disadvantages that are: design of CI is more complex than normal inductor design; a clamp circuit is required to absorb the leakage inductance energy; however, this energy is usually recycled to the output and contributes to extending the voltage gain.

This paper proposes a two-phase interleaved high-voltage gain DC-DC converter that is suitable for PV applications. Reduced input current ripples and components current stresses are obtained thanks to the interleaved structure. High-voltage gain and low-voltage stress across the semiconductor devices are achieved by combining three-winding CI and SC techniques. The secondary winding of each CI is inserted in the SC cell of the same phase, and the tertiary winding is inserted in the SC cell of the other phase. In each SC cell, there is one clamp diode, one clamp capacitor, one regenerative diode, one multiplier intermediate capacitor, and two windings of the CIs. The CIs' leakage inductance energy is absorbed and recycled by the SC cells into the output. Inserting the SC cells into the power branch, the voltage gain is increased significantly. Another advantage of the leakage inductance is that the zero ZCS is provided for the diodes at turn-off instants; accordingly, the reverse-recovery problem of the diodes is alleviated, and the switching loss is reduced. Thus, the conversion efficiency of the proposed converter is improved. In comparison with the similar interleaved high-voltage gain converter in [33], under the same turns-ratio and duty cycle condition, the proposed converter doubles the voltage gain, halves the voltage stresses on the switches, and employs one less output diode.

The organization of this paper is as follows: in Section 2, the topology of the proposed converter is presented, and the operating principles are analyzed. Section 3 is devoted to the steady-state analysis of the proposed converter. The design considerations are presented in Section 4. The performance of the proposed converter is validated through a comparative study in Section 5. The loss analysis is provided in Section 6, and experimental results are examined in Section 7. Finally, the conclusion is presented in Section 8.

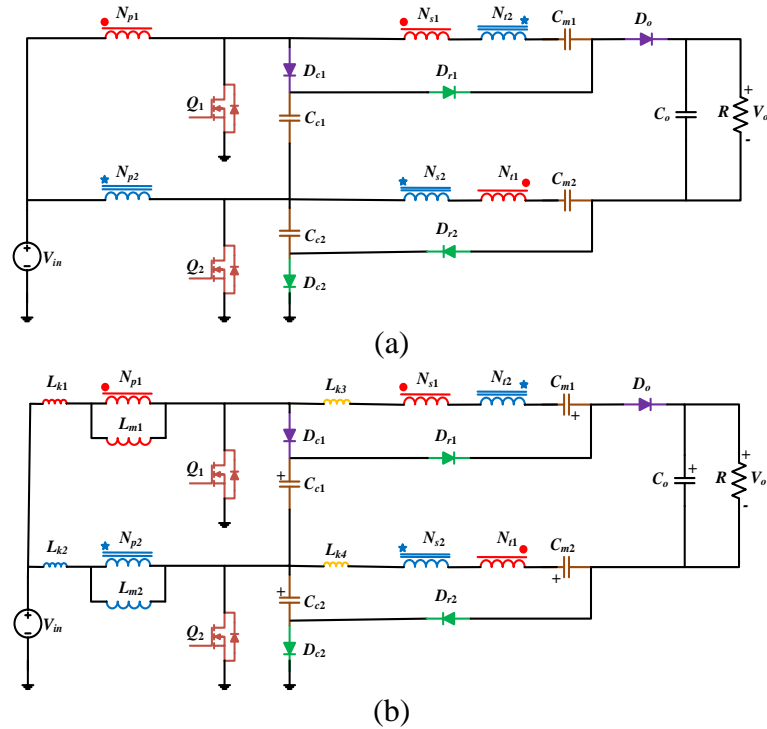


Figure 2. Proposed converter and its equivalent circuit; (a) proposed converter, (b) equivalent circuit.

2. TOPOLOGY AND OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

2.1. TOPOLOGY OF THE PROPOSED CONVERTER

Figure 2 shows the proposed high gain DC-DC converter and its equivalent circuit. It has an interleaved structure with two phases that reduces the current stress on the components and the input current ripple. There are two three-winding CIs, and their coupling references are denoted by \bullet and \star . The primary windings of the CIs with N_{p1} and N_{p2} turns are employed as the input inductors for the proposed interleaved converter. The secondary winding of the CI from one phase is paired with the tertiary winding of another

phase's CI to extend the voltage gain: N_{s1} with N_{t2} and N_{s2} with N_{t1} . The functions of the SC cells' elements are described in the following. D_{c1} and D_{c2} are the clamp diodes, C_{c1} and C_{c2} are the clamp capacitors, D_{r1} and D_{r2} represent the regenerative diodes, and multiplier capacitors C_{m1} and C_{m2} serve as DC-blocking capacitors that make the proposed converter operate in the continuous conduction mode (CCM). D_o and C_o represent the output diode and capacitor, respectively. The input voltage, output voltage, and load are represented by parameters V_{in} , V_o , and R , respectively. According to the equivalent circuit of the proposed converter, each three-winding CI is modeled by combining of a magnetizing inductance, an ideal three-winding transformer, and leakage inductances in each winding— L_{k1} and L_{k2} are the leakage inductances in the primary windings of CIs; L_{m1} and L_{m2} are the magnetizing inductances; L_{k3} is the summation leakage inductance of the secondary winding of CI for phase 1 and the tertiary winding of CI for phase 2; similarly, L_{k4} is the summation leakage inductance of the secondary winding and the tertiary winding of CI for phases 1 and 2, respectively.

2.2. OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

The duty cycle (D) of the switches are the same and more than 0.5, and there is a phase shift of 180° between their gate pulses. According to the conduction states of the switches and diodes, the operation of the converter during one switching period (T) is divided into 9 modes, as shown in Figure 3. The equivalent circuits of the proposed converter in all 9 operation modes are shown in Figure 4 and are described below. Note that $N_{sp1}=N_{s1}/N_{p1}$, $N_{sp2}=N_{s2}/N_{p2}$, $N_{tp1}=N_{t1}/N_{p1}$, and $N_{tp2}=N_{t2}/N_{p2}$; the arrows show the current path direction for the corresponding component.

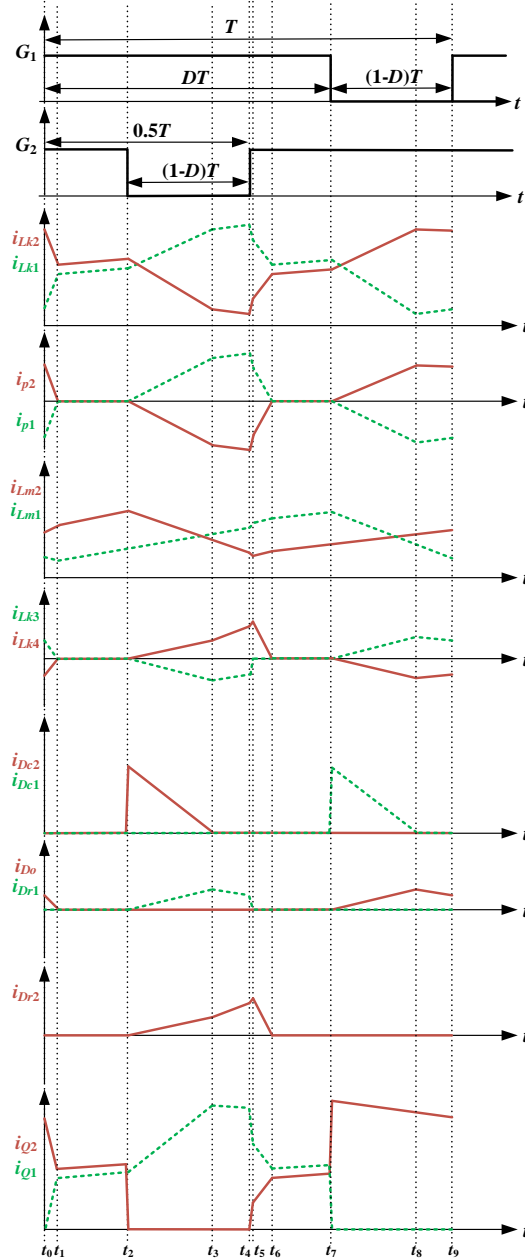


Figure 3. Key waveforms of the proposed converter.

Mode 1 ($t_0 \leq t \leq t_1$): Prior to t_0 , switch Q_1 is OFF, and switch Q_2 and output diode D_o are in ON-state. At $t = t_0$, switch Q_2 and output diode D_o remain in ON-state, and switch Q_1 is turned on. The key circuit relationships for this operation mode are obtained from (1).

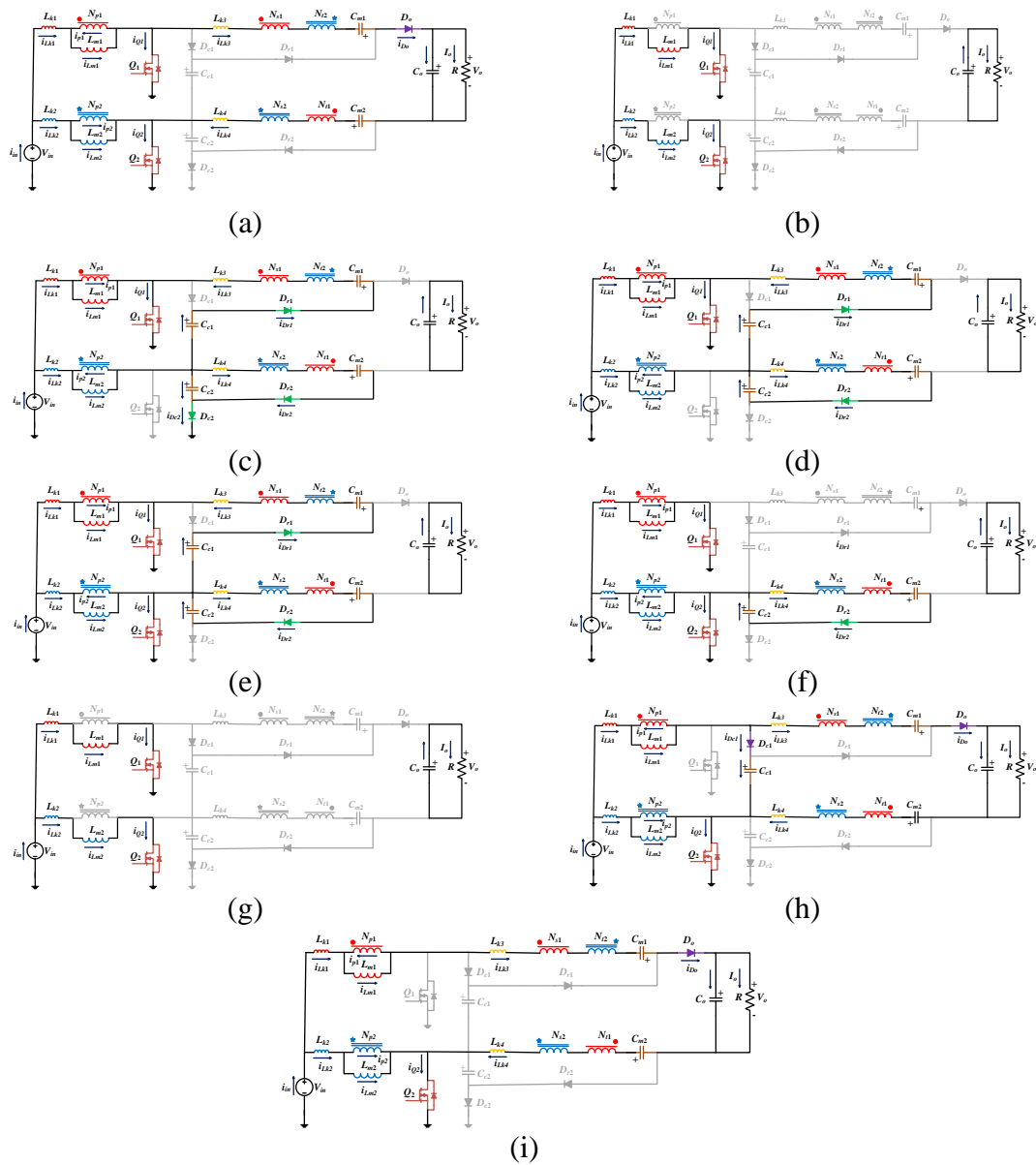


Figure 4. Operation modes in one switching period: (a) Mode 1 $[t_0-t_1]$, (b) Mode 2 $[t_1-t_2]$, (c) Mode 3 $[t_2-t_3]$, (d) Mode 4 $[t_3-t_4]$, (e) Mode 5 $[t_4-t_5]$, (f) Mode 6 $[t_5-t_6]$, (g) Mode 7 $[t_6-t_7]$, (h) Mode 8 $[t_7-t_8]$, (i) Mode 9 $[t_8-t_9]$.

The current through D_o is reduced to zero, and its falling rate is controlled by leakage inductances L_{k3} and L_{k4} ; thus, the reverse-recovery problem of D_o is alleviated. Leakage inductances L_{k3} and L_{k4} quickly release their stored energy to output capacitor C_o and load R through output diode D_o , and accordingly, the current through leakage inductance L_{k3}

decreases from an initial positive value to zero, and the current through leakage inductance L_{k4} increases from an initial negative value to zero. The current of leakage inductance L_{k1} increases linearly, while the current of leakage inductance L_{k2} decreases linearly. This operation mode ends when D_o turns off at $t=t_1$. This operation mode is transitional and too short.

Mode 2 ($t_1 \leq t \leq t_2$): At $t=t_1$, both switches Q_1 and Q_2 remain in ON-state, and output diode D_o turns off under ZCS condition; thus, all diodes are in OFF-state. During this mode, magnetizing and primary leakage inductances L_{m1} , L_{m2} , L_{k1} , and L_{k2} are charged by the input voltage linearly. Load R is being supplied by output capacitor C_o . The current relationships are as (2).

$$\begin{aligned}
 i_{D_o}(t) &= i_{D_o}(t_0) - \frac{(N_{sp2} + N_{tp2})V_{L_{m2}} - (N_{sp1} + N_{tp1})V_{L_{m1}} + V_{C_{m1}} + V_{C_{m2}} - V_o}{L_{k3} + L_{k4}}(t - t_0) \\
 i_{L_{k3}}(t) &= i_{L_{k4}}(t) = i_{D_o}(t) \\
 i_{p1}(t) &= (N_{sp1} + N_{tp1})i_{D_o}(t), \quad i_{p2}(t) = (N_{sp2} + N_{tp2})i_{D_o}(t) \\
 i_{L_{k1}}(t) &= i_{L_{m1}}(t) - i_{p1}(t), \quad i_{L_{k2}}(t) = i_{p2}(t) + i_{L_{m2}}(t)
 \end{aligned} \tag{1}$$

$$\begin{aligned}
 i_{L_{m1}}(t) &= i_{L_{k1}}(t) = i_{L_{m1}}(t_1) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_1) \\
 i_{L_{m2}}(t) &= i_{L_{k2}}(t) = i_{L_{m2}}(t_1) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_1)
 \end{aligned} \tag{2}$$

Mode 3 ($t_2 \leq t \leq t_3$): switch Q_2 turns off and clamp diode D_{c2} is forward-biased at $t=t_2$. When clamp diode D_{c2} is turned on, the voltage across Q_2 is clamped to $V_{C_{c2}}$. Simultaneously, the reverse voltages across regenerative diodes D_{r1} and D_{r2} reach zero, and they begin to conduct. The stored energy in magnetizing inductance L_{m2} is transferred to the secondary and tertiary sides through D_{r2} and D_{r1} , respectively. As the currents of D_{r1} and D_{r2} increase, the current passing through D_{c2} decreases. Clamp capacitor C_{c1} is

discharged and multiplier capacitors C_{m1} and C_{m2} are charged. Magnetizing inductance L_{m1} is charged as well. The current rising rate of D_{r1} and D_{r2} is controlled by leakage inductances L_{k3} and L_{k4} , respectively. The relationships for this mode are as (3).

Mode 4 ($t_3 \leq t \leq t_4$): At $t=t_3$, the current through clamp diode D_{c2} decreases to zero, and it is turned off with ZCS; this is because the current rate is controlled by the leakage inductance, and there is no reverse-recovery problem for the clamp diode. The current of D_{r1} starts to decrease in this mode, while the current of D_{r2} continues increasing. The current decreasing rate of D_{r1} is controlled by leakage inductance L_{k3} , and the current increasing rate of D_{r2} is controlled by leakage inductance L_{k4} . The energy stored in magnetizing inductance L_{m2} is continuously transferred to multiplier capacitors C_{m1} and C_{m2} . In this mode, the relationships as (4).

$$\begin{aligned}
i_{D_{r1}}(t) &= \frac{N_{sp1}V_{L_{m1}} + V_{C_{c1}} + V_{C_{c2}} - V_{C_{m1}} - N_{tp2}V_{L_{m2}}}{L_{k3}}(t-t_2) \\
i_{D_{r2}}(t) &= \frac{N_{tp1}V_{L_{m1}} + V_{C_{c2}} - N_{sp2}V_{L_{m2}} - V_{C_{m2}}}{L_{k4}}(t-t_2) \\
i_{L_{k1}}(t) &= i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_{sp1}i_{D_{r1}}(t) + N_{tp1}i_{D_{r2}}(t) \\
i_{L_{k2}}(t) &= i_{L_{m2}}(t) - i_{p2}(t) = i_{L_{m2}}(t) - N_{tp2}i_{D_{r1}}(t) - N_{sp2}i_{D_{r2}}(t) \\
i_{L_{k3}}(t) &= i_{D_{r1}}(t), \quad i_{L_{k4}}(t) = i_{D_{r2}}(t) \\
i_{D_{c2}}(t) &= i_{L_{k2}}(t) - i_{L_{k3}}(t) = i_{L_{m2}}(t) - (N_{tp2} + 1)i_{D_{r1}}(t) - N_{sp1}i_{D_{r2}}(t)
\end{aligned} \tag{3}$$

$$\begin{aligned}
i_{D_{r1}}(t) &= i_{D_{r1}}(t_3) - \frac{(N_{sp1} + 1)V_{in} + V_{C_{c1}} - (N_{tp2} + 1)V_{L_{m2}} - V_{C_{m1}} - N_{sp1}V_{L_{k1}}}{L_{k2} + L_{k3}}(t-t_3) \\
i_{D_{r2}}(t) &= i_{D_{r2}}(t_3) - \frac{N_{tp1}V_{L_{m1}} + V_{C_{c2}} - N_{sp2}V_{L_{m2}} - V_{C_{m2}}}{L_{k4}}(t-t_3) \\
i_{L_{k1}}(t) &= i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_{sp1}i_{D_{r1}}(t) + N_{tp1}i_{D_{r2}}(t) \\
i_{L_{k3}}(t) &= i_{L_{k2}}(t) = i_{D_{r1}}(t), \quad i_{L_{k4}}(t) = i_{D_{r2}}(t)
\end{aligned} \tag{4}$$

Mode 5 ($t_4 \leq t \leq t_5$): At $t=t_4$, switch Q_2 is turned on. Inductance L_{k2} is quickly charged by the input voltage V_{in} . This operation mode ends when the current through regenerative diode D_{r1} decreases to zero, and it is turned off with ZCS at $t=t_5$. The circuit relationships of this mode are as (5).

Mode 6 ($t_5 \leq t \leq t_6$): Diode D_{r1} is turned off at $t=t_5$, while switches Q_1 and Q_2 remain in ON-states, and the current of regenerative diode D_{r2} begins to decrease due to leakage inductance L_{k4} . At $t=t_6$, the current of D_{r2} reaches zero, and Mode 6 ends. The relationships are as (6).

$$\begin{aligned}
i_{D_{r1}}(t) &= i_{D_{r1}}(t_4) - \frac{-N_{sp1}V_{L_{m1}} + N_{tp2}V_{L_{m2}} - V_{C_{c1}} + V_{C_{m1}}}{L_{k3}}(t - t_4) \\
i_{D_{r2}}(t) &= i_{D_{r2}}(t_4) - \frac{N_{tp1}V_{L_{m1}} + V_{C_{c2}} - N_{sp2}V_{L_{m2}} - V_{C_{m2}}}{L_{k4}}(t - t_4) \\
i_{L_{k1}}(t) &= i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_{sp1}i_{D_{r1}}(t) + N_{tp1}i_{D_{r2}}(t) \\
i_{L_{k2}}(t) &= i_{L_{m2}}(t) - i_{p2}(t) = i_{L_{m2}}(t) - N_{tp2}i_{D_{r1}}(t) - N_{sp2}i_{D_{r2}}(t) \\
i_{L_{k3}}(t) &= i_{D_{r1}}(t), \quad i_{L_{k4}}(t) = i_{D_{r2}}(t)
\end{aligned} \tag{5}$$

$$\begin{aligned}
i_{D_{r2}}(t) &= i_{D_{r2}}(t_5) - \frac{N_{tp1}V_{L_{m1}} + V_{C_{c2}} - N_{sp2}V_{L_{m2}} - V_{C_{m2}}}{L_{k4}}(t - t_5) \\
i_{L_{k1}}(t) &= i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_{tp1}i_{D_{r2}}(t) \\
i_{L_{k2}}(t) &= i_{L_{m2}}(t) - i_{p2}(t) = i_{L_{m2}}(t) - N_{sp2}i_{D_{r2}}(t) \\
i_{L_{k4}}(t) &= i_{D_{r2}}(t)
\end{aligned} \tag{6}$$

Mode 7 ($t_6 \leq t \leq t_7$): This operation mode is similar to operation Mode 2. The relationships are:

$$\begin{aligned}
i_{L_{m1}}(t) &= i_{L_{k1}}(t) = i_{L_{m1}}(t_6) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_6) \\
i_{L_{m2}}(t) &= i_{L_{k2}}(t) = i_{L_{m2}}(t_6) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_6)
\end{aligned} \tag{7}$$

Mode 8 ($t_7 \leq t \leq t_8$): This mode is similar to Mode 3. At $t=t_7$, clamp diode D_{c1} is forward-biased; therefore, the voltage across Q_1 is clamped to $V_{C_{c1}}$. Simultaneously, the voltage across output diode D_o reaches zero, and it is turned on. The stored energy in magnetizing inductance L_{m1} is transferred to the secondary and tertiary sides and load through D_o . As the current of diode D_o increases, the current through D_{c1} decreases. As a result, multiplier capacitors C_{m1} and C_{m2} are discharged; magnetizing inductance L_{m2} is charged. The relationships for this mode are:

$$\begin{aligned} i_{D_o}(t) &= \frac{V_{L_{k3}} - V_{L_{k4}}}{L_{k3} + L_{k4}}(t - t_7) \\ &= \frac{V_{C_{c1}} + V_{C_{m1}} + V_{C_{m2}} + (N_{sp2} + N_{tp2})V_{L_{m2}} - (N_{sp1} + N_{tp1})V_{L_{m1}} - V_o}{L_{k3} + L_{k4}}(t - t_7) \end{aligned} \quad (8)$$

$$\begin{aligned} i_{L_{k1}}(t) &= i_{D_{c1}}(t) + i_{D_o}(t) = i_{L_{m1}}(t) - i_{p1}(t) = i_{L_{m1}}(t) - (N_{sp1} + N_{tp1})i_{D_o}(t) \\ i_{L_{k2}}(t) &= i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + (N_{sp2} + N_{tp2})i_{D_o}(t) \\ i_{L_{k3}}(t) &= i_{D_o}(t), \quad i_{L_{k4}}(t) = i_{D_o}(t) \end{aligned}$$

Mode 9 ($t_8 \leq t \leq t_9$): At $t=t_8$, the current through clamp diode D_{c1} decreases to zero, and it is turned off with ZCS due to leakage inductance L_{k1} . The current of D_o starts to decrease during this mode, and its decreasing rate is controlled by leakage inductances L_{k3} and L_{k4} . The energy stored in magnetizing inductance L_{m1} is continuously transferred to the output. The current relationships are:

$$\begin{aligned} i_{D_o}(t) &= i_{D_o}(t_8) \\ &\quad - \frac{(N_{sp2} + N_{tp2})V_{L_{m2}} - (N_{sp1} + N_{tp1} + 1)V_{L_{m1}} + V_{C_{m1}} + V_{C_{m2}} + V_{in} - V_o - V_{L_{k1}}}{L_{k3} + L_{k4}}(t - t_8) \\ i_{L_{k1}}(t) &= i_{L_{m1}}(t) - i_{p1}(t) = i_{D_o}(t) \\ i_{L_{k2}}(t) &= i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + (N_{sp2} + N_{tp2})i_{D_o}(t) \\ i_{L_{k3}}(t) &= i_{D_o}(t), \quad i_{L_{k4}}(t) = i_{D_o}(t) \end{aligned} \quad (9)$$

3. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis in CCM, the switches and diodes are assumed to be ideal. Also, leakage inductances L_{k1} , L_{k2} , L_{k3} , and L_{k4} are neglected. The capacitors are considered large enough to accommodate the operation modes; their voltages are constant during the switching period. Operation modes 1, 5, and 6 are relatively short, and because of that, they are first ignored in the steady-state analysis of the converter. Once the simplified voltage gain is obtained, the analysis is extended to the case where the leakage inductances are present.

3.1. VOLTAGE STRESS ACROSS THE CAPACITORS AND VOLTAGE GAIN

Applying voltage-second balance principle to magnetizing inductances L_{m1} and L_{m2} as well as the KVLs around the loops of the equivalent circuits, the following voltage relationships are yielded:

$$\begin{aligned}
 V_{C_{c1}} &= V_{C_{c2}} = \frac{1}{1-D} V_{in} \\
 V_{C_{m1}} &= \frac{2 + DN_{tp2} + (1-D)N_{sp1}}{1-D} V_{in} \\
 V_{C_{m2}} &= \frac{1 + DN_{sp2} + (1-D)N_{tp1}}{1-D} V_{in} \\
 V_{C_o} &= V_o = \frac{4 + N_{sp1} + N_{tp1} + N_{sp2} + N_{tp2}}{1-D} V_{in} \\
 M &= \frac{V_o}{V_{in}} = \frac{4 + N_{sp1} + N_{tp1} + N_{sp2} + N_{tp2}}{1-D}
 \end{aligned} \tag{10}$$

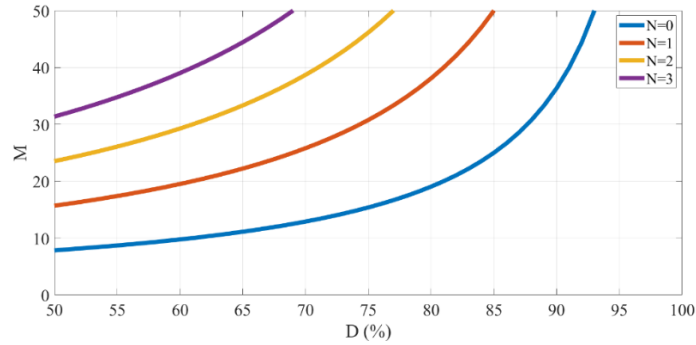


Figure 5. The voltage gain versus turns-ratio N and duty cycle D .

If all turns-ratios of CIs are same and equal to N (i.e., $N_{sp1}=N_{tp1}=N_{sp2}=N_{tp2}=N$), (10)

is simplified as:

$$\begin{aligned}
 V_{C_{c1}} &= V_{C_{c2}} = \frac{1}{1-D} V_{in} \\
 V_{C_{m1}} &= \frac{2+N}{1-D} V_{in} \\
 V_{C_{m2}} &= \frac{1+N}{1-D} V_{in} \\
 V_{C_o} = V_o &= \frac{4+4N}{1-D} V_{in} \\
 M = \frac{V_o}{V_{in}} &= \frac{4+4N}{1-D} = \frac{4(N+1)}{1-D}
 \end{aligned} \tag{11}$$

As seen from (10) and (11), the voltage gain of the proposed converter is controlled by the turns-ratios of the CIs and the duty cycle of the switches. The curve of the voltage gain for different values of N and D is sketched in Figure 5. Obviously, the the voltage gain increases significantly as duty cycle or turns-ratio increases; this makes the proposed converter reach high voltage gain without an extreme duty cycle. The proposed converter doubles the voltage gain under the same turns-ratio and duty cycle condition compared with the similar interleaved high step-up converters in [32] and [33] that each had two three-winding CIs and one more output diode.

In reality, the leakage inductances of the CIs cannot be zero. Considering the effect of the leakage inductances, by considering Mode 8, the voltage gain calculation can be revised to (12). If all the turns-ratios of the CIs are equal to N and all the leakage inductances are equal to L_k (i.e., $L_{k1}=L_{k2}=L_{k3}=L_{k4}=L_k$), the voltage gain can be written as in (13). According to (13), the voltage gain reduces as the leakage inductance increases.

$$\left\{ \begin{array}{l}
 V_{L_{k1}} = L_{k1} \frac{\Delta i_{L_{k1}}}{(1-D)T} = -\frac{2f_{sw}L_{k1}(N_{sp1} + N_{tp1})}{1-D} I_o \\
 V_{L_{k2}} = L_{k2} \frac{\Delta i_{L_{k2}}}{(1-D)T} = \frac{2f_{sw}L_{k2}(N_{sp2} + N_{tp2})}{1-D} I_o \\
 V_{L_{k3}} = L_{k3} \frac{\Delta i_{L_{k3}}}{(1-D)T} = \frac{2f_{sw}L_{k3}}{1-D} I_o \\
 V_{L_{k4}} = L_{k4} \frac{\Delta i_{L_{k4}}}{(1-D)T} = -\frac{2f_{sw}L_{k4}}{1-D} I_o \\
 V_{L_{k1}} = L_{k1} \frac{\Delta i_{L_{k1}}}{(1-D)T} = -\frac{2f_{sw}L_{k1}(N_{sp1} + N_{tp1})}{1-D} I_o \\
 V_{L_{k2}} = L_{k2} \frac{\Delta i_{L_{k2}}}{(1-D)T} = \frac{2f_{sw}L_{k2}(N_{sp2} + N_{tp2})}{1-D} I_o \\
 V_{L_{k3}} = L_{k3} \frac{\Delta i_{L_{k3}}}{(1-D)T} = \frac{2f_{sw}L_{k3}}{1-D} I_o \\
 V_{L_{k4}} = L_{k4} \frac{\Delta i_{L_{k4}}}{(1-D)T} = -\frac{2f_{sw}L_{k4}}{1-D} I_o \\
 V_o = \frac{4 + N_{sp1} + N_{tp1} + N_{sp2} + N_{tp2}}{1-D} V_{in} + (V_{L_{k3}} - V_{L_{k4}}) + (N_{sp1} + N_{tp1})V_{L_{k1}} - (N_{sp2} + N_{tp2})V_{L_{k2}} \\
 M = \frac{V_o}{V_{in}} = \frac{4 + N_{sp1} + N_{tp1} + N_{sp2} + N_{tp2}}{1-D} \times \\
 \frac{1}{1 + \frac{2f_{sw}}{(1-D)^2 R} ((N_{sp1} + N_{tp1})^2 L_{k1} + (N_{sp2} + N_{tp2})^2 L_{k2} + L_{k3} + L_{k4})}
 \end{array} \right. \quad (12)$$

$$M = \frac{V_o}{V_{in}} = \frac{4(N+1)}{1-D} \times \frac{1}{1 + \frac{4f_{sw}L_k(N^2+1)}{(1-D)^2 R}} \quad (13)$$

3.2. VOLTAGE STRESS ACROSS THE SEMICONDUCTOR DEVICES

Considering the same turns-ratios for all the windings, the maximum voltage stress across diodes and switches can be deduced as (14). It is obvious that as the turns-ratio increases from zero, the voltage stress of diodes D_{c1} and D_{c2} and both switches are reduced significantly compared with the conventional interleaved boost converter at the same input voltage and voltage gain; therefore, low-voltage-rated switches with low ON-state resistance could be employed, resulting in reducing the conduction losses. The voltage stress of regenerative diode D_{r2} is always a quarter of the output voltage.

$$\begin{aligned}
 V_{D_{c1}} &= \frac{2}{1-D} V_{in} = \frac{1}{2(N+1)} V_o \leq \frac{1}{2} V_o \\
 V_{D_{c2}} &= \frac{1}{1-D} V_{in} = \frac{1}{4(N+1)} V_o \leq \frac{1}{4} V_o \\
 V_{D_{r1}} &= \frac{N+3}{1-D} V_{in} = \frac{N+3}{4(N+1)} V_o \\
 V_{D_{r2}} &= \frac{N+1}{1-D} V_{in} = \frac{1}{4} V_o \\
 V_{D_o} &= \frac{2(2N+1)}{1-D} V_{in} = \frac{2N+1}{2(N+1)} V_o \\
 V_{Q_1} = V_{Q_2} &= \frac{1}{1-D} V_{in} = \frac{1}{4(N+1)} V_o \leq \frac{1}{4} V_o
 \end{aligned} \tag{14}$$

3.3. CURRENT STRESS OF THE COMPONENTS

Supposing that the output load current is I_o , the average input current is I_{in} , and the average currents of the magnetizing inductances L_{m1} and L_{m2} are I_{Lm1} and I_{Lm2} , respectively, the average and RMS currents of the CIs could be obtained as:

$$\begin{aligned}
I_{in} &= M \times I_o = \frac{4(N+1)}{1-D} I_o \\
I_{Lm_1} &= I_{Lm_2} = I_{L_{k1}(Avg)} = I_{L_{k2}(Avg)} = \frac{2(N+1)}{1-D} I_o \\
I_{L_{k3}(Avg)} &= I_{L_{k4}(Avg)} = 0 \\
I_{L_{k1}(RMS)} &= I_{L_{k2}(RMS)} = 2 \sqrt{\frac{(N+1)^2 + \frac{2}{3}N^2(1-D)}{1-D}} I_o \\
I_{L_{k3}(RMS)} &= I_{L_{k4}(RMS)} = \sqrt{\frac{8}{3(1-D)}} I_o
\end{aligned} \tag{15}$$

Also, the currents of the diodes and switches are:

$$\begin{aligned}
I_{D_{c1}(Avg)} &= I_{D_{c2}(Avg)} = I_{D_{r1}(Avg)} = I_{D_{r2}(Avg)} = I_{D_o}(Avg) = I_o \\
I_{D_{c1}(RMS)} &= I_{D_{c2}(RMS)} = \frac{2(N+1)}{\sqrt{6(1-D)}} I_o \\
I_{D_{r1}(RMS)} &= I_{D_{r2}(RMS)} = I_{D_o}(RMS) = \frac{2}{\sqrt{3(1-D)}} I_o \\
I_{Q_1(Avg)} &= I_{Q_2(Avg)} = \frac{2(N+1)}{1-D} I_o \\
I_{Q_1(RMS)} &= I_{Q_2(RMS)} = \frac{2(N+1)}{\sqrt{D(1-D)}} I_o
\end{aligned} \tag{16}$$

4. DESIGN CONSIDERATIONS

4.1. COUPLED INDUCTOR DESIGN

4.1.1. Limitation of Turns-Ratio. The duty cycles of switches Q1 and Q2 are higher than 0.5. Accordingly, from the voltage gain equation, the limitation of the turns-ratio can be obtained from:

$$D = 1 - \frac{4(N+1)}{M} \geq 0.5 \rightarrow N \leq \frac{M-8}{8} \tag{17}$$

4.1.2. Magnetizing Inductances. Considering maximum $\gamma\%$ current ripple, the magnetizing inductances of CIs can be calculated as:

$$\begin{aligned}
 I_{L_{m_1}} = I_{L_{m_2}} = I_{L_m} &\rightarrow \Delta i_{L_{m_{\max}}} = \frac{\gamma}{100} I_{L_m} = \frac{2\gamma(N+1)}{100(1-D)} I_o \\
 L_{m_1} = L_{m_2} = L_m &\geq \frac{V_{in} D}{\Delta i_{L_{m_{\max}}} f_{sw}} \\
 \rightarrow L_m &\geq \frac{100D(1-D)V_{in}}{2\gamma f_{sw} (N+1)I_o} = \frac{100D(1-D)^2 R}{8\gamma f_{sw} (N+1)^2}
 \end{aligned} \tag{18}$$

4.1.3. Flux Density Constraint. The maximum flux densities of CIs are calculated as:

$$\begin{aligned}
 B_{\max_1} = B_{DC_1} + \frac{\Delta B_1}{2} &= \frac{L_{m1} I_{L_{m1}}}{N_{p_1} A_{c_1}} + \frac{V_{in} D}{2N_{p_1} f_{sw} A_{c_1}} \\
 B_{\max_2} = B_{DC_2} + \frac{\Delta B_2}{2} &= \frac{L_{m2} I_{L_{m2}}}{N_{p_2} A_{c_2}} + \frac{V_{in} D}{2N_{p_2} f_{sw} A_{c_2}}
 \end{aligned} \tag{19}$$

where A_{c1} and A_{c2} are the cross-sectional areas of the magnetic paths in the CIs' cores. Maximum flux densities $B_{\max1}$ and $B_{\max2}$ are required to be smaller than the saturation flux density of the selected magnetic cores.

4.2. LEAKAGE INDUCTANCE IMPACT AND DESIGN

The leakage inductances of CIs have some impacts on the converter performance. The current falling rate of the diodes is controlled by the leakage inductances—as the leakage inductances increase, the current falling rate of the diodes decreases. Thus, the diodes are turned off at ZCS condition, and there is no reverse-recovery problem for them at the instant of turn-off, and the switching loss of the proposed converter is reduced. In addition, according to (13), the voltage gain of the converter decreases as the leakage

inductances increase. Accordingly, a trade-off should be considered to design the leakage inductance of CIs leakage inductance. Therefore, strict care of the physical arrangement of the windings of the CIs is required to make its coupling coefficient as close to 1 as possible (but not exactly 1) to minimize the leakage inductance, but not to make it zero.

For a specified coupling coefficient (k), the leakage inductance (L_k) is calculated from (20).

$$k = \frac{L_m}{L_m + L_k} \rightarrow L_k = L_m \left(\frac{k-1}{k} \right) \quad (20)$$

4.3. CAPACITORS DESIGN

The rated voltages of the capacitors can be determined from either (10) or (11). The capacitances can be determined using:

$$\begin{aligned} C_{c1} = C_{c2} &\geq \frac{(1-D) \times \frac{1}{1-D} I_o}{f_{sw} \Delta V_{C_{c1} \max}} = \frac{I_o}{f_{sw} \Delta V_{C_{c1} \max}} \\ C_{m1} &\geq \frac{(1-D) \times \frac{1}{1-D} I_o}{f_{sw} \Delta V_{C_{m1} \max}} = \frac{I_o}{f_{sw} \Delta V_{C_{m1} \max}} \\ C_{m2} &\geq \frac{(1-D) \times \frac{1}{1-D} I_o}{f_{sw} \Delta V_{C_{m2} \max}} = \frac{I_o}{f_{sw} \Delta V_{C_{m2} \max}} \\ C_o &\geq \frac{D I_o}{f_{sw} \Delta V_{C_o \max}} \end{aligned} \quad (21)$$

where parameters $\Delta V_{C_{c1} \max}$, $\Delta V_{C_{c2} \max}$, $\Delta V_{C_{m1} \max}$, $\Delta V_{C_{m2} \max}$, and $\Delta V_{C_o \max}$ are the maximum voltage ripples of the capacitors calculated by (20) considering maximum $x\%$ voltage ripple.

$$\begin{aligned}
\Delta V_{C_{c1} \max} &= \Delta V_{C_{c2} \max} = \frac{x}{100} V_{C_{c1}} = \frac{x}{400(1+N)} V_0 \\
\Delta V_{C_{m1} \max} &= \frac{x}{100} V_{C_{m1}} = \frac{x(2+N)}{400(N+1)} V_0 \\
\Delta V_{C_{m1} \max} &= \frac{x}{100} V_{C_{m2}} = \frac{x}{400} V_o \\
\Delta V_{C_o \max} &= \frac{x}{100} V_{C_o} = \frac{x}{100} V_o
\end{aligned} \tag{22}$$

The RMS ripple currents of the capacitors are:

$$\begin{aligned}
I_{C_{c1} (RMS)} &= I_{C_{c2} (RMS)} = \sqrt{\frac{1+2(2N+1)^2}{3(1-D)}} I_o \\
I_{C_{m1} (RMS)} &= I_{C_{m2} (RMS)} = \sqrt{\frac{8}{3(1-D)}} I_o \\
I_{C_o (RMS)} &= \sqrt{\frac{D(7-3D)}{3(1-D)}} I_o
\end{aligned} \tag{23}$$

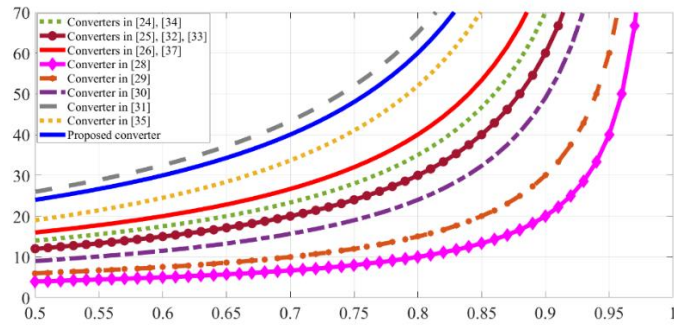
4.4. SEMICONDUCTOR DEVICES SELECTION

The voltage and current ratings obtained from (14) and (16) provide an estimation for the voltage and current ranges of the semiconductor devices. However, a safety margin is considered to account for the effect of the parasitic elements to make sure that the semiconductor devices always operate safely.

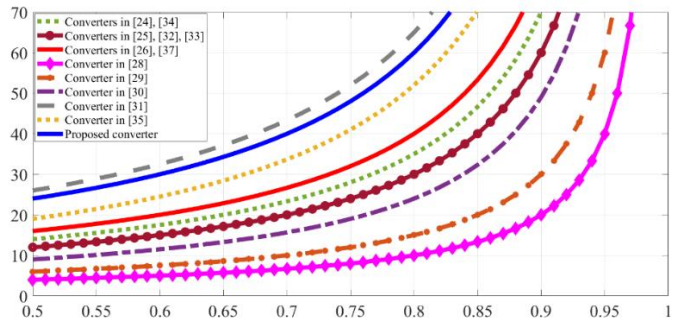
5. COMPARATIVE STUDY

In this section, the proposed converter is compared to 12 existing converters of its class; they are all CI-based interleaved high-voltage gain DC-DC topologies. Table 1

summarizes the number of passive and active components, voltage gains, and voltage stresses across the semiconductor devices. The interleaved converters in [24-27] employ two two-winding CIs, while the ones in [28-35] and the proposed converter are based on utilizing two three-winding coupled inductors; thus, there are four magnetic windings in the converters in [24-27] and six magnetic windings in the converters in [28-35] and proposed converter. The voltage gains from the converters are plotted in Figs 6(a) and 6(b) for $N=1$ and $N=2$, respectively. Comparing the three-winding CIs-based converters with the two-winding CIs-based converters, it is obvious that the use of more magnetic windings does not always result in increasing the voltage gain; For example, converters in [28-30, 32-34] with three-winding CIs have lower voltage gain than the converters in [26, 27] with two-winding CIs. However, for $N=1$, the proposed converter with three-winding CIs has the highest voltage gain; for $N=2$, the converter in [31] has the highest voltage gain, and the proposed converter has the next highest voltage gain among the competitors. Although for $N=2$, the converter in [31] has a higher voltage gain than the proposed converter, it has five more components compared to the proposed converter: two more capacitors, two more switches, and one more diode. In addition, although high N values for the CIs increases the voltage gain further, it is advisable to have a lower N to not only downsize the CIs but also to minimize the leakage inductances—thus, $N=1$ is used as the preferable value for the turns-ratios of the CIs. Moreover, with the exception of the



(a)



(b)

Figure 6. The voltage gain comparison for (a) $N=1$ and (b) $N=2$.

converter in [31] for $N \geq 1.5$, the proposed converter has the lowest voltage stress on the switches; therefore, switches with lower-rated voltages and smaller ON-state resistances could be adopted, resulting in decreased conduction losses and improved efficiency. Furthermore, with the exception of the converters in [24, 28, 29], the proposed converter has the smallest number of components, leading to reduced volume and cost. Also, it has relatively a low voltage stress on the output diode, implying that the diode with smaller voltage drop and ON-state resistance could be used, which contributes to reducing the conduction losses of the proposed converter.

Table 1. Comparison of proposed interleaved converter with other existing CI-based interleaved high gain DC-DC converters.

Interleaved converter	Voltage gain	No. of CIs	No. of capacitors	No. of switches	No. of diodes	Total No. of components	No. of magnetic windings	Maximum diode voltage stress	Voltage stress of main switches	Voltage gain for $D=0.6$ and $N=1$
Converter in [24]	$\frac{3N+1}{1-D}$	2	4	2	5	13	4	$\frac{2N}{3N+1}V_o$	$\frac{1}{3N+1}V_o$	10
Converter in [25]	$\frac{2N+2}{1-D}$	2	6	2	6	16	4	$\frac{1}{2}V_o$	$\frac{1}{2N+2}V_o$	10
Converter in [26]	$\frac{2N+4}{1-D}$	2	6	2	6	16	4	$\frac{N}{N+2}V_o$	$\frac{1}{2N+4}V_o$	15
Converter in [27]	$\frac{2N+4}{1-D}$	2	6	2	6	16	4	$\frac{N}{N+2}V_o$	$\frac{1}{2N+4}V_o$	15
Converter in [28]	$\frac{N}{1-D}$	2	2	3	2	9	6	$\frac{2N-1}{N}V_o$	$\frac{1}{N}V_o$	2.5
Converter in [29]	$\frac{N+1}{1-D}$	2	3	2	4	11	6	$\frac{2N+1}{N+1}V_o$	$\frac{1}{N+1}V_o$	5
Converter in [30]	$\frac{2+N+D(N-1)}{1-D}$	2	5	2	6	15	6	$\frac{N+1}{2+N+D(N)}$	$\frac{1}{2+N+D(N)}$	7.5
Converter in [31]	$\frac{6N+1}{1-D}$	2	7	4	6	19	6	$\frac{2N}{6N+1}V_o$	$\frac{1}{6N+1}V_o$	17.5
Converter in [32]	$\frac{2N+2}{1-D}$	2	5	2	6	15	6	$\frac{2N+1}{2N+2}V_o$	$\frac{1}{2N+2}V_o$	10
Converter in [33]	$\frac{2N+2}{1-D}$	2	5	2	6	15	6	$\frac{2N+1}{2N+2}V_o$	$\frac{1}{2N+2}V_o$	10
Converter in [34]	$\frac{3N+1}{1-D}$	2	7	2	8	19	6	$\frac{2N}{3N+1}V_o$	$\frac{1}{3N+1}V_o$	10
Converter in [35]	$\frac{2+3N+D(2N-1)}{1-D}$	2	8	2	9	21	6	$\frac{N+1}{2+3N+D(2)}$	$\frac{1}{2+3N+D(2)}$	14
Proposed Converter	$\frac{4N+4}{1-D}$	2	5	2	5	14	6	$\frac{2N+1}{2N+2}V_o$	$\frac{1}{4N+4}V_o$	20

Table 2. Parasitic elements of components used in experimental setup.

Component	Parasitic Elements
Switches	ON-state resistance: $R_{DS(on)}=0.0288 \Omega$ Output capacitance: $C_{oss}=189 \text{ pF}$ Turn-on and turn-off times: $t_{on}=40 \text{ ns}$, $t_{off}=54 \text{ ns}$
Diodes	Threshold forward voltage: $V_{F0, Dc1}=V_{F0}$, $Dc2=V_{F0}$, $Dr1=V_{F0}$, $Dr2=0.45 \text{ V}$ $V_{F0, Do}=0.75 \text{ V}$ ON-state resistance: $R_{on, Dc1}=R_{on, Dc2}=R_{on, Dr1}=R_{on, Dr2}=0.1 \Omega$ $R_{on, Do}=0.17 \Omega$
Capacitors	Equivalent series resistance: $R_{Cc1}=R_{Cc2}=0.004 \Omega$, $R_{Cm1}=R_{Cm2}=0.0033 \Omega$ $R_{Co}=0.0039 \Omega$
CIs with $N=1$	Resistance of primary, secondary, and tertiary windings: $R_{p1}=R_{s1}=R_{t1}=R_{p2}=R_{s2}=R_{t2}=0.01 \Omega$ Core loss $< 5 \text{ W}$

6. LOSS ANALYSIS

The analytical loss analysis of the proposed converter is performed by considering the parasitic elements of the components. The parasitic elements of the proposed converter are presented in Table 2.

The MOSFETs' losses comprise conduction losses ($P_{cond,Q}$) and switching losses ($P_{sw,Q}$), calculated as:

$$\begin{aligned}
 P_{cond,Q_1} &= R_{DS(on)} I_{Q_1(RMS)}^2 \\
 P_{cond,Q_2} &= R_{DS(on)} I_{Q_2(RMS)}^2 \\
 P_{sw,Q_1} &= f_{sw} V_{Q_1} \left(C_{oss} V_{Q_1} + \frac{1}{2} I_{L_{m1}} (t_{on} + t_{off}) \right) \\
 P_{sw,Q_2} &= f_{sw} V_{Q_2} \left(C_{oss} V_{Q_2} + \frac{1}{2} I_{L_{m2}} (t_{on} + t_{off}) \right) \\
 P_Q &= P_{cond,Q_1} + P_{cond,Q_2} + P_{sw,Q_1} + P_{sw,Q_2}
 \end{aligned} \tag{24}$$

The reverse-recovery losses of the diodes are zero and neglected because due to the leakage inductances of CIs, the diodes turn off naturally under the ZCS condition. The conduction losses of the diodes are extracted from (25).

The conduction losses of the capacitors are calculated by (26).

The CIs' losses include copper losses ($P_{cu,CI}$) and core losses ($P_{c,CI}$). The core loss of the CIs is extracted from the datasheet of the selected magnetic cores; the copper and total losses are obtained by (27).

$$\begin{aligned}
P_{cond,D_{c1}} &= V_{F0,D_{c1}} I_{D_{c1}}(Avg) + R_{on,D_{c1}} I_{D_{c1}}^2(RMS) \\
P_{cond,D_{c2}} &= V_{F0,D_{c2}} I_{D_{c2}}(Avg) + R_{on,D_{c2}} I_{D_{c2}}^2(RMS) \\
P_{cond,D_{r1}} &= V_{F0,D_{r1}} I_{D_{r1}}(Avg) + R_{on,D_{r1}} I_{D_{r1}}^2(RMS) \\
P_{cond,D_{r2}} &= V_{F0,D_{r2}} I_{D_{r2}}(Avg) + R_{on,D_{r2}} I_{D_{r2}}^2(RMS) \\
P_{cond,D_o} &= V_{F0,D_o} I_{D_o}(Avg) + R_{on,D_o} I_{D_o}^2(RMS) \\
P_D &= P_{cond,D_{c1}} + P_{cond,D_{c2}} + P_{cond,D_{r1}} + P_{cond,D_{r2}} + P_{cond,D_o}
\end{aligned} \tag{25}$$

$$\begin{aligned}
P_{C_{c1}} &= R_{C_{c1}} I_{C_{c1}}^2(RMS), \quad P_{C_{c2}} = R_{C_{c2}} I_{C_{c2}}^2(RMS) \\
P_{C_{m1}} &= R_{C_{m1}} I_{C_{m1}}^2(RMS), \quad P_{C_{m2}} = R_{C_{m2}} I_{C_{m2}}^2(RMS) \\
P_{C_o} &= R_{C_o} I_{C_o}^2(RMS) \\
P_C &= P_{C_{c1}} + P_{C_{c2}} + P_{C_{m1}} + P_{C_{m2}} + P_{C_o}
\end{aligned} \tag{26}$$

$$\begin{aligned}
P_{cu,CI_1} &= R_{p1} I_{L_{k1}}^2(RMS) + R_{s1} I_{L_{k3}}^2(RMS) + R_{t1} I_{L_{k4}}^2(RMS) \\
P_{cu,CI_2} &= R_{p2} I_{L_{k2}}^2(RMS) + R_{s2} I_{L_{k3}}^2(RMS) + R_{t2} I_{L_{k4}}^2(RMS) \\
P_{CI} &= P_{cu,CI_1} + P_{cu,CI_2} + P_{c,CI_1} + P_{c,CI_2}
\end{aligned} \tag{27}$$

Using (24)-(27), the total loss of the proposed converter is given by:

$$P_{Loss} = P_Q + P_D + P_C + P_{CI} \tag{28}$$

The analytical efficiency of the converter is obtained from (29).

$$\eta(\%) = 100 \times \frac{P_{out}}{P_{out} + P_{Loss}} \tag{29}$$

More detailed information about the analytically calculated loss breakdown and efficiency is provided in the next section.

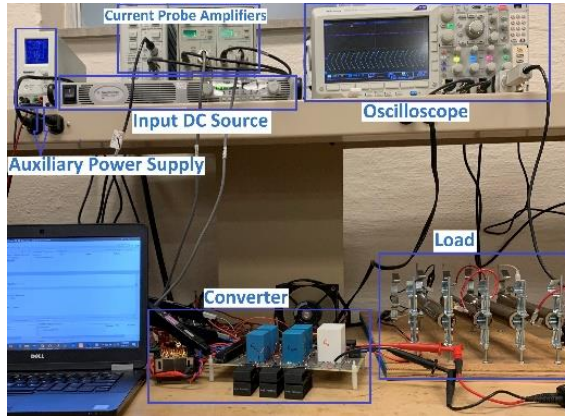


Figure 7. Photograph of the experimental prototype.

Table 3. Specifications of the experimental prototype.

Parameter/Component	Specification
Output voltage V_o	400 V
Rated Power	400 W
Magnetizing inductances L_{m1} and L_{m2}	80 μ H
Leakage inductances L_{k1} and L_{k2}	1.45 μ H
Leakage inductances L_{k3} and L_{k4}	2.90 μ H
Capacitors C_{c1} and C_{c2}	B32776G4506K000 50 μ F
Capacitors C_{cm1} and C_{cm2}	B32678G4206K000 20 μ F
Capacitor C_o	C4AEOBW5200A3LJ 20 μ F
Turns-ratios N_{sp1} , N_{ip1} , N_{sp2} , and N_{ip2}	1
Switches Q_1 and Q_2	PSMN016-100PS
Diodes D_{c1} , D_{c2} , D_{r1} , and D_{r2}	LQA06T300
Output diode D_o	C3D10060A

7. EXPERIMENTAL RESULTS

To experimentally verify the performance of the proposed converter, a 400 W prototype is developed, which is shown in Figure 7. The specifications for the implemented prototype are presented in Table 3. A C2000™ microcontroller TMS320F28335 is used to generate two interleaved gate signals for switches Q_1 and Q_2 . The proposed converter is tested with a switching frequency of 50 kHz. The turns-ratios of CIs are assumed to be

unity ($N=1$). A FerroxCube core ETD54/28/19-3C90-A250 with 12 turns in the primary winding and 12 turns in each of the secondary and tertiary windings is used for implementing each CI.

Experimental waveforms of the proposed converter for the input voltage of 20 V and the output voltage of 400 V at the full load of 400 W are shown in Figure 8(a)-(i); the converter needs to operate at the duty cycle of 0.6 for the switches. From (11), the theoretical value of the voltage gain is calculated as 20. Note that there is a little difference between the experimentally measured and theoretically calculated values, which is unavoidable due to the existence of parasitic elements, especially the leakage inductances, in the reality. The output voltage along with the output current is depicted in Figure 8(a), with average respective values of 383V and 0.98 A; the measured output voltage is close enough to the theoretical value of 400 V, which verifies the ability of the proposed converter to achieve a high-voltage gain of 20 without extreme duty cycles for the switches. The experimental voltage waveforms for capacitors C_{c1} , C_{c2} , C_{m1} , and C_{m2} are illustrated in Figure 8(b). The clamp capacitors voltages (V_{Cc1} and V_{Cc2}) are measured as 49 V, which verifies the calculated value of 50 V from (11). The voltages of multiplier capacitors are measured as 145 V and 94.5 V for C_{m1} and C_{m2} , respectively; these values are close to the theoretical calculations of 150 V and 100 V for V_{Cm1} and V_{Cm2} , respectively. The voltages across the semiconductor devices are depicted in Figures 8 (c) and (d); the voltage stresses of the switches and diodes confirm the calculated values from (14), which are: $V_{Q1}=V_{Q2}=V_{Dc2}=50$ V, $V_{Dc1}=V_{Dr2}=100$ V, $V_{Dr1}=200$ V, and $V_{Do}=300$ V. The voltage stresses of switches Q_1 and Q_2 are effectively clamped to a low voltage of 50 V because of clamp diodes D_{c1} and D_{c2} . The voltage stresses of all the semiconductor devices are reasonably

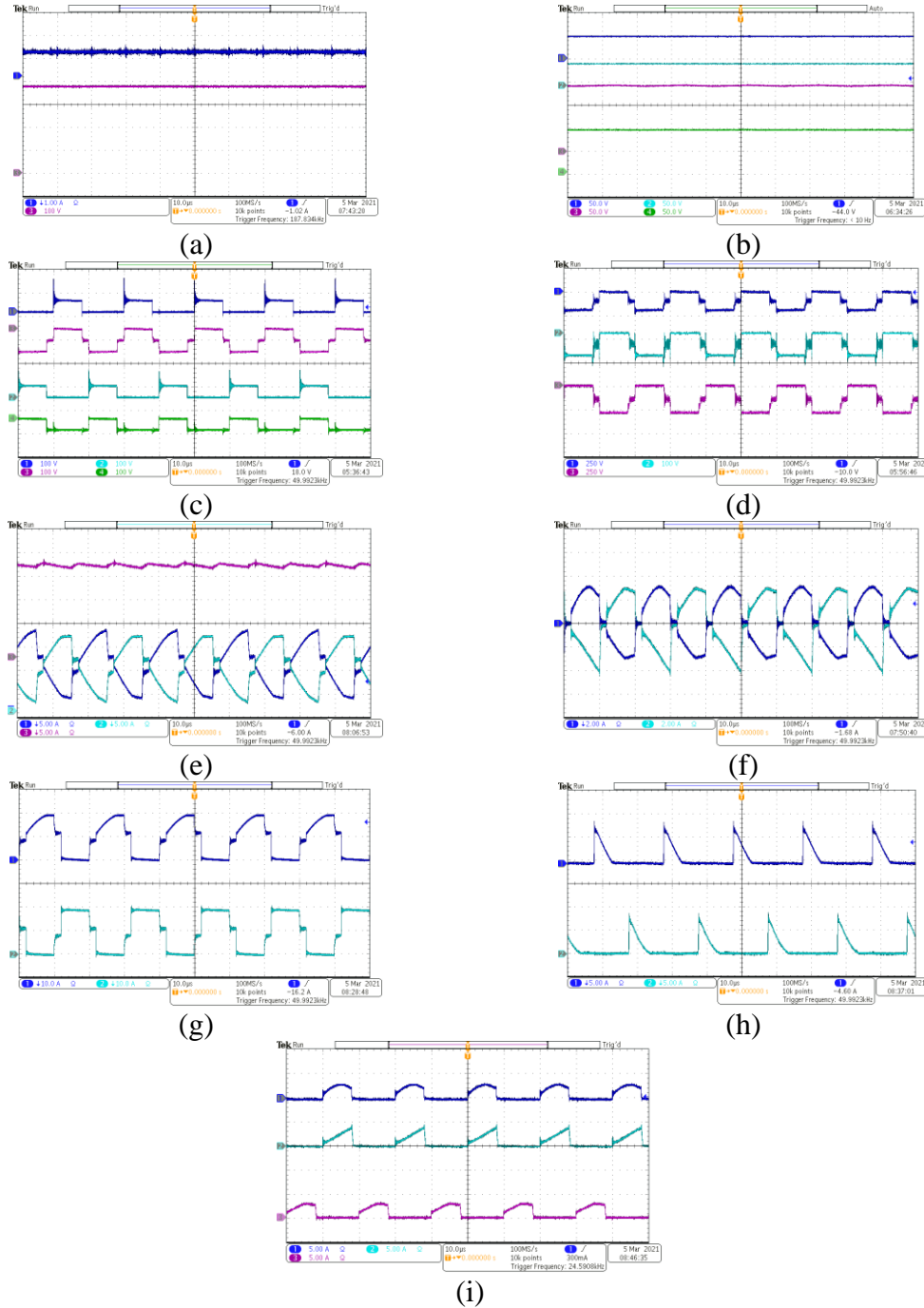


Figure 8. Experimental waveforms of the proposed converter: (a) output current (CH1) and output voltage (CH2) $[t_0-t_1]$; (b) voltages of capacitors C_{c1} (CH1), C_{c2} (CH2), C_{m1} (CH3), and C_{m2} (CH4); (c) voltages of switches Q_1 (CH1) and Q_2 (CH2) as well as diodes D_{c1} (CH3) and D_{c2} (CH4); (d) voltages of diodes D_{r1} (CH1), D_{r2} (CH2), and D_o (CH3); (e) currents of leakage inductances L_{k1} (CH1) and L_{k2} (CH2) as well as input current (CH3); (f) currents of leakage inductances L_{k3} (CH1) and L_{k4} ; (g) currents of switches Q_1 (CH1) and Q_2 (CH2); (h) currents of diodes D_{c1} (CH1) and D_{c2} (CH2); (i) currents of diodes D_{r1} (CH1), D_{r2} (CH2), and D_o (CH3).

lesser than the output voltage (400 V), and that enables the usage of the switches and diodes with low-voltage ratings; for this reason, the conduction losses are reduced, which contributes to efficiency improvement the proposed converter. The measured input current along with the currents of leakage inductances L_{k1} and L_{k2} are shown in Figure 8(e); the average values are measured to be about 20 A and 10 A for the input current and the currents of inductances L_{k1} and L_{k2} , respectively. Due to the interleaving effect, the input current ripple is low, which leads to a long lifetime for the input PV source [36, 37]. Furthermore, as expected, the average currents of L_{k3} and L_{k4} are zero, as illustrated in Figure 8(f). The currents for switches Q_1 and Q_2 are shown in Figure 8(f), and the diodes' currents are depicted in Figures 8(g) and (h); as seen, they are turned off under ZCS condition, and there is no reverse-recovery issue for the diodes.

Figure 9 shows the dynamic response of the output voltage for a step change in the load from 400 W to 250 W and vice versa. It is obvious that as the load power changes, the output voltage deviation from 400 V changes slightly: for the load powers of 400 W and 250 W, the output voltage is 383 V (with deviation of 17 V) and 388 V (with deviation of 12 V), respectively; the deviation is small and less than 5 %, which proves the inherent stability of the proposed converter. This deviation could be eliminated if any simple closed-loop control is applied to the converter.

Using the analytical loss calculations provided in Section VI, the efficiency curves of the converter for two different input voltages of 20 V and 15 V are obtained and compared with the experimental results in Figure 10. As seen, the full load experimental efficiency is about 94.05 % for the voltage gain of 20 (corresponding to $V_{in}=20$ V and $D=0.6$) and 92.50 % for the voltage gain of 26.67 (corresponding to $V_{in}=15$ V and $D=0.7$).

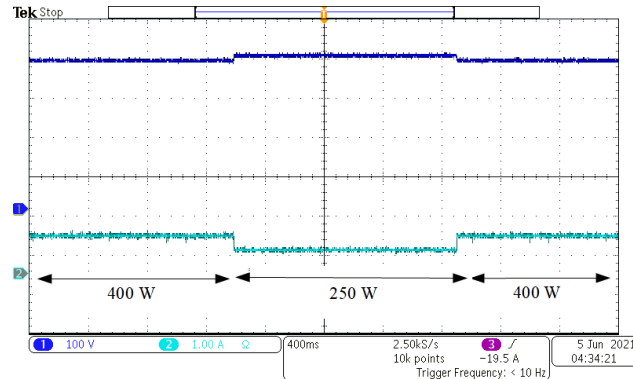


Figure 9. The dynamic response of the proposed converter: output voltage (CH1) and load current (CH2) for a step change in the load from 400 W to 250 W and vice versa for $V_{in}=20$ V and $D=0.6$.

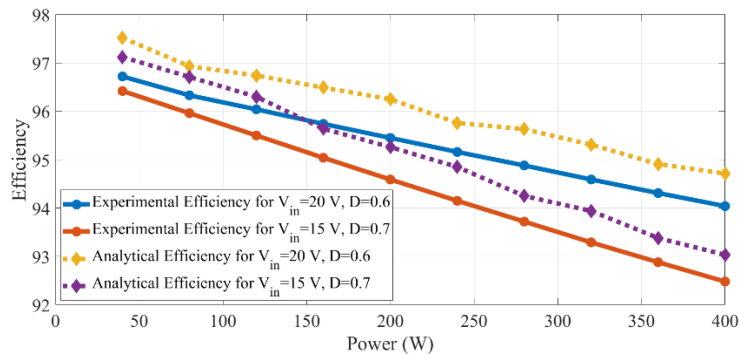
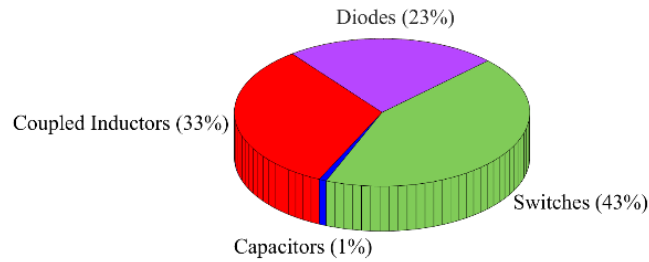
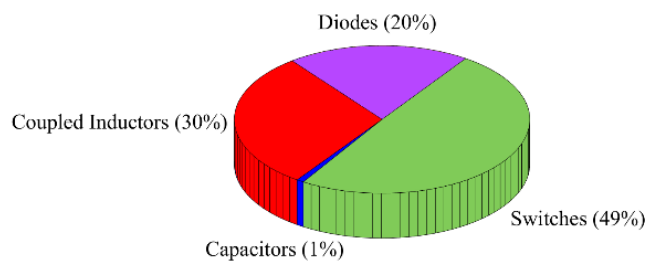


Figure 10. The analytically calculated and experimentally measured efficiency curves for two different input voltages.

Also, according to the analytical results, the full load analytical efficiency is 94.72 % and 93.05 % for the input voltages of 20 V and 15 V, respectively. As observed, there is a deviation less than 1 % between the analytical and experimental efficiency results. Figure 11 illustrates the analytical loss breakdown of the proposed converter at the full load of 400 W for two different input voltages of 20 V and 15 V. As observed, the power losses due to the CIs and MOSFETs are dominant and higher than other components.



(a)



(b)

Figure 11. Analytical loss breakdown of the proposed converter at the full load for two different input voltages and the same output voltage of 400 V: a) $V_{in}=20$ V and $D=0.6$, b) $V_{in}=15$ V and $D=0.7$.

8. CONCLUSION

An interleaved high-voltage gain DC-DC converter was proposed in this paper, which is suitable for PV systems. In an interleaved structure, three-winding CIs were combined with SC cells to achieve the following merits: high-voltage gain, low voltage stress on the switches and diodes, low current stress for the components, low input current ripple, and alleviation of the reverse-recovery problem of the diodes. The voltage stresses on the semiconductor devices were lesser than the output voltage, which leads to the employment of the low voltage-rating switches and diodes; thus, the conduction loss was

decreased, and the efficiency was improved. The alleviation of the reverse-recovery for the diodes was achieved by the ZCS conditions provided by CIs' leakage inductances. To verify the properties of the proposed converter, a comparative study was presented. In addition, to validate the theoretical analyses and calculations, a laboratory 400 W prototype was developed; the experimentally measured results were in agreement with the theoretically calculated values. The full load experimental efficiency was measured as 94.05 % for the input voltage of 20 V. All in all, it was concluded that the proposed interleaved converter is suitable for interfacing low-voltage PV panels to a high-voltage DC bus.

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II. A THREE-WINDING COUPLED INDUCTOR-BASED DUAL-SWITCH HIGH STEP-UP DC-DC CONVERTER FOR PHOTOVOLTAIC SYSTEMS

Ramin Rahimi, *Graduate Student Member, IEEE*, Saeed Habibi, *Graduate Student Member, IEEE*, Pourya Shamsi, *Senior Member, IEEE*, Mehdi Ferdowsi, *Member, IEEE*

ABSTRACT

This paper proposes a new high step-up DC-DC converter for photovoltaic (PV) applications. A dual-switch structure with a three-winding coupled inductor (3WCI), whose secondary and tertiary windings are integrated with switched-capacitor (SC) cells, is adopted to achieve a high-voltage gain with a small duty cycle, thus avoiding an extremely high duty cycle. The input current is continuous, and the voltage gain could be adjusted by two parameters: the switches' duty cycle and 3WCI's turns-ratio, thus increasing the design flexibility of the proposed converter. In addition, low-voltage-rated MOSFETs with small ON-state resistances are selected, and their losses are reduced due to the low voltage stress and small duty cycle of the switches. Moreover, the current-falling rates of most diodes are controlled by the 3WCI's leakage inductances. The operating modes, detailed analyses, and design considerations for the proposed converter are presented. Additionally, comparisons with other high step-up converters are provided. A 200-W laboratory prototype with an output voltage of 400 V is fabricated and tested using various input voltages to validate the theoretical analyses.

Keywords: High step-up DC-DC converter, high-voltage gain, coupled inductor, switched-capacitor, dual-switch, renewable energy, photovoltaic.

1. INTRODUCTION

Given the growing energy demands, conventional energy sources—such as fossil fuel and natural gas—can only last for a few decades; therefore, in the future, the world will face a serious problem due to the energy shortage crises and environmental pollutions [1]. Using clean renewable energy sources is a promising solution to the impending global energy crisis. With the reduction in the cost of photovoltaic (PV) systems, PV technology has the potential to become a primary renewable energy source for the future electricity supply [2]; however, output voltage of the PV panels is relatively low.

The series-connected configuration of the PV panels is a conventional solution to raise the voltage level, but due to any power mismatch of the panels and partial shading, the generated PV power is decreased. The most efficient solution is using a high step-up DC-DC converter to increase PV panel voltage to the desired value. Figure 1 depicts a general schematic of a PV generation system that includes a DC-AC converter to deliver power to the AC grid, a DC-DC converter to inject the power to the DC micro-grid, and a high step-up DC-DC converter to increase the voltage generated by the PV panel. A conventional DC-DC boost converter can increase the PV panel voltage to a high value with an extremely large duty cycle; accordingly, the output diode suffers from the reverse-recovery problem, and the voltage stress on the power switch is high and equal to the output voltage—consequently, a high-voltage-rated switch with high ON-state resistance $R_{DS(on)}$ is required, which increases the conduction losses and limits the voltage gain, even at extremely high duty cycles [3, 4]. Thereby, a conventional boost converter is not suitable for high-voltage gain PV applications.

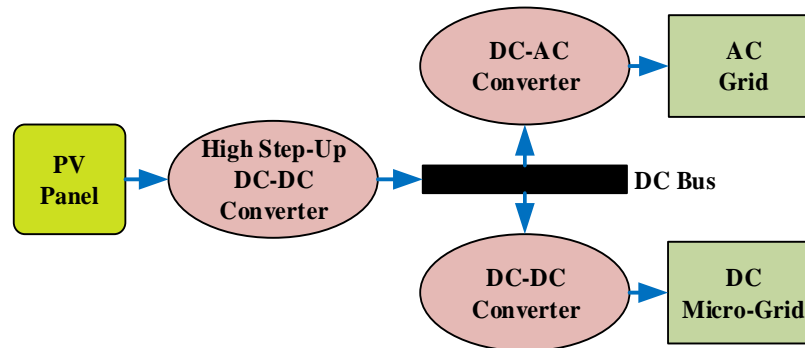


Figure 1. General schematic of a PV generation system.

Recently, using the voltage-boosting techniques, many high step-up DC-DC converters were proposed to achieve a high-voltage gain without extremely large duty cycles. The voltage-boosting techniques are based on 1) multi-stage structure; including cascade, quadratic, and multilevel; 2) voltage multiplier cells (VMCs) including switched-capacitor (SC) and switched-inductor (SL); 3) magnetic coupler, including coupled inductor (CI) and built-in transformer (BIT).

Multi-stage DC-DC converters suffer from large numbers of components that increase system size, volume, and cost of the system and decrease the conversion efficiency. The SC technique was adopted in [5-9] to obtain high step-up DC-DC converters. In SC-based converters, the capacitors operate alternately in parallel and series processes that correspond to charging and discharging states, respectively; consequently, at the capacitors' series-connected operating states, energy is released toward the output and a high output voltage is obtained. However, the main disadvantage of SC-based converters is that extreme instantaneous currents flow through the capacitors, leading to extra power losses and electromagnetic noises. In [10-12], the SL technique was used to improve the boost capability of the DC-DC converters. In SL-based high step-up

converters, an inherent high voltage gain can be achieved with the transition between inductors' parallel and series connections, relating to energizing and de-energizing states of the inductors, respectively. The SL cells can be either active or passive; active SL cells consist of active switches and inductors, and there are diodes and inductors in passive SL cells. The high step-up DC-DC converters in [3, 13-16] combined the SC and SL techniques to extend the voltage gains. The CI technique is integrated into SC, SL, or combined SC and SL techniques to further extend the voltage gain, examples of which were proposed in [17-25]. By employing CI, the voltage gain can be adjusted by two parameters: the turns-ratio of the CI and duty cycle of the power switches. These two degrees of freedom increase the converter design flexibility. These converters usually require a clamping circuitry to absorb the stored energy in the leakage inductance of the CI and to limit the voltage stresses on the switches. However, the duty cycle varies from 0 to 1 for CI-based converters in [17-25], therefore larger duty cycle must be used if a high-voltage gain is required, thus leading to high conduction losses on the power switches. Unlike the converters in [17-25], the CI-based converters in [26-36] have duty cycles ranging from 0 to 0.5, which leads to achieving a high-voltage gain with a small duty cycle range lower than 0.5. The converters in [26-31, 33-36] are based on the integration of the CI, Z-source (ZS) or quasi-Z-source (qZS) network, and SC techniques.

This paper proposes a dual-switch high step-up converter based on the combination of the CI and SC techniques, which is suitable for the PV applications. The initial idea with a two-winding CI was originally introduced in [32] by the authors, and in this paper, the modified version with a three-winding CI and different SC connections as well as the detailed analyses and experimental results are provided. Compared to the converter in [32],

the proposed converter offers higher voltage gain, lower voltage stresses on the switches, and higher efficiency. The voltage gain of the proposed converter is inversely proportional to $(1-2D)$, which is more commonly seen in the ZS- or qZS-based high step-up DC-DC converters; however, the proposed converter is not a type of ZS or qZS converter. That is, the proposed converter is a dual-switch converter whose voltage gain is like the ZS and qZS-based DC-DC converters.

The primary merits of the proposed converter are as follows:

1) Like the ZS and qZS converters, the proposed converter achieves high-voltage gains with small duty cycles varying from 0 to 0.5, thereby helping to reduce the conduction losses of the power switches. That is, because the range of the duty cycle does not exceed 0.5, the conduction losses on the power switches are reduced at high-voltage gains.

2) The energy stored in the leakage inductances of the CI is absorbed and recycled successfully by means of passive lossless clamping circuitry, which further extends the voltage gain of the proposed converter.

3) The voltage stresses on the semiconductor devices are low; thus, low-voltage-rated switches and diodes with low ON-state resistances are adopted, which reduces the conduction losses and improves the efficiency.

4) The current-falling rates of some diodes are controlled by the leakage inductances of the CI; accordingly, their reverse-recovery losses significantly decrease.

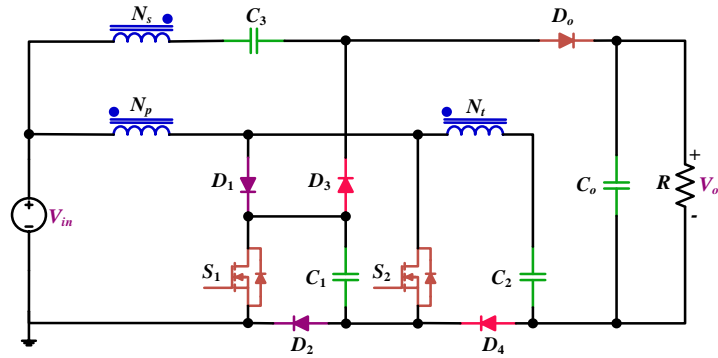
5) To adjust the converter's voltage gain, there are two degrees of freedom: CI's turns-ratio and duty cycle of the switches, thus making the proposed converter's design flexible.

The rest of the paper is organized as follows: Section 2 describes the circuit configuration and operating modes of the proposed converter. The steady-state analysis of the proposed converter is presented in Section 3. In Section 4, the main design considerations are provided. Comparisons with other similar high step-up DC-DC converters are given in Section 5. Section 6 describes the experimental results. The conclusion is drawn in Section 7.

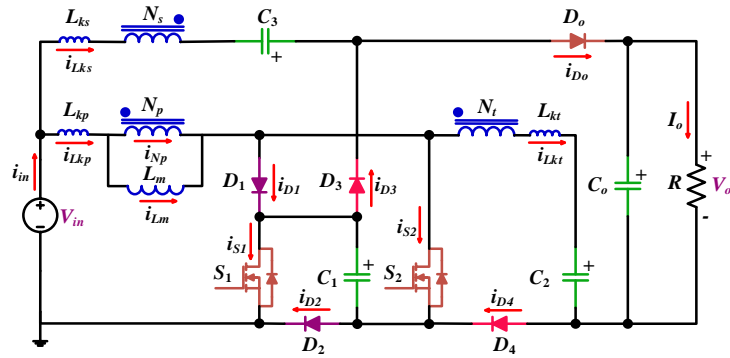
2. CIRCUIT CONFIGURATION AND OPERATING MODES OF THE PROPOSED CONVERTER

2.1. CIRCUIT CONFIGURATION

The topology of the proposed high step-up DC-DC converter is shown in Figure 2(a), and its equivalent power circuit is depicted in Figure 2(b). Two power switches (S_1 and S_2) are commanded simultaneously, and there is a three-winding CI (3WCI), which is modeled as a combination of a magnetizing inductor—representing the actual inductance of the 3WCI—an ideal three-winding transformer, and leakage inductances connected in series with the transformer windings. Parameters N_p , N_s , and N_t are the numbers of turns of the primary, secondary, and tertiary windings, respectively; L_{kp} , L_{ks} , and L_{kt} are the corresponding leakage inductances; L_m is the magnetizing inductance modeled in the primary side. In addition, five diodes (D_1 - D_4 and D_o) and four capacitors (C_1 - C_3 and C_o) are included in the proposed converter. The magnetizing inductance of the 3WCI serves as the boost inductor with turns number of N_p ; The secondary and tertiary windings with turns numbers of N_s and N_t are connected in series with capacitors C_3 and C_2 , respectively, to achieve a high-voltage gain. Coupling references of the 3WCI are represented with “●”, as



(a)



(b)

Figure 2. Proposed high step-up DC-DC converter and its equivalent circuit: (a) proposed converter, (b) equivalent circuit of the proposed converter.

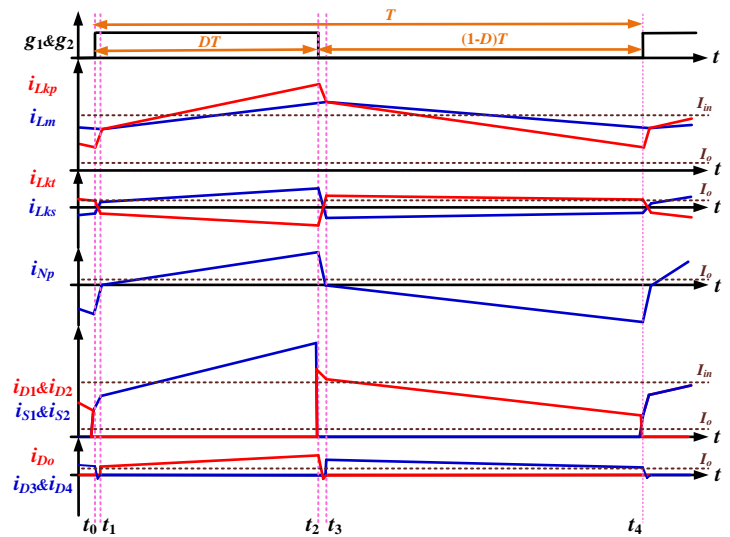


Figure 3. Key current waveforms of the proposed converter.

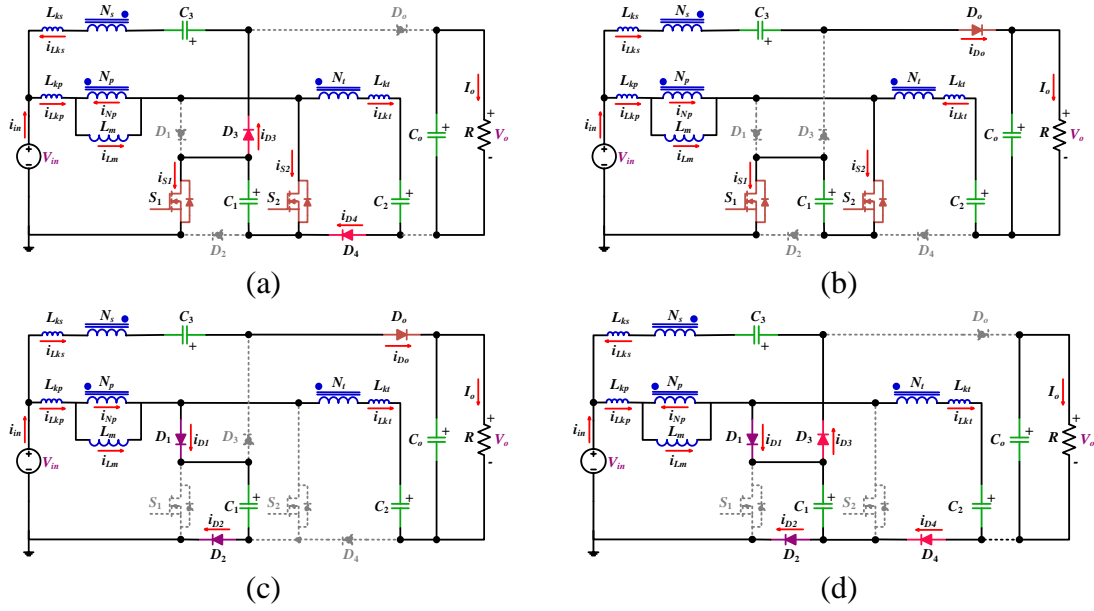


Figure 4. Equivalent circuits of the operating modes for the proposed converter: (a) Mode 1 $[t_0-t_1]$, (b) Mode 2 $[t_1-t_2]$, (c) Mode 3 $[t_2-t_3]$, (d) Mode 4 $[t_3-t_4]$.

given in Figure 2. Parameter R represents the load resistor; input and output voltages are V_{in} and V_o , respectively. Diodes D_1 and D_2 along with capacitor C_1 provide the passive lossless clamping circuitry for both switches S_1 and S_2 during their turn-off states.

2.2. OPERATING MODES OF THE PROPOSED CONVERTER

Two switches— S_1 and S_2 —commanded simultaneously with the duty cycle of D and switching period of $T=1/f_{sw}$, where f_{sw} is the switching frequency. The turns-ratios of 3WCI are $N_{sp}=N_s/N_p$ and $N_{tp}=N_t/N_p$. In continuous conduction mode (CCM), there are four operating modes in one switching period with the theoretical key current waveforms depicted in Figure 3. The average input and output currents are represented by I_{in} and I_o , respectively.

Mode 1 $[t_0-t_1]$: In this mode, as shown in Figure 4(a), both switches S_1 and S_2 turn on, and the current of the primary leakage inductance (i_{Lkp}) begins to increase at $t=t_0$. Diodes

D_3 and D_4 provide the path for the current of the secondary and tertiary leakage inductances ($i_{L_{ks}}$ and $i_{L_{kt}}$), respectively. At the end of this mode, current $i_{L_{kp}}$ reaches the magnetizing inductance's current (i_{L_m}) and diodes D_3 and D_4 turn off—the current-falling rate of these diodes are controlled by the leakage inductances of 3WCI. In this mode, output capacitor C_o provides the power to the load. The key circuit relationships for this mode are as in (1).

$$\begin{aligned}
V_{L_m} + V_{L_{kp}} &= V_{in} + V_{C_1}, \quad N_{tp}V_{L_m} + V_{L_{kt}} = -V_{C_2}, \quad N_{sp}V_{L_m} - V_{L_{ks}} = -V_{in} - V_{C_3} \\
i_{D_3}(t) &= i_{D_4}(t), \quad i_{L_{ks}}(t) = -i_{D_3}(t), \quad i_{L_{kt}}(t) = i_{D_4}(t) \\
i_{N_p}(t) &= N_{sp}i_{L_{ks}}(t) - N_{tp}i_{L_{kt}}(t) = -(N_{sp}i_{D_3}(t) + N_{tp}i_{D_4}(t)) \\
i_{L_{kp}}(t) &= i_{L_m}(t) + i_{N_p}(t) = i_{L_m}(t) - (N_{sp}i_{D_3}(t) + N_{tp}i_{D_4}(t)) \\
i_{S_1}(t) &= i_{S_2}(t) = i_{L_{kp}}(t) + i_{L_{ks}}(t) = i_{L_m}(t) - (N_{sp} + 1)i_{D_3}(t) - N_{tp}i_{D_4}(t)
\end{aligned} \tag{1}$$

Mode 2 [t_1 - t_2]: This mode, shown in Figure 4(b), begins at $t=t_1$ when the output diode starts to conduct as soon as the diodes D_3 and D_4 turn off. Current $i_{L_{kp}}$ is higher than i_{L_m} , and both increase linearly; current $i_{L_{ks}}$ increases in the positive direction, while current $i_{L_{kt}}$ increases in the negative direction. In this mode, the relationships are as:

$$\begin{aligned}
V_{L_m} + V_{L_{kp}} &= V_{in} + V_{C_1}, \quad (N_{sp} + N_{tp} + 1)V_{L_m} + V_{L_{kp}} - V_{L_{ks}} + V_{L_{kt}} = V_o - V_{C_2} - V_{C_3} \\
i_{L_{ks}}(t) &= i_{D_o}(t), \quad i_{L_{kt}}(t) = -i_{D_o}(t) \\
i_{N_p}(t) &= N_{sp}i_{L_{ks}}(t) - N_{tp}i_{L_{kt}}(t) = (N_{sp} + N_{tp})i_{D_o}(t) \\
i_{L_{kp}}(t) &= i_{L_m}(t) + i_{N_p}(t) = i_{L_m}(t) + (N_{sp} + N_{tp})i_{D_o}(t) \\
i_{S_1}(t) &= i_{S_2}(t) = i_{L_{kp}}(t) - i_{L_{kt}}(t) = i_{L_m}(t) + (N_{sp} + N_{tp} + 1)i_{D_o}(t)
\end{aligned} \tag{2}$$

Mode3 [t_2 - t_3]: At $t=t_2$, both switches turn off. As shown in Figure 4(c), diodes D_1 and D_2 start to conduct; meanwhile, diode D_o is still in ON-state to provide the path for both the secondary and tertiary sides' currents of the 3WCI. The currents of all the leakage inductances begin to decrease at $t=t_2$. At $t=t_3$, the current of L_m is equal to that of L_{kp} , and output diode D_o turns off naturally. The relationships of this mode are as:

$$\begin{aligned}
V_{L_m} + V_{L_{kp}} &= V_{in} - V_{C_1}, \quad (N_{sp} + N_{ip} + 1)V_{L_m} + V_{L_{kp}} - V_{L_{ks}} + V_{L_{kt}} = V_o - V_{C_2} - V_{C_3} \\
i_{L_{ks}}(t) &= i_{D_o}(t), \quad i_{L_{kt}}(t) = -i_{D_o}(t) \\
i_{N_{ip}}(t) &= N_{sp} i_{L_{ks}}(t) - N_{ip} i_{L_{kt}}(t) = (N_{sp} + N_{ip}) i_{D_o}(t) \\
i_{L_{kp}}(t) &= i_{L_m}(t) + i_{N_{ip}}(t) = i_{L_m}(t) + (N_{sp} + N_{ip}) i_{D_o}(t) \\
i_{D_2}(t) &= i_{D_1}(t) = i_{L_{kp}}(t) - i_{L_{kt}}(t) = i_{L_m}(t) + (N_{sp} + N_{ip} + 1) i_{D_o}(t)
\end{aligned} \tag{3}$$

Mode 4 [t_3 - t_4]: At the beginning of this mode, shown in Figure 4(d), diodes D_3 and D_4 turn on as soon as output diode D_o turns off, and currents $i_{L_{kp}}$ and i_{L_m} decrease to de-energize the 3WCI. The power of load is provided by output capacitor C_o . This mode's relationships are as:

$$\begin{aligned}
V_{L_m} + V_{L_{kp}} &= V_{in} - V_{C_1} \\
-(N_{sp} + 1)V_{L_m} - V_{L_{kp}} + V_{L_{ks}} &= V_{C_3}, \quad N_{ip} V_{L_m} + V_{L_{kt}} = V_{C_1} - V_{C_2} \\
i_{D_3}(t) &= i_{D_4}(t), \quad i_{L_{ks}}(t) = -i_{D_3}(t), \quad i_{L_{kt}}(t) = i_{D_4}(t) \\
i_{N_{ip}}(t) &= N_{sp} i_{L_{ks}}(t) - N_{ip} i_{L_{kt}}(t) = -(N_{sp} i_{D_3}(t) + N_{ip} i_{D_4}(t)) \\
i_{L_{kp}}(t) &= i_{L_m}(t) + i_{N_{ip}}(t) = i_{L_m}(t) - (N_{sp} i_{D_3}(t) + N_{ip} i_{D_4}(t)) \\
i_{D_2}(t) &= i_{D_1}(t) = i_{L_{kp}}(t) - i_{L_{kt}}(t) = i_{L_m}(t) - N_{sp} i_{D_3}(t) - (N_{ip} + 1) i_{D_4}(t)
\end{aligned} \tag{4}$$

3. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis of the proposed converter, all capacitors are assumed to be large enough with the constant voltages during a whole switching period. Additionally, only Modes 2 and 4 are considered, and transitional Modes 1 and 3 are ignored because their durations are too short.

3.1. IDEAL VOLTAGE GAIN CALCULATION

From the operating modes analysis in Section II, the voltage on the magnetizing inductance in Modes 2 and 4 are given. By ignoring the effect of the leakage inductances and applying the volt-second balance principle to the magnetizing inductance, the capacitors' voltages are obtained as in (5).

$$\begin{aligned} V_{C_1} &= \frac{1}{1-2D}V_{in}; & V_{C_2} &= \frac{1+2N_{tp}D}{1-2D}V_{in}; & V_{C_3} &= \frac{2(N_{sp}+1)D}{1-2D}V_{in} \\ V_{C_o} = V_o &= \frac{3+2(N_{sp}+N_{tp})}{1-2D}V_{in} \end{aligned} \quad (5)$$

The voltage gain (G) of the converter is given by:

$$G = \frac{V_o}{V_{in}} = \frac{3+2(N_{sp}+N_{tp})}{1-2D} \quad (6)$$

The duty cycle range is as $0 < D < 0.5$ for the proposed converter. As seen, the secondary and tertiary turns-ratios of the 3WCI have the same effects on the voltage gain; so, it is reasonable to assume that $N_{sp}=N_{tp}=N$ and simplify the voltage gain as:

$$G = \frac{V_o}{V_{in}} = \frac{3+4N}{1-2D} \quad (7)$$

Figure 5 illustrates the voltage gain variation plots based on changing the duty cycle for different turns-ratios. As observed, by increasing the duty cycle and turns-ratio, the voltage gain increases; thus, the desired voltage gain is achieved by having control over two parameters including the turns-ratio of the 3WCI and duty cycle of the switches—for instance, for $N=1$ and $D=0.25$, the voltage gain is 14.

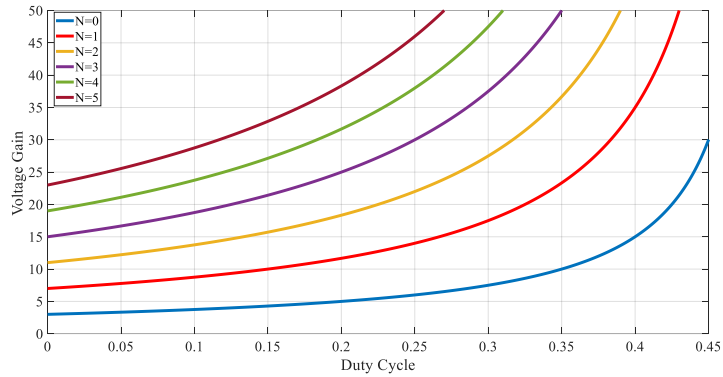


Figure 5. The ideal voltage gain versus the duty cycle for different turns-ratios.

3.2. LEAKAGE INDUCTANCE EFFECT ON VOLTAGE GAIN

By analyzing the current of output diode D_o , the effect of the 3WCI's leakage inductances on the voltage gain is clarified. Output diodes current (i_{D_o}) flows through the circuit during Modes 2 and 3; however, Mode 3 is too short and neglected. The duration of Mode 2 is DT . According to the converter's topology, the average current of diode D_o is equal to output current I_o . Thereby, the peak current of the output diode ($I_{D_o,\max}$) can be obtained as:

$$\frac{1}{T} \int_0^T i_{D_o}(t) dt = \frac{1}{T} \left(\frac{1}{2} \times I_{D_o,\max} \times DT \right) = I_o \rightarrow I_{D_o,\max} = \frac{2I_o}{D} = \frac{2V_o}{DR} \quad (8)$$

Knowing $I_{D_o,\max}$ and ignoring the current ripple of the magnetizing inductance of the 3WCI, in the presence of the leakage inductances, the calculation of the voltage gain is given as (9).

$$\begin{aligned}
\Delta i_{D_o} &= I_{D_o, \max} \\
V_{L_{kp}} &= L_{kp} \frac{di_{L_{kp}}}{dt} = L_{kp} \frac{d(i_{L_m} + 2Ni_{D_o})}{dt} = 2NL_{kp} \frac{di_{D_o}}{dt} \\
&= 2NL_{kp} \frac{\Delta i_{D_o}}{\Delta t} = 2NL_{kp} \frac{I_{D_o, \max}}{DT} = \frac{4Nf_{sw} L_{kp} V_o}{D^2 R} \\
V_{L_{ks}} &= L_{ks} \frac{di_{L_{ks}}}{dt} = L_{ks} \frac{di_{D_o}}{dt} = L_{ks} \frac{\Delta i_{D_o}}{\Delta t} = \frac{2f_{sw} L_{ks} V_o}{D^2 R} \\
V_{L_{kt}} &= L_{kt} \frac{di_{L_{kt}}}{dt} = -L_{kt} \frac{di_{D_o}}{dt} = -L_{kt} \frac{\Delta i_{D_o}}{\Delta t} = -\frac{2f_{sw} L_{kt} V_o}{D^2 R} \\
V_o &= (2N+1)V_{L_m} + V_{L_{kp}} - V_{L_{ks}} + V_{L_{kt}} + V_{C_2} + V_{C_3} \\
G &= \frac{V_o}{V_{in}} = \frac{3+4N}{(1-2D) \left(1 + \frac{2f_{sw} L_k}{D^2 R} (4N^2 L_{kp} + L_{ks} + L_{kt}) \right)}
\end{aligned} \tag{9}$$

If all the leakage inductances are equal to L_k (i.e., $L_{kp}=L_{ks}=L_{kt}=L_k$), the voltage gain can be written as in (10).

$$G = \frac{V_o}{V_{in}} = \frac{3+4N}{(1-2D) \left(1 + \frac{4f_{sw} L_k}{D^2 R} (2N^2 + 1) \right)} \tag{10}$$

According to (10), it is concluded that in the presence of the leakage inductance, the voltage gain is related to the switching frequency, leakage inductance, and load resistance, in addition to the duty cycle of the switches and turns-ratio of the 3WCI. Figure 6 shows the voltage gain plots versus the duty cycle for different values of leakage inductance with $N=1$. It is obvious that the leakage inductance degrades converter's voltage gain. Thus, the coupling coefficient (k) of the 3WCI must be as close to 1 as possible to minimize the leakage inductance impact on the voltage gain. On the other hand, a small amount of leakage inductance is required to limit the input current variation and current-falling rate of some diodes. Therefore, the leakage inductance must not be zero, but should be minimized.

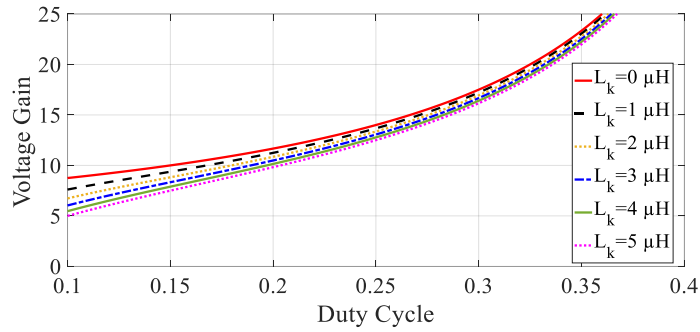


Figure 6. The effect of the leakage inductance on the voltage gain of the proposed converter for $N=1$.

3.3. VOLTAGE STRESSES OF SEMICONDUCTORS

Semiconductors' voltage stresses can be calculated when they are in OFF states.

Their voltage stresses are as:

$$\begin{aligned}
 V_{S_1} = V_{S_2} = V_{D_1} = V_{D_2} = V_{C_1} &= \frac{1}{1-2D} V_{in} = \frac{1}{3+4N} V_o \\
 V_{D_3} = V_{D_4} &= (N+1)V_{in} + NV_{C_1} + V_{C_3} = \frac{1+2N}{1-2D} V_{in} = \frac{1+2N}{3+4N} V_o \\
 V_{D_o} &= V_o - V_{C_1} = \frac{2+4N}{1-2D} V_{in} = \frac{2+4N}{3+4N} V_o
 \end{aligned} \tag{11}$$

Figure 7 presents the normalized voltage stresses (to the output voltage) of the semiconductors for the example duty cycle of 0.4. It is seen that the voltage stresses of switches S_1 and S_2 and diodes D_1 and D_2 decrease as the turns-ratio of the 3WCI increases. The voltage stresses on diodes D_3 , D_4 , and D_o increase as the turns-ratio increases, however they are always lower than the output voltage. Therefore, low-voltage-rated semiconductors with low ON-state resistances can be selected to yield low conduction losses.

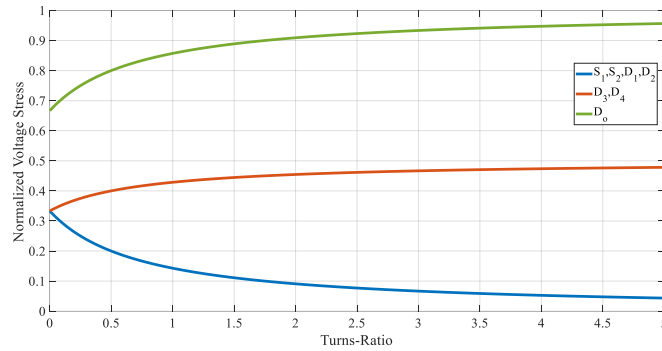


Figure 7. The semiconductors' normalized voltage stresses versus turns-ratio of the 3WCI for $D=0.4$.

3.4. CURRENT STRESSES OF COMPONENTS

The average input and output currents are I_{in} and I_o , respectively, and I_{Lm} is the average current of the magnetizing inductance L_m . Currents I_{in} and I_{Lm} are as:

$$I_{Lm} = I_{in} = \frac{3+4N}{1-2D} I_o \quad (12)$$

The root-mean-square (RMS) currents of capacitors are obtained as:

$$I_{C_{1,rms}} = \frac{2+4N+2D}{\sqrt{3}(1-2D)} I_o$$

$$I_{C_{2,rms}} = I_{C_{3,rms}} = \frac{2}{\sqrt{3D(1-D)}} I_o \quad (13)$$

$$I_{C_{o,rms}} = \sqrt{\frac{4-3D}{3D}} I_o$$

The average and RMS currents of the leakage inductances and semiconductors are given by (14).

$$\begin{aligned}
I_{L_{kp},avg} &= \frac{3+4N}{1-2D} I_o, \quad I_{L_{ks},avg} = I_{L_{kt},avg} = 0 \\
I_{S_1,avg} &= I_{S_2,avg} = \frac{2N+1.5}{1-2D} I_o \\
I_{D_1,avg} &= I_{D_2,avg} = \frac{2(N-D)+2.5}{1-2D} I_o \\
I_{D_3,avg} &= I_{D_4,avg} = I_{D_o,avg} = I_o \\
I_{L_{kp},rms} &= \sqrt{\left(\frac{3+4N}{1-2D}\right)^2 - \frac{8N^2}{3D(1-D)}} I_o \\
I_{L_{ks},rms} &= I_{L_{kt},rms} = \frac{2}{\sqrt{3D(1-D)}} I_o \\
I_{S_1,rms} &= I_{S_2,rms} = \frac{4N+3}{\sqrt{3D(1-2D)}} I_o \\
I_{D_1,rms} &= I_{D_2,rms} = \frac{4(N-D)+5}{\sqrt{3(1-D)(1-2D)}} I_o \\
I_{D_3,rms} &= I_{D_4,rms} = \frac{2}{\sqrt{3(1-D)}} I_o \\
I_{D_o,rms} &= \frac{2}{\sqrt{3D}} I_o
\end{aligned} \tag{14}$$

4. DESIGN CONSIDERATIONS

4.1. COUPLED INDUCTOR DESIGN

Assuming the current ripple of $\gamma\%$ and considering Mode 2, the magnetizing inductance L_m is obtained as:

$$\Delta i_{L_m} = \gamma\% I_{L_m} \rightarrow L_m = \frac{DV_{L_m}}{f_{sw} \Delta i_{L_m}} = \frac{D(2-2D)(1-2D)R}{(3+4N)^2 \gamma\% f_{sw}} \tag{15}$$

It is advisable to have a low N to downsize the 3WCI and minimize the leakage inductance; N is supposed to be 1 in this paper. After specifying N, the turn numbers for the primary, secondary, and tertiary windings of the 3WCI are obtained as:

$$N_p = \frac{L_m I_{Lm}}{B_{\max} A_c} + \frac{V_{in}(1-D)}{(1-2D)B_{\max} f_{sw} A_c} \quad (16)$$

$$N_s = N_t = NN_p$$

where A_c is the cross-sectional area of the magnetic path in the 3WCI, and B_{\max} is the specified maximum flux density that is required to be smaller than the saturation flux density of the selected magnetic core for the 3WCI.

To have a continuous input current, the input current variation (di_{in}/dt) must be limited by the leakage inductance of the 3WCI. Considering transitional Mode 1, for a given value of α as the maximum value of di_{in}/dt , the minimum leakage inductance is calculated as:

$$\frac{di_{in}}{dt} = \frac{di_{L_{kp}}}{dt} + \frac{di_{L_{ks}}}{dt} = \frac{1}{L_k} V_{L_{kp}} + \frac{1}{L_k} V_{L_{ks}}$$

$$V_{L_{kp}} + V_{L_m} = V_{in} + V_{C_1} = \frac{2-2D}{1-2D} V_{in}$$

$$\rightarrow V_{L_{kp}} + \frac{k}{1-k} V_{L_{kp}} = \frac{2-2D}{1-2D} V_{in} \rightarrow V_{L_{kp}} = \frac{(1-k)(2-2D)}{1-2D} V_{in} \quad (17)$$

$$V_{L_{ks}} - NV_{L_m} = V_{in} + V_{C_3} = \frac{1+2N}{1-2D} V_{in}$$

$$\rightarrow V_{L_{ks}} + \frac{k}{1-k} V_{L_{ks}} = \frac{1+2N}{1-2D} V_{in} \rightarrow V_{L_{ks}} = \frac{(1-k)(1+2N)}{1-2D} V_{in}$$

$$\frac{di_{in}}{dt} \leq \alpha \rightarrow L_k \geq \frac{(1-k)(3+2N-2D)V_{in}}{\alpha(1-2D)}$$

4.2. CAPACITORS DESIGN

The voltage stresses of all capacitors are presented in (5); their RMS current stresses are given by (13). By considering the maximum voltage ripple of $x\%$ for all capacitors, the capacitances can be calculated from Mode 2 by (18).

$$\begin{aligned}
C_1 &\geq \frac{D|I_{C_1,on}|}{x\%V_{C_1}f_{sw}} = \frac{(3+4N)(1+2N+D)}{x\%(1-2D)f_{sw}R} \\
C_2 &\geq \frac{D|I_{C_2,on}|}{x\%V_{C_2}f_{sw}} = \frac{3+4N}{x\%(1+2ND)f_{sw}R} \\
C_3 &\geq \frac{D|I_{C_3,on}|}{x\%V_{C_3}f_{sw}} = \frac{3+4N}{x\%(2N+2)Df_{sw}R} \\
C_o &\geq \frac{DI_{C_o,on}}{x\%V_{C_o}f_{sw}} = \frac{1-D}{x\%f_{sw}R}
\end{aligned} \tag{18}$$

5. COMPARISON STUDY

In this section, a comparison study is completed to demonstrate the merits of the proposed converter and confirm its performance. For a fair comparison, the proposed converter is compared with the CI-based converters whose voltage gain is proportional to $1/(1-2D)$ and their duty cycle ranges from 0 to 0.5. The comparison is summarized in Table 1. As seen, the number of switches, diodes, capacitors, magnetic cores, and magnetic windings, normalized current stress on the switches, maximum voltage stresses on the switches and diodes, total voltage stress on the semiconductors, and voltage gains are provided. The column named “Normalized current stress on switch(es)” indicates the average current of the switch(es) for each converter, which is normalized to the output current (I_o). In the comparison of the voltage gain, as can be observed from Figure 8(a), the proposed converter provides highest voltage gains for the whole duty cycle range from 0 to 0.5. Furthermore, under the same voltage gain and output current, the proposed converter and converter in [32] have the lowest current stress on the switches. Figure 8(b) shows the normalized maximum voltages stress on the switch(es) for all the converters

Table 1. Comparison of the proposed dc-dc converter with other similar converters.

Converter	Number of		Voltage gain (G)	Normalized current stress on switch(es)	Maximum voltage stress on		Total voltage stress on semiconductors
	Switch(es)/ Diodes/ Capacitors	Magnetic cores/ Magnetic windings			Switch(es)	diodes	
Ref. [26]	1/5/7	3/5	$\frac{1+2N-D}{1-2D}$	$G-1$	$\frac{2G-1}{1+4N}V_m$	$\frac{(2G-1)N}{1+4N}V_m$	$\frac{(2G-1)(2+4N)}{(1+4N)}V_m$
Ref. [27]	1/4/5	2/3	$\frac{N(1+D)}{1-2D}$	G	$\frac{2G+N}{3N}V_m$	$\frac{2G+N}{3}V_m$	$\frac{(2G+N)(1+4N)}{3N}V_m$
Ref. [28]	2/4/3	1/2	$\frac{1+2N}{1-2D}$	$G+N$	$\frac{G}{1+2N}V_m$	$\frac{2GN}{1+2N}V_m$	$\frac{G(4+4N)}{1+2N}V_m$
Ref. [29]	1/4/5	2/4	$\frac{1+2N}{1-2D}$	$G+1$	$\frac{G}{1+2N}V_m$	GV_m	$\frac{G(5+4N)}{1+2N}V_m$
Ref. [30]	1/4/5	2/3	$\frac{2+N}{1-2D}$	$G-1$	$\frac{G}{2+N}V_m$	$\frac{G(1+N)}{2+N}V_m$	$\frac{G(5+2N)}{2+N}V_m$
Ref. [31]	2/2/2	2/3	$\frac{1+N(1-D)}{1-2D}$	$G-1$	$\frac{2G-N}{2+N}V_m$	$\frac{(2G-N)N}{2+N}V_m$	$\frac{(2G-N)(3+N)}{2+N}V_m$
Ref. [32]	2/5/4	1/2	$\frac{3+2N}{1-2D}$	$\frac{G-1}{2}$	$\frac{G}{3+2N}V_m$	$\frac{G(2+2N)}{3+2N}V_m$	$\frac{G(9+4N)}{3+2N}V_m$
Ref. [33]	1/5/6	1/3	$\frac{2+N(2-D)}{1-2D}$	$G-1$	$\frac{G(2G-N)}{4G+N(3G-1)}V_m$	$\frac{G(2G-N)(1+N)}{4G+N(3G-1)}V_m$	$\frac{G(2G-N)(5+4N)}{4G+N(3G-1)}V_m$
Ref. [34]	1/4/5	2/3	$\frac{1+N}{1-2D}$	$G-1$	$\frac{G}{1+N}V_m$	$\frac{2G+N(G+N+1)}{2(1+N)}V_m$	$\frac{6G+N(5G+N+1)}{2(1+N)}V_m$
Ref. [35]	1/4/5	2/4	$\frac{2+2N+2D(N-1)}{1-2D}$	G	$\frac{G(G+N-1)}{G-1+N(3G+1)}V_m$	$\frac{G(G+N-1)(1+2N)}{G-1+N(3G+1)}V_m$	$\frac{G(G+N-1)(3+6N)}{G-1+N(3G+1)}V_m$
Ref. [36]	1/4/5	2/3	$\frac{2+N+DN}{1-2D}$	$G-1$	$\frac{2G+N}{4+3N}V_m$	$\frac{(2G+N)(1+N)}{(4+3N)}V_m$	$\frac{(2G+N)(5+3N)}{4+3N}V_m$
Proposed converter	2/5/4	1/3	$\frac{3+4N}{1-2D}$	$\frac{G}{2}$	$\frac{G}{3+4N}V_m$	$\frac{G(2+4N)}{3+4N}V_m$	$\frac{G(8+8N)}{3+4N}V_m$

with $N=1$; as obvious, under the same input voltage and voltage gain, the proposed converter has the lowest voltage stress on the switches compared to other converters. The maximum voltage stress on the diodes is always less than the output voltage for the proposed converter and other converters except the converter in [29]. Figure 8(c) shows the comparison of the normalized total voltage stress on the semiconductors with the same voltage gain and input voltage for $N=1$. As seen, for high voltage gains, the total voltage stress on semiconductors of the proposed converter is lower than other converters except the one in [35]. There is only one magnetic core in the proposed converter and topologies in [38, 32, 33], while other converters need multiple magnetic cores. Additionally, the converters in [28, 32] have two magnetic windings; there are five magnetic windings in the converter in [26] and three magnetic windings in other converters as well as the proposed converter. It is worth noting that the use of more magnetic windings does not always result

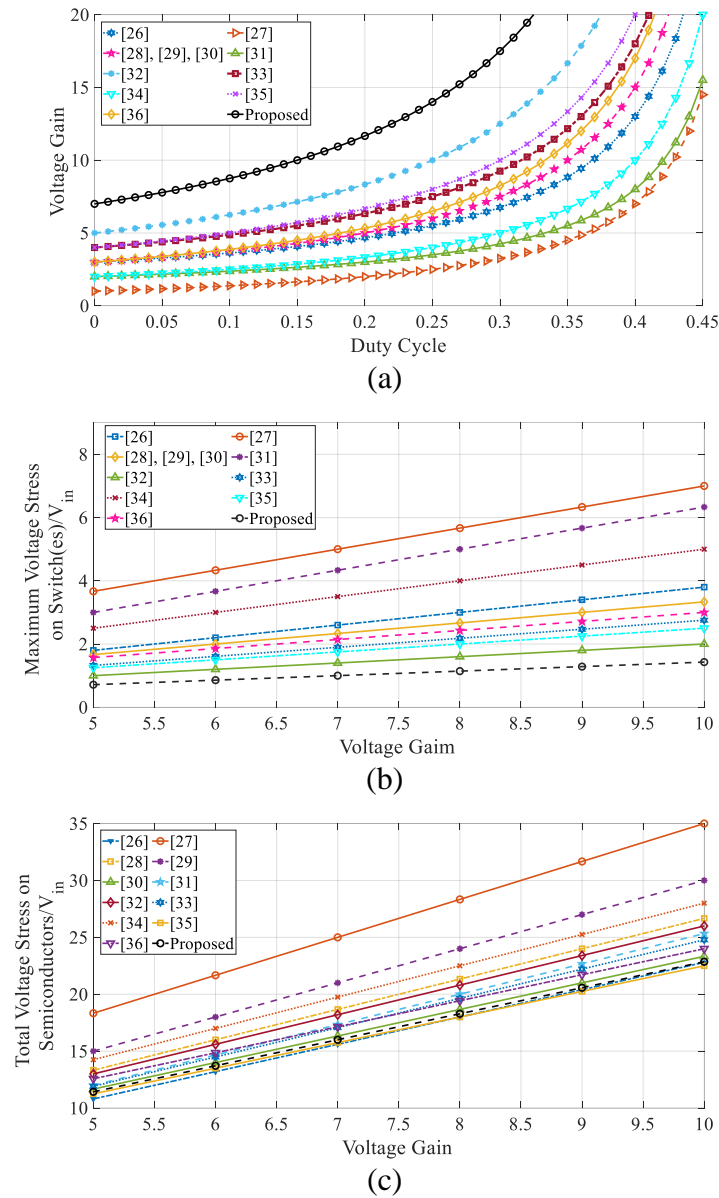


Figure 8. Comparison between the proposed converter and other similar converters for $N=1$: (a) voltage gain; (b) normalized maximum voltage stress on the switch(es); (c) normalized total voltage stress on the semiconductors.

in increasing the voltage gain significantly. For example, the converter in [33] with three magnetic windings has lower voltage gain than the converter in [32] with two magnetic windings; also, the converters in [26, 29, 35] have more than two magnetic windings, but lower voltage gains than the converter in [32]. However, the proposed converter with three

magnetic windings has the highest voltage gain among all the converters with any number of magnetic cores. Among all the converters, only the converters in [28, 31] use fewer number of the diodes and capacitors than the proposed converter; however, their voltage gains are limited and their voltage stresses across the switches are higher than the proposed converter. Moreover, like the converters in [26-29, 32], the proposed converter does not share a common ground between the input and output sides. As a result, the proposed converter can achieve a high voltage gain with a low duty cycle of less than 0.5, low voltage and current stresses on the switches, low total voltage stress on the semiconductors, and a continuous input current with only one magnetic core, thus causing a low-cost and high-efficiency system.

6. LOSS ANALYSIS

To analyze the analytical losses of the proposed converter, the parasitic elements of the components are considered, which are listed in Table 2.

The losses of switches S_1 and S_2 includes the conduction loss and switching loss, which are calculated from (19).

$$\begin{aligned}
 P_{S_1} &= P_{S_1,cond} + P_{S_1,sw} = R_{DS(on)} I_{S_1,rms}^2 + V_{S_1}^2 C_{oss} f_{sw} \\
 P_{S_2} &= P_{S_2,cond} + P_{S_2,sw} = R_{DS(on)} I_{S_2,rms}^2 + V_{S_2}^2 C_{oss} f_{sw} \\
 P_S &= P_{S_1} + P_{S_2}
 \end{aligned} \tag{19}$$

The 3WCI's loss is extracted by:

$$P_{3WCI} = R_p I_{L_{kp},rms}^2 + R_s I_{L_{ks},rms}^2 + R_l I_{L_{kl},rms}^2 + P_{core} \tag{20}$$

where P_{core} is the core loss of the 3WCI, which is extracted from the datasheet of the selected magnetic core.

The conduction losses of the diodes are extracted from:

$$\begin{aligned}
 P_{D_1,cond} &= V_{F_{D1}} I_{D_1,avg} + r_{D_1} I_{D_1,rms}^2 \\
 P_{D_2,cond} &= V_{F_{D2}} I_{D_2,avg} + r_{D_2} I_{D_2,rms}^2 \\
 P_{D_3,cond} &= V_{F_{D3}} I_{D_3,avg} + r_{D_3} I_{D_3,rms}^2 \\
 P_{D_4,cond} &= V_{F_{D4}} I_{D_4,avg} + r_{D_4} I_{D_4,rms}^2 \\
 P_{D_o,cond} &= V_{F_{D_o}} I_{D_o,avg} + r_{D_o} I_{D_o,rms}^2 \\
 P_D &= P_{D_1,cond} + P_{D_2,cond} + P_{D_3,cond} + P_{D_4,cond} + P_{D_o,cond}
 \end{aligned} \tag{21}$$

The reverse-recovery losses of the diodes are negligible and ignored in the loss calculation of the diodes.

The losses of the capacitors are given by:

$$\begin{aligned}
 P_{C_1} &= ESR_{C_1} I_{C_1,rms}^2 \\
 P_{C_2} &= ESR_{C_2} I_{C_2,rms}^2 \\
 P_{C_3} &= ESR_{C_3} I_{C_3,rms}^2 \\
 P_{C_o} &= ESR_{C_o} I_{C_o,rms}^2 \\
 P_C &= P_{C_1} + P_{C_2} + P_{C_3} + P_{C_o}
 \end{aligned} \tag{22}$$

The total loss of the proposed converter is given by:

$$P_{Loss} = P_S + P_D + P_C + P_{3WCI} \tag{23}$$

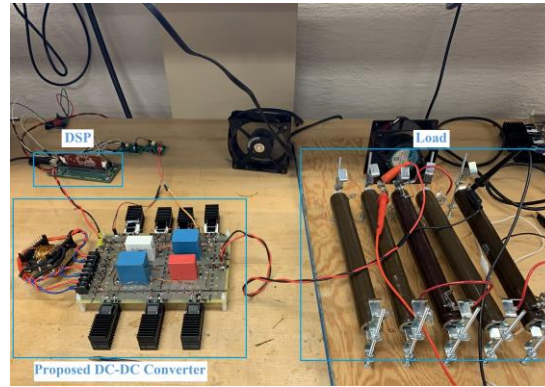
The analytical efficiency of the converter is calculated by:

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \tag{24}$$

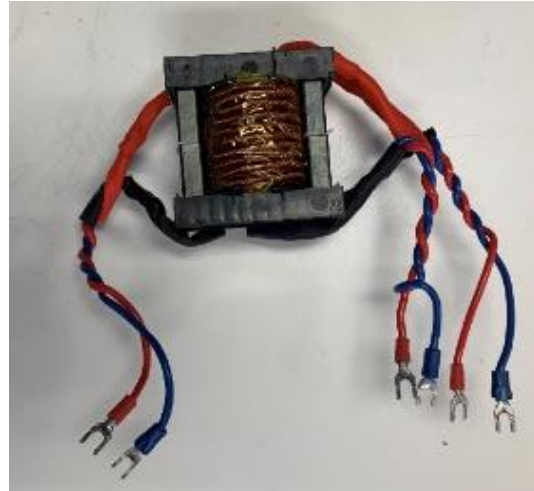
7. EXPERIMENTAL RESULTS

To verify the theoretical analysis and performance of the proposed high step-up converter, a 200 W prototype with the switching frequency of 50 kHz and an output voltage of 400 V was fabricated and tested. Figure 9 shows a photograph of the experimental setup and the designed 3WCI, and the specifications of the fabricated circuit are given in Table 2. The 3WCI was implemented using the ferrite core ETD54/28/19-3C90 with the turns-ratio of 1 (i.e., $N=1$).

Experimental waveforms are presented in Figure 10 for the input voltage of 20 V, duty cycle of 0.325, and output voltage of 400 V at the full load of 200 W. The capacitors' voltages are shown in Figure 10(a), which are consistent with the theoretical values calculated from (5) that: $V_{C1} \approx 57$ V, $V_{C2} \approx 97$ V, $V_{C3} \approx 74$ V, and $V_{Co} = V_o \approx 391$ V; the voltage gain is approximately 20, and that is consistent with (7). The voltages across the semiconductors are shown in Figures 10(b) and (c), and they agree with the theoretical values in (11) that are $V_{S1} = V_{S2} = V_{D1} = V_{D2} = 57.14$ V, $V_{D3} = V_{D4} = 171.42$ V, and $V_{Do} = 342.85$ V. As observed, the switches' voltages are clamped at a low voltage of 57.1 V, which is far less than the output voltage of 400 V; thus, the low-voltage-rated MOSFETs, with the part number of IRFP4568Pb and with a low $R_{DS(on)}$ of 4.8 m Ω were selected. It is worth noting that there are voltage spikes on the MOSFETS that are caused by the leakage inductances of the CI as well as the parasitic inductances of the electronic board's layout of the converter. As for the leakage inductances of the CI, diodes D_1 and D_2 along with capacitor C_1 provide a passive lossless clamp for both MOSFETs during their turn-off states to absorb the energy of the CI's leakage inductances. However, there may be still voltage



(a)



(b)

Figure 9. A photograph of the (a) whole experimental setup, (b) 3WCI.

Table 2. Specifications of the experimental setup.

Component/Parameter	Value/Part Number
Rated power	200 W
Capacitor C_1	UKL2A221KHD (220 μ F, ESR=13.3 m Ω) paralleled with C4ATFBW5100A3FJ (10 μ F, ESR=3.3 m Ω)
Capacitors C_2, C_3	B32678G4206K000 (20 μ F, ESR=3.3 m Ω)
Capacitor C_o	DCP4L052007GD4KSSD (20 μ F, ESR=6.2 m Ω)
Three-winding coupled inductor (3WCI)	Ferrite core ETD54/28/19-3C90 ($L_m=86 \mu$ H, $L_{kp}=L_{ks}=L_{kt}=1.5 \mu$ H, DCR: $R_p=R_s=R_t=10 \text{ m}\Omega$)
Switches S_1 and S_2	IRFP4568PbF ($R_{DS(on)}=4.8 \text{ m}\Omega$, $C_{oss}=977 \text{ pF}$)
Diodes D_1 and D_2	STPS30M120S ($V_f=0.45 \text{ V}$, $r_D=15 \text{ m}\Omega$)
Diodes D_3 and D_4	VS-15ETH03PbF ($V_f=0.8 \text{ V}$, $r_D=83 \text{ m}\Omega$)
Diode D_o	MUR1560G ($V_f=0.8 \text{ V}$, $r_D=80 \text{ m}\Omega$)

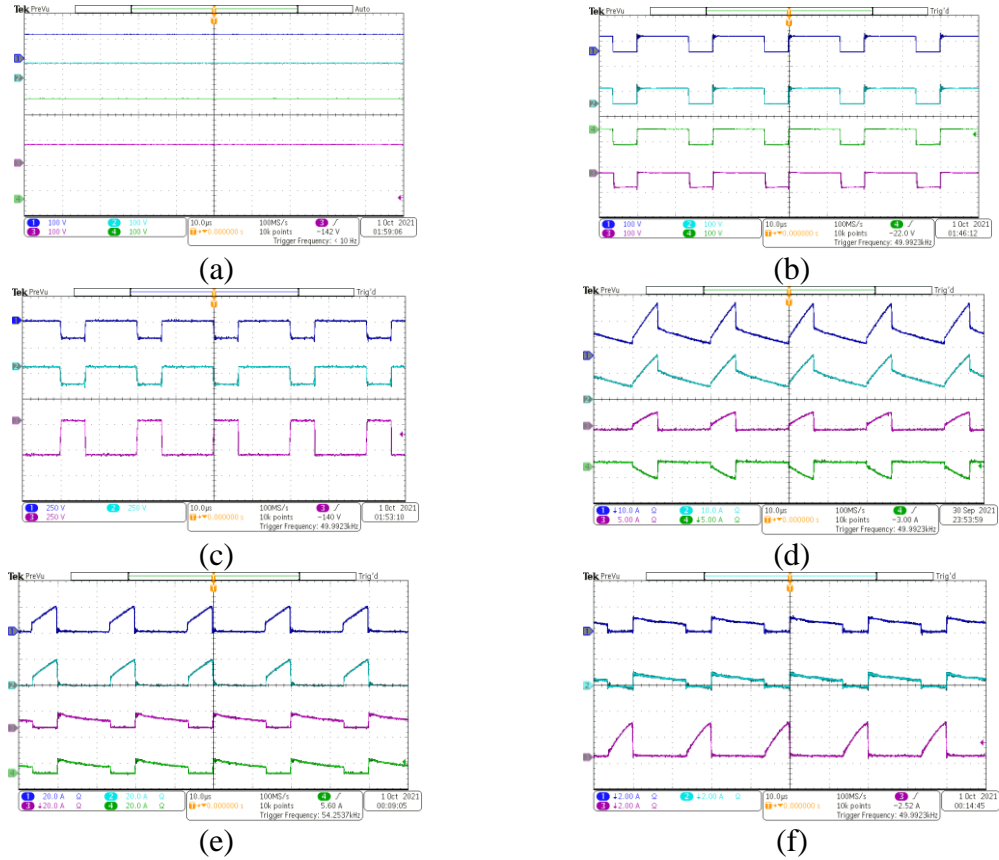


Figure 10. Experimental waveforms under full load for $V_{in}=20$ V and $D=0.325$: (a) voltages of capacitors C_1 (CH2), C_2 (CH1), C_3 (CH3), and C_o (CH4); (b) voltages of switches S_1 (CH1) and S_2 (CH2) and diodes D_1 (CH3) and D_2 (CH4); (c) voltages of diodes D_3 (CH1), D_4 (CH2), and D_o (CH3); (d) input current (CH1) and currents of leakage inductances L_{kp} (CH2), L_{ks} (CH3), and L_{kt} (CH4); (e) currents of switches S_1 (CH1) and S_2 (CH2) and diodes D_1 (CH3) and D_2 (CH4); (f) currents of diodes D_3 (CH1), D_4 (CH2), and D_o (CH3).

spikes on the MOSFETs due to parasitic inductances related the layout of the electronic board, which is reduced by utilizing a simple resistor-capacitor-diode (RCD) snubber in this paper. Moreover, since the voltage stress on the MOSFETs is about 57 V that is far less than the output voltage of 400 V, a low current flows through the RCD snubber. Accordingly, the elements of the RCD snubber have low ratings of the voltages and currents. Thus, the used snubber is very cheap with the low power loss and without a significant effect on the efficiency, size, and cost of the proposed DC-DC converter. The

input current and currents of the 3WCI's leakage inductances and semiconductors are shown in Figures 10(d)-(f); the RMS currents of the components are obtained as: $I_{S1, \text{rms}}=I_{S2, \text{rms}}=9.75 \text{ A}$, $I_{D1, \text{rms}}=I_{D2, \text{rms}}=7.5 \text{ A}$, $I_{D3, \text{rms}}=I_{D4, \text{rms}}=0.65 \text{ A}$, $I_{D_o, \text{rms}}=1 \text{ A}$, $I_{L_{kp}, \text{rms}}=9.7 \text{ A}$, $I_{L_{ks}, \text{rms}}=I_{L_{kt}, \text{rms}}=1.1 \text{ A}$, all of which are in good agreement with the theoretical calculations from (14) and the key waveforms in Figure (3), thus validating the performance and feasibility of the proposed converter and corresponding to the theoretical analyses. Clearly, the current-falling rates of diodes D_3 , D_4 , and D_o are controlled by the leakage inductances of the 3WCI, thereby leading to the significant reduction in the reverse-recovery losses of those diodes. As seen from Figure 10(d), the input current is continuous, which is helpful to increase the lifetime of the input renewable energy source. Note there is a little difference between practical and theoretical ideal current waveforms due to the parasitic elements of the circuit.

To verify the performance of the proposed converter under different input voltage and voltage gain conditions, the fabricated setup was tested at an input voltage of 34.5 V under the full load; keeping the constant output voltage at 400 V, the duty cycle was changed to approximately 0.2 to achieve the voltage gain of 11.6. The corresponding experimental waveforms are shown in Figure 11. It is experimentally observed that for the same output voltage, the voltage stresses of the switches and diodes remain constant when the input voltage and duty cycle vary. That is, the voltage stresses of the semiconductors are independent of the applied duty cycle. Figures 11(a)-(f) show that under new operating conditions, the proposed converter can ideally provide 400 V of fixed output voltage with a proper duty cycle and voltage gain.

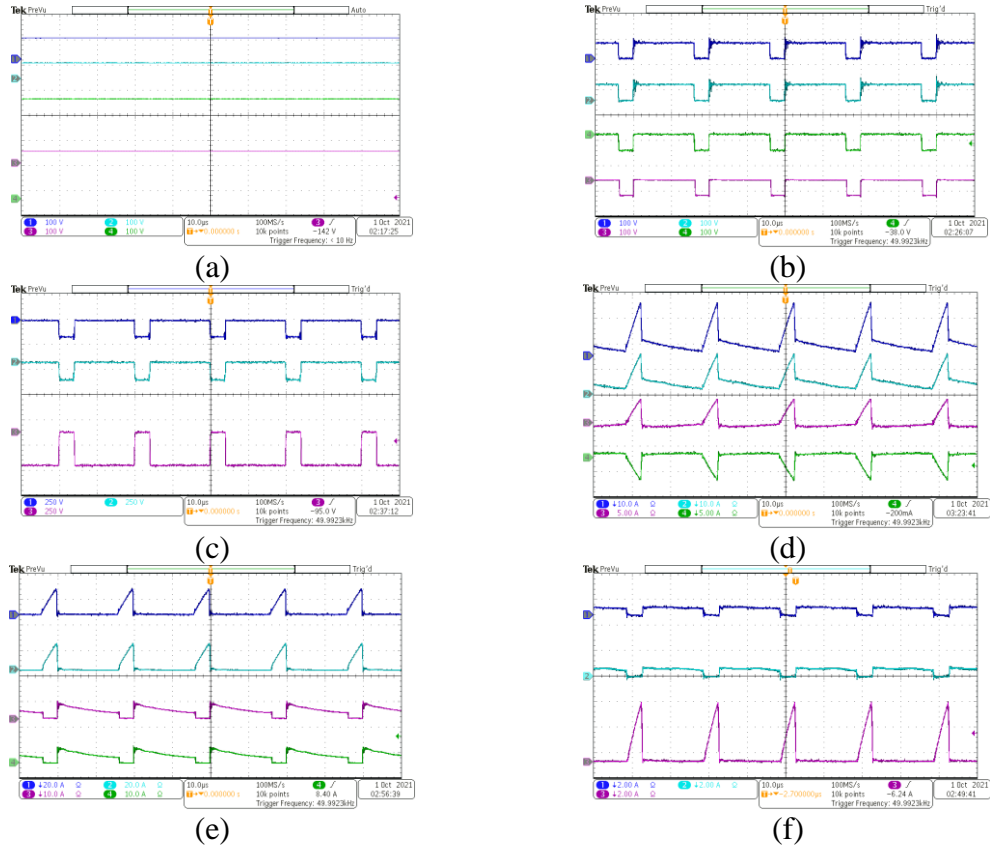


Figure 11. Experimental waveforms under full load for $V_{in}=34.5$ V and $D=0.2$: (a) voltages of capacitors C_1 (CH2), C_2 (CH1), C_3 (CH3), and C_o (CH4); (b) voltages of switches S_1 (CH1) and S_2 (CH2) and diodes D_1 (CH3) and D_2 (CH4); (c) voltages of diodes D_3 (CH1), D_4 (CH2), and D_o (CH3); (d) input current (CH1) and currents of leakage inductances L_{kp} (CH2), L_{ks} (CH3), and L_{kt} (CH4); (e) currents of switches S_1 (CH1) and S_2 (CH2) and diodes D_1 (CH3) and D_2 (CH4); (f) currents of diodes D_3 (CH1), D_4 (CH2), and D_o (CH3).

Since it is not possible to directly measure magnetizing current i_{Lm} with the current probe and oscilloscope, the data of all three leakage inductances' currents are imported into MATLAB to obtain i_{Lm} from $i_{Lm}=i_{Lkp}-Ni_{Lks}+Ni_{Lkt}$, showing in Figure 12 for two different test points. As seen, the magnetizing current ripple is in a good agreement with (15); for instance, according to Figure 12(a), under the full load for $V_{in}=20$ V, the duty cycle is 0.325 giving the current ripple of about 5.8 A with $L_m=86$ μ H.

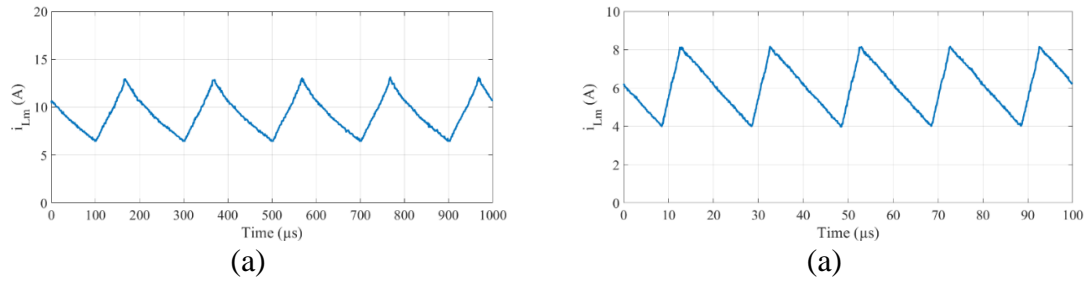


Figure 12. The experimental magnetizing current (i_{Lm}) under full load with $V_o=400$ V for (a) $V_{in}=20$ V, (b) $V_{in}=34.5$ V.

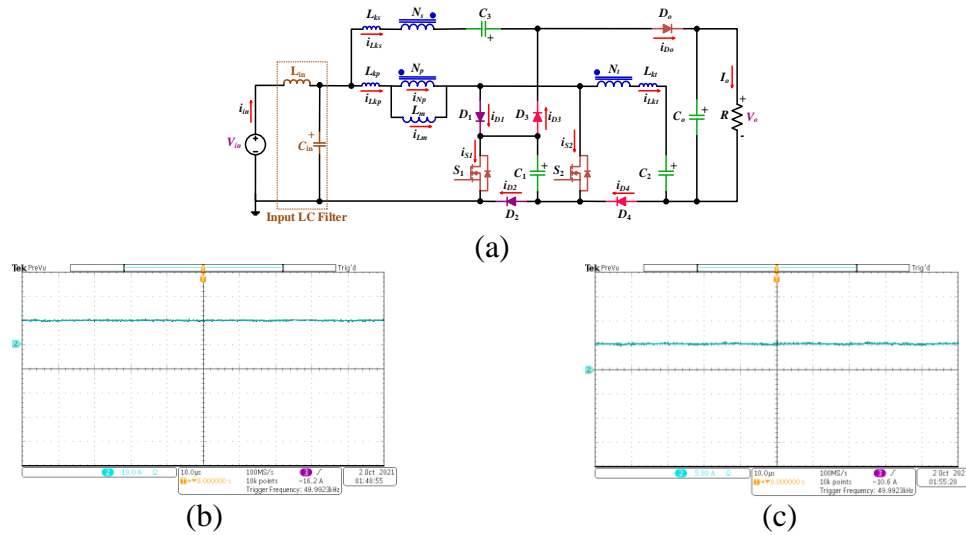


Figure 13. The effect of input filter on the input current: (a) proposed high step-up DC-DC converter with the input LC filter, (b) input current for $V_{in}=20$ V and $D=0.325$, (c) input current for $V_{in}=34.5$ V and $D=0.2$.

According to Figures 10(d) and 11(d), the proposed converter's input current ripple is as much as other high step-up DC-DC converters in [28, 32, 33] and less than the converters in [26, 29, 35]. However, using an input low-pass LC filter, the input current ripple is reduced. Figure 13(a) illustrates the proposed converter with an input LC filter, where $L_{in}=20$ μ H and $C_{in}=20$ μ F. Figures 13(b) and (c) depict the input current waveforms for two different operating conditions; as seen, thanks to the presence of the input filter, the input current is smooth that is preferable for the PV applications.

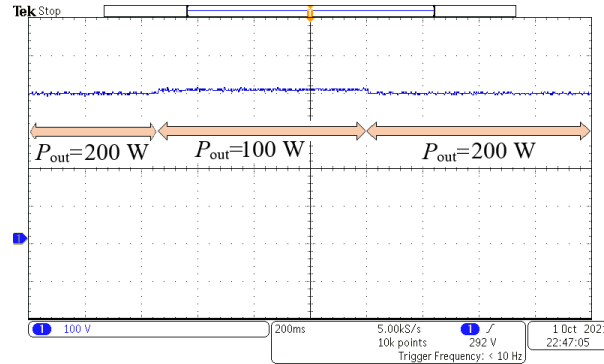


Figure 14. The dynamic response of the output voltage for a 50 % step change in the load for $V_{in}=34.5$ V.

Figure 14 presents the dynamic response of the output voltage for a 50 % step change in the load from 200 W to 100 W and vice versa for $V_{in}=34.5$ V; although the output voltage is not kept exactly constant at 400 V for different output load powers, the dynamic response illustrates the inherent stability of the proposed converter because the deviation from 400 V is small and less than 2.5 %.

Figure 15 shows the measured efficiency curve of the proposed converter from light load to full load for two different input voltages of 20 V and 34.5 V at the same output voltage of 400 V. Fluke 117 Multimeters were used to measure the input and output voltages and currents for calculating the efficiency. The full-load efficiency is 91.86 % and 95.21 % for the input voltage of 20 V with $G=20$ and 34.5 V with $G=11.6$, respectively. Meaning, the higher the input voltage, the higher the efficiency. Using (19)-(23), the analytical power loss distribution among the components of the proposed converter is obtained at full load of 200 W with output voltage of 400 V for two different input voltages of 20 V and 34.5 V, as illustrated in Figure 16. As seen, in the proposed converter, the largest losses occur in the diodes (36 %) and switches (51 %) for the input voltage of 20 V. Regarding the input voltage of 34.5 V, the loss in the 3WCI decreases by 0.5 %, and the

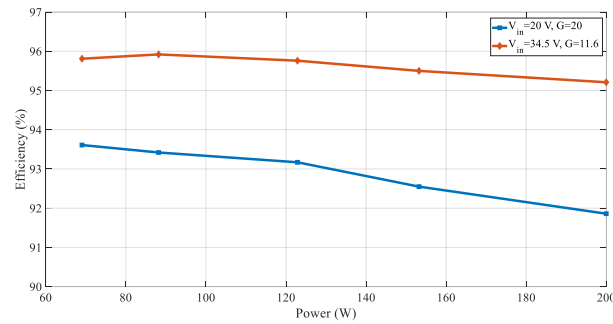


Figure 15. Measured efficiency versus the output power for the output voltage of 400 V under two different input voltages of 20 V and 34.5 V.

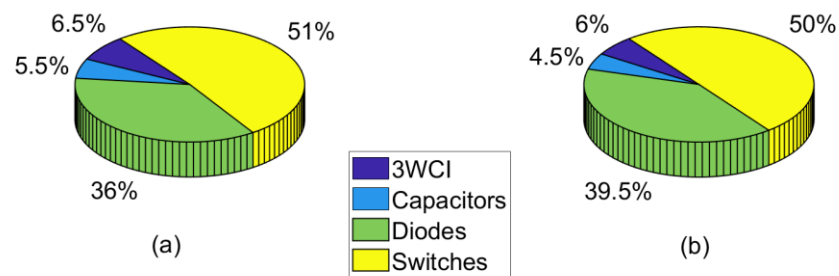


Figure 16. Power loss distribution of the proposed converter for the output voltage of 400 V at full load for (a) $V_{in}=20\text{ V}$ and (b) $V_{in}=34.5\text{ V}$.

capacitors loss reduces by 1 %, the diodes loss increases by 3.5 %, and the switches loss reduces by 1 %, when compared with the input voltage of 20 V.

As mentioned in Introduction, the proposed converter is an attempt to improve the converter in [32]. Considering the same components for both converters under the same input voltage of 20 V and voltage gain of 20, the analytical full-load efficiency is 92.07 % and 92.48 % for the converter in [32] and proposed converter, respectively. The proposed converter needs to operate at the duty cycle of 0.325, and the converter in [32] operates at the duty cycle of 0.375 to give the voltage gain of 20 with $N=1$ for the CI. Therefore, in the

proposed converter, the loss saved by the reduction of the duty cycle value is not counterbalanced by the additional winding ohmic loss of the 3WCI. The most important reason is that according to (19), the switching loss of a MOSFET is proportional to the squared voltage stress, and since the voltage stress of the switches is about 57 V and 80 V for the proposed converter and converter in [32], respectively, the proposed converter has lower MOSFETs' switching loss than the converter in [32]. In addition, it is possible to adopt lower-voltage-rated MOSFETs with lower ON-state resistance for our proposed converter compared to the converter in [32], which can contribute to the reduced conduction loss of the MOSFETs and improved efficiency for the proposed converter.

8. CONCLUSION

In this paper, a high step-up DC-DC converter was proposed for PV applications. Using a 3WCI in a dual-switch structure, a high-voltage gain was obtained without applying a high duty cycle to the switches. Other merits of the proposed converter are continuous input current, low current and voltage stresses on the semiconductors, simple topological structure, reduced number of magnetic cores, and increased design flexibility. Furthermore, the current-falling rates of most diodes are controlled by the leakage inductances of the 3WCI, leading to the significant reduction of their reverse-recovery losses. To investigate the proposed converter in detail, the operating modes, steady-state analyses, and design considerations were presented. Also, a comparison with other high step-up converters was conducted to verify the advantages of the proposed converter. The experimental results of a 200-W prototype with the output voltage of 400 V and two

different input voltages of 20 V and 34.5 V were presented to validate the theoretical analyses and calculations.

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III. Z-SOURCE-BASED HIGH STEP-UP DC-DC CONVERTERS FOR PHOTOVOLTAIC APPLICATIONS

Ramin Rahimi, *Student Member, IEEE*, Saeed Habibi, *Student Member, IEEE*, Mehdi Ferdowsi, *Member, IEEE*, and Pourya Shamsi, *Senior Member, IEEE*

ABSTRACT

This paper proposes three high step-up Z-source (ZS)-based DC-DC converters through integrating the conventional ZS network with switched-capacitor (SC) cells. The proposed converters offer a simple structure with a smooth input current, a high-voltage gain, and low voltage stress on the semiconductor devices. In addition, the proposed converters, unlike some existing ZS-based topologies in the literature, do not impose any limitation on the duty cycle of the power switch. These characteristics make the proposed converters excellent candidates to interface a low-voltage solar photovoltaic (PV) panel with a high-voltage DC bus in PV applications. Among the proposed three converters, the operating principles and steady-state analysis of the one with more components are presented in detail. However, the steady-state voltage and current relationships are also tabulated for two other proposed converters. In addition, design considerations are presented. The performance of the proposed converters is compared against similar existing high step-up DC-DC converters with regards to the component count, normalized voltage stress on the power switch and diodes, and voltage gain. Finally, the theoretical analyses and calculations are validated through experimental results using a 400 W/400 V laboratory prototype.

Keywords: DC-DC boost converter, high step-up DC-DC converter, solar photovoltaic (PV), Z-source (ZS) converter, impedance network, switched-capacitor cell, renewable energy.

1. INTRODUCTION

The deployment of photovoltaic panels has grown significantly over the past decade. The general schematic of a PV system is shown in Figure 1: the PV panels are connected to the DC bus through a high step-up DC-DC converter. One of the main drawbacks of the PV generation is the PV panels' low output voltage. Connecting the PV panels in series is the conventional solution to increase the voltage level of the PV generation. However, the output power of the PV panels drops greatly due to partial shading and module mismatches [1]. In such case, the parallel-connected configuration of the PV panels is more efficient than a series-connected configuration [2]. Nevertheless, PV output voltage is relatively low in the parallel-connected PV panels. Therefore, DC-DC converters with high-voltage gains are required to boost the PV voltage to high levels. A conventional DC-DC boost converter can provide a high-voltage gain; however, it needs to operate under an extremely high duty cycle close to unity. Operating under a high duty cycle, voltage and current stresses of the components will increase and the converter would suffer from high conduction losses because the power switch conducts for a long time close to the switching period. Moreover, the output diode will conduct for a very short period of time, which causes the diode to suffer from a severe reverse-recovery problem [3, 4]. Typically, isolated converters achieve high-voltage gains by adjusting the turns-ratio of

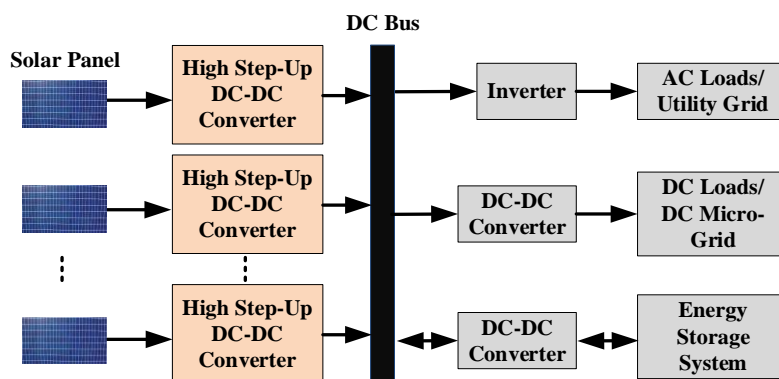


Figure 1. The general schematic of a PV system.

the transformer. However, they suffer from high cost as well as large voltage spikes on the switches due to the leakage inductance of the transformers, and the power dissipation will harm the overall efficiency [5]. By contrast, non-isolated high step-up DC-DC converters are becoming suitable solutions for improving system efficiency and reducing the system cost in PV applications due to omitting the galvanic isolation transformers. The key requirements of DC-DC converters in the PV applications are as follows: drawing a continuous input current with low ripple to provide an accurate maximum power point tracking (MPPT) function; achieving a high-voltage gain with low or medium duty cycle; having the low voltage stresses on the switches and a simple structure with a low number of components and high efficiency.

Many non-isolated DC-DC converters have been proposed for high step-up applications. These converters utilize voltage-boosting techniques including switched-capacitors (SC) cells [6-9], switched-inductor (SL)/voltage-lift (VL) cells [10-12], and coupled inductors [13]. Also, there are high step-up DC-DC converters derived from their isolated counterparts [14]. Recently, the Z-source (ZS) and quasi-Z-source (qZS) networks have been integrated with some voltage-boosting techniques to provide high step-up

converters. ZS and qZS configurations were originally proposed to overcome the problems of shoot-through and limited output voltage in traditional voltage-fed and current-fed inverters as well as to achieve a buck-boost voltage gain [15-17]. Consequently, the concept of boosting through ZS and qZS networks was extended to DC-DC converters. In [18], the operation states of the conventional ZS DC-DC converter were analyzed. In [19], the output diode was replaced with an inductor to further reduce the output voltage ripple. However, by replacing the output diode with an inductor, the voltage gain is lower compared to the conventional ZS converter in [18]. A modified ZS converter was proposed in [20], which can obtain lower voltage stresses on the switch and ZS network capacitors in comparison with the conventional ZS converter in [18]. However, the voltage gain was the same as that of the conventional ZS converter. In [21], the SL cells were integrated with the conventional ZS network, and consequently, a new SL ZS impedance network was proposed by adding six diodes and two inductors to the conventional ZS network. Although the voltage gain increased compared to the conventional ZS converter, the duty cycle was limited to 33.33 %, which is less than 50 % of the conventional ZS converter. In [22], a modified ZS converter was proposed in which the output diode and output capacitor were connected to a node before the ZS network instead of after the ZS network as is common for the conventional ZS converter. Compared with the conventional ZS converter, the converter in [22] obtained higher voltage gains and provided a common ground for the input and output sides. A family of qZS converters was presented in [23]. The qZS converter is a modified version of the ZS converter featuring improvements including low voltage stresses on capacitors and common input and output ground wire. However, the voltage gain for qZS converter is the same as the ZS converter. In [24], a family of ZS and

qZS converters was introduced, which incorporated bipolar output voltage and four-quadrant operation characteristics with a minimized number of switching devices, inductors, and capacitors; however, the voltage gain was not high enough. In [25], by integrating the SC technique with the qZS converter, a high-voltage gain sixth-order qZS converter is introduced which has higher voltage gain and reduced capacitor voltage stresses than conventional converters. This converter has a common ground between its input and output terminals; however, the voltage gain is not sufficiently high. Another qZS converter integrated with the SC technique was proposed in [26], which had high voltage gain. However, the voltage stresses on capacitors of the SC cells were high and the voltage gain was not high enough. In [27], the SC technique was integrated with the qZS network, which resulted in a new converter exhibiting a voltage gain higher than the conventional ZS and qZS converters while keeping the main advantages—low voltage stress on ZS network capacitors, common ground, and wider duty ratio range—of qZS converter intact. However, the voltage stress on the capacitors of the SC cells was high. A family of hybrid ZS converters was presented in [28]. However, the voltage stress on the semiconductor power switch was high, the number of elements was high, and the maximum duty cycle was limited to 25 % or 33.3 %. In [29], the VL technique was applied to the qZS converter for an increase in voltage gain. However, like [28], the voltage stresses across the devices were high and the duty cycle range was limited to 33.3 %. In [30], a hybrid SC-SL method was used to achieve a qZS high-voltage gain converter with a large number of the passive components. Integrating two SL cells to the qZS network, a high-voltage gain converter was proposed in [31]; however, the number of passive components and voltage stress

across the devices were high, and it suffered from a low duty cycle range limited to 23.6 %.

In this article, the SC technique is integrated into the conventional ZS network, and consequently, a new SC-based ZS (SCZS) network is proposed. The proposed SCZS network's structure can be symmetrical or asymmetrical, and the asymmetrical structure can have two different configurations. Additionally, the output diode and output capacitor are connected to the SCZS network in a different way in comparison with the conventional ZS converters. As a result, three new SCZS DC-DC converters are derived from the process. The proposed topologies are completely different from other existing ZS-based high step-up DC-DC converters. Compared to the conventional ZS converter, the proposed converters significantly increase the voltage gain and reduce the voltage stresses on the semiconductor devices. Also, voltage stresses on all capacitors of the ZS network and SC cells are equal and low. In addition, the proposed converters do not suffer from limitations on the duty cycle.

This paper is organized as follows: in Section 2, the topologies of the proposed high step-up DC-DC converters are presented, and then, the operating principles are analyzed in detail using steady-state analyses. The voltage and current stresses of the components are also tabulated in Section 2. The design considerations are presented in Section 3. In Section 4, a comparative analysis between the proposed converters and other ZS/qZS high step-up converters is given. In Section 5, the analytical loss analysis is provided. The experimental results are presented in Section 6 to validate the features of the proposed converters. The MATLAB-based simulation results of the MPPT performance are given in

Section 7 to verify the capability of the proposed converters to provide the MPPT function in the PV applications. Finally, the conclusion is presented in Section 8.

2. TOPOLOGIES AND OPERATING PRINCIPLES OF THE PROPOSED CONVERTERS

2.1. TOPOLOGIES OF THE PROPOSED CONVERTERS

The proposed high step-up DC-DC converters are comprised of an input inductor (L_{in}), an input capacitor (C_{in}), an input diode (D_{in}), an SCZS network, a power switch (Q), an output diode (D_o), and an output filter capacitor (C_o). The SCZS network can be either symmetrical SCZS (S-SCZS) or asymmetrical SCZS (AS-SCZS), and AS-SCZS network can have two variations: positive AS-SCZS (PAS-SCZS) network and negative AS-SCZS (NAS-SCZS) network. Thereby, three new SCZS DC-DC converters are derived, as shown in Figure 2. These topologies are named PAS-SCZS converter (PAS-SCZSC), NAS-SCZS converter (NAS-SCZSC), and S-SCZS converter (S-SCZSC), as presented in Figure 2(a), Figure 2(b), and Figure 2(c), respectively.

According to Figure 2, both the PAS-SCZS and NAS-SCZS networks contain two inductors (L_1, L_2), three capacitors (C_1, C_2, C_3), and one diode (D_1); the S-SCZS network contains two inductors (L_1, L_2), four capacitors (C_1, C_2, C_3, C_4), and two diodes (D_1, D_2). The PV panel is represented by a voltage source (V_{in}), and the load is represented by a resistor (R). The input inductor (L_{in}) and input capacitor (C_{in}) act as the input filter.

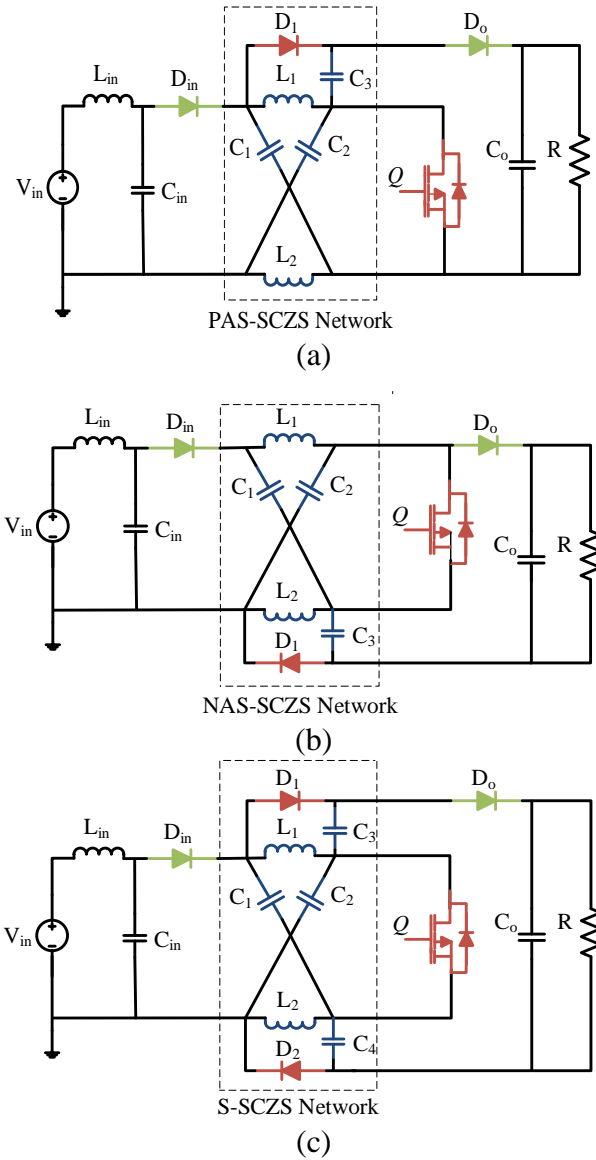


Figure 2. Topologies of the proposed ZS-based DC-DC converters: (a) PAS-SCZSC; (b) NAS-SCZSC; (c) S-SCZSC.

Table 1. Switching states of the proposed converters.

Semiconductor Device	Switching State I	Switching State II
Q	ON	OFF
D_{in}	OFF	ON
D_o	OFF	ON
D_1	ON	OFF
D_2 (only for S-SCZSC)	ON	OFF

2.2. OPERATING PRINCIPLES OF S-SCZSC

From the three proposed converters, only the S-SCZSC is analyzed here as it has more components than others. The analyses of the PAS-SCZSC and NAS-SCZSC can be easily made in a similar way. To analyze the proposed S-SCZSC, the following assumptions are made: it is operating at the steady-state condition; the capacitors are large enough such that their voltages are constant; all components are ideal, and their parasitic parameters are ignored; Switching transients are neglected. The input filter (consisting of L_{in} and C_{in}) is designed such that the voltage across the input capacitor is equal to the input voltage (i.e., $V_{C_{in}}=V_{in}$), and the average current of D_{in} equals the input current (I_{in}). If inductances L_1 and L_2 are greater than their critical values, there are two switching states in continuous conduction mode (CCM), as listed in Table 1: when switch Q is ON, S-SCZSC is in switching state I, and when switch Q is OFF, S-SCZSC is in switching state II. Both diodes D_1 and D_2 turn on simultaneously with switch Q , and they also turn off synchronically with switch Q . The key waveforms of the S-SCZSC are shown in Figure 3. Note that parameter D is the duty cycle of the power switch—which typically ranges from 0 to 50 % for ZS-based converters—and T is the switching period, which is the reciprocal of the switching frequency (f_{sw}). Also, the parameters with the subscripts of "on" and "off" represent the values when switch Q is ON and OFF, respectively.

Switching State I ($0 \leq t \leq DT$): Figure 4(a) shows the equivalent circuit of switching state I starting when switch Q turns on. In this state, switch Q and diodes D_1 and D_2 are in ON state, and diodes D_{in} and D_o are in OFF state. According to the current flow paths shown for this switching state in Figure 4(a), the inductors are charged, capacitors C_1 , C_2 , and C_o are discharged, and capacitors C_3 and C_4 are charged. By applying Kirchoff's

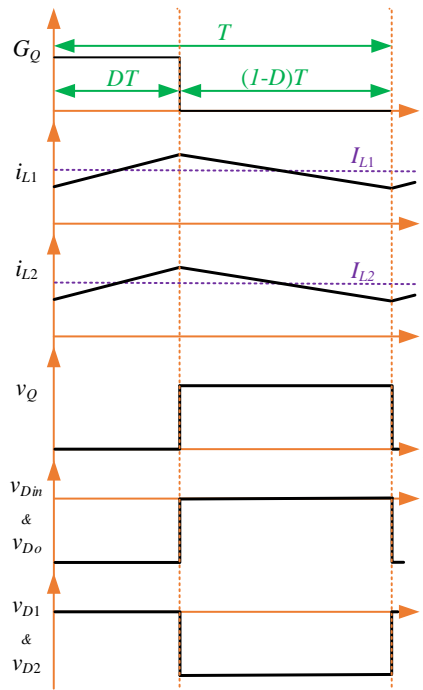


Figure 3. The key waveforms of proposed S-SCZSC.

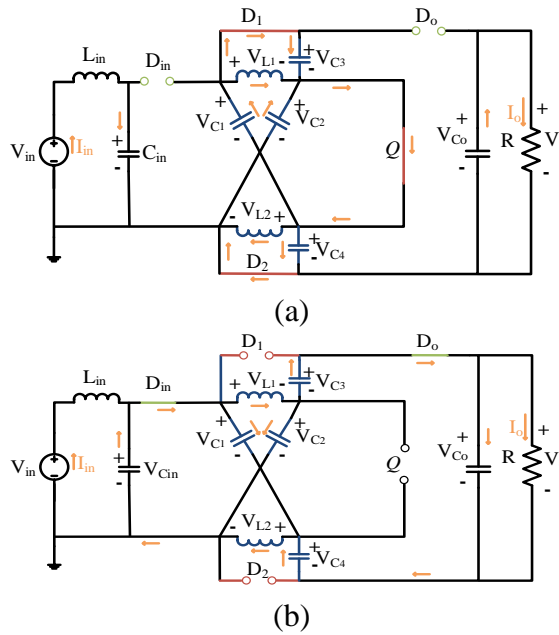


Figure 4. The equivalent circuit of the proposed S-SCZSC for (a) switching state I and (b) switching state II.

Voltage Law (KVL), the following voltage relationships are obtained for this switching state:

$$V_{L_1} = V_{L_{1on}} = V_{C_1} = V_{C_3} \quad (1)$$

$$V_{L_2} = V_{L_{2on}} = V_{C_2} = V_{C_4} \quad (2)$$

Switching State II ($DT \leq t \leq T$): Figure 4(b) represents the equivalent circuit of switching state II, which starts when switch Q turns off. In this operating state, switch Q and diodes D_1 and D_2 are in OFF state, and diodes D_{in} and D_o are in ON state. According to the current flow paths shown for this state in Figure 4(b), the inductors are discharged, capacitors C_1 , C_2 , and C_o are charged, and capacitors C_3 and C_4 are discharged. By applying KVL, the following voltage relationships are obtained for switching state II:

$$V_{L_1} = V_{L_{1off}} = V_{in} - V_{C_2} \quad (3)$$

$$V_{L_2} = V_{L_{2off}} = V_{in} - V_{C_1} \quad (4)$$

$$V_o = V_{C_1} + V_{C_2} + V_{C_3} + V_{C_4} - V_{in} \quad (5)$$

2.3. VOLTAGE STRESSES ACROSS CAPACITORS AND VOLTAGE GAIN OF S-SCZSC

Considering (1)-(4) and by applying the voltage–second balance principle to inductors L_1 and L_2 in CCM, the following equations are obtained:

$$V_{C_1} \times DT + (V_{in} - V_{C_2}) \times (1 - D)T = 0 \quad (6)$$

$$V_{C_2} \times DT + (V_{in} - V_{C_1}) \times (1 - D)T = 0 \quad (7)$$

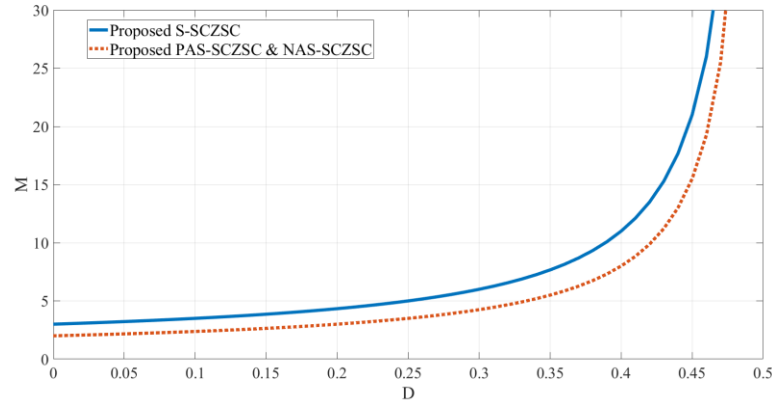


Figure 5. The voltage gain curves for the proposed high step-up converters.

From (1)-(7), the voltage stresses across the capacitors and voltage gain M of the proposed S-SCZS converter can be expressed as (8)-(10), where $0 < D < 0.5$.

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{C_4} = \frac{1-D}{1-2D} V_{in} = \frac{1-D}{3-2D} V_o \quad (8)$$

$$V_{C_o} = V_o = \frac{3-2D}{1-2D} V_{in} \quad (9)$$

$$M = \frac{V_o}{V_{in}} = \frac{3-2D}{1-2D} \quad (10)$$

From the analysis above, the voltage stresses across S-SCZS network's capacitors C_1 , C_2 , C_3 , and C_4 are the same and between $V_o/4$ and $V_o/3$. It is obvious that the voltage stress across output capacitor C_o is equal to the output voltage. By performing similar analyses, the voltage gain of the other two proposed topologies (i.e., PAS-SCZSC and NAS-SCZSC) can be obtained as $M = \frac{2-D}{1-2D}$. Figure 5 shows the voltage gain curves of the proposed PAS-SCZSC, NAS-SCZSC, and S-SCZSC. These curves show the capability of the proposed converters to achieve high voltage-gain gains. For example, when $D=0.4$, the voltage gain is 11 for S-SCZSC.

2.4. VOLTAGES STRESSES ACROSS THE POWER SEMICONDUCTOR DEVICES FOR S-SCZSC

Examining Figures 4(a) and (b), the reverse voltage stresses across diodes D_{in} , D_1 , D_2 , D_o , and the voltage stress across power switch Q can be deduced as (11)-(15).

$$V_{D_{in}} = V_{C_1} + V_{C_2} - V_{in} = \frac{1}{1-2D} V_{in} = \frac{1}{3-2D} V_o \quad (11)$$

$$V_{D_1} = V_{C_2} + V_{C_3} - V_{in} = \frac{1}{1-2D} V_{in} = \frac{1}{3-2D} V_o \quad (12)$$

$$V_{D_2} = V_{C_1} + V_{C_4} - V_{in} = \frac{1}{1-2D} V_{in} = \frac{1}{3-2D} V_o \quad (13)$$

$$V_{D_o} = V_o - V_{C_3} - V_{C_4} = \frac{1}{1-2D} V_{in} = \frac{1}{3-2D} V_o \quad (14)$$

$$V_Q = V_o - V_{C_3} - V_{C_4} = \frac{1}{1-2D} V_{in} = \frac{1}{3-2D} V_o \quad (15)$$

The voltage stresses across all the semiconductor devices are less than half of the output voltage ($<V_o/2$). This feature results in reducing the losses of the S-SCZSC.

2.5. CURRENT STRESSES OF THE COMPONENTS FOR S-SCZSC

In this section, as a contract, except for the input current, the positive current is defined as flowing into the positive voltage terminal of the components. The average load current is I_o , the average input current is I_{in} , and the average currents of inductors L_1 and L_2 are I_{L1} and I_{L2} , respectively. The average currents through capacitors C_1 , C_2 , C_3 , C_4 , and C_o are I_{C1on} , I_{C2on} , I_{C3on} , I_{C4on} , and I_{Coon} , when power switch Q is turned on, and I_{C1off} , I_{C2off} , I_{C3off} , I_{C4off} , and I_{Coff} , respectively, when the power switch Q is turned off. By applying Kirchhoff's Current Law (KCL) on the equivalent circuits of S-SCZSC in Figure 4, the following current relationships can be obtained:

$$I_{C_1on} = -(I_{L_1} + I_{C_3on}) \quad (16)$$

$$I_{C_2on} = -(I_{L_2} + I_{C_4on}) \quad (17)$$

$$I_{C_oon} = -I_o \quad (18)$$

$$I_{C_1off} = I_{L_2} + I_{C_4off} \quad (19)$$

$$I_{C_2off} = I_{L_1} + I_{C_3off} \quad (20)$$

$$I_{C_ooff} = -(I_o + I_{C_3off}) \quad (21)$$

$$I_{C_3off} = I_{C_4off} \quad (22)$$

By applying the ampere-second balance principle to capacitors C_1 , C_2 , C_3 , C_4 , and C_o in CCM, the following equations are obtained:

$$\begin{cases} I_{C_1on} \times DT + I_{C_1off} \times (1-D)T = 0 \\ -(I_{L_1} + I_{C_3on}) \times DT + (I_{L_2} + I_{C_4off}) \times (1-D)T = 0 \end{cases} \quad (23)$$

$$\begin{cases} I_{C_2on} \times DT + I_{C_2off} \times (1-D)T = 0 \\ -(I_{L_2} + I_{C_4on}) \times DT + (I_{L_1} + I_{C_3off}) \times (1-D)T = 0 \end{cases} \quad (24)$$

$$I_{C_3on} \times DT + I_{C_3off} \times (1-D)T = 0 \quad (25)$$

$$I_{C_4on} \times DT + I_{C_4off} \times (1-D)T = 0 \quad (26)$$

$$\begin{cases} I_{C_oon} \times DT + I_{C_ooff} \times (1-D)T = 0 \\ -I_o \times DT - (I_o + I_{C_3off}) \times (1-D)T = 0 \end{cases} \quad (27)$$

From (16)-(27), the following relationships are obtained:

$$I_{C_1on} = I_{C_2on} = -\frac{1}{D(1-2D)} I_o \quad (28)$$

$$I_{C_1off} = I_{C_2off} = \frac{1}{(1-D)(1-2D)} I_o \quad (29)$$

$$I_{C_3on} = I_{C_4on} = \frac{1}{D} I_o \quad (30)$$

$$I_{C_3off} = I_{C_4off} = -\frac{1}{1-D} I_o \quad (31)$$

$$I_{C_ooff} = \frac{D}{1-D} I_o \quad (32)$$

$$I_{L_1} = I_{L_2} = \frac{2}{1-2D} I_o \quad (33)$$

Given that the converter is assumed to be ideal without any power losses, the following equation can be written:

$$V_{in} \times I_{in} = V_o \times I_o \rightarrow I_{in} = M \times I_o = \frac{3-2D}{1-2D} I_o \quad (34)$$

Using Figure 4 and (28)-(34), the current stresses (equivalent average currents during the conduction states, not entire switching period) across diodes D_{in} , D_1 , D_2 , D_o and the switch Q can be derived as:

$$I_{D_{in}} = \frac{I_{in}}{1-D} = \frac{3-2D}{(1-D)(1-2D)} I_o \quad (35)$$

$$I_{D_1} = I_{C_3on} = \frac{1}{D} I_o \quad (36)$$

$$I_{D_2} = I_{C_4on} = \frac{1}{D} I_o \quad (37)$$

$$I_{D_o} = -I_{C_3off} = \frac{1}{1-D} I_o \quad (38)$$

$$I_Q = I_{L_1} + I_{C_3on} - I_{C_2on} = \frac{2}{D(1-2D)} I_o \quad (39)$$

Table 2. Voltage stress of the components for the proposed converters.

Component		Parameter	Proposed topology	
			PAS-SCZSC and NAS-SCZSC	S-SCZSC
Inductors	L ₁	$V_{L_{on}}$	$\frac{1-D}{2-D}V_o$	$\frac{1-D}{3-2D}V_o$
		$V_{L_{off}}$	$-\frac{D}{2-D}V_o$	$-\frac{D}{3-2D}V_o$
	L ₂	$V_{L_{on}}$	$\frac{1-D}{2-D}V_o$	$\frac{1-D}{3-2D}V_o$
		$V_{L_{off}}$	$-\frac{D}{2-D}V_o$	$-\frac{D}{3-2D}V_o$
Capacitors	C ₁	V_{C_1}	$\frac{1-D}{2-D}V_o$	$\frac{1-D}{3-2D}V_o$
	C ₂	V_{C_2}		
	C ₃	V_{C_3}		
	C ₄	V_{C_4}		
	C _o	V_{C_o}	V_o	V_o
Diodes	D _{in}	$V_{D_{in}}$	$\frac{1}{2-D}V_o$	$\frac{1}{3-2D}V_o$
	D _o	V_{D_o}		
	D ₁	V_{D_1}		
	D ₂	V_{D_2}		
Power switch	Q	V_Q	$\frac{1}{2-D}V_o$	$\frac{1}{3-2D}V_o$
Voltage gain			$\frac{2-D}{1-2D}$	$\frac{3-2D}{1-2D}$

A similar analysis of deriving the circuit relationships for both PAS-SCZSC and NAS-SCZSC can be made. The key circuit relationships of PAS-SCZSC and NAS-SCZSC, along with the ones for S-SCZSC, are included in Tables 2 and 3.

3. DESIGN CONSIDERATIONS FOR S-SCZSC

3.1. SEMICONDUCTOR DEVICES SELECTION

To operate within the safety operation area (SOA), the voltage and current ratings of the semiconductor devices should be higher than the calculated voltage stresses from (11)-(15) and current stresses from (35)-(39), respectively.

Table 3. Current stress of the components for the proposed converters.

Component		Parameter	Proposed topology		
			PAS-SCZSC	NAS-SCZSC	S-SCZSC
Inductors	L ₁	I_{L_1}	$\frac{1+D}{1-2D} I_o$	$\frac{2-D}{1-2D} I_o$	$\frac{2}{1-2D} I_o$
	L ₂	I_{L_2}	$\frac{2-D}{1-2D} I_o$	$\frac{1+D}{1-2D} I_o$	$\frac{2}{1-2D} I_o$
Capacitors	C ₁	$I_{C_{gen}}$	$-\frac{1-D+D^2}{D(1-2D)} I_o$	$-\frac{2-D}{1-2D} I_o$	$-\frac{1}{D(1-2D)} I_o$
		$I_{C_{eff}}$	$\frac{1-D+D^2}{(1-D)(1-2D)} I_o$	$\frac{D(2-D)}{(1-D)(1-2D)} I_o$	$\frac{1}{(1-D)(1-2D)} I_o$
	C ₂	$I_{C_{gen}}$	$-\frac{2-D}{1-2D} I_o$	$-\frac{1-D+D^2}{D(1-2D)} I_o$	$-\frac{1}{D(1-2D)} I_o$
		$I_{C_{eff}}$	$\frac{D(2-D)}{(1-D)(1-2D)} I_o$	$\frac{1-D+D^2}{(1-D)(1-2D)} I_o$	$\frac{1}{(1-D)(1-2D)} I_o$
	C ₃	$I_{C_{gen}}$	$\frac{1}{D} I_o$		$\frac{1}{D} I_o$
		$I_{C_{eff}}$	$-\frac{1}{1-D} I_o$		$-\frac{1}{1-D} I_o$
	C ₄	$I_{C_{gen}}$			$\frac{1}{D} I_o$
		$I_{C_{eff}}$			$-\frac{1}{1-D} I_o$
	C _o	$I_{C_{gen}}$	$-I_o$		$-I_o$
		$I_{C_{eff}}$	$\frac{D}{1-D} I_o$		$\frac{D}{1-D} I_o$
Diodes	D _{in}	$I_{D_{in}}$	$\frac{2-D}{(1-D)(1-2D)} I_o$	$\frac{3-2D}{(1-D)(1-2D)} I_o$	
	D _o	I_{D_o}	$\frac{1}{1-D} I_o$	$\frac{1}{1-D} I_o$	
	D ₁	I_{D_1}	$\frac{1}{D} I_o$	$\frac{1}{D} I_o$	
	D ₂	I_{D_2}			
Power switch	Q	I_{D_o}	$\frac{1+D}{D(1-2D)} I_o$	$\frac{2}{D(1-2D)} I_o$	

3.2. INDUCTORS DESIGN

The rated currents of inductors L_1 and L_2 can be determined from (33). These inductances are selected such that the proposed S-SCZSC operates in CCM. Due to having many capacitors, the high step-up DC-DC converters have inherently slow dynamic response to the solar irradiance and load changes. Thus, it is advisable to design the inductances based on the current ripple rather than dynamic response because a large inductance does not make the dynamic response significantly slow. Considering switching

state I shown in Figure 4(a), if both inductors are selected to have equal size ($L_1=L_2=L$), the ripple current expression for inductors L_1 and L_2 is obtained as:

$$\Delta i_{L_1} = \Delta i_{L_2} = \Delta i_L = \frac{D(1-D)}{(3-2D)f_{sw}L}V_o \quad (40)$$

To operate in CCM, the values of S-SCZSC inductances must be greater than the critical inductance of the circuit that is:

$$L_{crit} = \frac{D(1-D)(1-2D)R}{2f_{sw}} \quad (41)$$

Relationship (42) can be used if a certain ripple for the inductors' currents is desired.

$$L = \frac{V_{L_{on}}\Delta t}{\Delta i_L} = \frac{D(1-D)V_{in}}{(1-2D)f_{sw}\Delta i_L} = \frac{D(1-D)V_o}{(3-2D)f_{sw}\Delta i_L} \quad (42)$$

By having the maximum current ripple for the inductors, which is usually 20 % ($\Delta i_{L_{max}}=0.2I_L$), the required inductances L_1 and L_2 can be determined from (43), which is higher than the critical inductance calculated from (41).

$$L \geq \frac{D(1-D)V_o}{(3-2D)f_{sw}\Delta i_{L_{max}}} \quad (43)$$

If the values of inductances L_1 and L_2 become different, the only practical effect will be on their current ripples without violating KCL in any nodes of the circuit; in fact, the inductance with lower value will have a higher current ripple.

Although the proposed S-SCZSC can operate in discontinuous conduction mode (DCM) for small values of inductances L_1 and L_2 , it is recommended not to use S-SCZSC in DCM; the reason is that in DCM, the voltage gain depends on the load and design parameters such as the inductances and switching frequency. Also, the components' ripple

currents are higher compared to the CCM, which leads to lower efficiency in comparison with CCM.

3.3. CAPACITORS DESIGN

The rated voltages of the capacitors can be determined from (8) and (9). By knowing the maximum ripple voltages of the capacitors, the capacitances are determined to be as (44)-(48).

$$C_1 \geq \frac{D|I_{C_{1on}}|}{f_{sw}\Delta V_{C_1\max}} \rightarrow C_1 \geq \frac{I_o}{(1-2D)f_{sw}\Delta V_{C_1\max}} \quad (44)$$

$$C_2 \geq \frac{D|I_{C_{2on}}|}{f_{sw}\Delta V_{C_2\max}} \rightarrow C_2 \geq \frac{I_o}{(1-2D)f_{sw}\Delta V_{C_2\max}} \quad (45)$$

$$C_3 \geq \frac{DI_{C_{3on}}}{f_{sw}\Delta V_{C_3\max}} \rightarrow C_3 \geq \frac{I_o}{f_{sw}\Delta V_{C_3\max}} \quad (46)$$

$$C_4 \geq \frac{DI_{C_{4on}}}{f_{sw}\Delta V_{C_4\max}} \rightarrow C_4 \geq \frac{I_o}{f_{sw}\Delta V_{C_4\max}} \quad (47)$$

$$C_o \geq \frac{D|I_{C_{on}}|}{f_{sw}\Delta V_{C_o\max}} \rightarrow C_o \geq \frac{DI_o}{f_{sw}\Delta V_{C_o\max}} \quad (48)$$

As for input capacitor C_{in} , it is selected such that the input filter's cut-off frequency is much lower than the switching frequency. In this paper, C_{in} and L_{in} are selected as 20 μF and 20 μH , respectively, resulting in the cut-off frequency of 8 kHz, which is much lower than the switching frequency of 100 kHz.

4. COMPARATIVE STUDY

In this section, the proposed converters are compared against other ZS-/qZS-based high step-up DC-DC converters. Table 4 summarizes the number of passive and active components, voltage gain, maximum duty cycle, and normalized voltage stresses across the semiconductor devices, including power switches and diodes. All the selected converters have only one power switch. The comparison between the proposed converters with other topologies based on the voltage gain versus duty cycle is shown in Figure 6. As obvious, the high step-up converters in [21], [28], [29], and [31] have higher voltage gains compared to the basic ZS and qZS converters presented in [18], [19], [20], and [23], but they suffer from the limited duty cycle ranges. That is, for converters in [21], [28], [29], and [31], the maximum duty cycle is limited to values such as 33.3 %, 25 %, or 23.6 %, which are less than the maximum permissible duty cycle of 50 % for ZS-/qZS-based converters. However, the proposed converters—including PAS-SCZSC, NAS-SCZSC, and S-SCZSC—do not impose any limitation on the duty cycle ranges as their maximum duty cycle is 50 %. From the voltage gain point of view, it is fair to compare the proposed converters with existing topologies that can operate with wide ranges of duty cycles up to 50 %. As can be seen in Figure 6, among the converters with maximum duty cycle of 50 %, only the converter in [30] has a slightly higher voltage gain than proposed S-SCZSC but only for the duty cycle ranging from 33.3 % to 50 %, and the voltage gain of the converter in [27] is equal to that of the proposed S-SCZSC; however, converter in [27] does not draw a smooth DC current from input source that is critical in the PV applications for increasing the lifetime of PV panels and accurate implementation of the MPPT

Table 4. Comparison of proposed converters with other existing ZS/qZS step-up DC-DC converters.

Converter	Voltage gain	No. of inductors	No. of capacitors	No. of diodes	No. of switches	Maximum normalized voltage stress on diodes	Normalized voltage stress on power switch	Maximum duty cycle
Z-source converter in [18]	$\frac{1}{1-2D}$	2	3	2	1	1	1	50 %
Z-source converter in [19]	$\frac{1-D}{1-2D}$	3	3	1	1	$\frac{1}{1-D}$	$(1+D)$	50 %
Z-source converter in [20]	$\frac{1}{1-2D}$	2	3	2	1	1	1	50 %
Converter in [21]	$\frac{1+D}{1-3D}$	4	3	8	1	1	1	33.3 %
Converter in [22]	$\frac{2-2D}{1-2D}$	2	3	2	1	D	D	50 %
Quasi-Z-source converter in [23]	$\frac{1}{1-2D}$	2	3	2	1	1	1	50 %
Converter in [25]	$\frac{2-2D}{1-2D}$	2	4	3	1	$\frac{1}{2-2D}$	$\frac{1}{2-2D}$	50 %
Converter in [26]	$\frac{2}{1-2D}$	2	5	4	1	0.5	0.5	50 %
Converter in [27]	$\frac{3-2D}{1-2D}$	2	6	5	1	$\frac{1}{3-2D}$	$\frac{1}{3-2D}$	50 %
Hybrid two-quasi Z-source converter in [28]	$\frac{1}{1-3D}$	3	5	3	1	1	1	33.3 %
Hybrid three quasi-Z-source converter in [28]	$\frac{1}{1-4D}$	4	7	4	1	1	1	25 %
Hybrid Z-source/quasi-Z source converter in [28]	$\frac{1}{1-4D}$	4	7	4	1	1	1	25 %
Converter in [29]	$\frac{2-2D}{1-3D}$	4	4	3	1	$\frac{1}{1-D}$	1	33.3 %
Converter in [30]	$\frac{2+D}{1-2D}$	3	7	5	1	$\frac{1}{2+D}$	$\frac{1}{2+D}$	50 %
Converter in [31]	$\frac{2+2D}{1-4D-D^2}$	4	4	7	1	1	1	23.6 %
Proposed PAS-SCZSC and NAS-SCZSC	$\frac{2-D}{1-2D}$	3	5	3	1	$\frac{1}{2-D}$	$\frac{1}{2-D}$	50 %
Proposed S-SCZSC	$\frac{3-2D}{1-2D}$	3	6	4	1	$\frac{1}{3-2D}$	$\frac{1}{3-2D}$	50 %

algorithm, and the converter in [30] has more components than the proposed S-SCZSC.

Therefore, without having many components, the S-SCZSC has the highest voltage gain without suffering from the duty cycle limitation. According to Table 4, the normalized

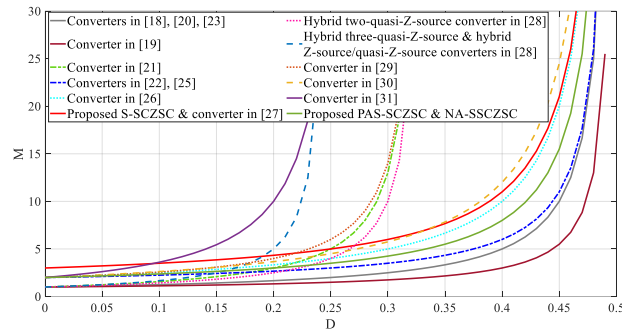


Figure 6. Comparison of the voltage gain versus the duty cycle.

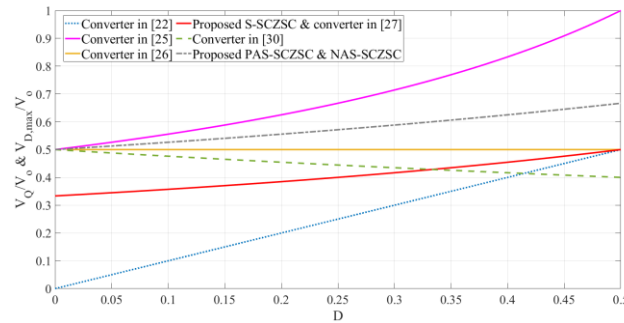


Figure 7. Comparison of the normalized voltage stress of the power switch and maximum normalized voltage stress of diodes versus the duty cycle.

voltage stress of power switch (i.e., V_Q/V_o) is 1 for the converters in [18], [20], [21], [23], [28], [29], and [31]; that is, the voltage stress on the power switch equals the output voltage. The normalized voltage stress of the converter in [19] is greater than 1, which means the voltage stress of the switch is higher than the output voltage. The maximum normalized voltage stress on diodes (i.e., $V_{D,max}/V_o$) is greater than 1 for the converters in [19] and [29] and equal to 1 for topologies in [18], [20], [21], [23], [28], and [31]. For the proposed converters and others in [22], [25], [26], [27], and [30], the normalized voltage stress of the switch and maximum normalized voltage stress of the diodes are equal to each other (i.e., $V_Q/V_o = V_{D,max}/V_o$), which is illustrated in Figure 7. As observed, the normalized

voltage stresses of the switch and diodes are less than 0.67 for proposed PAS-SCZSC and NAS-SCZSC and less than 0.5 for proposed S-SCZSC, considering the entire operating duty cycle range. Thereby, lower voltage stresses on the switch and diodes are realized for the proposed converters. As a result, among all converters, S-SCZSC is the best candidate for high step-up PV applications due to the following reasons: it offers lower voltage stresses on the power switch and diodes, which is less than the half the output voltage; it draws a smooth DC current from the input source; it has a higher voltage gain; it does not impose a limitation on the duty cycle range; and it does not need many components. Furthermore, like the hybrid ZS/qZS converter in [28] and those in [18], [19], [21], and [30], the proposed converters do not share the common ground between the input and output terminals. The only problem for these converters with non-common ground nature is that the leakage current may flow into the grid if a transformer-less grid connected PV system is considered. However, in such a case, the leakage current is usually suppressed by modifying the modulation strategy of the inverter that is placed between the DC-DC converter and grid, or by using a common-mode filter at the output side of the PV system.

5. ANALYTICAL LOSS ANALYSIS OF THE PROPOSED S-SCZSC

The power loss of the S-SCZSC includes the losses of switch Q , diodes D_{in} , D_1 , D_2 , and D_o , capacitors C_{in} , C_1 , C_2 , C_3 , C_4 , and C_o , and inductors L_{in} , L_1 , and L_2 . Having the parasitic elements of the components that are listed in Table 5, the losses of the components are computed as follows:

The loss of power switch Q includes the conduction loss and switching loss, which is calculated from:

$$P_Q = P_{Q,cond} + P_{Q,sw} = I_{Q,rms}^2 R_{DS(on)} + V_Q^2 C_{oss} f_{sw} \quad (49)$$

The root-mean-square (rms) and average (avg) currents and voltage stress of the switch are as (50).

$$\begin{aligned} I_{Q,avg} &= \frac{2}{1-2D} I_o \\ I_{Q,rms} &= \frac{2}{\sqrt{D}(1-2D)} I_o \\ V_Q &= \frac{1}{1-2D} V_{in} \end{aligned} \quad (50)$$

Substituting (50) in (49), the loss of the switch is written as:

$$\left\{ \begin{aligned} P_Q &= \frac{4}{D(1-2D)^2} I_o^2 R_{DS(on)} \\ &+ \frac{2}{(1-2D)^3} V_{in}^2 C_{oss} f_{sw} \end{aligned} \right. \quad (51)$$

The loss of the diodes is as:

$$\left\{ \begin{aligned} P_D &= P_{D_{in}} + P_{D_2} + P_{D_2} + P_{D_o} \\ &= V_{D,F0} (I_{D_{in},avg} + I_{D_1,avg} + I_{D_2,avg} + I_{D_o,avg}) \\ &+ R_D (I_{D_{in},rms}^2 + I_{D_1,rms}^2 + I_{D_2,rms}^2 + I_{D_o,rms}^2) \end{aligned} \right. \quad (52)$$

The rms and avg currents of the diodes are as:

$$\begin{aligned}
 I_{D_{in},avg} &= \frac{3-2D}{1-2D} I_o \\
 I_{D_{in},rms} &= \frac{3-2D}{\sqrt{1-D(1-2D)}} I_o \\
 I_{D_1,avg} &= I_{D_2,avg} = I_{D_o,avg} = I_o \\
 I_{D_1,rms} &= I_{D_2,rms} = \frac{1}{\sqrt{D}} I_o \\
 I_{D_o,rms} &= \frac{1}{\sqrt{1-D}} I_o
 \end{aligned} \tag{53}$$

Substituting (53) in (52), the loss of the diodes is written as:

$$\begin{cases}
 P_D = V_{D,F0} I_o \left(\frac{6-8D}{1-2D} \right) \\
 + R_D I_o^2 \left(\frac{10-16D+8D^2}{D(1-D)(1-2D)^2} \right)
 \end{cases} \tag{54}$$

The loss of the capacitors is calculated by:

$$\begin{aligned}
 P_C &= P_{C_{in}} + P_{C_1} + P_{C_2} + P_{C_3} + P_{C_4} + P_{C_o} \\
 P_{C_{in}} &= I_{C_{in},rms}^2 \times ESR_{C_{in}} \\
 P_{C_1} &= I_{C_1,rms}^2 \times ESR_{C_1} \\
 P_{C_2} &= I_{C_2,rms}^2 \times ESR_{C_2} \\
 P_{C_3} &= I_{C_3,rms}^2 \times ESR_{C_3} \\
 P_{C_4} &= I_{C_4,rms}^2 \times ESR_{C_4} \\
 P_{C_o} &= I_{C_o,rms}^2 \times ESR_{C_o}
 \end{aligned} \tag{55}$$

The rms currents of the capacitors are as:

$$\begin{aligned}
 I_{C_{in},rms} &= \frac{(3-2D)\sqrt{D}}{(1-2D)\sqrt{1-D}} I_o \\
 I_{C_1,rms} &= I_{C_2,rms} = \frac{1}{(1-2D)\sqrt{D(1-D)}} I_o \\
 I_{C_3,rms} &= I_{C_4,rms} = \frac{1}{\sqrt{D(1-D)}} I_o \\
 I_{C_o,rms} &= \sqrt{\frac{D}{1-D}} I_o
 \end{aligned} \tag{56}$$

The conduction loss of the inductors obtained by:

$$\begin{aligned}
 P_L &= P_{L_{in}} + P_{L_1} + P_{L_2} \\
 P_{L_{in}} &= I_{L_{in}}^2 \times DCR_{L_{in}} \\
 P_{L_1} &= I_{L_1}^2 \times DCR_{L_1} \\
 P_{L_2} &= I_{L_2}^2 \times DCR_{L_2}
 \end{aligned} \tag{57}$$

By neglecting the small current ripples, the rms currents of inductors are:

$$\begin{aligned}
 I_{L_{in},rms} &= \frac{3-2D}{1-2D} I_o \\
 I_{L_1,rms} &= I_{L_2,rms} = \frac{2}{1-2D} I_o
 \end{aligned} \tag{58}$$

The total loss of the proposed S-SCZS converter is given by:

$$P_{Loss} = P_Q + P_D + P_C + P_L \tag{59}$$

The analytical efficiency of the converter is calculated by:

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \tag{60}$$

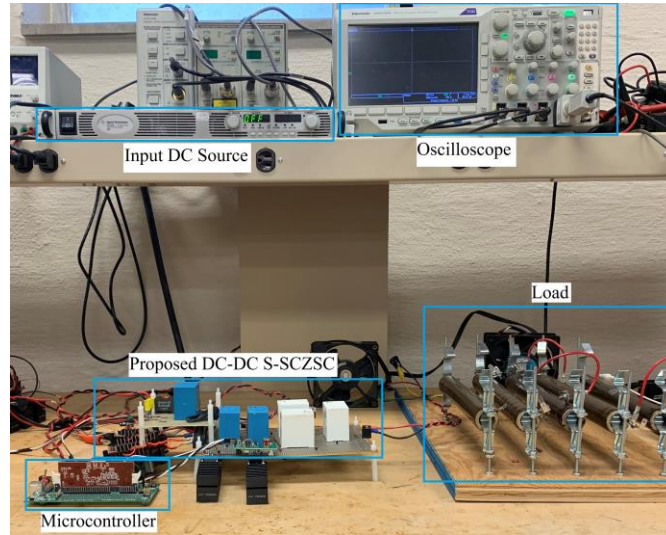


Figure 8. A view of the experimental prototype.

Table 5. Experimental components and parameters.

Components and Parameters	Values
Rated power P	400 W
Switching frequency f_{sw}	100 kHz
Inductors L_1, L_2	270 μ H $DCR_{L1}=DCR_{L2}=30$ m Ω
Input inductor L_{in}	20 μ H $DCR_{L_{in}}=10$ m Ω
Capacitors C_1, C_2	B32776G4506K000 50 μ F $ESR_{C1}=ESR_{C2}=4$ m Ω
Capacitors C_3, C_4, C_o	C4AQJBW5300P3LJ 30 μ F $ESR_{C3}=ESR_{C4}=ESR_{C_o}=3.5$ m Ω
Input capacitor C_{in}	B32678G4206K000 20 μ F $ESR_{C_{in}}=3.3$ m Ω
Diodes D_m, D_1, D_2, D_o	DSEC60-03A $R_D=15$ m Ω , $V_{D,F0}=0.45$ V
Power switch Q	IPW65R019C7 $R_{DS(on)}=19$ m Ω , $C_{oss}=160$ pF

6. EXPERIMENTAL RESULTS

To validate the theoretical analyses and feasibility of the proposed S-SCZSC, a 400 W prototype operating at 100 kHz was implemented, as shown in Figure 8. To design the capacitors and the inductors, the maximum voltage ripple of the capacitors and maximum

current ripple of the inductors are assumed to be 1 % and 20 %, respectively. The parameters and components used in the prototype are listed in Table 5. Inductors L_1 and L_2 are implemented with ETD54/28/19-3C90-A250 FerroxCube cores. The TMS320F28335 microcontroller is employed to generate the gate pulse for power switch Q . The current and differential voltage probes are used to measure the currents and voltages, respectively. The input DC voltage is provided with N5766A Agilent DC programmable power supply. Load resistance R is 400 Ω . The experimental results are presented for two different test points with input voltages of 28 V and 33 V, keeping output voltage ideally constant at 400 V.

Figure 9 shows the experimental results for $V_{in}=28$ V. According to (9), to achieve an ideal output voltage of 400 V, the microcontroller should provide a gate pulse with a duty cycle of 42.5 %, which gives rise to ideal voltage gain M of 14.3. From (33), the calculated average current is 13.3 A for inductors L_1 and L_2 , and the average input current is calculated as 14.3 A from (34); these values agree with the experimental results shown in Figure 9 (a). Additionally, the input current is smooth, which is very suitable for PV applications. Figure 9 (b) depicts the voltage stress across switch Q along with the output voltage, which almost match the theoretically calculated values of 187 V and 400 V, respectively. Therefore, the proposed converter achieves a high-voltage gain with low voltage stress on the power switch. The voltages of capacitors C_1 , C_2 , C_3 , and C_4 are depicted in Figure 9 (c); it is obvious that the capacitors' voltage ripples are small, which validates the correctness of the capacitors' design. Also, the voltages are close to the ideally calculated value of 107 V from (8). Figure 9 (d) shows the voltages of diodes D_{in} , D_1 , D_2 , and D_o , which are close to the calculated value of 187 V from (11)-(14).

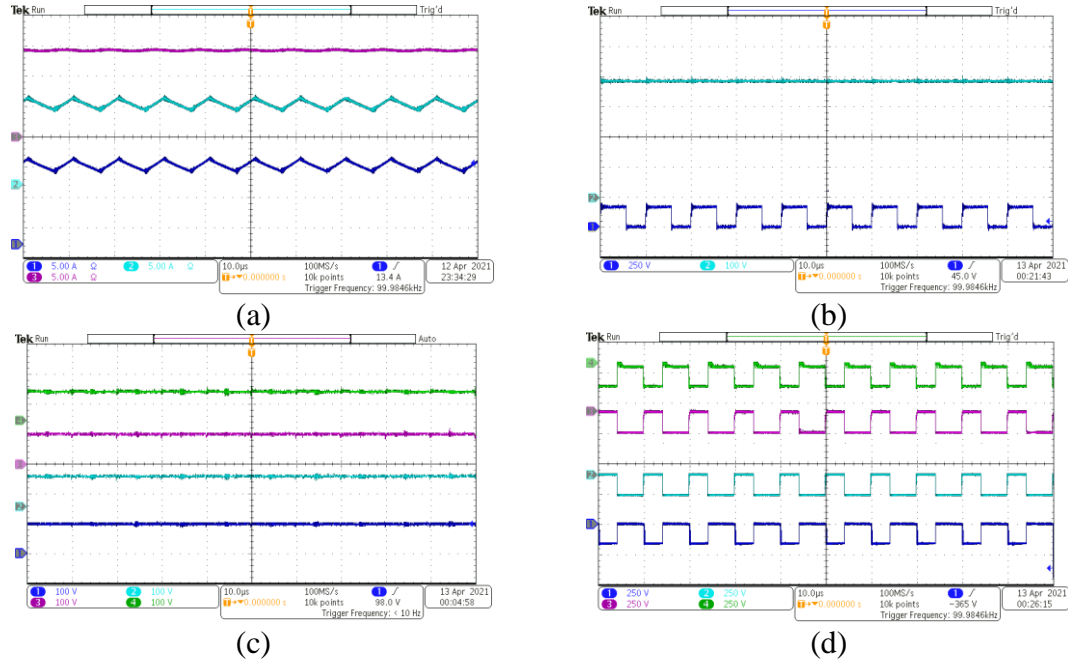


Figure 9. Experimental results of the proposed S-SCZSC for $V_{in}=28$ V, $D=42.5$ %, and $M=14.30$: (a) currents of inductors L_1 (CH 1) and L_2 (CH 2) and input current (CH 3); (b) voltage across switch Q (CH 1) and output voltage (CH 2); (c) voltages of capacitors C_1 (CH 1), C_2 (CH 2), C_3 (CH 3), and C_4 (CH 4); (d) voltages of diodes D_{in} (CH 1), D_1 (CH 2), D_2 (CH 3), and D_o (CH 4).

The experimental results for another test point with the input voltage of 33 V are illustrated in Figure 10. To keep the output voltage theoretically constant at 400 V, the duty cycle of switch Q is changed to 41 %, which results in voltage gain M of 12.12. Consequently, the calculated values of the parameters are as: $I_{in}=12.12$ A, $I_{L1}=I_{L2}=11.11$ A, $V_{C1}=V_{C2}=V_{C3}=V_{C4}=108.17$ V, and $V_Q=V_{Din}=V_{D1}=V_{D2}=V_{D0}=183.33$ V, all of which are in good agreement with the measured values shown in Figures 10 (a)-(d). Although there is little difference between experimentally measured and theoretically calculated values for all parameters, theoretical predictions are reasonably confirmed by experimental results. That is, the performance of the S-SCZSC is validated through the experimental results.

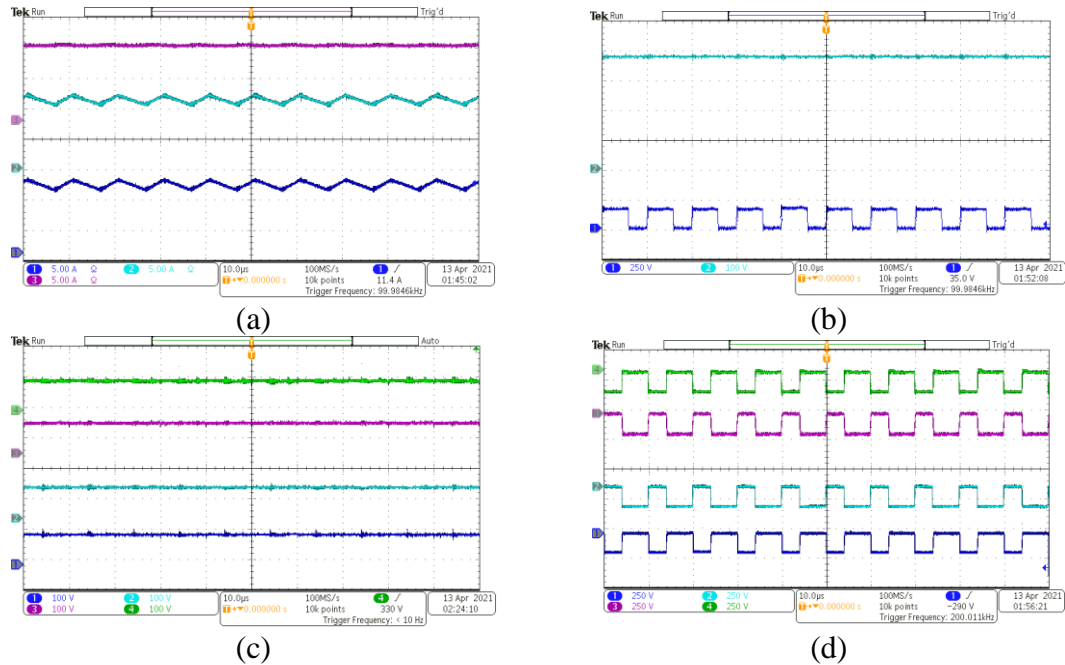


Figure 10. Experimental results of the proposed S-SCZSC for $V_{in}=33$ V, $D=41$ %, and $M=12.12$: (a) currents of inductors L_1 (CH 1) and L_2 (CH 2) and input current (CH 3); (b) voltage across switch Q (CH 1) and output voltage (CH 2); (c) voltages of capacitors C_1 (CH 1), C_2 (CH 2), C_3 (CH 3), and C_4 (CH 4); (d) voltages of diodes D_{in} (CH 1), D_1 (CH 2), D_2 (CH 3), and D_o (CH 4).

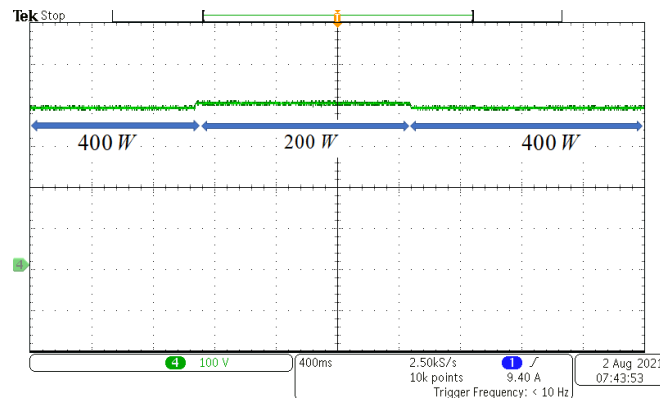


Figure 11. The dynamic response of the output voltage for a 50 % step change in the load from 400 W to 200 W and vice versa for $V_{in}=33$ V and $D=0.41$.

Figure 11 illustrates the dynamic response of the output voltage for a 50 % step change in the load from 400 W to 200 W and vice versa for $V_{in}=33$ V and $D=0.41$. Also,

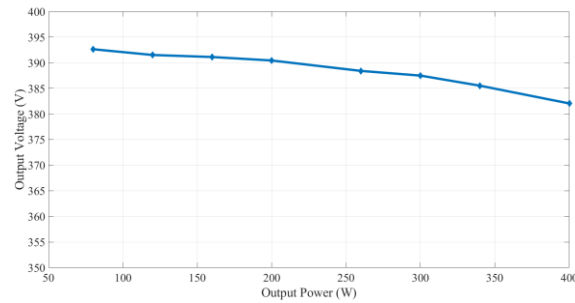


Figure 12. Output voltage regulation plot over the load power for $V_{in}=33$ V and $D=0.41$.

the output voltage regulation plot over the load is shown in Figure 12. Although the output voltage is not kept constant at 400 V for different output load powers, the dynamic response and output voltage regulation plot demonstrate the inherent stability of the proposed S-SCZSC because the deviation from 400 V is always small and less than 5 %; this voltage error can be compensated if any simple closed-loop controller is employed to control the duty cycle of switch Q .

Figure 13 shows the experimentally measured efficiency of the proposed S-SCZSC versus the load power with two different input voltages of 28 V and 33 V for the the output voltage of 400 V. As observed, the efficiency decreases as the input voltage decreases. That is, the higher the voltage gain, the lower the efficiency. Also, as output power increases, efficiency decreases. The efficiency for the input voltage of 33 V and full-load power of 400 W is approximately 91.25 %. The efficiency and key parameters of the proposed S-SCZSC is compared to other exiting ZS/qZS DC-DC converters in Table 6. As seen, only the converters in [26] and [28] have higher full-load efficiencies than proposed S-SCZS converter; however, their frequencies and voltage gains are lower than proposed S-SCZSC. Using (49)-(59), the analytical loss breakdowns among the components of

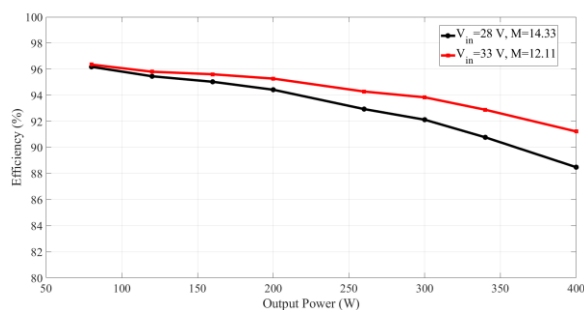
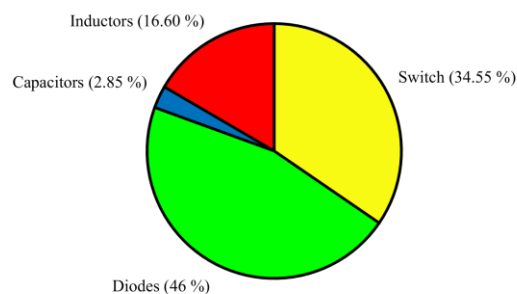
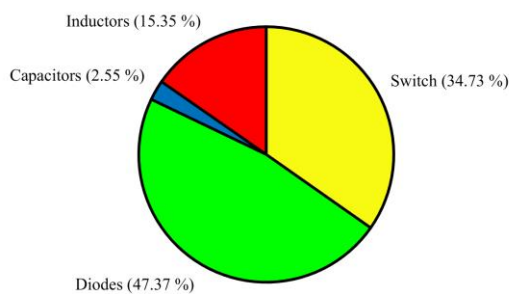


Figure 13. The experimental efficiency curve of the proposed S-SCZSC for the different input voltages of 28 V and 33 V.



(a)



(b)

Figure 14. The analytical loss breakdown of proposed S-SCZSC at full load for different input voltages: a) $V_{in}=28\text{ V}$; b) $V_{in}=33\text{ V}$.

proposed S-SCZSC for two input voltages of 28 V and 33 V at full load are obtained, shown in Figure 14. As seen, the dominant power losses occur in the diodes and switch.

Table 6. Full-load efficiency comparison of proposed S-SCZS converter with other existing ZS/qZS step-up DC-DC converters.

Converter	V_{in} (V)	V_o (V)	M	f_{sw} (kHz)	Rated power (W)	Full-load efficiency (%)
Converter in [19]	12	20	1.67	40	8	87
Converter in [22]	10	60	6	30	36	85
Converter in [26]	150	400	2.67	20	400	95.13
Converter in [27]	60	250	4.17	100	130	87
Hybrid two-quasi-Z-source converter in [28]	40	400	10	30	100	94
Hybrid three-quasi-Z-source converter in [28]	40	400	10	30	100	93
Converter in [30]	24	144	6	40	150	90.1
Converter in [31]	10	100	10	30	100	91
Proposed S-SCZS	33	400	12.11	100	400	91.25

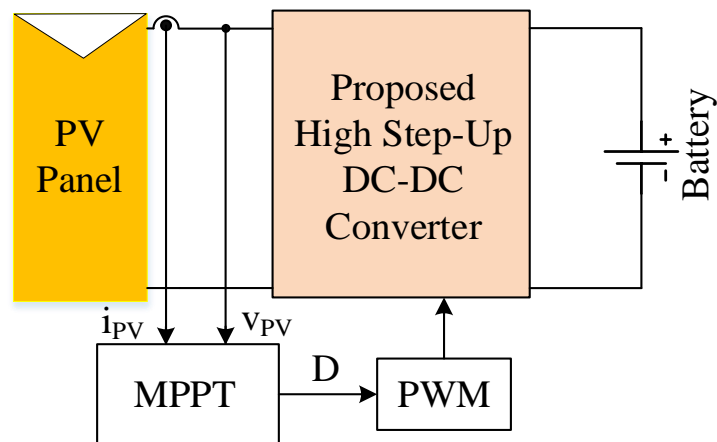


Figure 15. The schematic of the simulated PV system.

Table 7. Specifications of PV panel FSM400M-72-6.

Parameter	Value
Peak Power (P_{max})	400 W
Number of cells	72 pieces (6*12)
Maximum operating voltage (V_{MPP})	41.7 V
Maximum operating current (I_{MPP})	9.6 A
Open circuit voltage (V_{oc})	49.8 V
Short circuit current (I_{sc})	10.36 A

7. MPPT EVALUATION

In this section, the feasibility of the MPPT operation of the proposed S-SCZS converter in the PV application is verified through the simulation results in MATLAB. In the PV applications, the output voltage of the high step-up DC-DC converter is tightly regulated by the control block of a converter that is placed between the DC bus and grid (or load). Alternatively, the output side of the high step-up DC-DC converter is connected to a battery whose voltage is almost constant with low fluctuations. Thus, the output voltage of the high step-up DC-DC converter is relatively constant. Accordingly, the high step-up DC-DC converter is not in the charge of regulating its output voltage; it is only responsible to extract the maximum power of the solar panel. The simulated PV system is shown in Figure 15, in which the proposed high step-up DC-DC converter is used for extracting the maximum power of a PV panel, whose model is FSM400M-72-6 with the specifications given in Table 7. In the simulated PV system, a battery is used to represent a high-voltage DC bus with the voltage level of 400 V, and the perturbation and observation (P&O) method [32] is used to perform the MPPT function through sensing the current and voltage of the PV panel. The MPPT performance is evaluated under different levels of the solar irradiance, showing in Figure 16, in the PV panel surface temperature of 25 °C. Initially, the irradiance level is 1000 W/m² then decreases to 800 W/m² at $t=0.5$ sec, and at $t=1$ sec, the irradiance level drops to 400 W/m²; finally, the irradiance level increases to 1000 W/m² at $t=1.5$ sec. The I-V and P-V curves of the PV panel at the different irradiance levels are illustrated in Figure 17. Figure 18 depicts the results of the MPPT implementation for the different levels of the irradiance. As obvious, for all irradiance

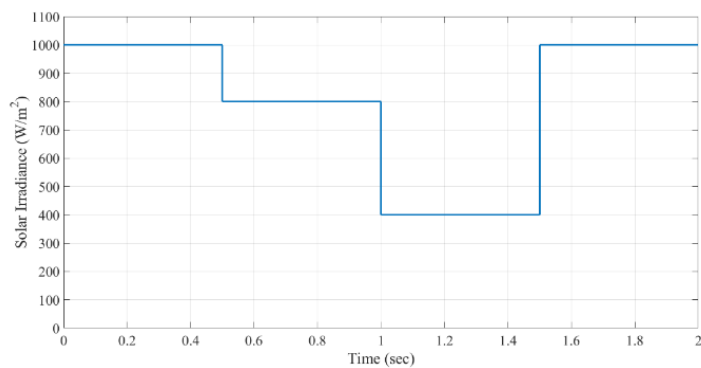


Figure 16. The varying irradiance of the solar panel.

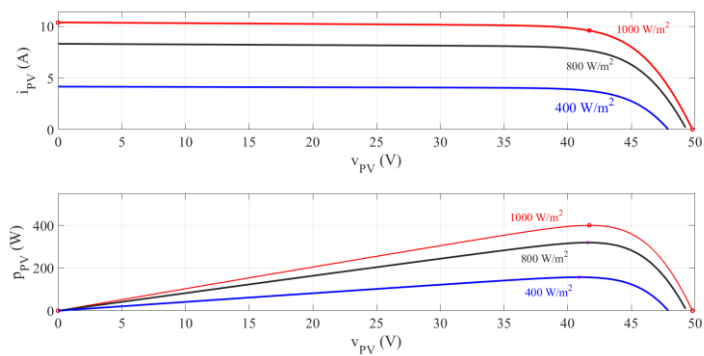


Figure 17. The I-V and P-V curves of the PV panel at different irradiance levels.

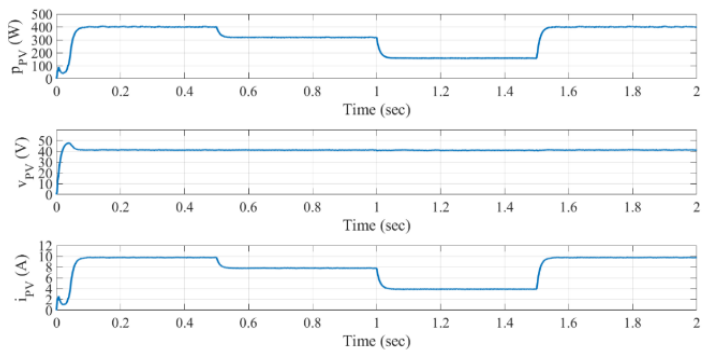


Figure 18. The simulation results of the MPPT implementation under different solar irradiance levels.

levels, the power and its corresponding voltage and current are very close to the maximum power points of the I-V and P-V curves of the PV panel. At startup, the MPPT time of the system is about 95 ms for the power change from 0 to 400 W. Accordingly, using the proposed S-SCZS converter, the MPPT algorithm offers proper performance; that is, the maximum power point of the PV panel is easily tracked at any solar irradiance level.

8. CONCLUSION

In this article, three ZS-based DC-DC converters—named PAS-SCZSC, NAS-SCZSC, and S-SCZSC—were proposed. Integrating the ZS network with SC cells resulted in new types of ZS networks, which were the main parts of the proposed converters. The proposed topologies offer advantages of simple configuration, a low number of components, a smooth input current, a high step-up voltage gain, low voltage stresses on the semiconductor devices, and full operating duty cycle range for ZS-based converters that is from 0 to 50 %. Thanks to these features, the proposed converters are suitable interfaces between a low-voltage solar PV panel and a high-voltage DC bus in the PV applications. This paper discussed the operating principles of the proposed S-SCZSC in detail, and then provided the voltage and current stresses of all components for all three proposed converters. In addition, the proposed converters were compared with other existing ZS-/qZS-based high step-up DC-DC converters in terms of voltage conversion ratio, voltage stresses on the diodes and power switch, duty cycle range, and the number of the components. Furthermore, the analytical results and the performance of the proposed S-SCZSC were verified through experimental results of a 400 W-400 V prototype. In

addition, the feasibility of the MPPT function was verified through the simulation results for the proposed S-SCZSC.

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IV. AN INTERLEAVED HIGH STEP-UP DC-DC CONVERTER BASED ON INTEGRATION OF COUPLED INDUCTOR AND BUILT-IN-TRANSFORMER WITH SWITCHED-CAPACITOR CELLS FOR RENEWABLE ENERGY APPLICATIONS

Ramin Rahimi, (Graduate Student Member, IEEE), Saeed Habibi, (Graduate Student Member, IEEE), Mehdi Ferdowsi, (Member, IEEE), Pourya Shamsi, (Senior Member, IEEE)

Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65409 USA

Corresponding author: Ramin Rahimi (e-mail: r.rahimi@mst.edu).

ABSTRACT

This paper proposes an interleaved high step-up DC-DC converter with the coupled inductor (CI) and built-in transformer (BIT) for renewable energy applications. Two double-winding (2W) CIs and one triple-winding (3W) BIT are integrated with the switched-capacitor (SC) voltage multiplier cells (VMCs) to achieve high-voltage gains without extreme duty cycles. The CIs and BIT turns-ratios provide two other degrees of freedom—in addition to the duty cycle—to adjust the voltage gain that leads to increased design flexibility. The diodes turn off naturally under the zero-current switching (ZCS) conditions because their current falling rates are controlled by the leakage inductances of the CIs and BIT; therefore, the diodes' reverse-recovery problems are alleviated. Moreover, employing passive diode-capacitor clamp circuits, the voltage stresses of the switches are limited to a low value far less than the output voltage. Additionally, the leakage inductances energies are recycled and transferred to the output to further extend the voltage gain. Furthermore, due to the interleaved structure, the input current ripple and

current stresses of the components are reduced. The proposed converter is analyzed in detail and then compared with similar converters that employed two 2W CIs and one 3W BIT along with passive clamp circuits for the MOSFETs. Finally, to verify the feasibility of the proposed converter, the experimental results of a 200 W prototype with output voltage of 400 V and voltage gain of 25 are presented.

Keywords: DC-DC converter, high step-up, high-voltage gain, coupled inductor, built-in transformer, switched-capacitor (SC), voltage multiplier cell (VMS), photovoltaic, fuel cell, renewable.

1. INTRODUCTION

Renewable energy sources, such as photovoltaic (PV) and fuel cells have received much attention in recent years [1, 2]. A hybrid renewable energy-based system is shown in Figure 1, where the PV and fuel cells are used as renewable energy sources; the voltage of these renewable energy sources is less than 50 V, which is relatively low compared to that of the DC link's voltage (e.g., 300-400 V) [3]. Thus, a high step-up DC-DC converter is required as an interface between the renewable energy sources and DC link, as depicted in Figure 1.

The traditional boost DC-DC converter can provide a high-voltage gain under extremely large duty cycles; however, it suffers from high voltage and current stresses in the semiconductor devices, reverse-recovery problem in the output diode, large ripple on the input current and the output voltage and high power losses [4, 5]. To eliminate these effects, voltage-boosting (VB) techniques were presented to extend the voltage gain of the

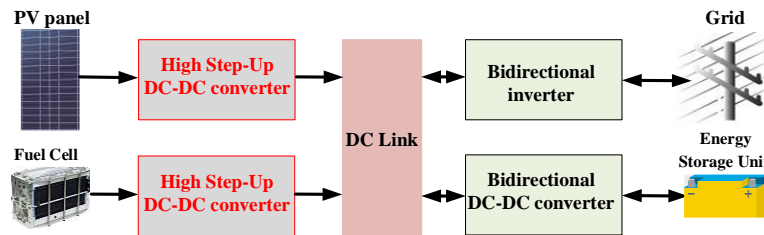


Figure 1. A hybrid renewable energy-based system with PV and fuel cells.

conventional boost converter without an extremely high duty cycle. The VB techniques are based on switch-capacitor (SC) voltage multiplier cells (VMCs) [6], switched-inductor (SL) VMCs [7], coupled-inductor (CI) [8], built-in transformer (BIT) [9], cascaded structure [10], quadratic converter [11], and Z-source/quasi Z-source converters [12]. Any potential combination of the mentioned VB techniques were considered to achieve a high step-up converter, such as those in [13-16]. Along with VB techniques, the interleaved structure is beneficial because a low input current ripple is obtained that reduces the size of the input filter, increases the lifetime of the renewable energy sources, reduces the current stresses on the components, and improves the efficiency [17, 18]. In [19-21], interleaved converters integrated with SC VMCs were introduced, and they suffered from high current transitions on the capacitors and required a large number of diodes and capacitors to achieve high-voltage gains. To eliminate the extreme instantaneous currents of the capacitors in the SC CMCs, the boost inductors can be replaced by CIs, or a BIT can be inserted into the converter topology—the energy stored in the leakage inductances of the CIs and BIT can be absorbed and recycled by either passive or active clamped techniques [22, 23]. In addition, the existence of the leakage inductances meant the current

falling rates of diodes were controlled, and zero-current switching (ZCS) conditions are achieved in the turn-off instants of the diodes, thereby improving the converter efficiency. In [24], an interleaved converter was presented that integrated an asymmetric SC VMC with double-winding (2W) CIs and employed passive clamp circuits to recycle the energy of the leakage inductances and limit the voltage stresses on the main switches. Another 2W CI-based interleaved converter was introduced in [25] in which, like the topology in [24], the secondary windings of the CIs were integrated into SC VMCs to extend the voltage gain. Other 2W CI-based interleaved converters were proposed in [26-29]. The interleaved converters in [30-33] used two triple-winding (3W) CIs to further extend the voltage gains. The interleaved converters in [34] and [35] utilized the 2W and 3W BIT, respectively. In interleaved converters without CI and BIT, the voltage gain is only adjusted with the duty cycle of the main switches. By contrast, for the converters with either CI or BIT, there were two degrees of freedom—duty cycle and turns-ratio—that made the voltage gain adjustment flexible. The interleaved converters in [36, 37] took advantage of both the CI and BIT to further enhance the voltage gain; these converters utilized two 2W CIs and one 3W BIT, where the secondary windings of CIs, along with the secondary and tertiary windings of BIT, were combined with the SC VMCs to achieve a high voltage gain. Having three degrees of freedom for converters with both CI and BIT (duty cycle of the main switches, turns-ratio of the CIs, and turns-ratio of the BIT) resulted in a flexible design that was appropriate for the high-voltage gain applications. Therefore, the usage of the CI together with BIT integrated with SC VMCs is the most effective technique used to further increase the voltage gain.

Considering the previously discussed information, in this paper, an interleaved high step-up DC-DC converter with two 2W CIs and one 3W BIT is proposed to achieve high-voltage gains without extremely high cycle cycles. Passive clamped circuits are used to absorb and recycle the leakage inductances energies and limit switches voltage stresses to a value far less than the output voltage. The leakage inductances provide the proposed converter with turn-off ZCS conditions for the diodes that improve efficiency. Also, the reverse recovery problem of the diodes is suppressed. The voltage gain and the voltage stresses for the semiconductor devices can be controlled flexibly by three parameters, including turns-ratio of the 2W CIs, turns-ratio of the 3W BIT, and duty cycle of the switches. Furthermore, low-voltage-rated semiconductor devices with low ON-state resistances are adopted for the proposed converter, thus leading to the reduction of the conduction losses. Additionally, due to the interleaved structure of the proposed converter, the input current ripple and the current stresses of the components decrease significantly.

The rest of this paper is organized as follows: Section 2 introduces the topology of the proposed converter and analyzes its operation modes. Section 3 presents a steady-state analysis of the proposed converter. The design considerations of the proposed converter are presented in Section 4. In Section 5, a comparison analysis in terms of voltage gain, normalized voltage stresses, and components count is accomplished, and that proves the superior performance of the proposed converter compared to other similar existing counterparts. Section 6 presents experimental results to validate the study, and the overall conclusion is presented in Section 7.

2. PROPOSED CONVERTER AND OPERATING MODES

The proposed converter is shown in Figure 2; the power switches are denoted by Q_1 and Q_2 , which are gated in interleaved manner with a 180° phase shift. There are two 2W CIs whose coupling references are denoted by “●” and “★”—each CI is modeled as the combination of a magnetizing inductance, an ideal 2W transformer, and the leakage inductance for each winding; L_{k1} and L_{k2} are the leakage inductances of primary windings; L_{m1} and L_{m2} are the magnetizing inductances; N_{p1} and N_{p2} are the number of the primary turns; the secondary turns are shown by N_{s1} and N_{s2} . Also, there is a 3W BIT whose reference points are represented by “■”; the primary, secondary, and tertiary windings’ turns of the BIT are denoted by n_p , n_s , and n_t , respectively; L_{k3} is the leakage inductance of the primary side for BIT. Each of secondary and tertiary windings of the BIT are connected in-series with the secondary winding of CI for each phase, resulting in the total leakage inductances of L_{k4} and L_{k5} . D_{c1} and D_{c2} are the clamp diodes; C_{c1} and C_{c2} are the clamp capacitors. Diode-capacitors pairs (D_{c1}, C_{c1}) and (D_{c2}, C_{c2}) make the clamp circuits, leading to limit the voltage stresses on switches Q_1 and Q_2 , and they recycle the energy stored in the leakage inductances; D_{r1} and D_{r2} represent the regenerative diodes; C_{m1} and C_{m2} denote the intermediate energy storage capacitors; D_o and C_o represent the output diode and capacitor, respectively. There is a total of five diodes and five capacitors. The input voltage, output voltage, and load are represented by V_{in} , V_o , and R , respectively. The turns-ratios of the CIs represented by $N_1=N_{s1}/N_{p1}$, $N_2=N_{s2}/N_{p2}$; for the BIT, the turns-ratios are denoted by $n_{sp}=n_s/n_p$ and $n_{tp}=n_t/n_p$. The duty cycle (D) of the power switches is more than 0.5, and during a switching period T , the proposed converter has 8 operation modes. Figure 3

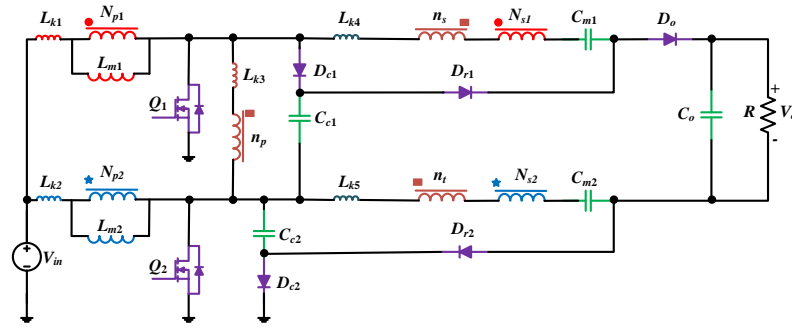


Figure 2. Proposed converter.

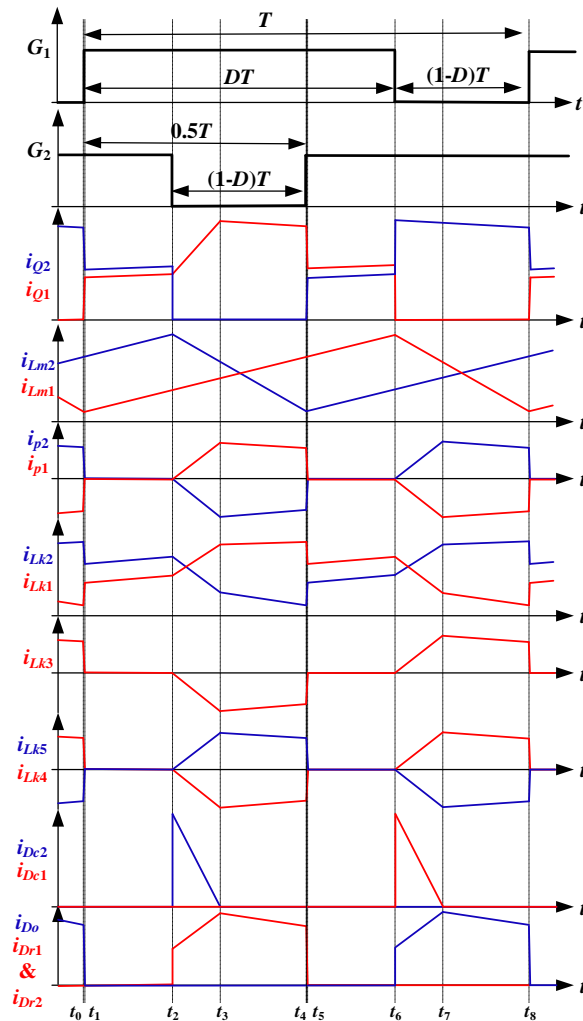


Figure 3. Key waveforms of the proposed converter.

$$\left\{ \begin{aligned} (n_{sp} + n_{p})L_{k3} \frac{di_{L_{k3}}(t)}{dt} &= -L_{k4} \frac{di_{L_{k4}}(t)}{dt} + L_{k5} \frac{di_{L_{k5}}(t)}{dt} - V_o \\ &- N_1 V_{L_{m1}} + N_2 V_{L_{m2}} + V_{C_{m1}} + V_{C_{m2}} \end{aligned} \right. \quad (4)$$

Mode 2 (Figure 4b, $t_1 \leq t \leq t_2$): This operation mode begins when D_o turns off with ZCS condition at $t=t_1$; both switches Q_1 and Q_2 remain in ON state. Inductances L_{m1} , L_{m2} , L_{k1} , and L_{k2} are charged by the input voltage, and the load is supplied solely by the output capacitor. The key relationships are as:

$$\left\{ \begin{aligned} V_{L_{m1}} + V_{L_{k1}} &= V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ i_{L_{m1}}(t) &= i_{L_{k1}}(t) = i_{L_{m1}}(t_1) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_1) \\ i_{L_{m2}}(t) &= i_{L_{k2}}(t) = i_{L_{m2}}(t_1) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_1) \end{aligned} \right. \quad (5)$$

Mode 3 (Figure 4c, $t_2 \leq t \leq t_3$): At $t=t_2$, the gate signal becomes zero for Q_2 , and clamp diode D_{c2} turns on to clamp the voltage across Q_2 to $V_{C_{c2}}$; simultaneously, regenerative diodes D_{r1} and D_{r2} start to conduct because the reverse voltages across them becomes zero. As the currents through diodes D_{r1} and D_{r2} increase, the current through diode D_{c2} decreases. By means of the conducting current through the secondary windings of the CIs and secondary and tertiary windings of the BIT, clamp capacitor C_{c1} is discharged and intermediate capacitors C_{m1} and C_{m2} are charged. The magnetizing inductance L_{m1} is charged, while L_{m2} transfers the energy to the secondary side. When the energy of leakage inductance L_{k2} is completely absorbed by C_{c2} , diode D_{c2} is reverse-biased and turns off with ZCS condition at the end of this mode. The relationships for this mode are as (6)-(8).

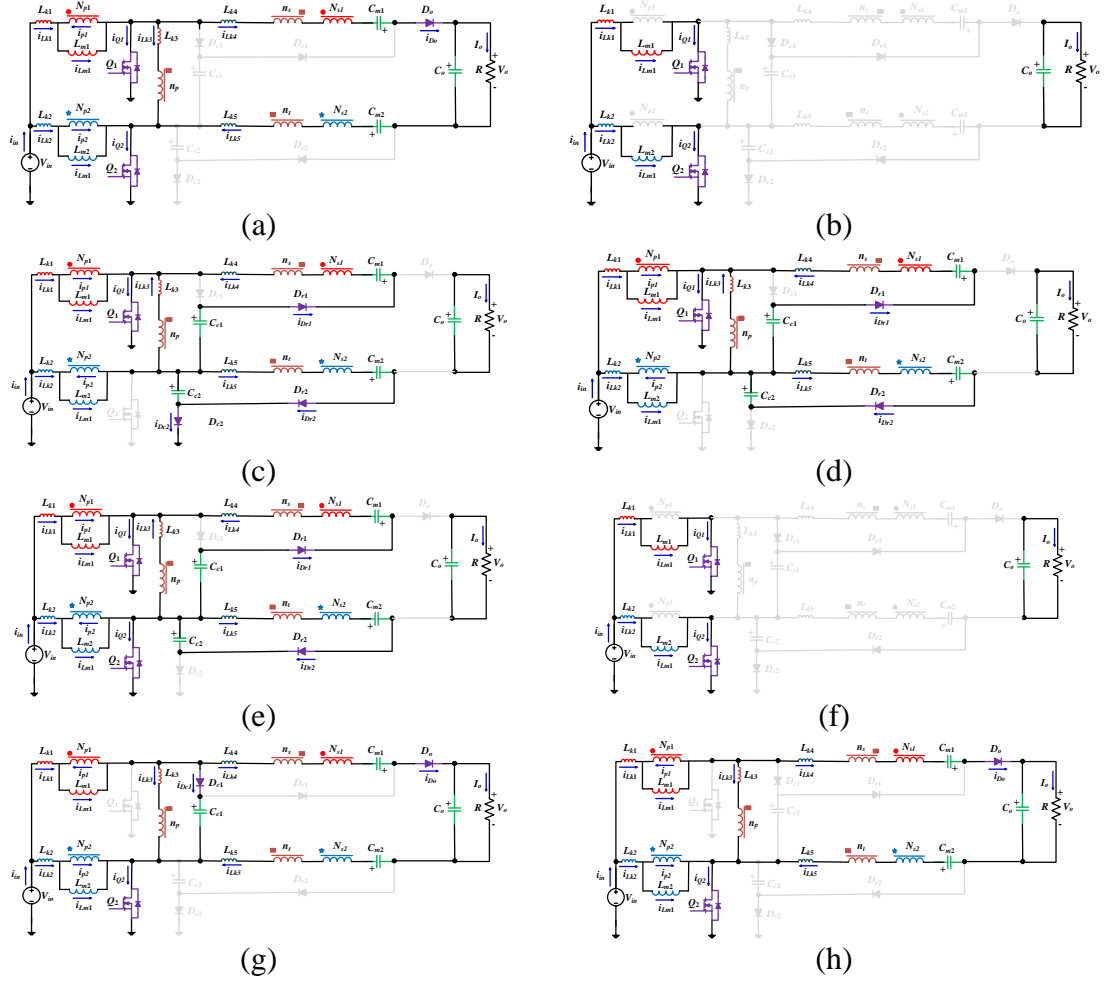


Figure 4. Operation modes in one switching period: (a) Mode 1 $[t_0-t_1]$, (b) Mode 2 $[t_1-t_2]$, (c) Mode 3 $[t_2-t_3]$, (d) Mode 4 $[t_3-t_4]$, (e) Mode 5 $[t_4-t_5]$, (f) Mode 6 $[t_5-t_6]$, (g) Mode 7 $[t_6-t_7]$, (h) Mode 8 $[t_7-t_8]$.

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ V_{P_{BTR}} + V_{L_{k3}} = -V_{C_{c2}} \end{cases} \quad (6)$$

$$\begin{cases} N_1 V_{L_{m1}} + V_{L_{k4}} + n_{sp} V_{L_{k3}} = V_{C_{m1}} - V_{C_{c1}} - (n_{sp} + 1) V_{C_{c2}} \\ N_2 V_{L_{m2}} + V_{L_{k5}} - n_{tp} V_{L_{k3}} = (n_{tp} + 1) V_{C_{c2}} - V_{C_{m2}} \end{cases} \quad (7)$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{tp} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \quad (8)$$

Mode 4 (Figure 4d, $t_3 \leq t \leq t_4$): At $t=t_3$, clamp diode D_{c2} turns off with ZCS condition because its current decreases to zero after the leakage energy of L_{k2} is fully transferred. The diode current rate is controlled by the leakage inductance, thus there is no turn-off reverse-recovery problem. The currents of both diodes D_{r1} and D_{r2} start to decrease. The mechanism of the energy transferring is the same as the previous operation mode. In this mode, the relationships are obtained as (9)-(12).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} - V_{p_{BIT}} - V_{L_{k3}} = V_{in} \\ V_{p_{BIT}} + V_{L_{k3}} = V_{L_{m2}} + V_{L_{m1}} + V_{L_{k2}} - V_{L_{k1}} \end{cases} \quad (9)$$

$$\begin{cases} (N_1 + n_{sp} + 1)V_{L_{m1}} - (n_{sp} + 1)(V_{L_{m2}} + V_{L_{k2}} - V_{L_{k1}}) \\ + V_{L_{k4}} + n_{sp} V_{L_{k3}} = V_{C_{m1}} - V_{C_{c1}} \end{cases} \quad (10)$$

$$\begin{cases} n_{tp}(V_{L_{m1}} + V_{L_{k1}} + V_{L_{k3}} - V_{L_{k2}}) \\ -(N_2 + n_{tp})V_{L_{m2}} - V_{L_{k5}} = V_{C_{m2}} - V_{C_{c2}} \end{cases} \quad (11)$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{tp} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \quad (12)$$

Mode 5 (Figure 5e, $t_4 \leq t \leq t_5$): At $t=t_4$, this mode begins when switch Q_2 turns on. This operation mode ends when the currents through regenerative diodes D_{r1} and D_{r2}

decrease to zero, and accordingly, the energy at the secondary/tertiary windings of the CIs and BIT reaches zero. D_{r1} and D_{r2} turn off with ZCS condition at $t=t_5$. The circuit relationships of this mode are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} = -V_{L_{k3}} \end{cases} \quad (13)$$

$$\begin{cases} N_1 V_{L_{m1}} + V_{L_{k4}} + n_{sp} V_{L_{k3}} = V_{C_{m1}} - V_{C_{c1}} \\ -N_2 V_{L_{m2}} - V_{L_{k5}} + n_{ip} V_{L_{k3}} = V_{C_{m2}} - V_{C_{c2}} \end{cases} \quad (14)$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{ip} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \quad (15)$$

Mode 6 (Figure 4f, $t_5 \leq t \leq t_6$): Diodes D_{r1} and D_{r2} turn off at $t=t_5$, while switches Q_1 and Q_2 remain in ON state. Magnetizing inductances L_{m1} and L_{m2} are charged by the input voltage, which is the same as Mode 2. The relationships are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} = 0 \end{cases} \quad (16)$$

$$\begin{cases} i_{L_{m1}}(t) = i_{L_{k1}}(t) = i_{L_{m1}}(t_6) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_6) \\ i_{L_{m2}}(t) = i_{L_{k2}}(t) = i_{L_{m2}}(t_6) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_6) \\ i_{p1}(t) = i_{p2}(t) = i_{L_{k3}}(t) = i_{L_{k4}}(t) = i_{L_{k5}}(t) = 0 \end{cases} \quad (17)$$

Mode 7 (Figure 4g, $t_6 \leq t \leq t_7$): This mode is similar to Mode 3. At $t=t_6$, clamp diode D_{c1} is forward-biased, then the voltage across Q_1 is clamped to $V_{C_{c1}}$; the voltage across output diode D_o reaches zero, and it is forward-biased. The stored energy in magnetizing inductance L_{m1} is transferred to the secondary side. As the current through D_o increases, the current through D_{c1} decreases. Intermediate capacitors C_{m1} and C_{m2} are discharged. The relationships for this mode are as (18)-(20).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{P_{BT}} + V_{L_{k3}} = V_{C_{c1}} \end{cases} \quad (18)$$

$$\begin{cases} N_2 V_{L_{m2}} - N_1 V_{L_{m1}} - V_{L_{k4}} + V_{L_{k5}} \\ -(n_{sp} + n_{tp}) V_{L_{k3}} = V_o - (n_{sp} + n_{tp} + 1) V_{C_{c1}} - V_{C_{m1}} - V_{C_{m2}} \end{cases} \quad (19)$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = (n_{sp} + n_{tp}) i_{D_o}(t) \\ i_{L_{k4}}(t) = i_{D_o}(t) \\ i_{L_{k5}}(t) = -i_{D_o}(t) \end{cases} \quad (20)$$

Mode 8 (Figure 4h, $t_7 \leq t \leq t_8$): At $t=t_7$, the current through clamp diode D_{c1} decreases to zero, and it turns off with ZCS condition due to leakage inductance L_{k1} . The current of D_o starts to decrease, and its decreasing rate is controlled by the leakage inductances. The energy stored in the magnetizing inductor L_{m1} is continuously transferred to output. The relationships for this mode are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} + V_{P_{BT}} + V_{L_{k3}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{P_{BT}} + V_{L_{k3}} = V_{L_{m2}} - V_{L_{m1}} + V_{L_{k2}} - V_{L_{k1}} \end{cases} \quad (21)$$

$$\begin{cases} -(N_1 + n_{sp} + n_{ip} + 1)V_{L_{m1}} + (N_2 + n_{sp} + n_{ip} + 1)V_{L_{m2}} \\ -(n_{sp} + n_{ip})V_{L_{k3}} + (n_{sp} + n_{ip} + 1)(V_{L_{k2}} - V_{L_{k1}}) \\ -V_{L_{k4}} + V_{L_{k5}} = V_o - V_{C_{m1}} - V_{C_{m2}} \end{cases} \quad (22)$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = (n_{sp} + n_{ip})i_{D_o}(t) \\ i_{L_{k4}}(t) = i_{D_o}(t) \\ i_{L_{k5}}(t) = -i_{D_o}(t) \end{cases} \quad (23)$$

3. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis of the proposed converter, Modes 1 and 5 with the short durations were ignored.

3.1. VOLTAGE GAIN

Ignoring the leakage inductances, Modes 3 and 4 are the same; similarly, Modes 7 and 8 are assumed to be the same. The, by applying the voltage-second balance law to magnetizing inductances L_{m1} and L_{m2} , the following equations are written:

$$2(D - \frac{1}{2})V_{in} + 2(1 - D)V_{in} + (1 - D)V_{C_{c1}} = 0 \quad (24)$$

$$2(D - \frac{1}{2})V_{in} + 2(1 - D)V_{in} + (1 - D)V_{C_{c2}} = 0 \quad (25)$$

From (24) and (25), the voltages on capacitors C_{c1} and C_{c2} are obtained as:

$$V_{C_{c1}} = V_{C_{c2}} = \frac{1}{1 - D} V_{in} \quad (26)$$

Considering Mode 3, the following relationship is written:

$$\begin{cases} V_{C_{m1}} = V_{C_{c1}} + (n_{sp} + 1)V_{C_{c2}} + N_1 V_{in} \\ V_{C_{m2}} = (n_{tp} + 1)V_{C_{c2}} - N_2(V_{in} - V_{C_{c2}}) \end{cases} \quad (27)$$

Substituting (26) in (27), the voltages across capacitors C_{m1} and C_{m2} are obtained

as:

$$\begin{cases} V_{C_{m1}} = \frac{2 + n_{sp} + (1 - D)N_1}{1 - D} V_{in} \\ V_{C_{m2}} = \frac{1 + n_{tp} + DN_2}{1 - D} V_{in} \end{cases} \quad (28)$$

Considering Mode 7, the following equation is obtained:

$$V_o = (n_{sp} + n_{tp} + 1)V_{C_{c1}} + V_{C_{m1}} + V_{C_{m2}} \quad (29)$$

Substituting (26) and (28) in (29), the voltage of the output capacitor is extracted

as:

$$V_{C_o} = V_o = \frac{4 + 2(n_{sp} + n_{tp}) + N_1 + N_2}{1 - D} V_{in} \quad (30)$$

Accordingly, the ideal voltage gain is obtained as:

$$M = \frac{V_o}{V_{in}} = \frac{4 + 2(n_{sp} + n_{tp}) + N_1 + N_2}{1 - D} \quad (31)$$

If the turns-ratios of the CIs are equal to N (i.e., $N_1=N_2=N$) and the turns-ratios of the BIT are equal to n (i.e., $n_{sp}=n_{tp}=n$), the capacitors' voltages and voltage gain are simplified as in (32) and (33).

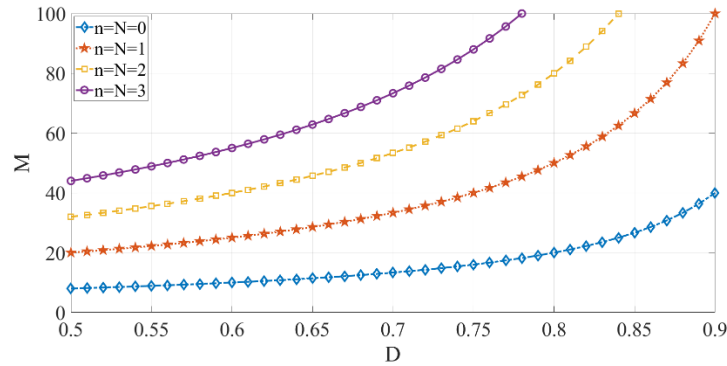


Figure 5. Voltage gain versus duty cycle for different values of N and n .

$$\begin{aligned}
 V_{C_{c1}} &= V_{C_{c2}} = \frac{1}{1-D} V_{in} \\
 V_{C_{m1}} &= \frac{2+n+(1-D)N}{1-D} V_{in} \\
 V_{C_{m2}} &= \frac{1+n+DN}{1-D} V_{in} \\
 V_{C_o} = V_o &= \frac{4+4n+2N}{1-D} V_{in}
 \end{aligned} \tag{32}$$

$$M = \frac{V_o}{V_{in}} = \frac{4+4n+2N}{1-D} = \frac{4(1+n+\frac{N}{2})}{1-D} \tag{33}$$

As explored in the above analysis, the voltage gain of the proposed converter is controlled by three parameters: the turns-ratio of the CIs (N), the turns-ratio of the BIT (n), and the duty cycle of the switches (D); thus, there are three degrees of freedom to extend the voltage gain without an extreme duty cycle at high voltage gains. The plot of the voltage gain is sketched in Figure 5 for different values of N , n , and D . As observed, the voltage gain increases significantly as the duty cycle and the turns-ratios increase, which makes the proposed converter reach high voltage gains without extreme duty cycles in high step-up applications.

3.2. EFFECT OF LEAKAGE INDUCTANCES ON VOLTAGE GAIN

In fact, the leakage inductances of the CIs and BIT are not zero. By analyzing the current of the output diode, the effect of leakage inductances on the voltage gain is clarified. The current of D_o flows through the circuits during Modes 7 and 8; the duration of the Mode 7 ($\Delta t_7 = t_7 - t_6$) is supposed to be $0.6 \times (1-D)T$ for the designed converter in this paper. Additionally, the current-falling rate of diode D_o (di_{D_o}/dt) is nearly zero during Mode 8. Additionally, the average current of D_o is equal to the output current (I_o). Thus, the peak current of the output diode can be obtained as:

$$\left\{ \begin{array}{l} \frac{1}{T} \int_0^T i_{D_o}(t) dt = I_o \\ \rightarrow \frac{1}{T} \left(\frac{1}{2} \times 0.6 \times (1-D)T \times I_{D_o,peak} + 0.4 \times (1-D)T \times I_{D_o,peak} \right) = I_o \\ \rightarrow I_{D_o,peak} = \frac{10I_o}{7(1-D)} \end{array} \right. \quad (34)$$

Knowing the peak current of D_o , the voltage gain is obtained as (35).

$$M = \frac{4(1+n+\frac{N}{2})}{1-D + \frac{50f_{sw}}{21(1-D)R} (N^2(L_{k1} + L_{k2}) + 4n^2L_{k3} + L_{k4} + L_{k5})} \quad (35)$$

As obvious, the voltage gain reduces slightly as the leakage inductances increase.

3.3. SEMICONDUCTOR DEVICES VOLTAGE STRESSES

The voltage stresses of the semiconductor devices are given by (36)-(41).

$$V_{Q_1} = V_{Q_2} = \frac{1}{1-D} V_{in} = \frac{1}{4(1+n+\frac{N}{2})} V_o \quad (36)$$

$$V_{D_{c1}} = \frac{2}{1-D} V_{in} = \frac{1}{2(1+n+\frac{N}{2})} V_o \quad (37)$$

$$V_{D_{c2}} = \frac{1}{1-D} V_{in} = \frac{1}{4(1+n+\frac{N}{2})} V_o \quad (38)$$

$$V_{D_{r1}} = \frac{2(1+n+\frac{N}{2})}{1-D} V_{in} = \frac{1}{2} V_o \quad (39)$$

$$V_{D_{r2}} = \frac{2n+N}{1-D} V_{in} = \frac{n+\frac{N}{2}}{2(1+n+\frac{N}{2})} V_o \quad (40)$$

$$V_{D_o} = \frac{2(1+2n+N)}{1-D} V_{in} = \frac{1+2n+N}{2(1+n+\frac{N}{2})} V_o \quad (41)$$

As the turns-ratio of either CIs or BIT increases, the voltage stresses of semiconductors D_{c1} , D_{c2} , Q_1 , and Q_2 decrease significantly when compared to the output voltage; thus, low-voltage-rated switches with a low $R_{DS(on)}$ are employed, which reduces the conduction losses. Also, the voltage stress of the regenerative diode D_{r1} is equal to half the output voltage, and $V_{D_{r2}}$ is less than the output voltage.

3.4. COMPONENTS AVERAGE CURRENT

The average currents of the leakage and magnetizing inductances are calculated as:

$$\begin{cases} I_{L_{m1}} = I_{L_{m2}} = I_{L_m} = \frac{2+2n+N}{1-D} I_o \\ I_{L_{k1}} = I_{L_{k2}} = I_{L_m} \\ I_{L_{k3}} = I_{L_{k4}} = I_{L_{k5}} = 0 \end{cases} \quad (42)$$

The average root mean square (rms) currents of the semiconductor devices are as:

$$\begin{cases} I_{D_{c1}avg} = I_{D_{c2}avg} = I_{D_{r1}avg} = I_{D_{r2}avg} = I_{D_oavg} = I_o \\ I_{Q_{1}avg} = I_{Q_{2}avg} = \frac{2 + 2n + N}{1 - D} I_o \\ I_{D_{c1}rms} = I_{D_{c2}rms} = \frac{10}{3\sqrt{2(1-D)}} I_o \\ I_{D_{r1}rms} = I_{D_{r2}rms} = I_{D_orms} = \frac{2 + 2n + N}{(1 + 2n + N)\sqrt{1-D}} I_o \\ I_{Q_{1}rms} = I_{Q_{2}rms} = \frac{(4 + 4n + 2N)\sqrt{D}}{1 - D} I_o \end{cases} \quad (43)$$

4. DESIGN CONSIDERATIONS

4.1. COUPLED INDUCTORS AND BUILT-IN TRANSFORMER DESIGN

4.1.1. Limitation of Turns-Ratio. Given that the duty cycle of the switches is higher than 0.5, it can be written as:

$$D = 1 - \frac{4(1 + n + \frac{N}{2})}{M} \geq 0.5 \rightarrow n + \frac{N}{2} \leq \frac{M - 8}{8} \quad (44)$$

4.1.2. Magnetizing Inductances of CIs. For any arbitrary ripple current, $L_{m1}=L_{m2}=L_m$ is obtained from:

$$L_m = \frac{V_{in} D}{f_{sw} \Delta i_L} \quad (45)$$

To operate in CCM, the magnetizing inductance of CIs must be higher than the critical inductance that is obtained from (46).

$$\begin{cases} \Delta i_{Lm} = \frac{V_{in}D}{f_{sw}L_m} = \frac{V_oD}{f_{sw}L_mM} \\ I_{Lm} = I_{Lm1} = I_{Lm2} = \frac{2+2n+N}{1-D} I_o = \frac{M}{2} I_o \\ R = \frac{V_o}{I_o} \end{cases} \quad (46)$$

$$\Delta i_{Lm} = 2I_{Lm} \rightarrow L_m = L_{crit} \rightarrow L_{crit} = \frac{DR}{M^2 f_{sw}}$$

4.1.3. Number of Turns of CIs' Windings. Having the flux density variation (ΔB_{CI}) and the cross-sectional area of the core ($A_{c,CI}$) for the CIs, the number of turns for the primary winding (N_p) is determined from (47); then, the number of the secondary winding' turns (N_s) is obtained by having the CIs turns-ratio (N).

$$N_p = \frac{V_{in}D}{\Delta B_{CI} A_{c,CI} f_{sw}} \quad (47)$$

4.1.4. Number of Turns of CIs' Windings. Using ΔB_{BIT} and $A_{c,BIT}$ for the BIT mean the number of turns for the primary winding (n_p) is calculated from (48), and the numbers of turns for the secondary and tertiary windings (n_s, n_t) are obtained from the obtained BIT turns-ratio (n).

$$n_p = \frac{V_{c1}D}{\Delta B_{BIT} A_{c,BIT} f_{sw}} = \frac{V_{in}D}{(1-D)\Delta B_{BIT} A_{c,BIT} f_{sw}} \quad (48)$$

4.2. CAPACITORS DESIGN

The voltages of the capacitors are determined from (32). By knowing the maximum ripple voltages (ΔV_{Cmax}) of the capacitors, the capacitances can be determined as:

$$\begin{cases} C_{c1}, C_{c1}, C_{m1}, C_{m2} \geq \frac{4 + 4n + 2N}{5f_{sw}(1 + 2n + N)\Delta V_{C_{max}}} I_o \\ C_o \geq \frac{DI_o}{f_{sw}\Delta V_{C_{max}}} \end{cases} \quad (49)$$

5. CIRCUIT PERFORMANCE COMPARISON

In this section, comparisons are made between the proposed converter and other interleaved high step-up converters in terms of the component's numbers, voltage gains, normalized voltage stress on power switches, and normalized total voltage stress on all diodes, as listed in Table 1; the voltages are normalized to the input voltage. The high step-up converters in [16, 34, 35] are based on the integration the normal inductor and BIT with the SC VMCs, and the converters in [27, 30, 32, 33] extend the voltage gain through integration the CIs with the SC VMCs. To adjust the voltage gain, there are two degrees of freedom for the converters in [16, 27, 30, 32-35], one of which is the duty cycle of the switches and the other is the turns-ratio of the CIs or BIT. However, the proposed converter and converters in [36, 37] offer three degrees of freedom (i.e., D , n , N) for adjusting the voltage gain because they are developed based on the combination of BIT and CIs into the SC VMCs, which results in a flexible design that is appropriate for high-voltage gain applications. The converters in [16, 34, 35] have three magnetic cores, while other converters and proposed converter have two magnetic cores.

In the comparison of the voltage gain, as seen from Figure 6, the proposed converter has the highest voltage gain for the whole duty cycle range. According to Figure 7, illustrating the normalized voltage stress on the switches, the proposed converter offers the

Table 1. Comparison of proposed converter with other interleaved high step-up converters.

Converter	Number of		Voltage gain (M)	Normalized voltage stress on switches	Normalized total voltage stress on all diodes
	Switches/Diodes/Capacitors	Inductors/CIs/BIT/ Total magnetic cores			
Ref. [16]	2/6/5	2/0/1/3	$\frac{2(1+n)}{1-D}$	$\frac{1}{2+2n}M$	$\frac{3+4n}{1+n}M$
Ref. [27]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+2N}{1+N}M$
Ref. [30]	2/2/1	0/2/0/2	$\frac{1+N}{1-D}$	$\frac{1}{1+N}M$	$\frac{2+3N}{1+N}M$
Ref. [32]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+4N}{1+N}M$
Ref. [33]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+4N}{1+N}M$
Ref. [34]	4/4/3	2/0/1/3	$\frac{1+n}{1-D}$	$\frac{1}{1+n}M$	$4M$
Ref. [35]	4/4/5	2/0/1/3	$\frac{2(1+n)}{1-D}$	$\frac{1}{2+2n}M$	$4M$
Ref. [36]	2/6/5	0/2/1/2	$\frac{2(1+n+\frac{N}{2})}{1-D}$	$\frac{1}{2+2n+N}M$	$\frac{6+8n+4N}{2+2n+N}M$
Ref. [37]	2/8/7	0/2/1/2	$\frac{2(1+n+N)}{1-D}$	$\frac{1}{2+2n+2N}M$	$\frac{3+4n+2N}{1+n+N}M$
Proposed converter	2/5/5	0/2/1/2	$\frac{4(1+n+\frac{N}{2})}{1-D}$	$\frac{1}{4+4n+2N}M$	$\frac{7+8n+4N}{4+4n+2N}M$

lowest voltage stress on the switches under the same turns-ratios and voltage gain. As for the voltage stresses on the diodes, it is fair to compare the total voltage stress on all the diodes, which is performed in the last column of Table 1 and depicted in Figure 8. As obvious, under the voltage gain and input voltage, the proposed converter provides the lowest total voltage stress on the diodes compared to other converters. Thus, semiconductor devices with low ON-state resistances and low-forward-voltage drops could be employed, which reduces the conduction losses and converter cost.

Among all the converters, the two converters in [36, 37] are the most similar ones to the proposed converter. Like the proposed converter, the converters in [36, 37] took advantage of an interleaved structure with two 2W CIs and one 3W BIT to achieve high

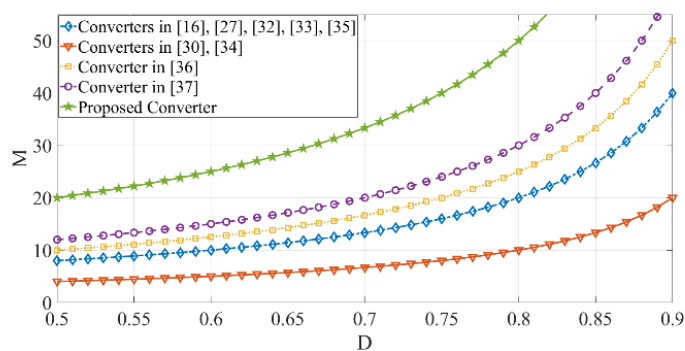


Figure 6. The voltage gain comparison for $N=n=1$.

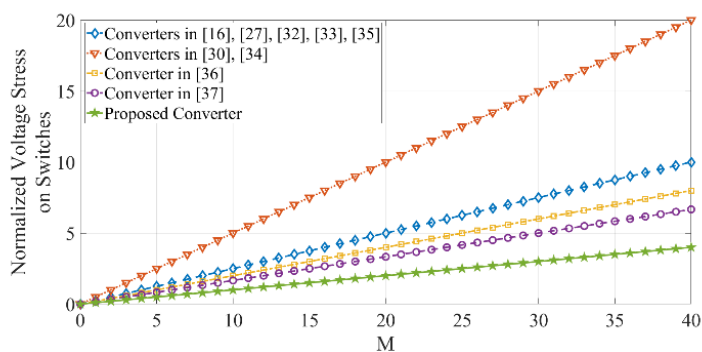


Figure 7. The comparison of the normalized voltage stress on switches for $N=n=1$.

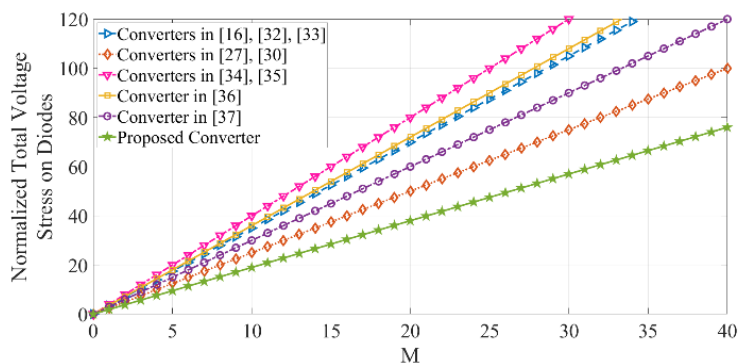


Figure 8. The comparison of the normalized total voltage stress on diodes for $N=n=1$.

voltage gains. Also, all three converters employ passive diode-capacitor clamp circuits to absorb the leakage energy of the circuit and pass it to the output to further extend the voltage gain. However, the proposed converter approximately doubles the voltage gain under the same turns- ratios and duty cycle conditions and with lower number of components compared with the converters in [36, 37]. Furthermore, for a given voltage gain with the same turns-ratios for the magnetically coupled devices, the proposed converter has a smaller duty cycle compared to the converters in [16, 27, 30, 32-37]; thus, according to (49), the proposed converter has the smallest output voltage ripple.

6. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed converter, an experimental setup was developed, as shown in Figure 9, with the specifications listed in Table 2. Ferrite cores ETD59/31/22-3C97 and ETD54/28/19-3C90 were used to implement the 2W CIs and 3W BIT, respectively. The DC resistances of the windings for 2W CIs are as $R_{p1}=R_{s1}=R_{p2}=R_{s2}=0.01 \Omega$, and for the 3W BIT, the windings' DC resistances are as $R_p=R_s=R_t=0.06 \Omega$, where R_p , R_s , and R_t represent the DC resistances of the primary, secondary, and tertiary windings, respectively.

Figures 10(a)-(h) show the experimental current and voltage waveforms for in the input voltage of 16 V and duty cycle of 0.6. According to Figure 10(a), the measured output voltage and current are 391 V and 0.5 A, respectively. As exemplified, the proposed converter achieves a high voltage of 391 V from a low input voltage of 16 V with the duty cycle of 0.6 that is not an extreme duty cycle. There is a deviation of 9 V from the ideally

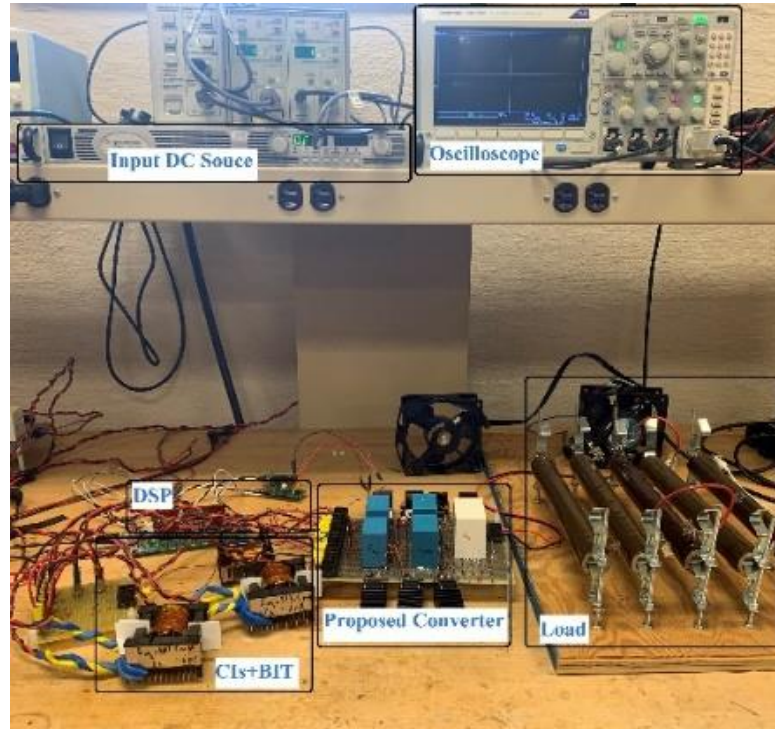


Figure 9. The experimental prototype.

Table 2. Specifications of experimental setup.

Parameters/Components	Values/Part Number
Output voltage V_o	400 V
Rated power	200 W
Switching frequency f_{sw}	50 kHz
Capacitors C_{c1} and C_{c2}	B32776G4506K000 50 μ F, $ESR=0.004 \Omega$
Capacitors C_{cm1} and C_{cm2}	B32678G4206K000 20 μ F, $ESR=0.0033 \Omega$
Capacitor C_o	C4AE0BW5200A3LJ 20 μ F, $R_C=0.0039 \Omega$
Turns-ratios N and n	1
Magnetizing inductances L_{m1} and L_{m2}	190 μ H
Leakage inductances L_{k1} and L_{k2}	1.5 μ H
Leakage inductances L_{k3}	3 μ H
Leakage inductances L_{k4} and L_{k5}	4.5 μ H
Switches Q_1 and Q_2	PSMN016-100PS $R_{DS(on)}=0.0288 \Omega$, $C_{oss}=189$ pF
Diodes D_{c1} , D_{c2} , D_{r1} , and D_{r2}	LQA06T300 $R_D=0.1 \Omega$, $V_F=0.45$ V
Output diode D_o	C3D10060A $R_D=0.17 \Omega$, $V_F=0.75$ V

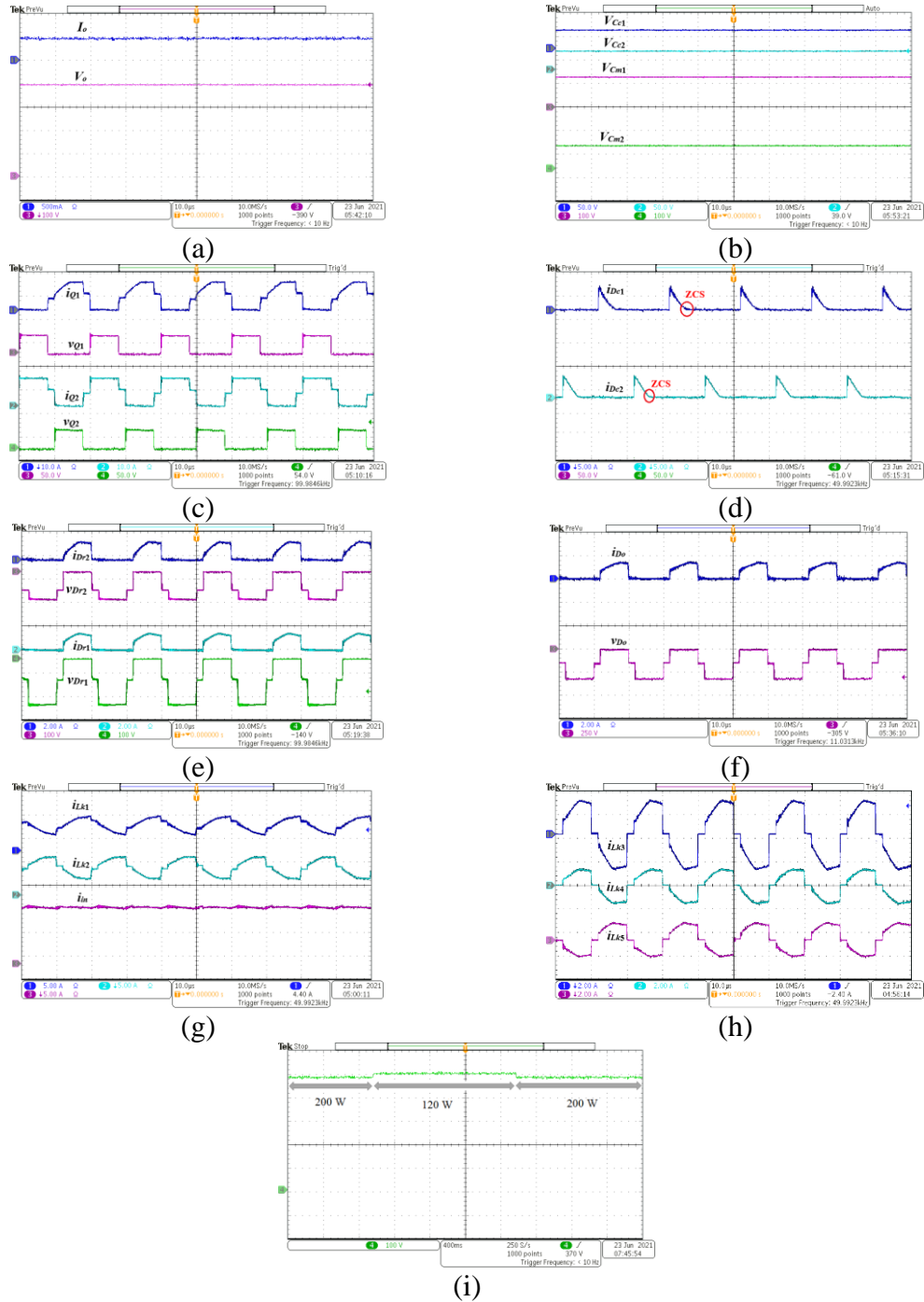


Figure 10. The experimental results under full load for $V_{in}=16\text{ V}$: (a)-(h) current and voltage waveforms; (i) dynamic response of the output voltage for the 40 % step change in the load.

calculated 400 V in (32), which is due to the parasitic elements of the circuit. Figure 10(b) illustrates the voltages across capacitors C_{c1} , C_{c2} , C_{m1} , and C_{m2} , which are relatively in agreement with the values calculated from (32), namely are $V_{C_{c1}}=V_{C_{c2}}=40$ V, $V_{C_{m1}}=136$ V, and $V_{C_{m2}}=104$ V. The semiconductors' voltages and currents are shown in Figures 10(c)-(f). As presented, the measured voltage stresses match theoretically calculated values from (36) and (39)-(41) as $V_{Q1}=V_{Q2}=40$ V, $V_{Dr1}=200$ V, $V_{Dr2}=120$ V, and $V_{Do}=320$ V. As seen, the voltage stresses across the switches are far less than the high output voltage, thus leading to adopting low-voltage-rated MOSFETs with low ON-state resistances. In addition, there is no reverse-recovery problem for the diodes because they turn off naturally with ZCS conditions. Figure 10(g) shows the input current and currents of leakage inductances L_{k1} and L_{k2} . The input current ripple is small, and that is beneficial for the input renewable energy source. The average currents of L_{k1} and L_{k2} are about 6.25 A, showing a proper current sharing between CIs in the interleaved structures, thereby resulting in the reduction of the components' current stresses. The currents of leakage inductances L_{k3} , L_{k4} , and L_{k5} are shown in Figure 10(h), and they agree with Figure 3.

In addition, the dynamic response of the output voltage for a 40% step change in the output load is depicted in Figure 10(i). The output power is changed from 200 W to 120 W and vice versa. This dynamic response illustrates the inherent stability of the proposed converter; there is a little voltage change that can be eliminated if a closed-loop control with a proper bandwidth is employed to manipulate the duty cycle of the switches for compensating the voltage change.

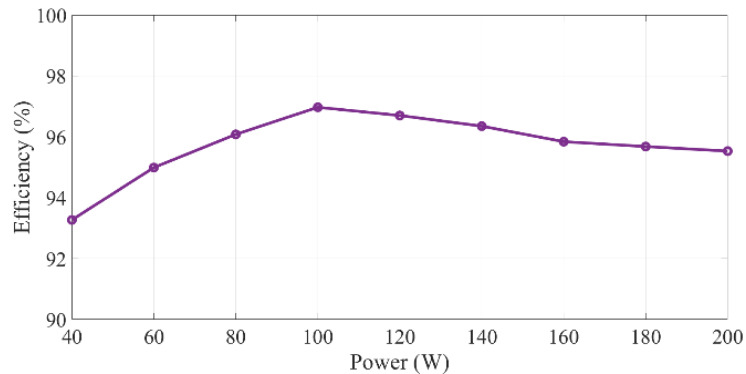


Figure 11. The measured efficiency versus the output power for the proposed converter.

Figure 11 shows the measured efficiency curve of the proposed converter for the various load powers—with the input voltage of 16 V and duty cycle of 0.6. The maximum efficiency is 96.97 % at the load of 100 W, and the full-load efficiency is 95.53 %. As seen from Figure 11, the efficiency of the proposed converter rises first and then reduces as the output power increase. The reason is that for the output power less than 100 W, the converter operates in discontinuous conduction mode (DCM); however, for output power higher than 100 W, the converter operates in CCM. In the DCM, the components' ripple currents are higher compared to the CCM, which leads to lower efficiency in comparison with CCM.

To evaluate analytical loss distribution in the components of the proposed converters, the parasitic elements of the components are considered to calculate the losses of the components, which are described below.

The losses of the switches consist of the conduction loss and switching loss, which are expressed as (50).

Due to the turn-off ZCS conditions, the reverse-recovery losses of the diodes are ignored in the loss and only their conduction losses are considered; thus, the diodes losses are expressed as (51).

$$\begin{cases} P_{Q_1} = P_{Q_1,cond} + P_{Q_1,sw} = R_{DS(on)} I_{Q_1,rms}^2 + V_{Q_1}^2 C_{oss} f_{sw} \\ P_{Q_2} = P_{Q_2,cond} + P_{Q_2,sw} = R_{DS(on)} I_{Q_2,rms}^2 + V_{Q_2}^2 C_{oss} f_{sw} \\ P_Q = P_{Q_1} + P_{Q_2} \end{cases} \quad (50)$$

$$\begin{cases} P_{D_{c1}} = R_{D_{c1}} I_{D_{c1},rms}^2 + V_{F_{D_{c1}}} I_{D_{c1},avg} \\ P_{D_{c2}} = R_{D_{c2}} I_{D_{c2},rms}^2 + V_{F_{D_{c2}}} I_{D_{c2},avg} \\ P_{D_{r1}} = R_{D_{r1}} I_{D_{r1},rms}^2 + V_{F_{D_{r1}}} I_{D_{r1},avg} \\ P_{D_{r2}} = R_{D_{r2}} I_{D_{r2},rms}^2 + V_{F_{D_{r2}}} I_{D_{r2},avg} \\ P_{D_o} = R_{D_o} I_{D_o,rms}^2 + V_{F_{D_o}} I_{D_o,avg} \\ P_D = P_{D_{c1}} + P_{D_{c2}} + P_{D_{r1}} + P_{D_{r2}} + P_{D_o} \end{cases} \quad (51)$$

The losses of the capacitors are given by (52).

$$\begin{cases} P_{C_{c1}} = R_{C_{c1}} I_{C_{c1},rms}^2 \\ P_{C_{c2}} = R_{C_{c2}} I_{C_{c2},rms}^2 \\ P_{C_{m1}} = R_{C_{m1}} I_{C_{m1},rms}^2 \\ P_{C_{m2}} = R_{C_{m2}} I_{C_{m1},rms}^2 \\ P_{C_o} = R_{C_o} I_{C_o,rms}^2 \\ P_C = P_{C_{c1}} + P_{C_{c2}} + P_{C_{m1}} + P_{C_{m2}} + P_{C_o} \end{cases} \quad (52)$$

The losses of the 2W CIs and 3W BIT are extracted by (53), where $P_{core, CI1}$, $P_{core, CI2}$, $P_{core, BIT}$ are the core losses of the 2W CIs and 3W BIT, which are extracted from the datasheets of the selected magnetic cores.

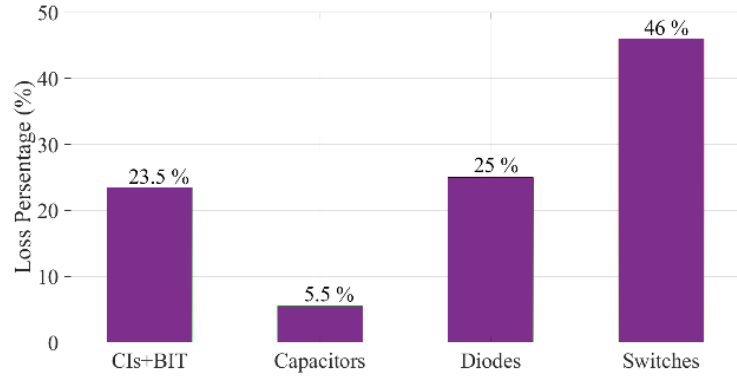


Figure 12. The analytical loss distribution of the proposed converter at full load.

$$\begin{cases} P_{CI1} = R_{p1} I_{L_{k1},rms}^2 + R_{s1} I_{L_{k4},rms}^2 + P_{core,CI1} \\ P_{CI2} = R_{p2} I_{L_{k2},rms}^2 + R_{s2} I_{L_{k5},rms}^2 + P_{core,CI2} \\ P_{BIT} = R_p I_{L_{k3},rms}^2 + R_s I_{L_{k4},rms}^2 + R_t I_{L_{k5},rms}^2 + P_{core,BIT} \\ P_{CIs+BIT} = P_{CI1} + P_{CI2} + P_{BIT} \end{cases} \quad (53)$$

The total loss of the proposed converter is given by (54).

$$P_{Loss} = P_Q + P_D + P_C + P_{CIs+BIT} \quad (54)$$

Considering (50)-(54), the analytical loss distribution in the components at full load is obtained, which shown in Figure 12; as observed, the largest losses occur in the power switches.

7. CONCLUSION

In this paper, an interleaved high step-up DC-DC converter was introduced for renewable energy applications, including the PV and fuel cells. Double 2W CIs and one 3W BIT are combined with the SC VMCs to offer increased design flexibility to adjust the voltage gain. Compared to competitors presented in literature, the proposed converter

yields the highest voltage gain and lowest voltage stresses on the switches with a low number of magnetic cores. Due to the low voltage stresses on the switches, which are provided by the passive diode-capacitor clamps, low-voltage-rated MOSFETs with low ON-state resistances are selected, which contributes to the reduction in conduction losses. Due to the interleaved structure, the input current ripple and current stresses for the components are reduced. The diodes' reverse-recovery problem is suppressed because leakage inductances of the CIs and BIT provide the diodes with turn-off ZCS conditions. The feasibility and performance of the proposed converter were validated through a 200 W experimental setup with a voltage gain of 25 and full-load efficiency of 95.53 %. The proposed converter could be utilized for the integration of PV and fuel cells onto a 400 V DC bus in the renewable energy applications.

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V. AN INTERLEAVED QUADRATIC HIGH STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTOR

Ramin Rahimi, *Student Member, IEEE*, Saeed Habibi, *Student Member, IEEE*, Mehdi Ferdowsi, *Member, IEEE*, and Pourya Shamsi, *Senior Member, IEEE*

ABSTRACT

A new high step-up DC-DC converter for renewable energy applications is proposed in this paper. Employing an interleaved quadratic structure, two two-winding coupled inductors (CIs), and voltage multiplier cells (VMCs), the proposed converter can provide high-voltage gains, continuous input current with low ripple, reduced voltage stresses on semiconductors, common ground between input and output sides, and low numbers of components. In addition, diode-capacitor lossless clamp circuits are utilized to limit the voltage stresses of the power switches and further extend the voltage gain. The operating and steady-state analyses, design considerations, and a comparison with other previously published high step-up converters are presented. Lastly, experimental results of a 400 W prototype with 400 V output voltage are illustrated to verify the theoretical analysis and the functionality of the proposed converter.

Keywords: Interleaved DC-DC converter, quadratic DC-DC converter, high step-up, renewable energy, photovoltaic (PV), fuel cell (FC), coupled inductor (CI), voltage multiplier cell (VMC).

1. INTRODUCTION

In recent decades, renewable energy sources (RESs), such as solar photovoltaic (PV) panel and fuel cell (FC), were the focal points for electricity production because they do not deplete finite fossil fuel resources and are non-polluting. However, the RESs generate a low voltage ranging from 12 to 48 V [1]; thus, they require a high step-up DC-DC converter, which provides high-voltage gains [2, 3]. Figure 1 shows how a high step-up DC-DC converter interfaces a low-voltage RES to a high-voltage DC bus (200-800 V) in a DC micro-grid. Boosting the output voltage of RESs to the voltage of DC bus can be a challenge because at high-voltage gains, conventional boost converter suffers from extreme duty cycle, high voltage stresses on the switches, and diode reverse-recovery problems [3, 4]. Thus, the development of high step-up DC-DC converters to provide high output voltages from the low voltage of RESs is an essential step toward the integration of RESs into DC micro-grids. To this point, literature presented techniques to derive high step-up topologies [5].

In general, high step-up converters are based on classical DC-DC topologies in which voltage-boosting techniques are applied to increase the voltage gain under low or medium duty cycles, reduce the voltage and current stresses on components, and achieve high efficiency [6]. Voltage-boosting techniques are based on voltage multiplier cell (VMC)—including switched inductor (SL) and switched capacitor (SC)—multilevel, cascade, quadratic, interleaved structures, coupled inductor (CI), and built-in transformer (BIT), in addition to combinations of the aforementioned. The SC technique was applied to converters in [7-9]—the main drawback of these converters was that they suffered from

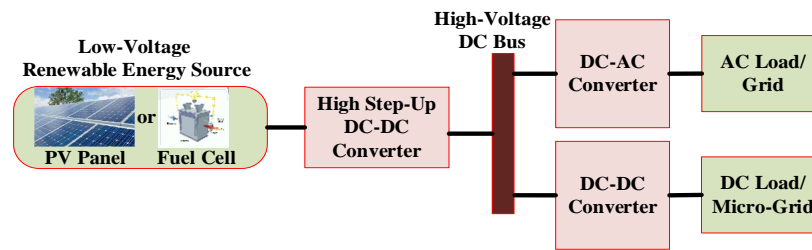


Figure 1. High step-up DC-DC converter in a DC micro-grid.

high surge current in the capacitors and increased conduction losses. The SL technique was adopted to obtain high-voltage gain in converters proposed in [10, 11]. The converters in [12-14] combined the interleaved and BIT techniques to further increase the voltage gain. For converters in [15-18], the voltage gain had quadratic dependency on the duty cycle, resulting in large gains. The CI technique was integrated with the quadratic converters in [19-23]. Using either CI or BIT, there were two degrees of freedom to adjust the voltage gains: one is the duty cycle of the power switch; another is the turn-ratio of the CI or BIT. Accordingly, the design of such converters is more flexible. Additionally, in the converters adopting the CI or BIT, a clamped circuit is required to dissipate the energy of the leakage inductance. Furthermore, the leakage inductance energy is effectively recycled to further extend the voltage gain in the high step-up converters. A clamped circuit can be either active or passive; in comparison with an active clamped circuit, the passive clamped circuit is lossless and simple without impacting the control system. Thereby, the passive lossless clamped circuit was widely employed in the high step-up converters, with either BIT or CI, to recycle the energy stored in the leakage inductance [23]. The combination of CI and interleaved techniques were adopted in the high step-up converters in [24-31]. Thanks to the interleaved structure, the input current ripple was reduced, which helped to increase the

lifetime of RESs. In addition, an interleaved structure is useful for high-power applications because the current stresses on the components are decreased significantly compared to the non-interleaved topologies. Converters in [32-34] had interleaved structure with quadratic voltage gain, while the converter proposed in [35] combined the CI, interleaved, and quadratic techniques to extend the voltage gain significantly. To summarize, all high step-up converters have VMCs composed of capacitors and diodes, along with other voltage boosting techniques.

In this paper, a new DC-DC converter is proposed to boost the voltage of the RESs. The proposed converter incorporates the interleaved, quadratic, CI, and VMC techniques to reach a high voltage gain with low voltage stresses on the semiconductor devices; thus, switches with low voltage-rating and low ON-state resistance, which reduce the conduction losses and costs, are selected. The voltage gain of the proposed converter depends on the duty cycle and turns-ratio of CI, which helps to avoid operating at extreme duty cycle to achieve a high voltage gain; the two degrees of freedom—duty cycle and turns-ratio—make the converter design more flexible. Lossless clamped circuits are used to absorb the energy of the CIs' leakage inductances, limit the voltage stress on the power switches, and further extend the voltage gain. In addition, the proposed converter has continuous input current with low ripple and low current stresses on the switches and CIs due to the use of interleaved structure, and the proposed converter has a simple structure with a common ground between the input source and output load and a low number of components. The low input current ripple of the proposed converter prolongs the lifetime of the input RES.

This paper is organized as follows: the circuit configuration of the proposed converter and its operating analysis are presented in Section 2. The steady-state circuit

performance analysis is illustrated in Section 3. The design guidelines of the proposed converter are explained in Section 4. A comprehensive comparison with other similar topologies is given in Section 5. Experimental verification of the proposed converter is outlined in Section 6, and finally, the study is concluded in Section 7.

2. CONFIGURATION AND OPERATING ANALYSIS OF THE PROPOSED CONVERTER

2.1. CONFIGURATION OF THE PROPOSED CONVERTER

Figure 2 shows the configuration of the proposed converter and its equivalent circuit. Switches Q_1 and Q_2 are commanded in an interleaved manner with the phase shift of 180° ; that is, the proposed converter has a two-phase interleaved structure. There is a CI in each phase. The CIs have primary turns of N_{p1} and N_{p2} and secondary turns of N_{s1} and N_{s2} . Each CI is modeled with an ideal transformer, a magnetizing inductance placed in the primary side, and leakage inductances placed on the primary and secondary sides. The coupling references of the CIs are represented by “●” and “*”. Parameters L_{m1} and L_{m2} denote the magnetizing inductances for the couple inductors; L_{k1} and L_{k2} represent the primary leakage inductances; L_{k3} denotes the summation leakage inductance of two CIs in the secondary sides. The secondary windings of the CIs are connected in series with the leakage inductance L_{k3} and an intermediate energy storage capacitor C_m to extend the voltage gain of the proposed converter. The diode-capacitor pairs (D_{c1}, C_{c1}) and (D_{c2}, C_{c2}) provide the clamp circuits for the power switches to recycle the leakage energy caused by the leakage inductances. Diode D_r is the regenerative diode; the output diode and capacitor

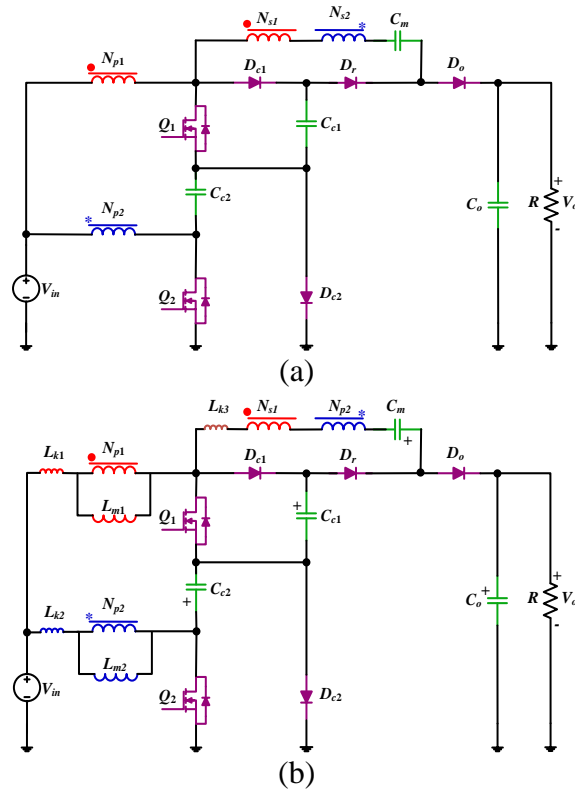


Figure 2. Proposed converter and its equivalent circuit: (a) proposed converter, (b) equivalent circuit.

are D_o and C_o , respectively; V_{in} and V_o are the input and output voltages, respectively; R is the load; $N_1=N_{s1}/N_{p1}$ and $N_2=N_{s2}/N_{p2}$ are the turns-ratios of the CIs.

2.2. OPERATING ANALYSIS OF THE PROPOSED CONVERTER

Two gate signals with the same frequencies f_{sw} and the same duty cycles D are applied to the power switches, where there is a phase shift of 180° between the gate signals. Using the steady-state analysis, 7 operation stages exist during one switching period T . Figure 3 illustrates the key current waveforms of the proposed converter. The equivalent circuits for the different operation stages are shown in Figure 4, which are:

Stage 1 [$t_0 \sim t_1$]: During this stage, both switches Q_1 and Q_2 and output diode D_o are in ON state; other diodes are reverse-biased; both CIs are energized, and their secondary windings and intermediate capacitor C_m release the energy to output capacitor C_o and load R . The key circuit relationships of this stage are as (1). The current of D_o decreases during this stage. Ignoring the current ripples of magnetizing inductances of the CIs, the output diode's current variation rate (di_{D_o}/dt) is obtained; as obvious, the output diode's current-falling rate is controlled by the leakage inductances.

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -N_1 V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k3}} = V_o + V_{C_{c2}} - V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = i_{D_o}(t) \\ V_{L_{kj}} = L_{kj} \frac{di_{L_j}}{dt} \quad (\text{for } j=1,2,3) \\ \frac{di_{D_o}(t)}{dt} = -\frac{V_o + (N_1 - N_2)V_{in} + (N_1 - 1)V_{C_{c2}} - V_{C_m}}{N_1^2 L_{k1} + N_2^2 L_{k2} + L_{k3}} \end{array} \right. \quad (1)$$

Stage 2 [$t_1 \sim t_2$]: At $t=t_1$, regenerative diode D_r turns on and output diode D_o turns off; both switches Q_1 and Q_2 remain in ON states, resulting in linear increases of the current for magnetizing inductances L_{m1} and L_{m2} ; capacitor C_m begins to charge, and the primary winding's current direction is reversed for both CIs; the energy to the load is provided by output capacitor C_o . For this stage, the key relationships as (2).

Stage 3 [$t_2 \sim t_3$]: At $t=t_2$, switch Q_2 turns off and clamp diode D_{c2} is forward-biased; accordingly, the voltage across switch Q_2 is clamped to the $V_{C_{c2}}$. The relationships for this stage are as (3).

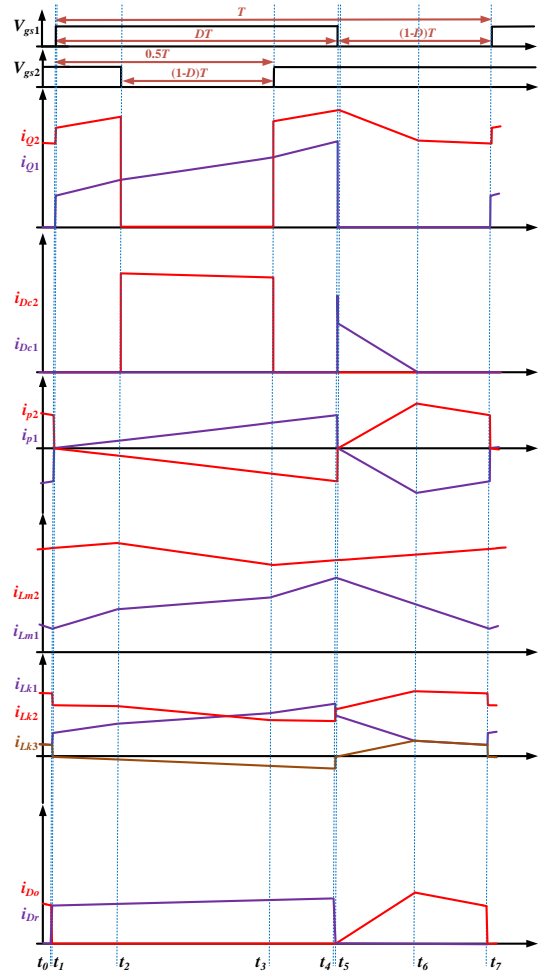


Figure 3. Key waveforms of the proposed converter.

$$\begin{cases}
 V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} \\
 V_{L_{m2}} + V_{L_{k2}} = V_{in} \\
 N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\
 i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\
 i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\
 i_{L_{k3}}(t) = -i_{D_r}(t)
 \end{cases} \quad (2)$$

Stage 4 [$t_3 \sim t_4$]: At the beginning of this operation stage, switch Q_2 turns on and clamp diode D_{c2} turns off, resulting in the relationships as (4).

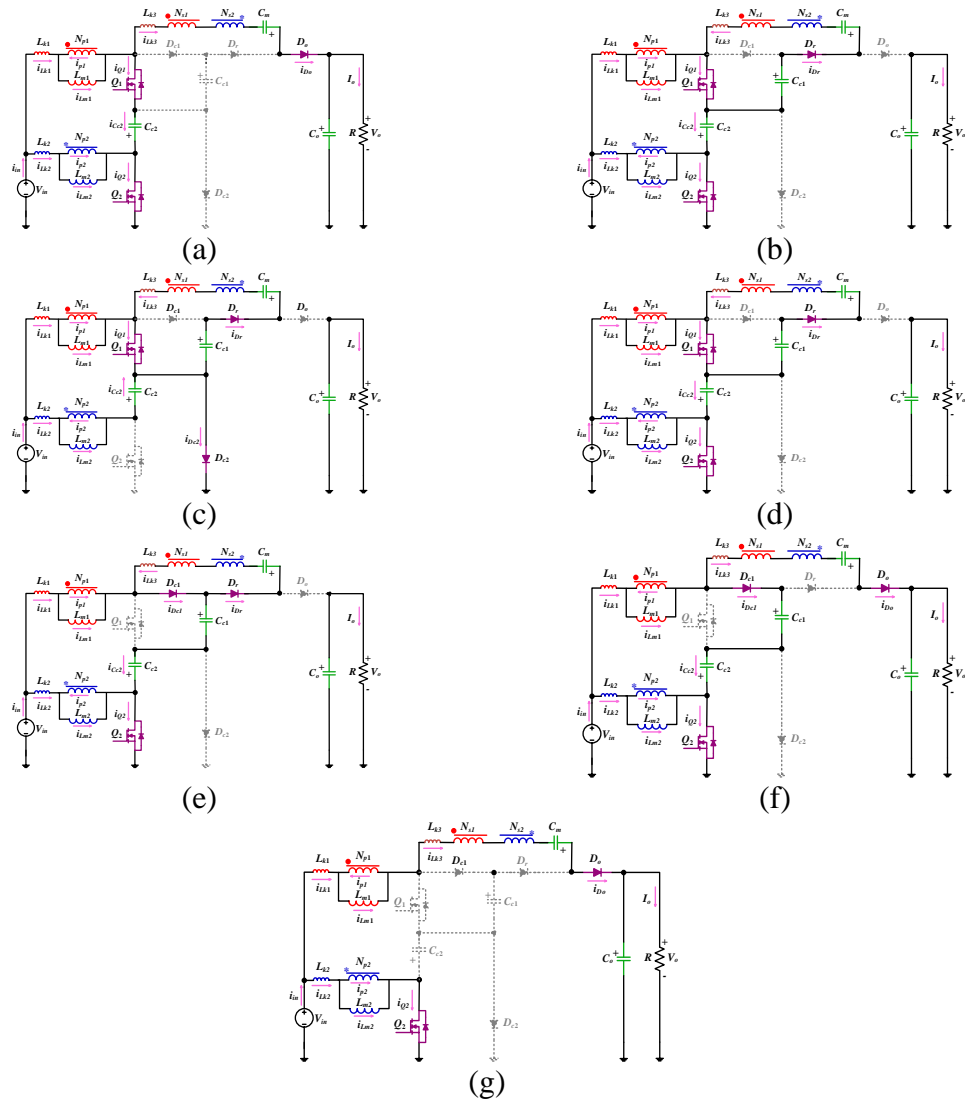


Figure 4. Operation stages in one switching period: (a) Stage 1 [t_0 - t_1]; (b) Stage 2 [t_1 - t_2]; (c) Stage 3 [t_2 - t_3]; (d) Stage 4 [t_3 - t_4]; (e) Stage 5 [t_4 - t_5]; (f) Stage 6 [t_5 - t_6]; (g) Stage 7 [t_6 - t_7].

Stage 5 [t_4 - t_5]: This stage begins when switch Q_1 turns off clamp diode D_{c1} turns on at $t=t_4$; thus, the voltage of switch Q_1 is clamped to $V_{C_{c1}}$. The current of D_r starts to decrease linearly in this stage, and the relationships are yielded as (5).

Stage 6 [t_5 - t_6]: At $t=t_5$, the regenerative diode D_r turns off; simultaneously, output diode D_o turns on and its current increases linearly, while the current of clamp diode D_{c1}

decreases linearly. The power of the load and output capacitor C_o is provided by the input source through the secondary windings of the CIs and intermediate capacitor C_m . The relationships of this stages are as (6).

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c2}}(t) = i_{L_{k1}}(t) + i_{L_{k2}}(t) - i_{L_{k3}}(t) - i_{D_r}(t) \\ \quad = i_{L_{m1}}(t) + i_{L_{m2}}(t) + (N_1 - N_2) i_{D_r}(t) \end{array} \right. \quad (3)$$

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c2}}(t) = i_{L_{k1}}(t) + i_{L_{k2}}(t) - i_{L_{k3}}(t) - i_{D_r}(t) \\ \quad = i_{L_{m1}}(t) + i_{L_{m2}}(t) + (N_1 - N_2) i_{D_r}(t) \end{array} \right. \quad (4)$$

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c1}}(t) = i_{L_{k1}}(t) - i_{L_{k3}}(t) = i_{L_{m1}}(t) + (N_1 + 1) i_{D_r}(t) \end{array} \right. \quad (5)$$

Stage 7 [$t_6 \sim t_7$]: At $t=t_6$, the current through clamp diode D_{c1} decreases to zero, and it turns off. The current of output diode D_o starts to decrease, and its decreasing rate is

controlled by the leakage inductances. Like previous stage, the input energy is continuously transferred to output capacitor C_o and the load R . The relationships of this stage are as (7).

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -N_1 V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k3}} = V_o + V_{C_{c2}} - V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = i_{D_o}(t) \\ i_{D_{c1}}(t) = i_{L_{k1}}(t) - i_{L_{k3}}(t) = i_{L_{m1}}(t) - (N_1 + 1) i_{D_o}(t) \end{array} \right. \quad (6)$$

$$\left\{ \begin{array}{l} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -(N_1 + 1) V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k1}} - V_{L_{k3}} = V_o - V_{in} - V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{k3}}(t) = i_{D_o}(t); i_{L_{m1}}(t) = (N_1 + 1) i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \end{array} \right. \quad (7)$$

3. STEADY-STATE CIRCUIT PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis of the proposed converter, the following assumptions are made:

1. The equivalent series resistance (ESR) of all passive components is neglected.
2. The voltages of all capacitors are constant throughout the whole switching period because they are assumed to be large enough.
3. The voltage drops and internal resistances of all semiconductor devices are ignored.
4. The turns-ratios of both the CIs are equal to N ; that is $N_1 = N_2 = N$.

5. Stages 1 and 5 are neglected because they are transitional modes with very short times.
6. The converter operates in continuous conduction mode (CCM).

3.1. VOLTAGE GAIN DERIVATION

By ignoring the voltage drops on the leakage inductances and applying the volt–second balance principle to the magnetizing inductances L_{m1} and L_{m2} , the voltages across capacitors C_{c1} and C_{c2} are:

$$\begin{cases} V_{C_{c1}} = \frac{1}{(1-D)^2} V_{in} \\ V_{C_{c2}} = \frac{1}{1-D} V_{in} \end{cases} \quad (8)$$

Having the voltages of the clamp capacitors, from Stage 2, the voltage of C_m is given by:

$$V_{C_m} = V_{C_{c1}} + NV_{C_{c2}} = \frac{(1-D)N + 1}{(1-D)^2} V_{in} \quad (9)$$

From Stage 6, the voltage of C_o and the voltage gain (M) of the converter can be given by:

$$\begin{cases} V_{C_o} = V_o = V_{C_m} + (N+1)(V_{C_{c1}} - V_{C_{c2}}) = \frac{1+N+D}{(1-D)^2} V_{in} \\ M = \frac{V_o}{V_{in}} = \frac{1+N+D}{(1-D)^2} \end{cases} \quad (10)$$

Figure 5 shows the plot of the voltage gain of the proposed converter. It is clear that when either duty cycle or turns-ratio increases, the voltage gain increases. Additionally, the voltage gain has a quadratic dependency on the duty cycle, providing a large gain.

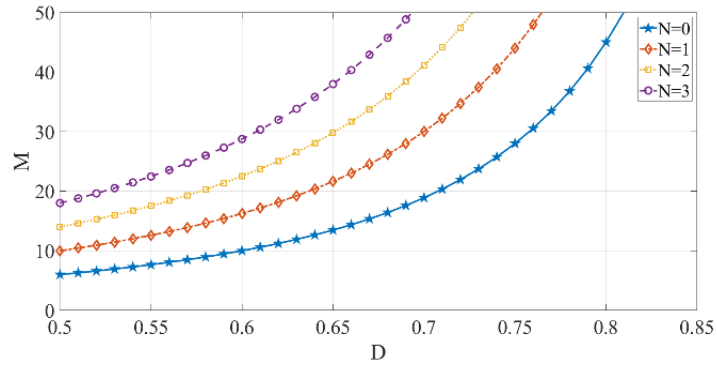


Figure 5. The voltage gain of the proposed converter versus turns-ratio N and duty cycle D .

In what follows, considering the leakage inductances of CIs, the voltage gain is obtained.

Neglecting transitional Stage 5 and considering Stage 6, the following voltage relationship is obtained:

$$V_o = (1+N)V_{C_{c1}} - (1+N)V_{C_{c2}} + V_{C_m} + NV_{L_{k1}} - NV_{L_{k2}} - V_{L_{k3}} \quad (11)$$

Ignoring the current ripples of the CIs' magnetizing inductances and voltage ripples of capacitors, (12) can be written, where kT is the time duration of Stage 6. Substituting (8), (9), and (12) in (11), in the presence of leakage inductances, the voltage gain is derived as in (13).

It is observed that the leakage inductances of the circuit lead to a slight decrease in the voltage gain; thus, the higher the leakage inductances, the lower the voltage gain.

$$\left\{ \begin{array}{l}
\Delta i_{D_o} = I_{D_o, \max} = \frac{(N+2)I_o}{(N+1)(1-D)} = \frac{(N+2)V_o}{(N+1)(1-D)R} \\
V_{L_{k1}} = L_{k1} \frac{di_{L_{k1}}}{dt} = L_{k1} \frac{d(i_{L_m} - Ni_{D_o})}{dt} = -NL_{k1} \frac{\Delta i_{D_o}}{\Delta t} \\
= -NL_{k1} \frac{I_{D_o, \max}}{kT} = -\frac{N(N+2)f_{sw}L_{k1}V_o}{k(N+1)(1-D)R} \\
V_{L_{k2}} = L_{k2} \frac{di_{L_{k2}}}{dt} = L_{k2} \frac{d(i_{L_m} + Ni_{D_o})}{dt} = NL_{k2} \frac{\Delta i_{D_o}}{\Delta t} \\
= NL_{k2} \frac{I_{D_o, \max}}{kT} = \frac{N(N+2)f_{sw}L_{k2}V_o}{k(N+1)(1-D)R} \\
V_{L_{k3}} = L_{k3} \frac{di_{L_{k3}}}{dt} = L_{k3} \frac{di_{D_o}}{dt} = L_{k3} \frac{\Delta i_{D_o}}{\Delta t} \\
= L_{k3} \frac{I_{D_o, \max}}{kT} = \frac{(N+2)f_{sw}L_{k3}V_o}{k(N+1)(1-D)R}
\end{array} \right. \quad (12)$$

$$M = \frac{V_o}{V_{in}} = \frac{1+N+D}{(1-D)^2 + \frac{f_{sw}(N+2)(1-D)(N^2(L_{k1}+L_{k2})+L_{k3})}{k(N+1)R}} \quad (13)$$

3.2. VOLTAGE STRESS ON SEMICONDUCTOR DEVICES

The maximum voltage stresses of the semiconductor devices are obtained from

(14).

$$\left\{ \begin{array}{l}
V_{Q_1} = V_{D_{c1}} = V_{C_{c1}} = \frac{1}{(1-D)^2} V_{in} = \frac{1}{1+N+D} V_o \\
V_{Q_2} = V_{D_{c2}} = V_{C_{c2}} = \frac{1}{1-D} V_{in} = \frac{1-D}{1+N+D} V_o \\
V_{D_r} = V_{D_o} = V_o + V_{C_{c2}} - V_{C_{c1}} = \frac{1+N}{(1-D)^2} V_{in} = \frac{1+N}{1+N+D} V_o
\end{array} \right. \quad (14)$$

Figure 6 shows the normalized voltage stresses of the semiconductor devices for the sample duty cycle of 0.65; the voltages are normalized to the output voltage. It is observed that as N increases, the voltage stresses on the switches and clamp diodes decrease

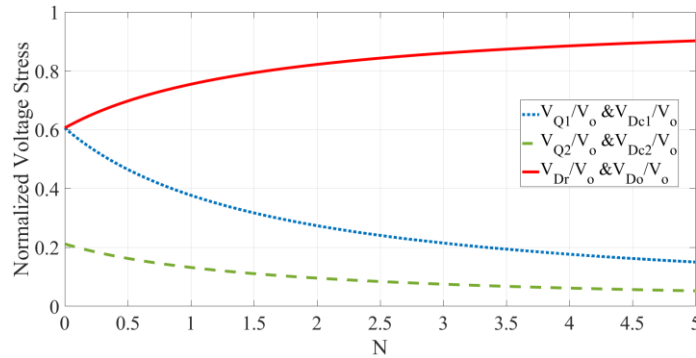


Figure 6. The normalized voltage stresses of switches and diodes versus turns-ratio N for $D=0.65$.

and voltage stresses on the regenerative and output diodes increase, but they are always lower than the output voltage.

3.3. CURRENT STRESS OF SEMICONDUCTOR DEVICES

By applying the amp-second balance principle to the capacitors, the average currents of the capacitors for the main operating Stages 2, 3, 4, 6, and 7 are obtained. It is worth noting that the average currents of the capacitors for the entire switching cycle are zero; however, for an individual stage, they may not be zero. Then, using the average currents of the capacitors for stages, the average currents of the CIs' magnetizing inductances as well as the maximum currents of the semiconductors are extracted. It must be noted that the equivalent average currents of the semiconductors during their ON states (not entire switching period) are considered as the maximum current stresses of the semiconductors in this paper. The current relationships are as:

$$\begin{cases} I_{Lm1} = \frac{2+N}{1-D} I_o \\ I_{Lm2} = \frac{(3+N)D-1}{(1-D)^2} I_o \end{cases} \quad (15)$$

$$\begin{cases} I_{Dc1_avg} = I_{Dr_avg} = I_{Dco_avg} = I_o; \quad I_{Dc2_avg} = \frac{1+N+D}{1-D} I_o \\ I_{Q1_avg} = I_{Lm1} = \frac{2+N}{1-D} I_o; \quad I_{Q2_avg} = I_{Lm2} = \frac{(3+N)D-1}{(1-D)^2} I_o \end{cases} \quad (16)$$

$$\begin{cases} I_{Dc1_max} = \frac{1}{k} I_o; \quad I_{Dc2_max} = \frac{1+N+D}{(1-D)^2} I_o \\ I_{Dr_max} = \frac{2N}{(1+N)(1-D)} I_o \\ I_{Do_max} = \frac{2+N}{(1+N)(1-D)} I_o \\ I_{Q1_max} = \frac{2+3N}{1-D} I_o; \quad I_{Q2_max} = \frac{1+N+D}{(1-D)^2} I_o \end{cases} \quad (17)$$

The root-mean-squared (RMS) current stresses of the switches are as (18).

$$\begin{cases} I_{Q1_RMS} = \frac{N+1}{(1-D)\sqrt{D}} I_o \\ I_{Q2_RMS} = \frac{(3+N)D-1}{(1-D)^2\sqrt{D}} I_o \end{cases} \quad (18)$$

4. DESIGN CONSIDERATIONS

4.1. COUPLED INDUCTOR DESIGN

If the required voltage gain and the duty cycle are provided, the turns-ratio of the CIs is:

$$N = M(1-D)^2 - (1+D) \quad (19)$$

Assuming the maximum current ripple of $x\%$, the magnetizing inductances are determined. Considering Stages 6 and 7 in which switch Q_1 is in OFF state and the current of the magnetizing inductance L_{m1} is falling from the maximum to the minimum value, L_{m1} is obtained by using:

$$\begin{cases} \Delta i_{L_{m1_max}} = x\% I_{L_{m1}} \\ I_{L_{m1}} = \frac{2+N}{1-D} I_o \\ V_{L_{m1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} = \frac{(1-D)(2-D)-1}{(1-D)^2} V_{in} \\ L_{m1} \geq \frac{|V_{L_{m1}}|(1-D)}{f_{sw} \Delta i_{L_{m1_max}}} = \frac{(1-(1-D)(2-D))V_{in}}{(2+N)x\% I_o f_{sw}} \end{cases} \quad (20)$$

For the design of magnetizing inductance L_{m2} , Stage 2 is considered and L_{m2} is calculated as:

$$\begin{cases} \Delta i_{L_{m2_max}} = x\% I_{L_{m2}} \\ I_{L_{m2}} = \frac{(3+N)D-1}{(1-D)^2} I_o \\ V_{L_{m2}} = V_{in} - V_{C_{c2}} = \frac{-D}{1-D} V_{in} \\ L_{m2} \geq \frac{|V_{L_{m2}}|(1-D)}{f_{sw} \Delta i_{L_{m2_max}}} = \frac{D(1-D)^2 V_{in}}{((3+N)D-1)x\% I_o f_{sw}} \end{cases} \quad (21)$$

As for the leakage inductance of the CIs, it must not be too large because it decreases the voltage gain of the converter.

4.2. CAPACITORS DESIGN

The rated voltages of the capacitors were determined from (8)-(10). By applying the amp-balance law to the capacitors, their average currents could be determined for all the operation stages. For Stage 3, the average currents of the capacitors are given by (22).

Then, by considering the maximum voltage ripple of $y\%$, the capacitances can be calculated from (23).

$$\begin{cases} I_{C_{c1}} = -\frac{N}{(N+1)(1-D)} I_o \\ I_{C_{c2}} = \frac{(N^2 + 5N + 3)D - (2N + 1)}{(N+1)(1-D)^2} I_o \\ I_{C_m} = \frac{N}{(N+1)(1-D)} I_o \\ I_{C_o} = -I_o \end{cases} \quad (22)$$

$$\begin{cases} C_{c1} \geq \frac{(1-D)|I_{C_{c1}}|}{y\%V_{C_{c1}}f_{sw}} = \frac{N(1+N+D)}{y\%(N+1)f_{sw}R} \\ C_{c2} \geq \frac{(1-D)I_{C_{c2}}}{y\%V_{C_{c2}}f_{sw}} = \frac{(1+N+D)((N^2 + 5N + 3)D - (2N + 1))}{y\%(N+1)(1-D)^2 f_{sw}R} \\ C_m \geq \frac{(1-D)I_{C_m}}{y\%V_{C_m}f_{sw}} = \frac{N(1+N+D)}{y\%(N+1)(2+(1-D)N)f_{sw}R} \\ C_o \geq \frac{(1-D)|I_{C_o}|}{y\%V_{C_o}f_{sw}} = \frac{1-D}{y\%f_{sw}R} \end{cases} \quad (23)$$

4.3. SEMICONDUCTORS SELECTION

From (14) and (16)-(18), the voltage and current stresses of semiconductors were calculated, which provided an estimation for the voltage and current ratings of the switches and diodes. To consider the effect of the parasitic elements and to make sure that the semiconductors always operate within the safe operating area, the voltage and current ratings of the selected semiconductors must be higher than the calculated values.

5. CIRCUIT PERFORMANCE COMPARISON

As established from (10), the voltage gain of the proposed converter is a quadratic function of the duty cycle, leading to extended significant voltage gains. The voltage gain is adjustable with two parameters: duty cycle (D) of the switches and turns-ratio (N) of the CIs; these two degrees of freedom make the design of the converter more flexible. In addition, the proposed converter has an interleaved structure that leads to a low input current ripple and low current stresses of the components. Thus, it was helpful to compare the proposed converter with two categories of existing high step-up converters: 1) non-interleaved quadratic converters, including both non-CI-based topologies in [16-18] and CI-based structures in [19-23]; 2) interleaved converters, including both non-quadratic converters in [24-31] and quadratic topologies in [32-35]. Thus, the proposed converter is compared to 20 existing converters in the literature to cover all aspects of comparison; 12 of them are quadratic high step-up converters and the rest is non-quadratic. Such a comparison is made in Table 1. The curves of the voltage gain using the same turns-ratio (if applicable) are sketched in Figure 7, where $N=1$ is used as the comparative reference. Furthermore, the voltage gain values of all converters are calculated for the example case of $N=1$ and $D=0.7$, listed in the second column from the last of Table 1. The voltage gains of the quadratic converters in [16-18] are adjusted only by duty cycle, which are not high enough compared to the proposed converter. In addition, the converters in [16-18] lack the interleaved configuration that is useful for renewable energy applications where a low input current ripple is required. Considering the CI-based quadratic converters in [19-23], the voltage gain of the converter in [23] is higher than the proposed converter, but it has two

additional components. The voltage gain of the converter in [21] is slightly higher than the proposed converter, but the difference is not significant, and it does not have the interleaved configuration that is essential to reduce the input current ripple. Although the converter in [20] has the same voltage gain as the proposed converter, it has two more components and is lack of the interleaved structure. Other non-interleaved CI-based quadratic converters have lower voltage gains than the proposed converter. Among the interleaved converters in [24-35], only the CI-based interleaved converter in [35] has higher voltage gain than the proposed converter; however, it has six more components with the three-winding CIs. The proposed converter has the best voltage-boosting capability with highest voltage gain compared to the other quadratic or non-quadratic interleaved converters in [24-34]. In addition, Figure 8 shows the comparison of the maximum normalized voltage stress on the switches for $N=1$. It is obvious that the proposed converter has lower maximum voltage stress on the switches compared to the converters in [16-19, 22, 32-34]. Moreover, Figure 9 depicts the comparison of the normalized voltage stress on the output diode for $N=1$; as seen, like many other high step-up DC-DC converters, the voltage stress of the output diode is lower than the output voltage. Thus, the proposed converter has a low number of the components with low voltage stresses on the semiconductors, resulting in selecting low voltage-rated switches and diodes with low ON-state resistances that causes the reduction in the conduction losses. Furthermore, according to the last column of Table 1, unlike some converters in the literature, the input and output sides of the proposed converter share the common ground that increases the reliability. Overall, the proposed converter stands out from the prior works as a suitable candidate for RE applications because it has a high voltage gain, an interleaved structure with low input current ripple, high reliability, low

Table 1. Comparison of the presented DC–DC converter with several other similar topologies.

Topology	Number of Components						Normalized voltage stresses on switches ($\frac{V_{os}}{V_o}$)	Normalized voltage stress on output diode ($\frac{V_{D_o}}{V_o}$)	Voltage gain ($M = \frac{V_o}{V_i}$)	Voltage gain for D=0.7 and N=1 (if applicable)	Common ground for input and output	
	S	D	C	CI	L	Total						
Non-Interleaved Quadratic Converters	[16]	2	2	2	0	2	8	$\frac{1}{D(2-D)}$ $\frac{1-D}{D(2-D)}$	$\frac{1}{D(2-D)}$	$\frac{D(2-D)}{(1-D)^2}$	10.10	NO
	[17]	1	4	3	0	2	10	$\frac{1}{2-D}$	$\frac{1}{2-D}$	$\frac{2-D}{(1-D)^2}$	14.44	YES
	[18]	2	3	3	0	2	10	$\frac{1+D}{2D}$ $\frac{1-D}{2D}$	$\frac{1+D}{2D}$	$\frac{2D}{(1-D)^2}$	15.55	NO
	[19]	1	4	3	1	1	10	$\frac{1}{DN+1}$	$\frac{N}{DN+1}$	$\frac{DN+1}{(1-D)^2}$	18.88	YES
	[20]	1	6	5	1	1	14	$\frac{2+D(N-1)}{N(3D+2)+(2-D)}$	$\frac{2N}{N(3D+2)+(2-D)}$	$\frac{N(3D+2)+(2-D)}{2(1-D)^2}$	30	YES
	[21]	1	5	4	1	1	12	$\frac{1}{N+2}$	$\frac{N+1}{N+2}$	$\frac{N+2}{(1-D)^2}$	33.33	YES
	[22]	1	5	4	1	1	12	$\frac{1}{N+1}$	$\frac{2N-2ND}{N+1}$	$\frac{N+1}{(1-D)^2}$	22.22	YES
	[23]	1	6	5	1	1	14	$\frac{1}{N+ND+2}$	$\frac{N+1}{N+ND+2}$	$\frac{N+ND+2}{(1-D)^2}$	41.11	YES
Interleaved Non-Quadratic and Quadratic Converters	[24]	2	4	4	2	0	12	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	$\frac{2N+4}{1-D}$	20	YES
	[25]	4	2	3	2	0	11	$\frac{1}{2N+2}$	$\frac{2N+1}{2N+2}$	$\frac{2N+2}{1-D}$	13.33	YES
	[26]	2	7	7	2	0	18	$\frac{1}{2N+2}$	$\frac{2}{2N+2}$	$\frac{2N+2}{1-D}$	13.33	NO
	[27]	2	4	4	2	0	12	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	$\frac{2N+4}{1-D}$	20	YES
	[28]	2	6	6	2	0	16	$\frac{1}{2N+4}$	$\frac{2N}{2N+4}$	$\frac{2N+4}{1-D}$	20	NO
	[29]	2	4	3	2	0	11	$\frac{1}{2N+1}$	$\frac{2N}{2N+1}$	$\frac{2N+1}{1-D}$	10	YES
	[30]	4	4	5	2	0	15	$\frac{1}{4N+2}$	$\frac{1}{2}$	$\frac{4N+2}{1-D}$	20	NO
	[31]	2	5	4	2	0	13	$\frac{1}{3N+1}$	$\frac{2N}{3N+1}$	$\frac{3N+1}{1-D}$	13.33	YES
	[32]	2	6	3	0	4	15	1	1	$\frac{1}{(1-D)^2}$	11.11	YES
	[33]	2	6	4	0	4	16	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{2}{(1-D)^2}$	22.22	YES
	[34]	2	6	4	2	0	14	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{2}{(1-D)^2}$	22.22	YES
	[35]	2	8	6	2	0	18	$\frac{1}{2N+2}$	$\frac{2}{2N+2}$	$\frac{2N+2}{(1-D)^2}$	44.44	YES
Proposed converter	2	4	4	2	0	12	$\frac{1}{1+N+D}$ $\frac{1-D}{1+N+D}$	$\frac{1+N}{1+N+D}$	$\frac{1+N+D}{(1-D)^2}$	30	YES	

(S=switch, D=diode, C=capacitor, CI=coupled inductor, L=simple inductor, T=total number of components)

voltage stresses on the semiconductors, and simple structure with a low number of components.

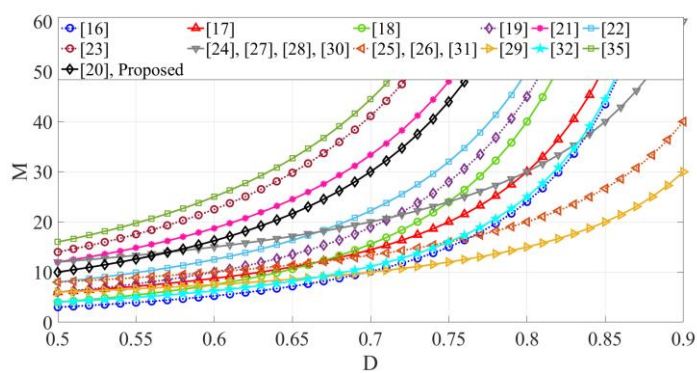


Figure 7. The voltage gain comparison for $N=1$.

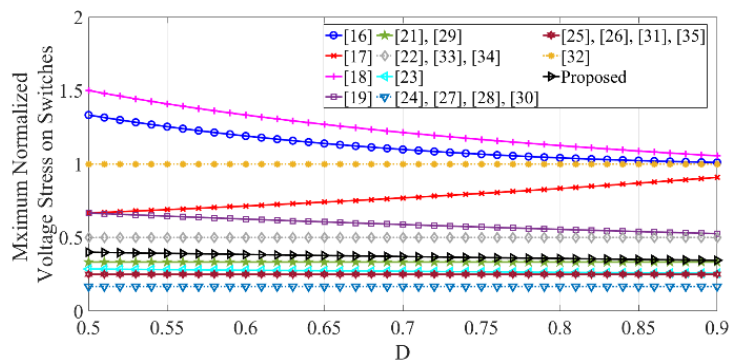


Figure 8. Comparison of the maximum normalized voltage stress of switches for $N=1$.

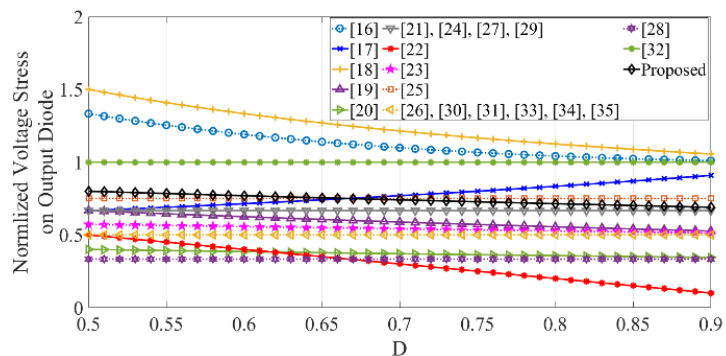


Figure 9. Comparison of the normalized voltage stress of output diode for $N=1$.

6. EXPERIMENTAL RESULTS

Considering the design of Section IV, a 400 W laboratory prototype, as shown in Figure 10, is implemented to verify the theoretical analysis and the effectiveness of the proposed converter. Assuming the maximum current ripple of 25 % for the CIs' magnetizing inductances and maximum voltage ripple of 2 % for the capacitors for $N=1$, $V_{in}=25$ V, and $V_o=400$ V, the required inductances and capacitances are as: $L_{m1} \geq 293.6$ μ H, $L_{m2} \geq 136$ μ H, $C_{c1} \geq 1.3$ μ F, $C_{c2} \geq 49$ μ F, $C_m \geq 20$ μ F, and $C_o \geq 1$ μ F. The selected components and specifications of the experimental setup are listed in Table 2.

Figures 11-18 illustrate the experimental voltage and current waveforms of the proposed converter for the input voltage of 25 V. To achieve the output voltage of 400 V, the switches operate at the equal duty cycle of 0.597 but 180° out of phase; the gate pulses of the MOSFETs are generated by the TMS320F28335 microcontroller. Figure 11 illustrates the voltages across the capacitors; the experimental results of $V_{C_{c1}}=145$ V, $V_{C_{c2}}=60$ V, $V_{C_m}=206$ V, and $V_o=V_{C_o}=381$ V are close enough to the theoretical results that are as: $V_{C_{c1}}=154$ V, $V_{C_{c2}}=62$ V, $V_{C_m}=216$ V, and $V_o=V_{C_o}=400$ V. Figures 12-14 demonstrate the input current and the currents of magnetizing and leakage inductances of the CIs. As observed, currents i_{Lk1} and i_{Lk2} (similarly currents i_{Lm1} and i_{Lm2}) are 180° out of phase from each other, which verifies the interleaved operation of the proposed converter. Also, due to interleaved operation of proposed converter, the input current has a small ripple, which helps for the long lifetime of the input RES. Note that it is not possible to directly measure the magnetizing inductances' currents i_{Lm1} and i_{Lm2} ; however, since the turns-ratios of the CIs are unity (i.e., $N=1$), currents i_{p1} and i_{p2} are equal to $-i_{Lk3}$ and $+i_{Lk3}$, respectively.

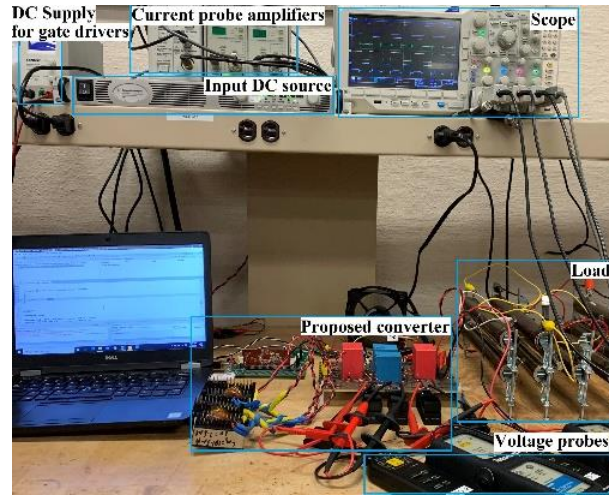
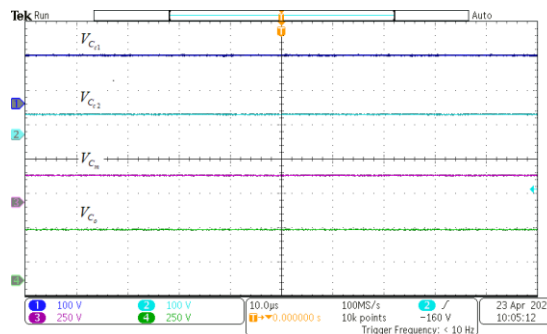


Figure 10. Experimental setup.

Table 2. Specifications of the experimental setup.

Parameters	Values/Part number
Rated Power	400 W
f_{sw}	50 kHz
Capacitors C_m, C_o	DCP4L052007GD4KSSD (20 μ F, $R_{Cm}=R_{Co}=6.25$ m Ω)
Capacitor C_{c1}	B32678G4206K000 (20 μ F, $R_{C_{c1}}=3.3$ m Ω)
Capacitor C_{c2}	B32776G4506K000 (50 μ F, $R_{C_{c2}}=4$ m Ω)
Switch Q_1	FDH44N50 ($R_{DS(on)}=110$ m Ω , $C_{oss}=645$ pF, $t_{on}=100$ ns, $t_{off}=124$ ns)
Switch Q_2	IRFP4668PBF ($R_{DS(on)}=8$ m Ω , $C_{oss}=810$ pF, $t_{on}=146$ ns, $t_{off}=138$ ns)
Diodes D_{c1}, D_r, D_o	VS-ETL1506-M3 ($V_{F0, D_{c1}}=V_{F0, D_r}=V_{F0, D_o}=0.6$ V, $R_{on, D_{c1}}=R_{on, D_r}=R_{on, D_o}=17$ m Ω)
Diode D_{c2}	APT60S20BG ($V_{F0, D_{c2}}=0.3$ V, $R_{on, D_{c2}}=7$ m Ω)
CI's	Core: ETD59/31/22-3C97 ($N=1$, $L_{m1}=314$, $L_{m2}=191$ μ H, $L_{k1}=1.5$, $L_{k2}=1$, $L_{k3}=3.5$ μ H, $R_{p1}=R_{s1}=30$ m Ω , $R_{p2}=R_{s2}=20$ m Ω)

Figure 11. Voltages of capacitors C_{c1} (CH1), C_{c2} (CH2), C_m (CH3), and C_o (CH4).

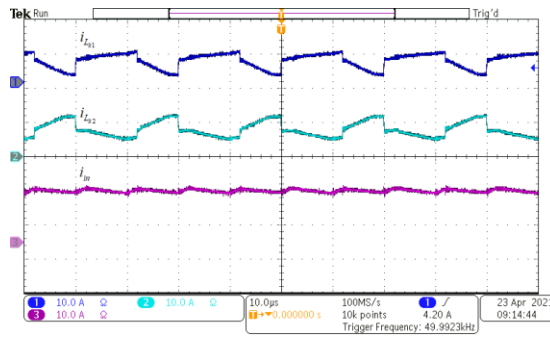


Figure 12. Currents i_{Lk1} (CH1) and i_{Lk2} (CH2) along with input current (CH3).

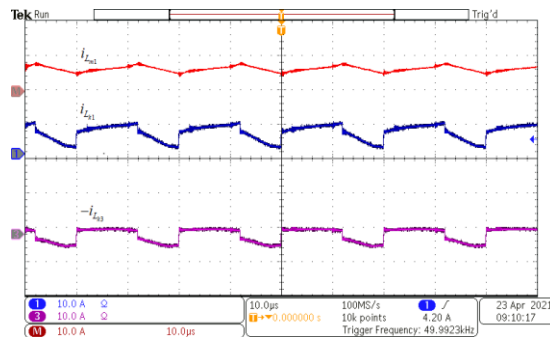


Figure 13. Currents i_{Lk1} (CH1) and $-i_{Lk3}$ (CH3) along with current i_{Lm1} (Math).

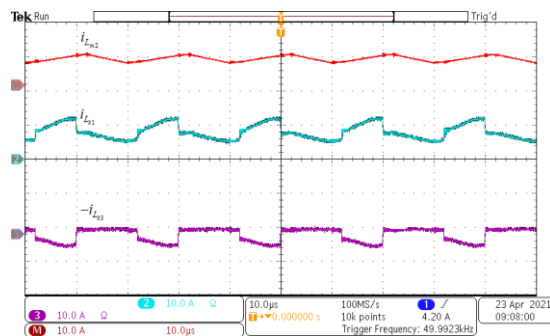


Figure 14. Currents i_{Lk2} (CH2) and $-i_{Lk3}$ (CH3) along with current i_{Lm2} (Math).

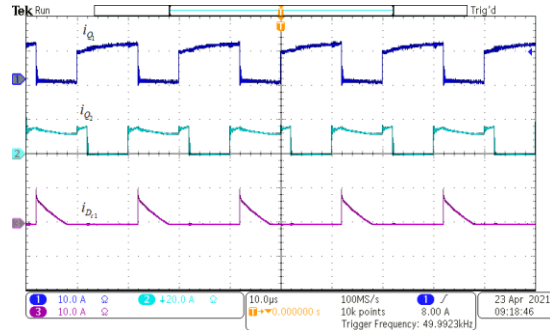


Figure 15. Currents of switches Q_1 (CH1) and Q_2 (CH2) and diode D_{c1} (CH3).

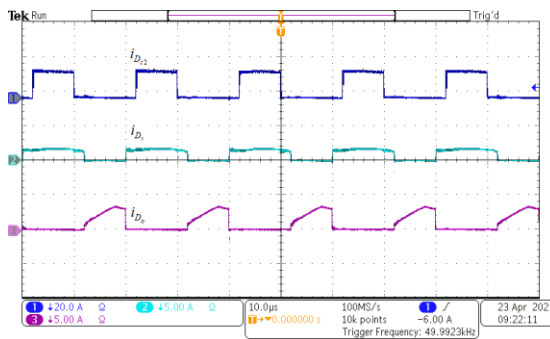


Figure 16. Currents of diodes D_{c2} (CH1), D_r (CH2), and D_o (CH3).

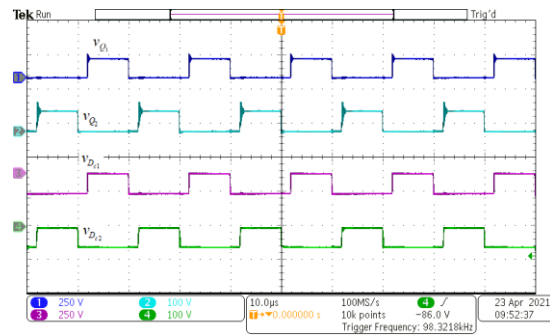


Figure 17. Voltages of switches Q_1 (CH1) and Q_2 (CH2) and diodes D_{c1} (CH3) and D_{c2} (CH4).

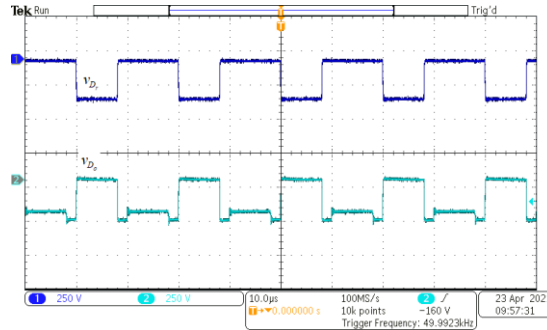


Figure 18. Voltages of diodes D_r (CH1) and D_o (CH2).

Accordingly, as shown in Figures 13 and 14, Math Channel of the oscilloscope is used to extract i_{Lm1} and i_{Lm2} from $i_{Lm1}=i_{Lk1}+i_{Lk3}$ and $i_{Lm2}=i_{Lk2}-i_{Lk3}$, respectively. The currents of switches Q_1 and Q_2 , as well as the currents of diodes D_{c1} , D_{c2} , D_r , and D_o are shown in Figures 15 and 16. Moreover, as observed in Figures 13-16, all the currents of inductances and semiconductor devices are consistent with the key waveforms of Figure 3. The voltages of the switches and diodes are depicted in Figures 17 and 18, where the approximate voltage stresses of $V_{Q1}=V_{Dc1}=154$ V, $V_{Q2}=V_{Dc2}=62$ V, and $V_{Dr}=V_{Do}=308$ V are observed, validating (14). As seen, the voltage stresses of the power switches are far less than the output voltage that enables the designers to select low-voltage-rating MOSFETs with low ON-state resistance, which contributes to improving the converter's efficiency.

Figure 19 shows the measured efficiency at input voltage values of 25 V and 40 V for the same output voltage of 400 V; the proposed converter operates at the different duty cycles of 0.597 and 0.5 for input voltages of 25 V and 40 V, respectively. At the full load, the efficiency is 92.3% and 94.4 % for the input voltages of 25 V (with $M=16$) and 40 V (with $M=10$), respectively. The full-load efficiency of the proposed converter is compared to other CI-based quadratic converters in Table 3. Furthermore, using the loss analysis presented in [36], the analytical power loss distribution of the proposed is obtained;

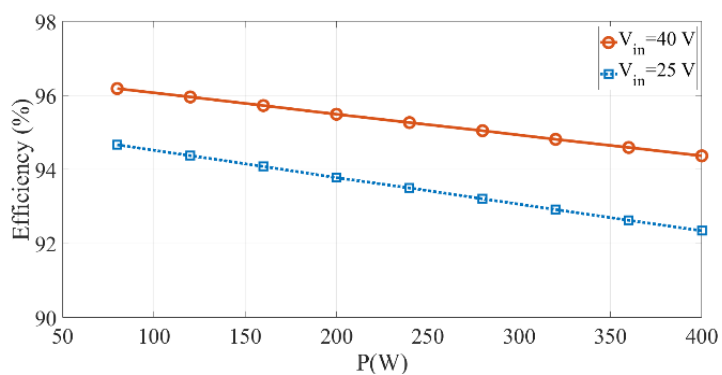


Figure 19. The measured efficiency of the proposed converter versus the power for the input voltages of 25 V and 40 V.

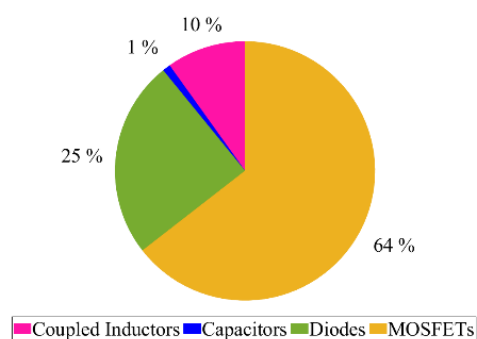


Figure 20. The analytical power loss distribution of the proposed converter at full load for $V_{in}=25$ V.

Figure 20 shows the analytical loss distribution of the proposed converter at 400 W for the input voltage of 25 V. The MOSFETs, diodes, coupled inductors, and capacitors have the power losses of 19.6 W, 7.5 W, 3 W, and 0.3 W, respectively. So, the MOSFETs have dominant power losses with 64 %.

Table 3. Full-load efficiency comparison of proposed converter with other CI-Based quadratic converters.

Topology	Parameters	Full-load efficiency
[19]	$V_{in}=40$ V, $V_o=400$ V, $f_{sw}=40$ kHz, $P_{rated}=280$ W	93.3 %
[20]	$V_{in}=24$ V, $V_o=400$ V, $f_{sw}=50$ kHz, $P_{rated}=250$ W	93.96 %
[21]	$V_{in}=32$ V, $V_o=380$ V, $f_{sw}=40$ kHz, $P_{rated}=500$ W	91.1 %
[22]	$V_{in}=20$ V, $V_o=400$ V, $f_{sw}=50$ kHz, $P_{rated}=200$ W	89.5 %
[23]	$V_{in}=30$ V, $V_o=400$ V, $f_{sw}=50$ kHz, $P_{rated}=300$ W	92.2 %
[35]	$V_{in}=18$ V, $V_o=380$ V, $f_{sw}=50$ kHz, $P_{rated}=150$ W	95 %
Proposed converter	$V_{in}=40$ V, $V_o=400$ V, $f_{sw}=50$ kHz, $P_{rated}=400$ W	94.4 %

7. CONCLUSION

In this paper, a new high step-up DC-DC converter was proposed for renewable energy applications. A pair of two-winding CIs and SC-based VMCs were employed in an interleaved quadratic structure. Additionally, diode-capacitor based clamp circuitries were used to limit the switches' voltage stresses, recycle the leakage inductances' energies, and further increase the voltage gain. The high-voltage gain, continuous input current with low ripple, low voltage stresses on the semiconductors, and simple structure are the primary merits of the proposed converter. The operating principles, steady-state analysis, and design considerations were presented. To justify the merits of the proposed converter, its

key indicators were compared with other high-voltage gain converters found in the literature. The theoretical operation and analysis of the proposed converter were validated by the experimental results of a 400 W prototype with a voltage gain of 16. The efficiency is found to be 92.3 % and 94.4 % for the voltage gains of 16 and 10 at the full load. The presented results verified that the proposed converter is a promising candidate for renewable energy applications.

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SECTION

2. CONCLUSIONS

In this dissertation, using various combinations of VB techniques, several advanced high step-up DC-DC converters were proposed that are suitable for the integration of low-voltage solar PV panels and FC stacks into a high-voltage DC bus in renewable energy applications.

In the first paper, two three-winding CIs were combined with SC-based VM cells to propose an interleaved high step-up DC-DC converter with desirable characteristics such as high voltage gain, low voltage stresses on the semiconductors, low current stresses of the components, low input current ripple, and alleviation of the reverse-recovery problem of the diodes. A 400-W prototype was built to validate the performance and theoretical calculations of the proposed converter with an output voltage of 400 V. The full-load experimental efficiency was measured as 94.05 % for a voltage gain of 20. In the second paper, using a three-winding CI in a dual-switch structure, an advanced high step-up DC-DC converter was obtained, which can achieve a high voltage gain without applying a high duty cycle to the switches. The experimental results of a 200-W prototype with the output voltage of 400 V and two different voltage gains of 20 and 11.6 were presented to verify the theoretical calculations and analyses. In the third paper, three ZS-based high step-up DC-DC converters, named PAS-SCZSC, NAS-SCZSC, and S-SCZSC, were introduced that are based on the integration of the conventional ZS network with SC-based VM cells. The feasibility of the proposed S-SCZSC and analytical results were verified by the

experimental results of a 400-W prototype with a voltage gain of 20, which converts the input voltage of 20 V to the output voltage of 400 V. In the fourth paper, an interleaved high step-up DC-DC converter was presented, which is based on the integration of two double-winding CIs and one three-winding BIT with the SC-based VM cells. The performance of the proposed converter was confirmed by a 200-W prototype with a voltage gain of 25 and full-load efficiency of 95.53 % at an output voltage of 400 V. In the fifth paper, an advanced high step-up DC-DC converter was developed, which has an interleaved quadratic structure combined with two double-winding CIs and SC-based VM cells. The theoretical operation and analyses of the proposed converter were verified by the experimental results of a 400-W prototype with a voltage gain of 16 and full-load efficiency of 92.3 %.

Table 2.1 lists some other features of the proposed advanced high step-up DC-DC converters, including the employed VB techniques, number of components, voltage gain, duty cycle range, and nature of input current ripple. As obvious, all proposed converters can achieve high voltage gains without a large number of components. Also, the input currents of all the proposed converters are continuous with low or medium ripples. Therefore, all proposed converters are suitable candidates for renewable energy applications. Moreover, the duty cycle varies from 0.5 to 1 for the converters proposed in Papers I, IV, and V and from 0 to 0.5 for the converters proposed in Papers II and III. Thus, if a high voltage gain with a low duty cycle is desired, the converters in Papers II and III are suitable choices. However, if an ultra-high voltage gain with a medium duty cycle is desired, the converters in Papers I, IV, and V are proper choices.

Table 2.1. Features of the proposed advanced high step-up DC-DC converters.

Converter	VB Techniques	Number of Components							Voltage Gain	Duty Cycle Range	Input Current Ripple
		Inductors	CI's	BITs	Capacitors	Diodes	Switches	Total			
Paper I	Interleaved, SC, and CI	0	2	0	5	5	2	14	$\frac{4N+4}{1-D}$	$0.5 \leq D \leq 1$	Low
Paper II	SC and CI	0	1	0	4	5	2	12	$\frac{4N+3}{1-2D}$	$0 \leq D \leq 0.5$	Medium
Paper III (PAS-SCZSC and NAS-SCZSC)	SC	3	0	0	5	3	1	12	$\frac{2-D}{1-2D}$	$0 \leq D \leq 0.5$	Low
Paper III (S-SCZSC)	SC	3	0	0	6	4	1	14	$\frac{3-2D}{1-2D}$	$0 \leq D \leq 0.5$	Low
Paper IV	Interleaved, SC, CI, and BIT	0	2	1	5	5	2	15	$\frac{2N+4n+4}{1-D}$	$0.5 \leq D \leq 1$	Low
Paper V	Interleaved, Quadratic, SC, and CI	0	2	0	4	4	2	12	$\frac{N+D+1}{(1-D)^2}$	$0.5 \leq D \leq 1$	Low

CI=Coupled Inductor, BIT=Built-in Transformer, D =Duty Cycle of Switch(es), N =Turns-Ratio of CI(s), n =Turns-Ratio of BIT(s)

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VITA

Ramin Rahimi received his B.Sc. degree in electrical engineering from the University of Tabriz, Tabriz, Iran in 2013, and his M.Sc. degree in electrical engineering from University of Tehran, Tehran, Iran in 2016. In July 2022, he received his Ph.D. degree in electrical engineering from the Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO, USA. His research interests included power electronics, DC distribution systems, and design and implementation of power converters for the renewable energy applications and electric vehicles.