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Characterization and modeling of ESD events, risk and protection

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CHARACTERIZATION AND MODELING OF ESD EVENTS, RISK AND PROTECTION

by

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This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I, found on pages 3-24, “ESD spark behavior and modeling for geometries having spark lengths greater than the value predicted by Paschen's law.”, has been published in the IEEE Transactions on Electromagnetic Compatibility.

Paper II, found on pages 25-50 “Characterization of the ESD Risk for Wearable Devices”, has been published in the IEEE Transactions on Electromagnetic Compatibility.

Paper III, found on pages 51–72 “Race Conditions among Protection Devices for a High Speed USB 3.x Interface,” to be published in the IEEE Transactions on Electromagnetic Compatibility.”

ABSTRACT

The ESD (Electrostatic discharge) failures have been raising critical reliability problems in electronic devices design. However, not all the ESD scenarios have been specified by the IEC standard and the characterizations of the ESD risk for different scenarios are essential to evaluate the ESD robustness of the devices in the real word.

The insulation of plastic enclosures provides protection against ESD to the electronic system inside. However, seams between plastic parts are often unavoidable. Different plastic arrangements are constructed to investigate the spark length and current derivatives and to understand the ESD spark behavior for geometries having spark lengths longer than the values predicted by Paschen's law.

For the wearable devices, the core difference between the posture assumed for IEC 61000-4-2 human metal discharge and a discharge to a wearable device is the impedance between the charged body and the grounded structure discharged to. The results show that the current measured in the brush-by scenario can reach values twice as high as the current specified in the IEC standard. A simulation model using the measured impedance and Rompe and Weizel's law provides predictions on the peak current derivative when the spark length is varied. The increasing peak current derivative with shorter spark length indicates stronger field coupling to the devices.

SEED(System-efficient ESD design) modeling helps the designer to predict the ESD risk at the early stage, an accurate TVS model can be used to study the transient response of the external TVS and the on-chip protection when applied in a typical high-speed input/output (I/O) interface.

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1. INTRODUCTION

1.1. ELECTROSTATIC DISCHARGE

The ESD (Electrostatic discharge) failures have been raising critical reliability problems in electronic devices design. Characterization of the ESD events to understand the risk level in different real-life scenarios are necessary to guide the designer to prevent the damage for the products.

The IEC-61000-4-2 standard specified a test scenario that the discharge occurs from a metal object holding in a human hand for the system-level ESD testing. However, the ESD could occur in many other scenarios in the real life causing potential failures to the device even it has been tested for the IEC standard.

The goal of this dissertation is to provide characterization and modeling for those ESD scenarios not specified by the IEC standard to provide a better understanding of these phenomena and a simulation platform which can be used by the designer to predict potential problems.

1.2. OUTLINE

Paper I reproduce a test scenario that the spark occurs along the plastic surface to investigate the spark length and current derivatives and to understand the ESD spark behavior for geometries having spark lengths longer than the values predicted by Paschen's law. The spark resistance is modeled by a modified Rompe and Weizel's law which distinguishes the spark development in the air and along the plastic surface.

For the wearable devices, Paper II shows the brush-by scenarios may be insufficiently covered by testing using the standard IEC ESD test set-up. The lower impedance formed between the human body and grounding structure lead to much higher currents relative to the human metal ESD. Besides the currents, the enhanced transient fields may lead to soft failures in wearable devices at lower charge voltages.

Careful selection of the TVS protection device is critical for ESD design. A test board to understand adding components to provide an additional impedance between the external TVS and the on-chip diode will be discussed in Paper III. The SEED modeling process helps design engineer to intelligently select protection devices and other components to maximize protection against a range of transient events while also ensuring the signal integrity of the design.

PAPER

I. ESD SPARK BEHAVIOR AND MODELING FOR GEOMETRIES HAVING SPARK LENGTHS GREATER THAN THE VALUE PREDICTED BY PASCHEN'S LAW

ABSTRACT

The insulation of plastic enclosures provides protection against direct ESD discharges to the system inside. However, seams between plastic parts are often unavoidable. To increase the voltage at which an ESD will penetrate the structure of the seam can be modified. Four plastic arrangements are constructed to investigate the spark length and current derivatives and to understand the ESD spark behavior for geometries having spark lengths longer than the values predicted by Paschen's law. A two to threefold increase of spark lengths was found for sparks guided by plastic surfaces compared to spark length expected from the Paschen value at the same voltage level. In spite of the longer path, a faster spark development is observed for sparks along the plastic surface. Plastic arrangements which provide detour and fold-back paths hardly reduced the total spark length. No significant effects of the plastic materials or the polarity were observed. The spark length increased as the (absolute humidity) AH increased, and the current derivative decreased by about 20% as the spark length increased with (relative humidity) RH changing from 9% to 65% at 29 ℃.

The spark resistance is modeled by a modified Rompe and Weizel's law which distinguishes the spark development in the air and along the plastic surface.

1. INTRODUCTION

One method to achieve ESD robust electronic system design is to prevent sparking into the system. This can be achieved by a sufficiently insulating barrier. While even 0.3 mm plastic is usually not penetrated by ESD up to 25 kV difficulties are introduced by seams between plastic parts and openings that expose the inner circuits. The design choice can influence the tightness of adjacent plastic parts, the plastic materials, the wall thickness, and the distance to the electronics. Further the designer can shape the seams of adjacent plastic parts such that detours lengthen the spark path, or introduce fold-back structures that force the spark to develop against the electrostatic field direction. This article analyzes the effect of such design choices and provides an improved simulation model for the spark resistance which also includes situations in which the spark develops parallel to plastic surfaces.

A good starting point is to remind ourselves of Paschen's law. It describes the relation between the static breakdown voltage as a function of the gap distance for homogeneous fields.

$$U=25.4d+6.64\sqrt{d} \tag{1}$$

where U is the voltage in kV and d is the distance in cm.

However, few practical electrode arrangements offer a homogeneous field. They differ in the following aspects:

- Electrodes, such as PCBs may have sharp tips or edges.
- The spark path maybe guided along plastic surfaces as the spark penetrates between adjacent plastic parts of the enclosure.

- The IEC 61000-4-2 test standard asks to approach the (device under test) DUT while attempting to discharge to it, thus, this leads to a change of the electric field strength.

It is generally known that sharp electrodes and paths parallel to insulating surfaces increase the length the spark can bridge. Our study has shown that for the voltage range relevant to ESD these geometric factors can increase the length by twofold or more relative to the value predicted by Paschen's law. For approaching electrodes the opposite can happen: The discharge occurs at distances less than the value predicted by the Paschen law. This discrepancy is explained by a delay of the onset of the spark due to the statistical time lag while the gap is closing due to the approach velocity. This phenomenon leads to spark lengths below the Paschen value, reduced rise times and larger peak values. For approaching electrodes, the spark resistance behavior and its simulation is well documented in the literature [1][2]. However, the lack of information on the spark behavior for spark lengths longer than the values predicted by Paschen's law, requires more investigation. Spark lengths longer than Paschen's value are certainly more likely for voltages exceeding 8 kV as the effect of sharp edges is more pronounced at higher voltages. Further plastic surfaces, metallic edges, surface contaminations and humidity will reduce the statistical time lag. With reduced statistical time lag it becomes unlikely to experience shortening of the spark length due to the interplay of the approaching speed and statistical time lag. To our knowledge there is no comprehensive study of the spark behavior for plastic enclosures in a voltage range relevant to ESD.

The main questions addressed in this contribution are: What is the distance that a spark will bridge if it is guided by insulating surfaces of different shapes? How large are

the current derivatives? And how can the current rise be simulated for this type of geometries?

This knowledge can guide the designer in selecting gap shapes and geometries that maximize the voltage needed to breakdown through a gap into an enclosure. If the breakdown cannot be prevented, the simulation models will allow estimating the peak current derivative, which has been shown to be strongly related to soft-failures in products [5].

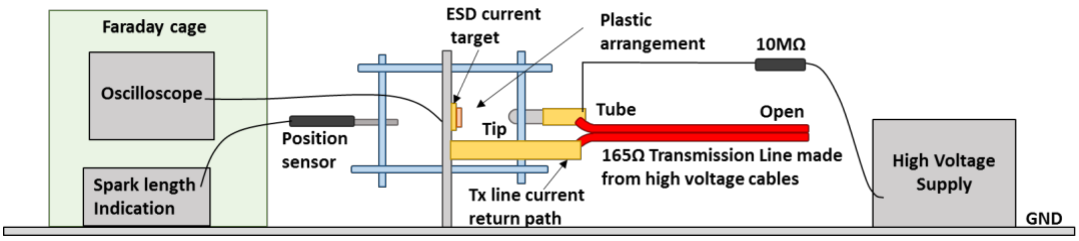

Figure 1. Test setup showing (from left to right) the spark length measurement (see Figure 2 for details): oscilloscope, current target, discharge tip, transmission line and the high voltage supply.

2. MEASUREMENT SETUP AND RESULTS

2.1. EXPERIMENTAL SETUP

The experimental setup allows controlling and capturing the following parameters:

- The charge voltage is set by the operator. The setup is limited to 25 kV. The ground of the high voltage supply is connected to the ground plane which forms the transmission line's return path. The ESD current target is also grounded, thus the voltage is applied between the tip and the ESD current target.

- The electrode shape and the geometry of the plastic arrangement is set to allow straight, detour and reversing spark paths, see Figure 3.
- Four different types of plastic materials have been used.
- Testing is performed inside a climate chamber. The climate chamber does not allow changing the air pressure. However, it has been shown that the value predicted by Paschen's law is proportional to the air pressure for typical values on earth's surface, i.e., it is reasonable that the results for spark lengths longer than the Paschen's value will scale proportionally with air pressure. The testing has been done at a height of 300 m above sea level at about 40% RH and 23 °C.
- The setup measures the discharge current and the electrode distance in the moment of the spark. The discharge current is measured via a current sensor as described in IEC 61000-4-2.
- For measuring the spark length the moving electrode is attached to a slider via insulating fiberglass, see Figure 1 and Figure 2. The slider's position is captured using a resistive position sensor. The discharge current triggers a S/H circuit which records the position of the moving electrode in the moment of the discharge.

A 7.5 m, 165 Ω transmission line was selected as discharging structure to provide a long enough square pulse. A value of 165 Ω is used as a compromise between the impedance of 266 Ω derived from the peak current definition of the IEC 61000-4-2 standard (3.75 A/kV), charged cable discharges and lower impedance seen for the discharge of body worn equipment [3].

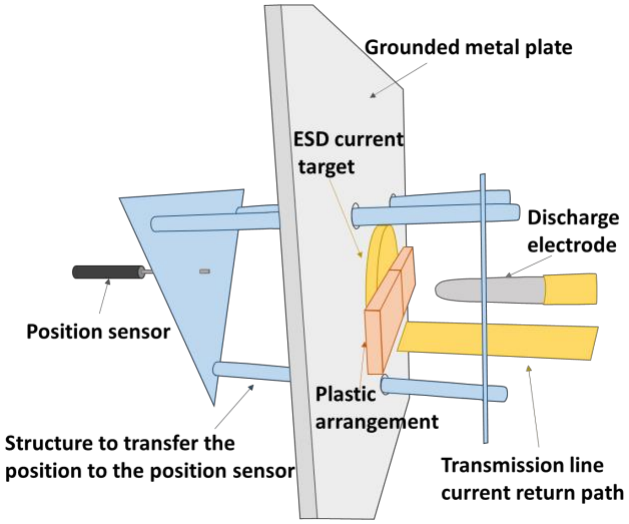

Figure 2. Details of the spark length measurement and the plastic arrangement which is mounted in front of the ESD current target. The spark bridges the center of the current target (hidden by the plastic arrangement) via the gap in the plastic arrangements to the discharge electrode. The triangular structures and the connecting rods transfer the movement of the electrode to the position sensor which is placed behind the ESD current target.

If no plastic arrangement or a straight path arrangement (Figure 3, (a) and (b)) is used then the spark length equals the distance between the moving electrode and the current sensor. If arrangements (c) or (d) are used then the extra length within the plastic arrangement needs to be added to the electrode distance to obtain the total length of the spark path.

In plastic enclosures different types of interfaces are used. Some are folded back to increase the length of the gap and to force the spark to propagate against the electrostatic field. This approach increases the voltage needed for breakdown. To reproduce a set of different interfaces, the plastic surface has been machined to be smooth and pressed tightly to reproduce the situation encountered on products. One might expect that a spark cannot penetrate the gap between two plastic parts that are pressed together.

However, it is known that holes as small as 10 μm will allow a spark to penetrate through a seam, thus machining the surfaces on a milling machine does not prevent sparking. The four different plastic arrangements used for this investigation are shown in Figure 3. They differ in the path style and path length. Arrangement (a) and (b) offer a straight spark paths parallel to the electrostatic field. Arrangement (a) used 3.2 mm thick plastic parts, while arrangement (b) uses 6.4 mm thick plastic parts. Arrangement (c) is created by offsetting two stacked 3.2 mm plastic parts. This leads to a detour for the spark, in which it partially travels perpendicular to the electrostatic field. Arrangement (d) forces the spark to travel against the electrostatic field. The total path that the spark travels along the plastic surface is 7.3 mm for arrangement (d). To obtain the total spark length, the section the spark bridges between the electrode and the plastic arrangement needs to be added.

If the voltage is above the minimal breakdown voltage the spark will partially travel guided by the plastic, and then bridge the section from the plastic surface to the rounded electrode in air. The length ratio between these two sections of the total spark length, depends on the plastic arrangement and the voltage. This experiment used a flat electrode (from the ESD current target) directly behind the plastic arrangement and the air discharge ESD generator tip as moving electrode. During the experiment the voltage was set and the electrode was approached towards the plastic arrangement. The approach speed was less than 10 mm/sec. While this speed is much less than the typical speed during ESD testing, it was observed that increasing the approach speed did not affect the results strongly for experiments that included a plastic arrangement. This indicates that the plastic arrangements lead to short statistical time lags. A short statistical time lag will

lead to a breakdown at the moment the gap distance is reduced to a length that allows a breakdown [1][6].

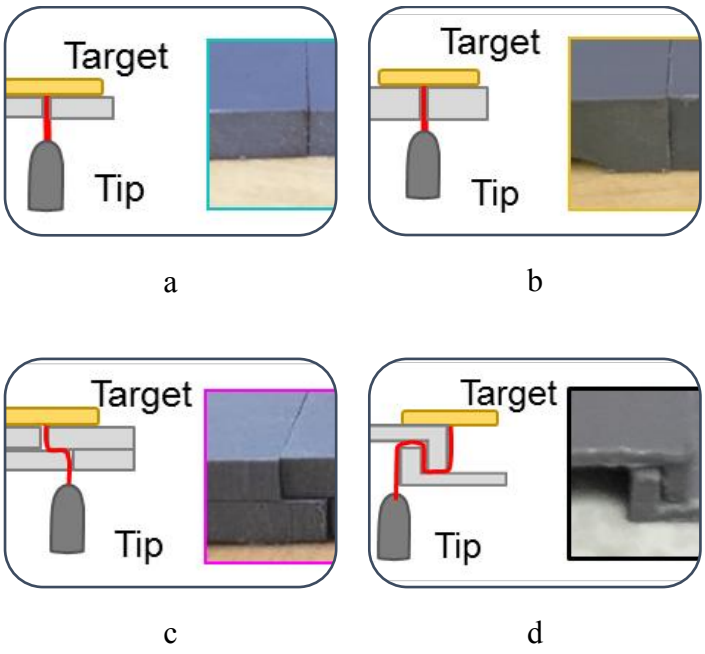

Figure 3. Plastic arrangements used in the experiments. Arrangement (a) and (b) offers a straight spark path, (c) forces the spark to travel perpendicular to the static field and arrangement (d) forces the spark to travel against the static field. The spark path is indicated by the red line.

The current sensor captures the current waveform leading to a system bandwidth (scope + cables + target) of about 3 GHz. Besides the spark length and the waveform, the peak current derivative is analyzed. This parameter has been selected as it has been shown that the peak current derivative often correlates to soft-failure thresholds on electronic systems [5].

2.2. SPARK LENGTH

The experiments involved setting the plastic arrangement, the charge voltage and then approaching the electrodes. Sparking occurred above a voltage determined by the plastic arrangement. The current and the electrode distance at the moment of the sparking were measured and analyzed. Figure 4 shows the spark lengths for different arrangements. Additionally, spark lengths according to Paschen's law are included as a reference. A second reference shown in Figure 4, is the discharge distance between two razor blades, arranged at 90^{o}. The spark lengths obtained without plastic arrangement are very close to the Paschen's values. This behavior is expected, as the arrangement is similar to the requirement for Paschen's law, thus this result can be seen as indication for the correctness of the voltage setting and spark length measurement.

On the other extreme, Figure 4 shows the measured breakdown distances for the razor blade setup. Here, additional measures were needed to reduce corona at the corners of the blades. The blades have been encapsulated in rounded electrodes for all regions except the region in which the sparking occurs. In spite of these measures, corona occurring at the sparking location (the center of the blades front edge) prevented the measurement for voltages exceeding 10 kV in the razor blade arrangement.

Using 3.2 mm thick plastic (Figure 3 (a)) the spark values increased by a factor of about 2 compared to the Paschen value. For example for 10 kV, the values increased from 2.8 mm to 6~6.3 mm. Results using the 6.4 mm thick plastic (Figure 3 (b)) indicate a further increase of the distance the spark can bridge. For example the value at 10 kV increased to 6.5~7 mm.

Intuitively one may expect that forcing the spark to propagate perpendicular or even against the electrostatic field would significantly decrease the distance a spark can bridge. However, the data does not support this hypothesis. The reverse arrangement having a plastic guided path of 7.3 mm, the spark length is 9.8~10.5 mm. This falls into a similar range as the arrangement (b) having a straight plastic guided path of 6.4 mm. The distance between the ESD current target and the air discharge tip is reduced because of the detour and the fold-back.

The seemingly counterintuitive observation that even a spark path against the electrostatic field will only marginally reduce the bridged distance, can be resolved if one considers that the developing spark modifies the local field as the streamer advances as an electrode [6].

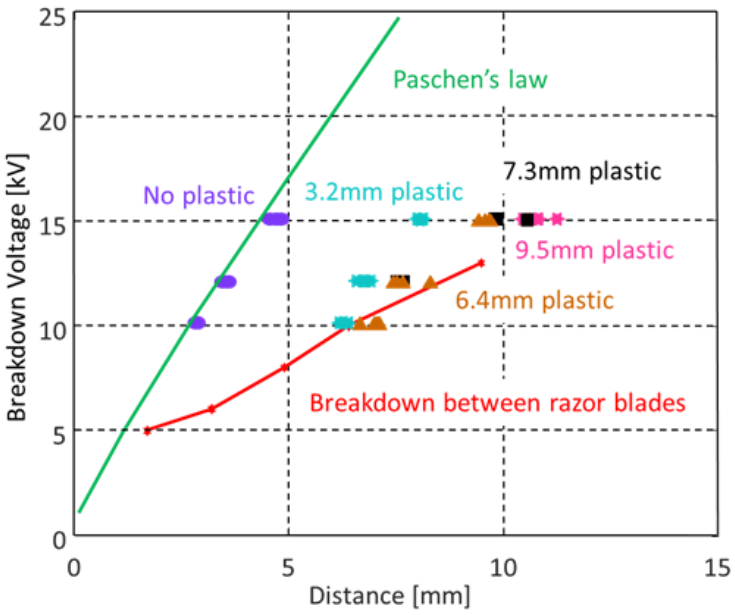

Figure 4. Measured breakdown distances for different plastic arrangements. Distance predicted from Paschen's law (left) and measured breakdown between two razor blades mounted perpendicular to each other.

While the underlying physical processes may not be fully understood the results clearly show a strong increase of the spark length if the spark is guided by plastic surfaces. This indicates that thicker plastic walls, or detour and reverse arrangements may not achieve the expected result of preventing sparking.

2.3. EFFECT OF THE PLASTIC MATERIAL

Table 1 presents data on the effect of selecting different plastic materials investigated for 15 kV using arrangement (b). The data is typical for other voltages and arrangements and gives evidence that the selection of the plastic material does not strongly influence the sparking behavior. However, an important effect common to all plastic materials, is that the plastic arrangements significantly reduce the rise time and increase the peak current derivative of the discharge current. The results repeated well, see Figure 5. This indicates that effects of possible surface changes or charge accumulation over repeated testing do not influence the results significantly. This is probably a result of having short pulses that transfer charges of less than 5 μC.

Further evidence to this effect is given by a direct comparison of the discharge currents presented in Figure 5. (The waveforms are obtained using an RC discharge network instead of the transmission line structure.) Similar discharge currents have been observed for different plastic materials indicating that the discharge currents are independent of the plastic material. This might be explained by the fact that all plastic materials investigated have a somewhat similar relative permittivity in the range of 2.4 – 3.7. The data shown in Figure 5 is supported by measurements at from -18 kV to 15 kV. The second, more pronounced effect is a faster spark development for the cases in which

the spark is along a plastic surface. While the reason for the faster spark development has not been clarified in this study, the data clearly give evidence that the current derivative is increased, thus, the likelihood of damage or upset by ESD may be increased by spark paths along plastic surfaces. However, it was observed that the total distance the spark needed to bridge, has been increased by at least twofold.

Table 1. Comparison of the spark length and current between different materials for the plastic arrangement (b) at 15 kV.

Plastic Arrangement	Relative Permittivity	Spark Length (mm)	Max(dI/dt) (A/ns)	Rise time 20-80% (ns)	Max(I) (A)
No plastic	-	3~5	2.6	22	41.44
Chemical-and-War Resistant Acetal	3.7	9.0~9.9	7.2~8	3.8~4.1	43
Formable Chemical-Resistant Kydex Acrylic/PVC	2.6	8.9~10	6.5~7.6	3.9~4.2	43
Chemical-Resistant Type II PVC	3.0	8.6~9.5	6.6~8.2	3.5~4.6	40
Easy-to-Form Clear PETG Sheet	2.4	8.8~10	5.8~7	4.2~5.1	43

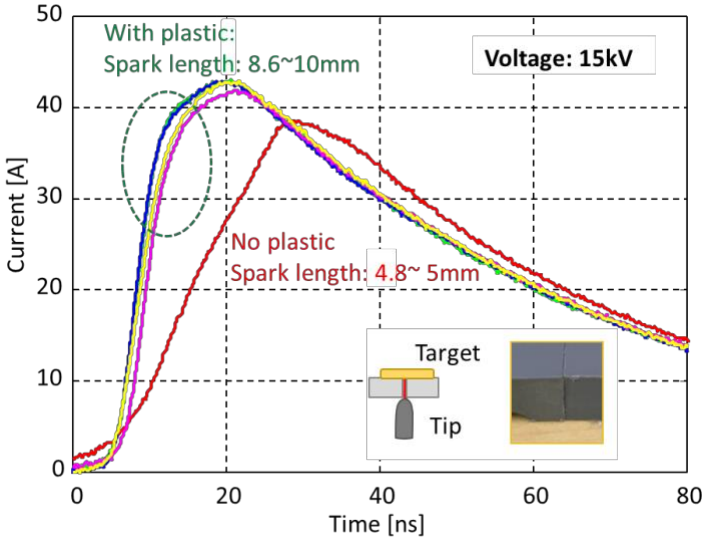

Figure 5. A discharges without plastic compared to discharges with plastic for different plastic materials (arrangement (b), 15 kV).

We did not observe a strong effect of the polarity. This can be explained by the rather symmetric setup used in this investigation. One electrode is formed by the flat ESD current sensor while the other electrode is formed by the rounded ESD simulator air discharge tip.

2.4. CURRENT DERIVATIVE

As discussed in the introduction section it is known that approaching electrodes can lead to spark lengths much shorter than the value predicted by Paschen's law. During the delayed onset of the spark, the electrodes continue to approach, which increases the field strength in the gap. Once the discharge is initiated, the spark resistance will drop faster due to the increased field strength. This will also result into large peak current derivatives that may reach values of 1000A/ns or more [1]. However, a long statistical time lag is required for voltages exceeding 8 kV to reach such high current derivative

values. This requires a quasi-homogeneous field, clean electrodes and dry air. Most spark gap topologies encountered during air discharge mode ESD testing on products do not fulfill these conditions, i.e., the statistical time lag will be short. Throughout all our measurements, the peak current derivative remained in the range of 3-10A/ns. Care must be taken to generalize these numbers as they will certainly be influenced by the source impedance of the discharge arrangement which was set to 165 Ω. However, the values will remain much lower than the values published for spark lengths shorter than the Paschen value [1]. Thus one can use this value range to estimate the current derivatives and consequently induced voltages during ESD testing.

After having shown that neither polarity nor the plastic material selection strongly influenced the spark behavior the attention is moved to the effect of the plastic arrangement on the current derivative. The scatter plot presented in Figure 6 details the effect of the spark length on the current derivative for different voltages and plastic arrangements. Data points on the left side of Figure 6 shows spark lengths equal to the Paschen's length (no plastic). The peak current derivatives slightly reduced as the voltage was increased from 10 kV to 15 kV. The middle section from 6-8 mm spark length of Figure 6 shows results for plastic arrangement (a) that allows a straight spark (Figure 3, (a)) guided by 3.2 mm plastic. Although the spark length has increased from about 2.8 mm to 6.2 mm for 10 kV, the peak current derivative increased on average by 2 A/ns. This again indicates that the plastic surface not only allows the spark to bridge larger distances, but also confirms that the spark develops faster in spite of its longer length. The right section of the plot presents the data for the detour and the counter field arrangements (Figure 3, (c) and (d).) The data is only shown for 15 kV, as not all

arrangement showed a breakdown at lower voltages. In spite of spark lengths of more than 10 mm (about 3x the Paschen's value for 15 kV) the spark development led to peak current derivatives in the range of 5.5-8.5A/ns.

In summary, we conclude that the peak current derivatives for spark lengths longer than the values predicted by Paschen's are in the range of 3-10 A/ns. The plastic guided spark can bridge up to 3 times the distance predicted by the Paschen's value. In spite of these longer distances, the spark develops faster, leading to moderately increased peak current derivatives.

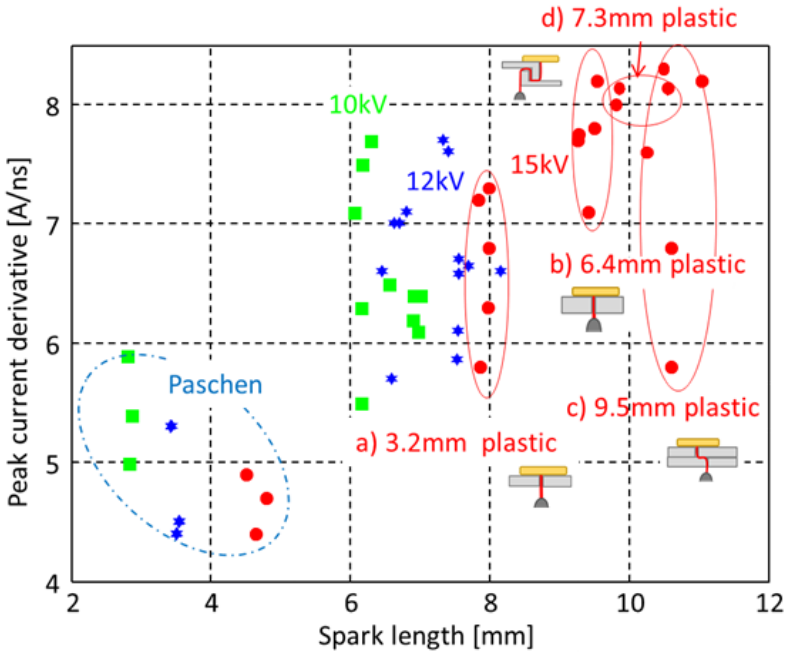

Figure 6. Peak current derivatives for the different plastic arrangement.

2.5. INFLUENCE OF THE HUMIDITY

ESD is affected by humidity by three mechanisms: In high humidity, the tribo-chargining is reduced [8]-[10], the conductivity of many materials is increased, leading to

a faster charge decay, and the statistical time lag is strongly reduced [1]. The measurements, shown in Figure 7 were conducted in a climate chamber where the environmental conditions can be varied between a relative humidity of 9% to 65% in a temperature range of 24 ℃ to 29 ℃. The 6.4 mm plastic (Figure 3, (b)) is used for the presented data at the right of the Figure. For sparks guided by the plastic surface, the overall effect of the humidity on the current derivative is not strong. The spark length increases from 9.1~9.3 mm to 10.5~11.1 mm at 15 kV as the AH increases from 0.003 kg/m3 to 0.019 kg/m3. The data at 12 kV and 15 kV both show that by increasing AH, the peak current derivative decreases as the spark length increases. Overall, humidity has a minor effect on the experimental results.

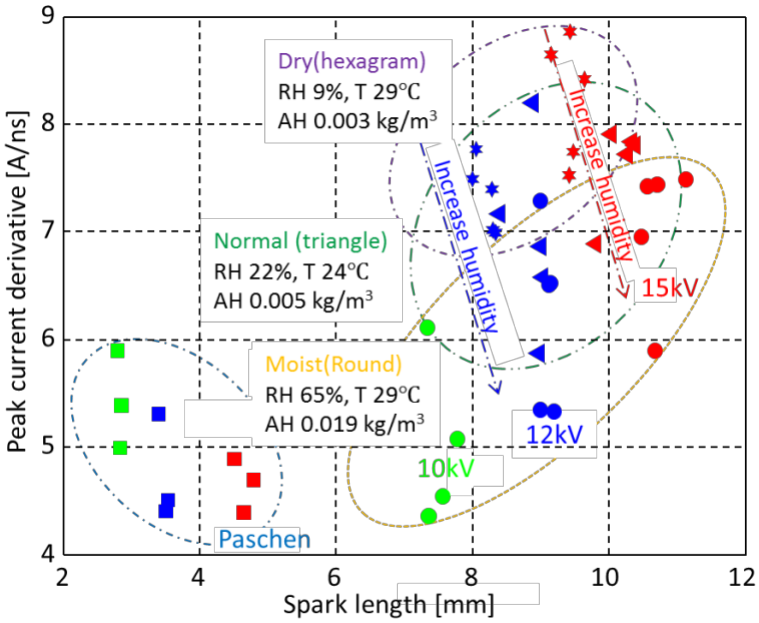

Figure 7. Peak current derivative for different humidity conditions.

3. SIMULATION OF THE SPARK RESISTANCE

3.1. EXPERIMENTAL SETUP

It has been shown that the spark resistance law from Rompe and Weizel predicts the maximal current derivative over a large range of voltages and spark lengths in the range of 1.5 – 25 kV [1][2][11].

$$\mathrm{r(t)} = \frac{l}{\sqrt{2K_R \int_0^t i(t')^2 dt'}} \tag{2}$$

Based on the measured discharges in air while trying to achieve a good match between simulation and measurement, the spark constant K_R is typically selected in the range of 0.5-1e-4 $m^2/(V^2 s)$. However, the shorter rise times observed for sparks guided by plastic, (shown in Figure 5 and Figure 6), indicate that the spark develops faster if it is guided by plastic surfaces. To maintain a good match between simulation and measurements the value of Kr needs to be modified if the spark is guided by a plastic surface. As seen in Figure 8, a value of about 4e-4 $m^2/(V^2 s)$ is most suitable for predicting the spark resistance drop for plastic guided sparks.

A second aspect that needs to be considered is that the initial spark originating from an ESD simulator tip, may be partially in air, until it reaches the plastic surface. Thus, one needs to consider both the spark distance in air and the spark distance along the plastic surface. Rompe and Weizel's spark resistance law needs to be modified to simulate these cases. This is achieved by introducing a weighting function:

$$K_R = p \cdot K_{Plastic} + (1 - p) \cdot K_{air} \tag{3}$$

Where p is the portion of the spark along plastic, $K_{plastic}$ is the constant for the section parallel to the plastic and K_{air} is the constant needed to describe the spark development for the section in the air. The best match was achieved when $K_{air} = 0.7\text{e-}4\ m^2/(V^2 s)$ is used to model the section not guided by plastic, and $K_{plastic} = 5\text{e-}4\ m^2/(V^2 s)$ is used for the plastic guided distance.

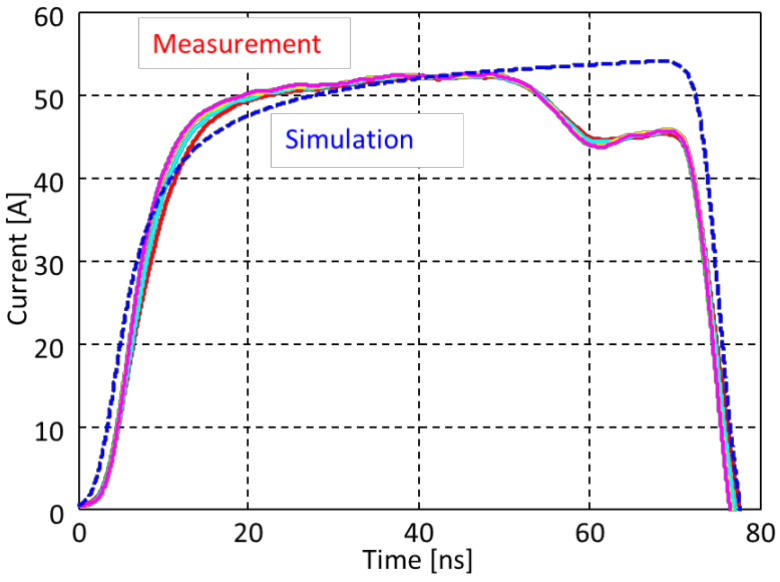

Figure 8. Simulated and measured discharge current for arrangement (a) at 10 kV.

To apply the modified law one should take the following steps:

1) Know the maximal voltage one wants to protect for.

2) Know the length of the section which is parallel to the plastic. This can be obtained from the mechanical drawings.

3) Estimate the total length of the spark, based e.g., on information shown in Figure3.

4) Subtract the plastic guided path length from the total spark length. This provides the length of the section of the spark which is in air.

Using this information the both sections of the spark path are calculated and the modified law can be applied.

Using this modified spark resistance law, discharge waveforms have been simulated and compared to measurements, (for a constant path length along the plastic, but varying path lengths in the air (Figure 9). This is achieved by increasing the voltage beyond the minimal value required to spark along the plastic. If the voltage exceeds this minimum limit, the distance of the section in air will increase. In the experiment the spark length section in air was measured using the setup shown in Figure 1.

The peak current derivative is an important parameter as it often determines the peak induced voltage. The peak current derivatives and associated spark lengths are shown in Table 2.

Table 2. Peak current derivatives for the data shown in Figure 9.

Voltage [kV]	Spark length [mm]	Peak current derivative [A/ns]	
		Measurement	Simulation
10	7.0	6.2	5.9
12	8.1	6.5	6.7
15	9.2	8.0	8.4

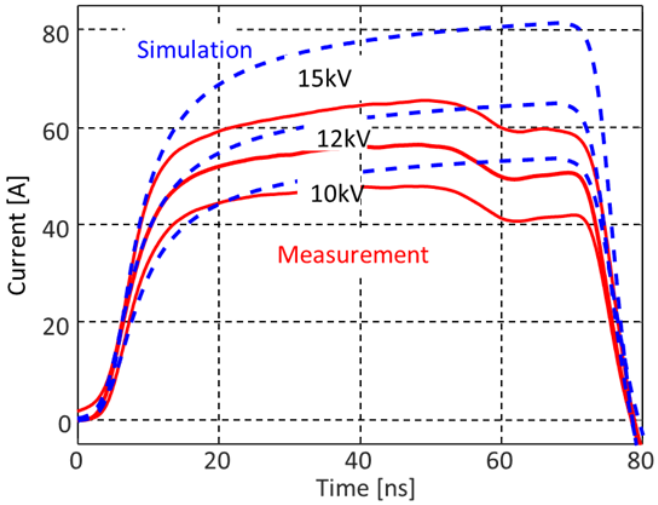

Figure 9. Simulated and measured discharge current for arrangement (b). The simulation uses the modified spark resistance law (eqn. 3).

The results shown in Figure 9 and Table 2 indicate that the modified law can predict the current waveform and especially the peak current derivative for sparks that are partially guided along a plastic surface.

4. CONCLUSION

This experimental investigation into spark distances, current rise times and the modeling of the spark resistance showed that sparks guided along plastic surfaces can bridge distances two to three times longer than the distances predicted by Paschen's law. The introduction of detour paths or paths against the electrostatic field did not increase the voltage needed to bridge a spark.

In spite of the longer spark path, a strongly reduced rise time was observed for sparks along plastic surfaces comparing discharges at the same voltage. This accelerated

spark development requires a modification in Rompe and Weizel's spark resistance law to allow predicting the peak current derivative for arrangements in which the spark partially is guided by a plastic surface. Further the results indicate that using different types of plastic materials hardly affected the measured currents or sparking distance.

Increasing RH resulted in a longer spark and a slightly smaller current derivative. However, humidity was not a strongly influencing factor.

It is suggested that the seam structure of the plastic enclosure for the electronic system be carefully designed to increase the voltage at which ESD will penetrate into the system by providing detour paths or paths against the electrostatic field to allow placing the electronics closer to the enclosure.

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II. CHARACTERIZATION OF ESD RISK FOR WEARABLE DEVICES

ABSTRACT

The core difference between the posture assumed for IEC 61000-4-2 human metal discharge and a discharge to a wearable device is the impedance between the charged body and the grounded structure discharged to. Especially for a waist-worn device, a larger portion of the body is close to the grounded structure; thus the geometry forms a much lower impedance which will lead to higher currents. Despite the variability for the air discharge, in most cases, the current will be higher than 3.75 A/kV as specified for contact mode ESD calibration. Even for the most slowly rising discharges having a spark length equal to the value given by Paschen's law, a 10 kV ESD from the waist will surpass 37.5 A for a waist-worn metal part discharged (e.g., to a door frame). Modeling the wearable device discharge provides predictions on the current derivative and the transient field a wearable device is subjected to. Observed failure levels of a wearable electronic device and comparing discharges according to the IEC 61000-4-2 test standard against discharges from the device while wearable showed that the IEC set-up may be insufficient to ensure the robustness of the wearable devices.

1. INTRODUCTION

The ESD scenario specified by the IEC 61000-4-2 standard is based on a human holding a metal piece in the hand and discharging to the ground plane [1], referred to as

the human metal model (HMM). However, for wearable devices the ESD scenario is different: a wearable device may spark to a door frame if the person brushes by the door frame. In a 'brush-by' situation currents can reach levels twice as high as a human metal discharge at the same voltage. This posture related reliability risk has been shown to possibly endanger medical equipment [2], e.g., during patient movement on a transfer board. The impedance formed between the ground and the wearable device is much lower compared to the impedance between the hand-held metal and ground in the HMM scenario, as shown in Figure 1.

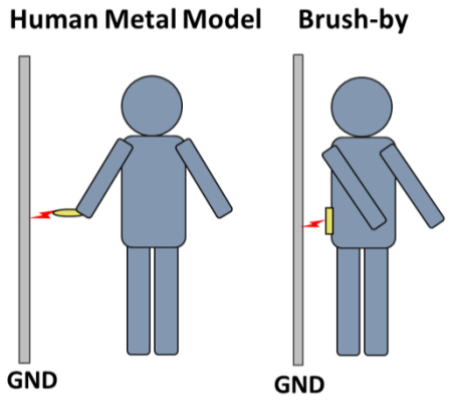

Figure 1. Different ESD scenarios for Brush-by and HMM.

The discharge current in the brush-by scenario can be much higher than 3.75 A/kV specified by the IEC standard in calibration. That leads to the question of whether the IEC test set-up is realistic for wearable devices.

The investigations from Ishida [3] have shown at 1 kV, the peak current for different positions of wearable devices rank from largest to smallest in the order of: waist, arm, head, and hand. However, Ishida did not consider the spark resistance effect

[3]. At higher voltages, especially if the spark length is long, the rise time will be increased and the peak value will not increase linearly with voltage. Thus, one cannot conclude from 1 kV measurements of the risk ESD poses to wearable devices at higher voltages. Full wave simulations give further evidence of higher currents driven by lower impedances [4] for wearable devices

Measuring the impedance between the wearable device and ground allows prediction of the maximal current. This extreme is reached if the spark forms an ideal switch and if the wearable device is well connected to the body. Knowing the impedance and the spark length, it is possible to simulate the discharge current by modeling the time-dependent spark resistance using the spark resistance law from Rompe and Weizel [5]. This method is used in this research to predict currents for spark lengths shorter than the value predicted by Paschen's law [6].

Some additional factors that need to be considered for the discharge current are the wearable device may have a plastic chassis or there may be garments between the device and the skin of the person forming a capacitive insulating barrier. This makes it necessary to further investigate the effect of the different connection conditions.

On-die sensors capable of transient event detection and level sensing are used to capture the current induced on an I/O of wearable devices [7], however, without capturing the waveforms.

This paper indicates that such brush-by scenarios maybe insufficiently covered by testing using the standard IEC ESD test set-up. The lower impedance formed between the human body and grounded structure lead to much higher currents relative to the human

metal ESD. Besides the currents, the enhanced transient fields may lead to soft failures in wearable devices at lower charge voltages [8-10].

2. CURRENT MEASUREMENTS

2.1. EXPERIMENTAL SET-UP AND RESULTS FOR DIFFERENT POSITIONS

The experimental set-up shown in Figure 2 allowed measurement of the current for HMM and wearable devices in a brush-by scenario. The person, standing on the 0.5 mm insulator, was charged to the set voltage level. For the HMM scenario, the person held the air discharge tip of an ESD generator in their hand and approached the air discharge tip to the current target which was mounted onto a grounded metallic wall. For the brush-by scenario, a semi-sphere mounted on the metal plate with dimensions of 12 cm× 12 cm was used as the wearable device. Both geometries lead to a quasi-homogeneous electrostatic field prior to the breakdown. For the wrist position the size of the metal piece was reduced to 5 cm × 5 cm, which is a more realistic watch size.

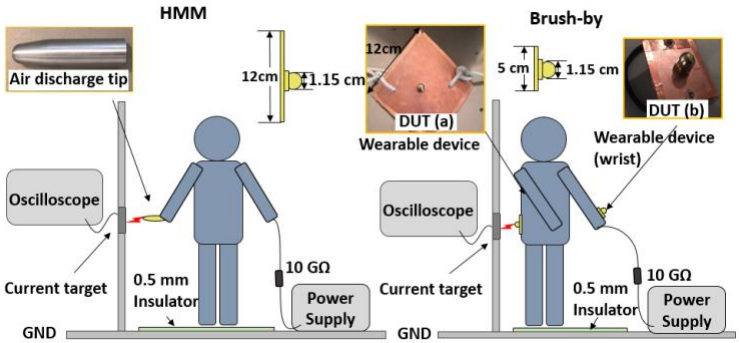

Figure 2. Current measurement set-up for HMM and wearable devices for brush-by scenarios.

The discharge currents for different positions of the wearable devices at 1 kV are shown in Figure 3. The peak currents for all the positions of the wearable devices are higher than the currents in the HMM case. This difference is most pronounced in the waist position, where the current can reach levels twice as high as in the HMM scenario. Ishida [3] observed similar current values for discharges at 1 kV.

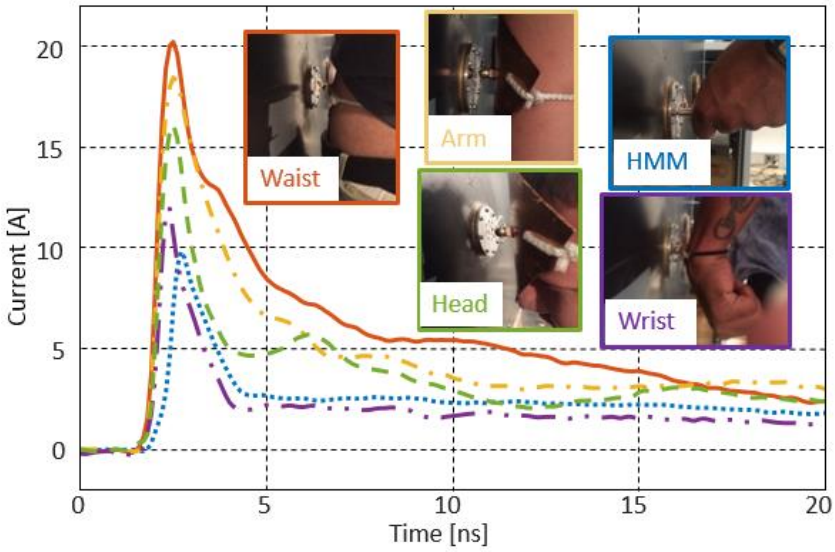

Figure 3. Discharge current for different positions of the wearable device compared to HMM at 1 kV.

When the voltage level increases, the effect of varying spark lengths is more visible. For a homogeneous field (round, no approaching electrodes), the sparking distance is determined by Paschen's law, which describes the relationship between the static breakdown voltage U and the gap distance d.

$$U = 25.4d + 6.64\sqrt{d} \quad (1)$$

where U is the voltage in kV and d is the distance in cm. This provides the longest sparking distance in a homogeneous field.

For most electrostatic discharges, the spark length is shorter than the Paschen value. This is caused by the speed of approach and the statistical time lag, which may delay the spark development [11][12]. To achieve a spark length around Paschen, one must approach the target slowly. Graphite has strong electron emissions, thus adding pencil marks on the surface of the electrodes will reduce the time lag and lead to discharges having spark lengths in accordance to the distance predicted by Paschen's law. It is possible to measure the spark length for the HMM discharge, however, it is difficult to perform the same measurement for a brush-by situation. For that reason we only measured the currents for lengths that equal the distance predicted by Paschen's law. To obtain discharge currents having shorter lengths the well-established simulation method using Rompe and Weizel's spark resistance law was used.

Currents were measured at 1 kV, 5 kV, and 10 kV. The current waveforms for the HMM and waist-worn cases are shown in Figure 4. The repeatability of the measurements is insured by repeating them five times at each voltage level. The different waveforms are plotted in different colors. The parameters used to compare those two cases are shown in Table 1. The normalized peak current is obtained by normalizing to the charged voltage level. The normalized peak current decreases as the voltage increases. These test results are partially validated by the total charge, which increases in a nearly linear fashion. The peak current derivative is within the range of a typical value for the Paschen spark length.

For the HMM case, as the voltage increases, the normalized peak current decreases and is lower than 3.75 A/kV after 5 kV. For the waist-worn device, it is noteworthy that the normalized peak current is still higher than 3.75 A/kV even when the voltage increases to 10 kV and additionally using long spark lengths. This indicates that testing in contact mode will not be sufficient to ensure robustness in a brush-by discharge at 10 kV.

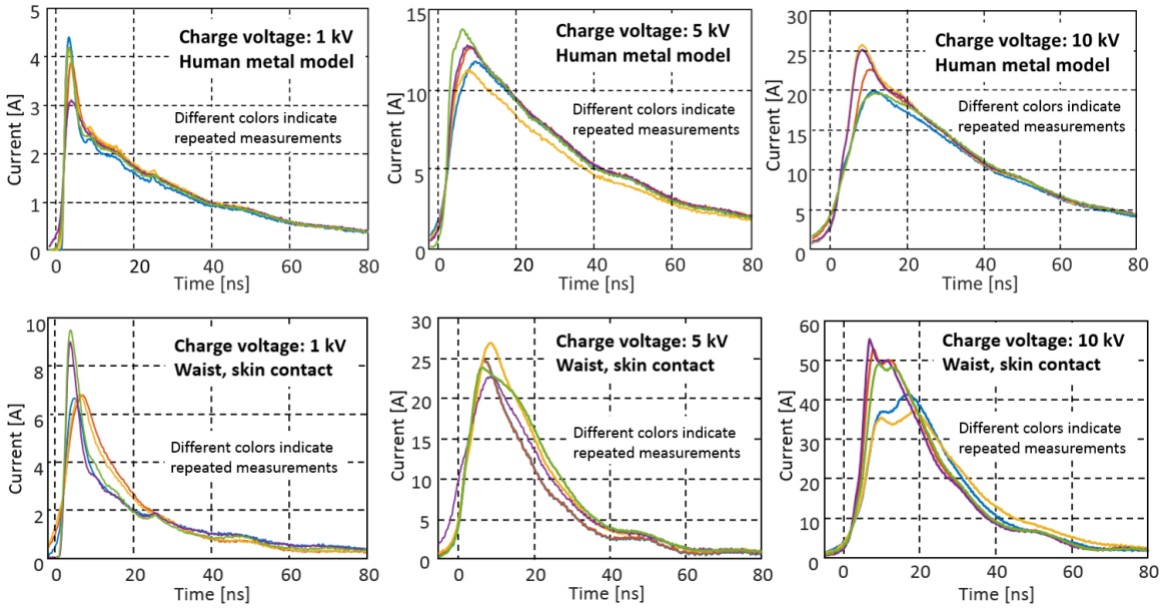

Figure 4. Measured currents for HMM and waist-worn devices at different voltage level.

Without a special test method for wearable devices they will be tested in the standard test set-up. The IEC 61000-4-2 standard set-up places the DUT on a 0.5 mm insulator which is on the horizontal coupling plane where an ESD generator applies a discharge to the DUT in contact or in air discharge mode [13]. To show how realistic this

set-up can represent the discharge current in the brush-by scenario, the wearable devices are tested in contact discharge mode using the IEC 61000-4-2 test set-up.

Table 1. Comparison of current measurements for HMM and waist-worn devices at different voltage levels.

Voltage [kV]	Set-up	Peak Current [A]	Normalized Peak Current [A/kV]	Total Charge [$\times 10^{-7}$C]	Rise Time [ns]	Peak Current Derivative [A/ns]
1	HMM	3.1~4.4	3.1~4.4	0.9~1.0	0.7~1.6	1.7~4.4
	Waist-Worn	6.7~9.5	6.7~9.5	1.3~1.4	1.2~3.7	1.6~5.8
5	HMM	11.1~13.7	2.2~2.74	4.9~5.1	1.8~4.5	2.5~6.1
	Waist-Worn	22.8~27.0	4.56~5.4	5.4~6.5	3.7~6.6	4.0~5.8
10	HMM	19.6~25.8	1.9~2.5	9.2~10.0	4.3~6.5	3.0~5.1
	Waist-worn	37.1~55.4	3.71~5.5	12.6~ 13.3	3.1~5.4	7.8~15.9

The discharge currents are compared with the currents measured using the brush-by and HMM set-ups illustrated in Figure 5. The red curve is the HMM measurement which was considered the reference. The brush-by set-up can have peak currents reaching two times higher for positions like waist and arm than those in the IEC 61000-4-2 set-up and HMM.

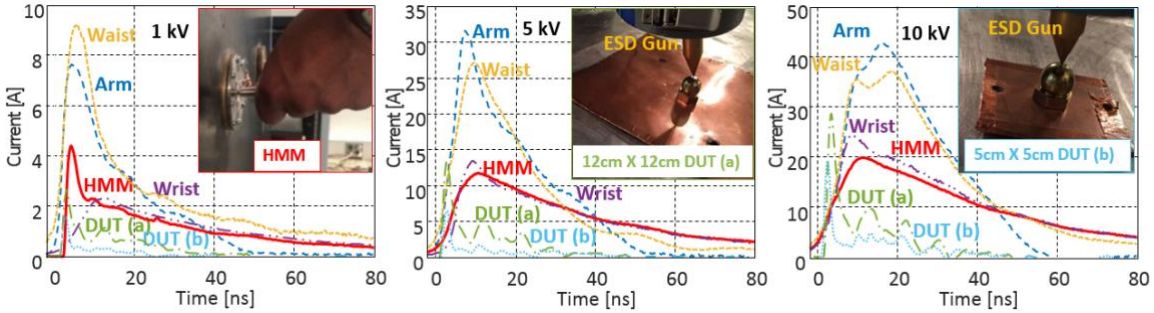

Figure 5. Discharge current from the brush-by set-up, HMM and the IEC 61000-4-2 set-up., For the HMM setup, the person holds an air discharge tip in hand and approach to current target; for the IEC setup, the DUT (see the DUT described in Figure 2) is placed on a 0.5 mm insulator which is on the horizontal coupling plane where an ESD generator applies a discharge to the DUT in contact mode, the size of the metal plate is 12 cm× 12 cm for DUT (a), and 5 cm×5 cm for DUT (b).

2.2. EFFECT OF DIFFERENT CONNECTIONS BETWEEN THE BODY AND THE DEVICES

The capacitance variations for the different connections between the body and the devices makes it necessary to investigate the effect of different possible connection conditions.

Moist thin cloth or direct contact lead to the same waveforms. As shown in Figure 6, dry insulating cloths or using a 0.5 mm plastic sheet having the dielectric constant of 3.5 also yielded similar results.

The local geometry around the discharge point, e.g., the distance from the body to the grounded plate dominates the discharge current. The overall posture, or the thickness of the insulating shoes affects the total capacitance, but it has little effect on the most important peak value and rise time.

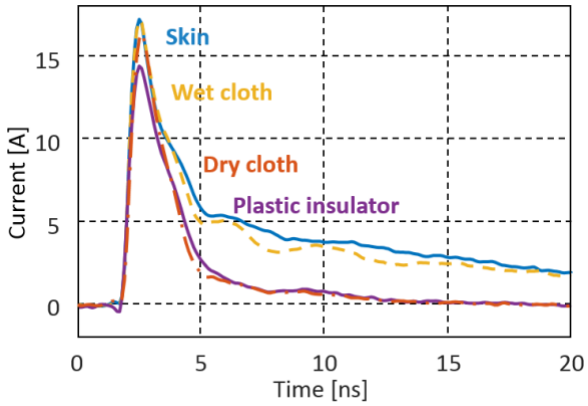

Figure 6. Discharge currents for different connections for the waist-worn device at 1 kV.

3. IMPEDANCE MEASUREMENTS AND SIMULATION

The human body impedance measured by the VNA can also be used to determine the step response, which directly reveals the ESD current waveform under the assumptions that the spark acts as an ideal switch. A second necessary assumption is linearity. The usefulness of this approach was shown in [14-16]. If a breakdown of the skin is a part of the current path, this method will only work [17] if the skin resistance is reduced, e.g., by using salt water as metal-to-body contact media.

3.1. EXPERIMENTAL SET-UP AND RESULTS FOR DIFFERENT POSITIONS

The impedance formed by the body and the vertical ground plane is measured using a coax connection having the same dimensions as the ESD current target, shown in Figure 7. This ensures similar postures during impedance measurement and discharge measurement.

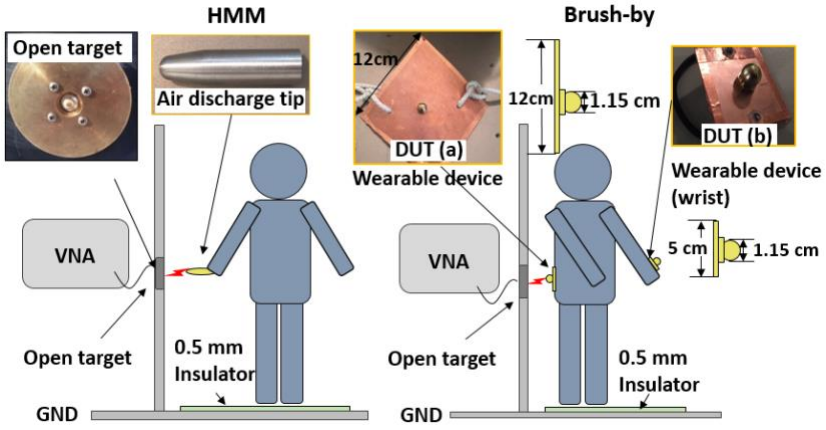

Figure 7. Impedance measurement set-up.

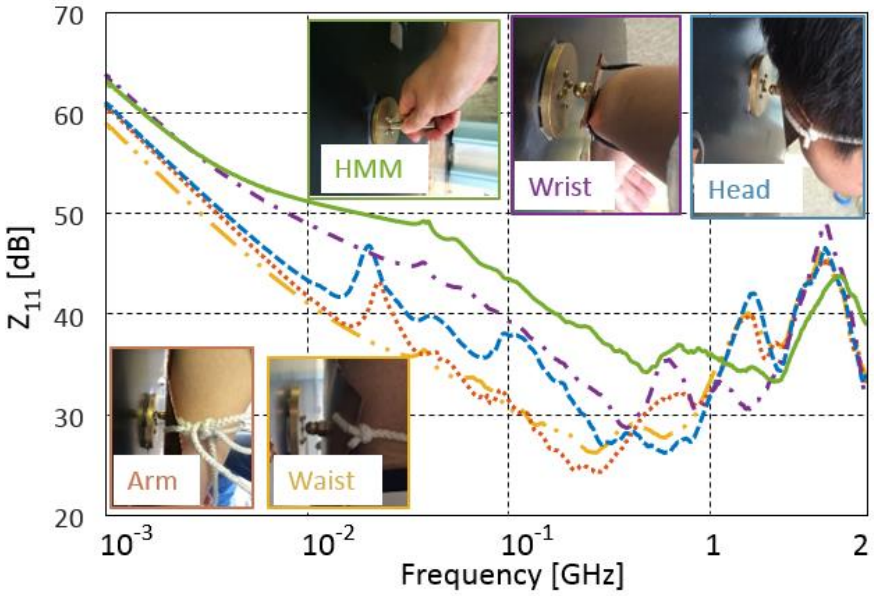

Figure 8. Impedance measurements for different positions of the wearable devices.

The capacitance between the human body and the ground plane can be measured using a capacitance meter to affirm the low frequency part of the impedance measurements by VNA. The impedances for different positions of the wearable devices

are shown in Figure 8, and the total charges obtained from the current measurements are presented again to show their correlation with the capacitance.

Table 2. Impedance measurement for different positons of the wearable devices.

Position	Capacitance Meter [pF]	VNA Measurement [pF]	Measured Total Charge [$\times 10^{-7}$ C]	Total charge from Reconstructed Current [$\times 10^{-7}$ C]
Waist	170	178	1.48	1.76
Arm	145	144	1.35	1.45
Head	150	144	1.14	1.36
Wrist	147	102	0.76	0.98
HMM	130	111	1.1	1.03

3.2. CURRENT RECONSTRUCTION FROM THE IMPEDANCE MEASUREMENTS

As mentioned above, because of experimental limitations only currents having spark lengths in accordance to Paschen's law were measured. Currents with shorter spark lengths were determined using simulation. This is based on the impedance measurement. The current is determined combining the measured impedances (transformed to time domain) with a spark resistance law.

At first this was performed assuming the spark is an ideal switch. Using the impedances measured by the VNA, PSPICE was used to reconstruct the current. A 1 kV step source was used as excitation and the reconstructed currents for different positions

are shown in Figure 9. The current values are large for 1kV. This is a result of the low impedance due to the proximity of the body to the grounded metal. Figure 8 shows that the impedance around a couple hundred MHz is only a few 10's of ohms. This leads to currents much larger than the 3.75A/kV used in the IEC standard for contact mode. The simulated currents are larger than the measured as this simulation assumes spark as an ideal switch. Other simulations use Rompe and Weizel's spark resistance law to provide a better match to the measurements [17][18]. The simulation data shown in Figure 9 describes the highest possible discharge current. However, the data shows that here is a significant drop along the spark even at 1 kV. The total charge does agree to within 20% as shown in Table 2.

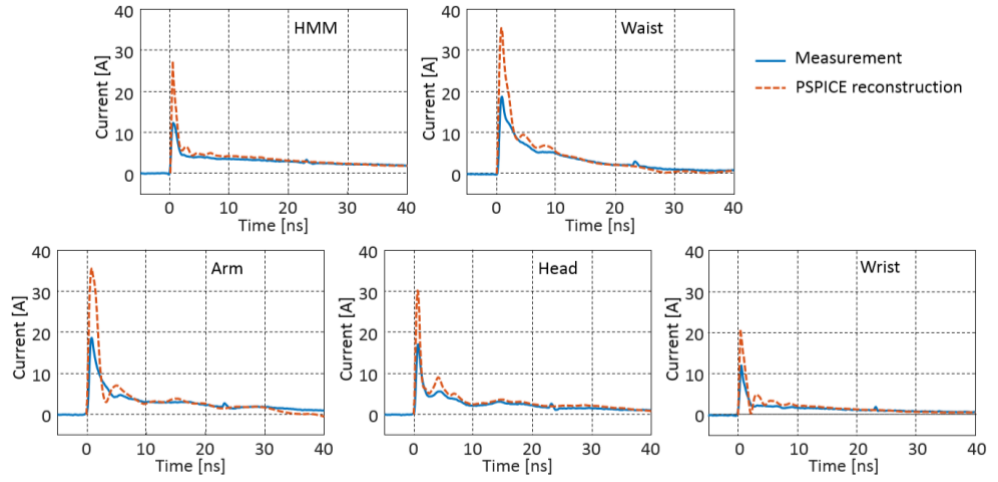

Figure 9. Comparison of currents obtained using PSPICE with measurements for different positions of the wearable devices and HMM scenario at 1 kV.

3.3. RLC MODELING

The impedance between ground and the wearable device attached to the human body can be approximated as an RLC circuit.

Using the RLC model of the body, the discharge current's upper limit can be simulated again using the assumption that the spark acts as ideal switch. Attention must be paid to the meaning of the rise time obtained in such a simulation, as the rise time may be a result of the voltage rise used in the simulation or of the high frequency impedance provided by the S-parameter and the RLC circuit [18] [19].

Figure 10 shows such a result for the HMM case. The impedance and the reconstructed current are compared with the measurement in Figure 11 again showing that the simulation provides an upper bound. The measured peak current is less due to remaining spark resistance effects during the discharge even at only 1 kV.

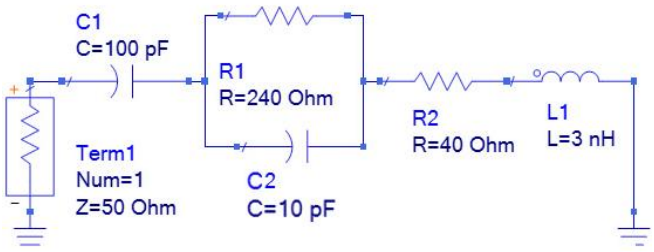

Figure 10. RLC model for HMM.

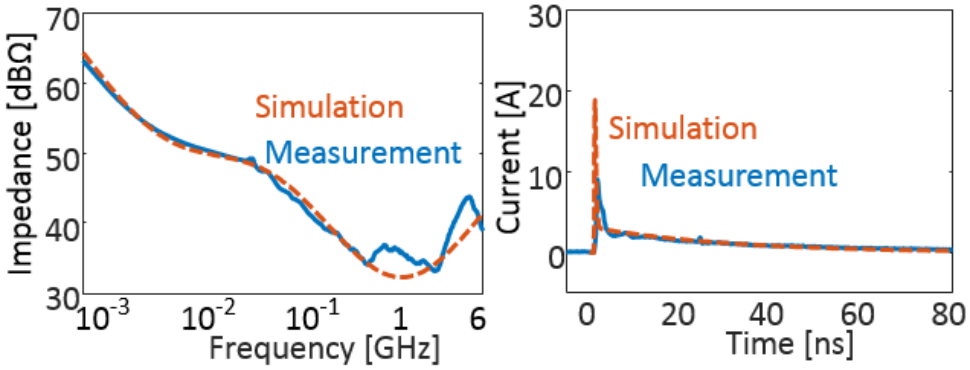

Figure 11. Impedance and the reconstructed current for HMM at 1kV.

The parameters in the RLC models are tuned to achieve the best match with the measured impedance for each position, the values of the RLC parameters are shown in Table 3. C1 describes the capacitance of the body to ground. It dominates the impedance behavior in the frequency range from 1 MHz to 200 MHz.

Table 3. RLC parameters of the wearable devices modeling for different positons.

Position	R1 [Ω]	R2 [Ω]	C1 [pF]	C2 [pF]	L1 [nH]
Waist	240	24	220	150	4
Arm	380	20	220	125	9
Head	220	24	150	40	8
Wrist	350	29	120	20	8
HMM	240	40	100	10	3

3.4. SPARK RESISTANCE

After developing the linear parts of the models, the spark resistance effect can be added using Rompe and Weizel's law.

$$\mathrm{r(t)} = \frac{l}{\sqrt{2K_R \int_0^t i(t')^2 dt'}} \tag{2}$$

where r(t) is the spark resistance at time t,l is the spark length, and K_R is a constant that is related to the gas pressure and type. Typically, Kr= (0.5~1) $\times 10^{-4}$ $\mathrm{m^2/(V^2 s)}$.

It has been shown that Rompe and Weizel's law can provide good predictions for the spark resistance having a spark length around or lower than the Paschen's value[11] [20] [21].

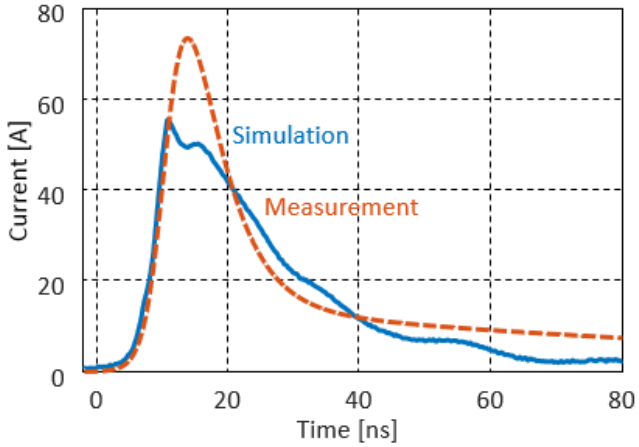

Figure 12. Comparing simulated and measured current for waist-worn device at 10 kV. l=2.7 mm, Kr= 0.5e-4 $m^2/(V^2s)$.

Figure 12 shown an example for the waist-worn position having a direct connection to the body. The voltage level is 10 kV and the Paschen length is used as spark length. The constant value found for the best match is $0.5 \times 10^{-4}\ m^2/(V^2 \cdot s)$.

In Figure 13 the discharge current is measured at 10 kV and simulated using the Paschen spark length and the RLC model obtained in section III C. Setting the RW constant to a value of Kr =$0.5 \times 10^{-4}\ m^2/(V^2 \cdot s)$ achieved the best match for the current derivative. The value of Kr is within its typical range. Kr was set for best match of the current derivative. The current derivative was selected as it relates to the maximal induced voltage for inductive coupling.

The simulation allows one to vary the spark length to investigate its effect. This allows to avoiding to perform measurements at higher voltages and at different spark lengths. Only the Paschen value is measured and used to compare to the simulation.

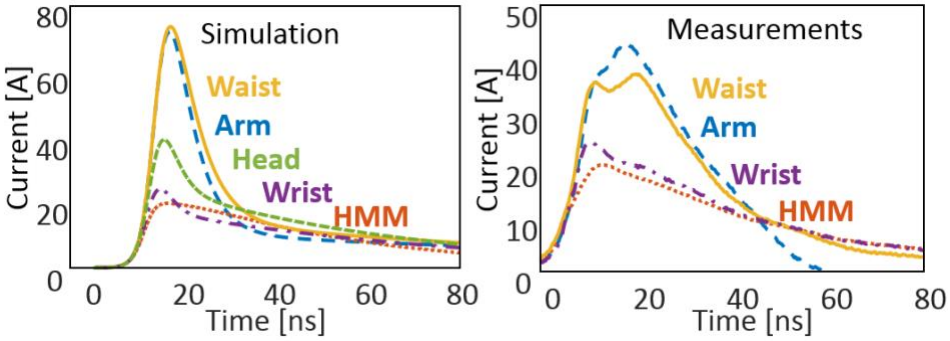

Figure 13. Comparison between simulation and measurements for different positions of the wearable devices at 10 kV. l= 2.7 mm, Kr= 0.5e-4 $m^2/(V^2s)$.

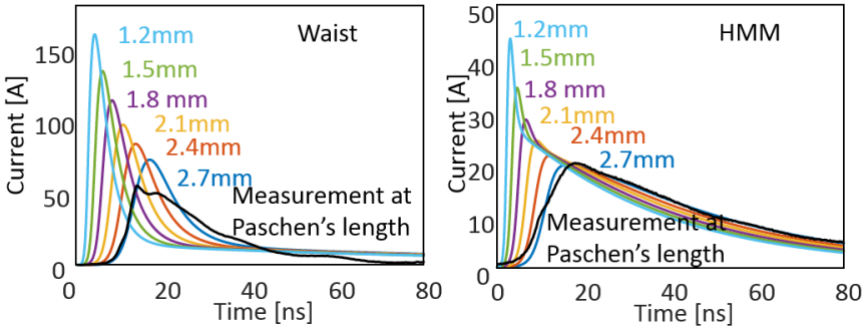

Figure 14. Current for waist and HMM simulation when the spark length is varied from Paschen length 2.7 mm to 1.2 mm.

From the simulation results shown in Figure14, we see for both the waist-worn device and the HMM set-up that the current increases as the spark length decreases. For 44% of Paschen's value, the peak increased almost twice as much as the in the Paschen length case, and the peak current derivative increased 8-10 times as much, which leads to stronger field coupling to the device.

The peak current derivative behavior for wearable devices is compared to the published data [1] in Figure . The best match was found for the Paschen case when Kr = $0.5 \times 10^{-4}\ m^2/(V^2 \cdot s)$ was used. However, the relatively low constant value may

underestimate the peak current derivative for shorter spark lengths. The range of the peak current derivative is given for the waist and HMM case to predict the peak current derivative while the upper limit is developed for a Kr = 1×10^{-4} $m^2/(V^2s)$, which is the commonly used value for the spark resistance simulation.

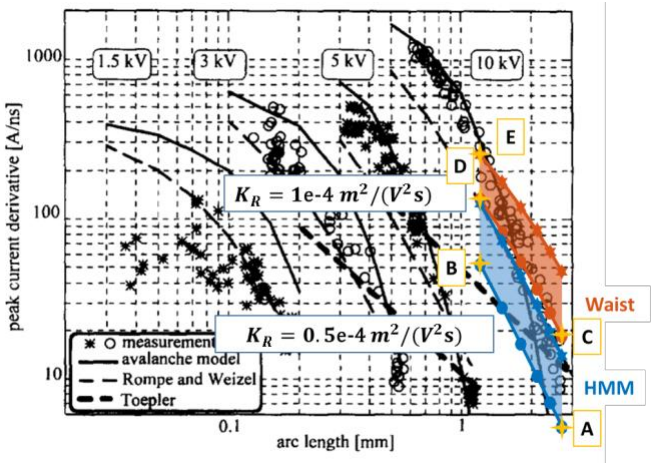

Figure 15. Comparison of the peak current derivative for simulated currents of a waist-worn device relative to discharges from a hand held metal part and literature data.

- The current derivative depends on the spark length. For example, if a Kr is set to 0.5×10^{-4} $m^2/(V^2 \cdot s)$ (point A vs. point B), then the derivative will increase from 2 A/ns to 60 A/n if the spark length is reduced from 2.7 mm (Paschen value) to 1.1 mm for the discharge of a human.
- If the same parameters are used for the discharge of a waist-worn device (point C vs. point D), then the current derivative is already 10x larger (20 A/ns) for the discharge at 2.7 mm and rises to about 150 A/ns for the reduced spark length.
- If the higher value is used for Kr (point E) then the discharge of the waist-worn device can reach 300 A/ns

No matter which spark length is used, or which reasonable value is assumed for Kr the discharge of the waist-worn device will always allow much larger current derivative values, thus posing a significantly larger risk of disturbances. Comparing current derivatives for the same parameters an average increase of the current derivative by four times was observed. This indicates a higher risk of disturbances and is more likely to lead to soft failures such as fast transient latch up [22].

4. SOFT FAILURE TEST

4.1. EXPERIMENTAL SET-UP

The IEC set-up is shown in Figure 6, both contact discharge mode and air discharge mode are used. The DUT is a camera module integrated with an LCD display. Discharges are applied to the shell of the USB connector. The discharge current is measured by the F65 current probe for the IEC set-up.

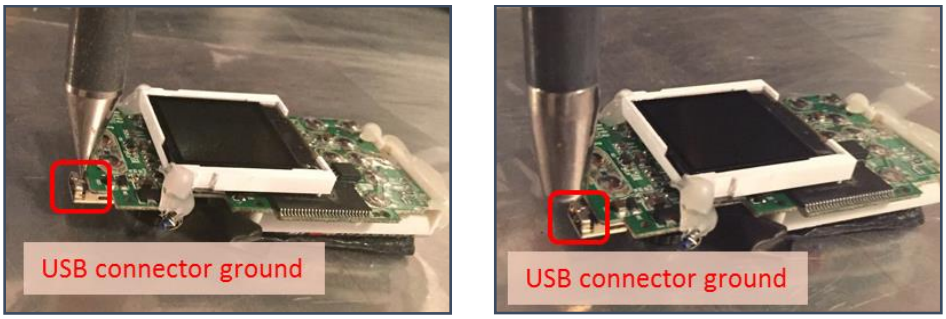

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Figure 16. IEC 61000-4-2 set-up, the plastic enclosure has been removed. (a) Discharge to the USB connector in contact mode. (b) Discharge to the USB connector in air discharge mode.

In the brush-by set-up, the DUT is mounted on the waist of one of the authors and then discharged to the current target. Two variations of the connection between the human and the wearable device are considered: Contacted and insulated. Figure shows these two type of connections. A situation in which the device is connected to the body is shown in Figure (a). Here, the connection is assured by copper on the backside. Figure (b) shows the case that the board is isolated from the body by a plastic layer of 0.5 mm thickness. The capacitance between the body and the DUT is approximately 30 pF.

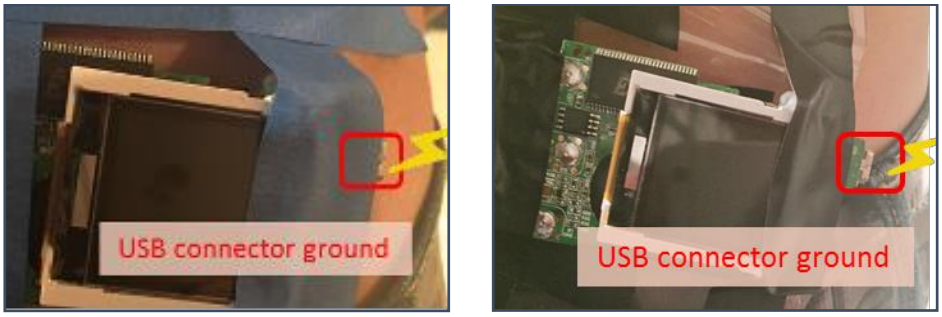

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Figure 17. DUT is placed on the body. (a) The DUT is directly connected to the body skin. (b) the DUT is isolated from the body by the plastic insulator.

4.2. SOFT FAILURES AND CORRELATED CURRENTS

Above a threshold, a soft failure occurs as shown in Figure . Both shut down and blurred screen have been observed. To ensure reliable results the test was started at 1 kV and incremented in 1 kV steps until a soft failure occurred. To ensure reliable results the test was repeated at least 50 times. If the DUT failed at the voltage level V_{fail}, and the failure could be reproduced at least three times, then a robustness level of V_{fail} was recorded.

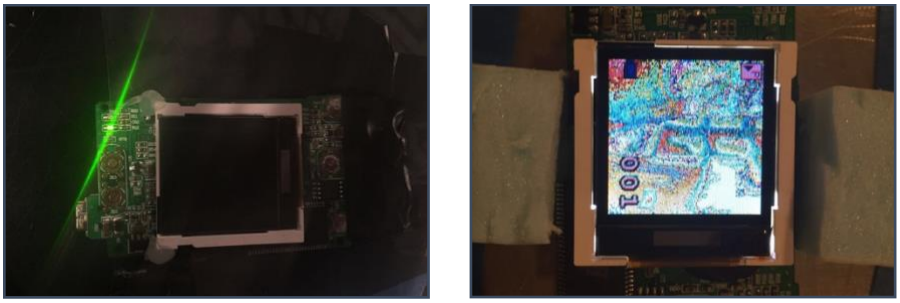

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Figure 18. Failure phenomenon caused by ESD. (a) Failure phenomenon: shut down. (b) Failure phenomenon: blurred screen.

Using the IEC set-up, failure levels of 3 kV in contact discharge mode and 2 kV in air discharge mode have been observed for the camera module. The discharge current were captured when the failure occurs and shown in Figure 19. Different colors represent data from repeated measurements.

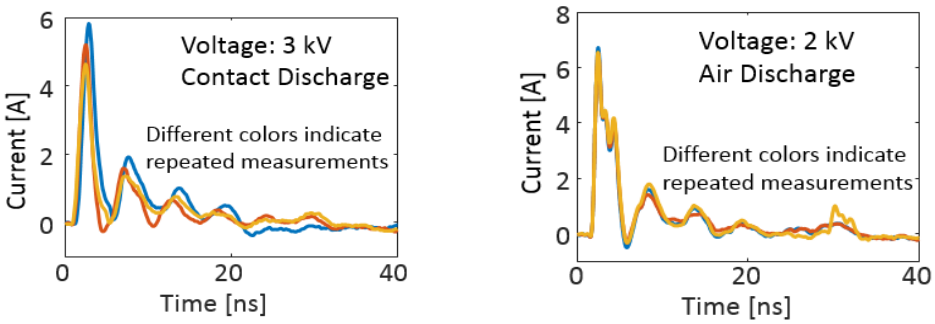

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Figure 19. Discharge current when the system is upset using the IEC set-up. (a) Discharge current for contact mode at 3 kV. (b) Discharge current for air discharge mode at 2 kV.

A similar procedure was followed for the brush-by test, but used smaller voltage increments as the failure threshold was lower. The test was started at 0.2 kV using 100 V steps. The wearable equipment may be insulated to the body, or it may contact the body. Both cases were tested. The discharge currents shown in Figure are captured at the failure threshold. Two types of DUT to body connections were investigated: insulated and in contact. The peak current for those two connections are in the same range. The effect of the different capacitance values begins to dominate after the first 3 ns.

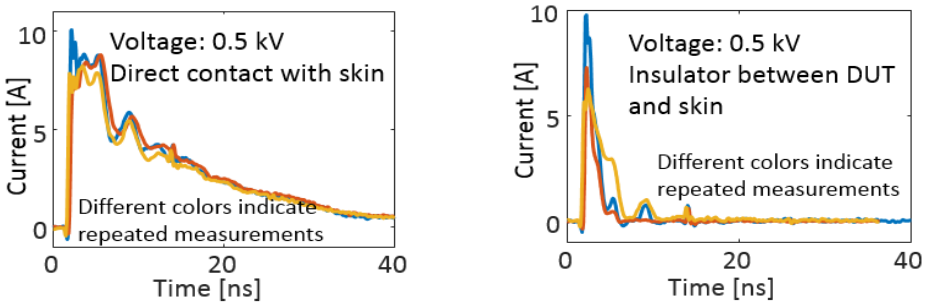

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Figure 20. Discharge current when the system is upset using the brush-by set-up. (a) Discharge current for direct contact at 0.5 kV. (b) Discharge current for insulator between the DUT and skin at 0.5 kV.

The failure level for the IEC set-up and the brush-by set-up are summarized in Table 4, four different kinds of set-ups were used to determine the failure level for the wearable device. For the brush-by situation a much lower failure level was observed which indicates that the IEC set-up will underestimate the ESD risk for the wearable device. To match the currents an IEC test would have to use at least double the voltage as test level.

Table 4. Comparison of failure level for different set-up.

Set-up	Failure Level	Peak Current at the Failure Level	Failure Phenomenon
IEC 61000-4-2 set-up contact discharge mode	3 kV	5-6 A	Blurred screen
IEC 61000-4-2 set-up air discharge mode	2 kV	7 A	Blurred screen
Brush-by set-up for direct connection	0.5 kV	8-10 A	Blurred screen Shut down
Brush-by set-up for indirect connection	0.5 kV	6-10 A	Blurred screen Shut down

5. CONCLUSION

The investigations answer the question whether IEC 61000-4-2 ESD testing will ensure ESD reliability of wearable equipment as well as it ensures it for table top equipment. This is investigated by comparing the discharge current levels, the impedance seen between the ground and the body, and the failure levels obtained in testing a sample DUT.

The results show that the current measured in the brush-by scenario can reach values twice as high as the current specified in the IEC standard. This is caused by the much lower impedance caused by having a body close to a metal structure such as a door frame. It is known that the peak current for the air discharge does not increase linearly as

the voltage increases. The peak current of a wearable devices, however, is still higher than the 3.75 A/kV specified by the IEC standard at voltages as high as 10 kV at Paschen spark length.

Rompe and Weizel's law provides predictions on the peak current derivative when the spark length is varied. The increasing peak current derivative with shorter spark length indicates stronger field coupling to the devices.

Soft failure testing on a DUT provides additional evidence that the brush-by scenario may endanger wearable equipment. The soft failure voltage threshold levels observed between IEC testing and brush-by testing showed a ratio of 1:6 which is supported by the measured current values. Although these results cannot be taken as general proof, it is consistent with the theoretical investigations and measurements. It indicates that IEC testing on the HCP is probably insufficient for ensuring the robustness of wearable equipment. A higher voltage level may be needed if IEC testing is used to ensure robustness for wearable equipment.

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III. TRANSIENT RESPONSE OF PROTECTION DEVICES FOR A HIGH-SPEED I/O INTERFACE

ABSTRACT

System-efficient electrostatic discharge (ESD) design (SEED) models of a diode and transient voltage suppressor (TVS) were developed to study their transient response in a high-speed input/output (I/O) interface. Previously reported SEED models were improved to strengthen their convergence stability and facilitate accurate predictions over a wide range of conditions. These improvements were required to accurately capture the race conditions between the TVS and on-chip diode, where the diode's turn-on may prevent turn-on of the TVS. Simulations and measurements were performed to demonstrate the impact of the ESD pulse's rise time on race conditions. During a race, results showed the worst-case quasi-static diode current could be twice as high for long rise-time pulses than for short rise-times where the TVS does not turn on, and on-chip diode current may be larger at low test voltages than at high test voltages where the TVS does turn on. Adding a small passive impedance between the external TVS and the on-chip diode helps the TVS turn on and reduce the current through the on-chip diode by more than 50%. Similarly, lengthening the trace between the TVS and diode could reduce on-chip diode current by up to a factor of two.

1. INTRODUCTION

With the increasing speed of digital communications channels, the input/output (I/O) interface is at higher risk to electrostatic discharge (ESD) due to the thinner gate oxide of the I/O drivers and other FET characteristics. For a 35 nm complementary metal oxide semiconductor (CMOS) technology, the gate oxide film can be as thin as 1.2 nm, making it susceptible to damage from relatively small gate-to-source or gate-to-drain voltages. As logic gates shrink, there is increasing pressure to shrink the size of I/O cells, which means that the energy transferred during an ESD event can easily cause thermal damage to the on-die drivers and associated ESD protection [1].

Although the input/output (I/O) pin is designed with on-chip diode protection, the protection may not be sufficient to guarantee robust ESD design due to its limited capability for energy dissipation [2]. An external transient voltage suppression (TVS) device can clamp the peak voltage seen by an IC during an ESD event and can significantly reduce the current into the I/O pin [3-5].

There is a common misconception that meeting component-level immunity standards [6] will ensure system-level immunity [7]. Component-level ESD tests use human body model (HBM) ESD pulses with long rise times of up to tens of nanoseconds [8], which may be insufficient to guarantee passing the IEC system-level test [7]. The IEC-61000-4-2 standard, for example, specifies use of the human metal model (HMM), which has a much faster initial rise time and a higher peak. ESD events in real systems, modified through coupling and parasitics from the location of the ESD event to the point

where it encounters the IC and TVS, may differ substantially from the standard pulses [10].

SEED simulation provides a methodology for ensuring the system's robustness against ESD events. The TVS device characteristics alone do not ensure it will turn-on when placed on the PCB along with the IC. Test structures including the external TVS and the on-chip ESD protection were used to investigate race conditions in [11, 12], to understand when the TVS would and would not protect the IC and the influence of passive components and the ESD pulse rise time on TVS performance. Results showed that an extra inductance between the TVS and on-chip diode, and the associated rapid voltage change at the TVS during a fast transient event, is important for helping the external TVS turn on to protect the IC.

The external TVS device and on-chip ESD protection diode were modeled in [11, 12] using the simulation framework shown in Figure 1 [13, 14]. This framework has been shown to accurately model the quasi-static IV characteristics and the transient behavior of ESD protection device. The framework includes both a passive linear network and a non-linear modeling block to account for conductivity modulation and snapback delay. The simulation model used in [11] was preliminary and used to predict the transient behavior of a protection device for an ideal TLP source, however, the convergence stability of the model and accuracy need to be improved if the model is to be implemented in a complex system with multiple ESD protection devices. This model will be improved in the following paper using a better-defined switch for the conductivity modulation and the snapback delay module. Improvements were also made to the overall measurement methodology.

The TVS model will be developed in section II and validated against TLP measurements. In section III, the model will be incorporated into a larger model of an I/O port, including a TVS device and on-chip diode, to evaluate the impact of the TLP rise time and the use of passive impedances between the TVS and the on-chip diode on the TVS performance. In section IV, the effects of including a filter between the TVS and I/O pin and the location of the TVS are investigated through simulation.

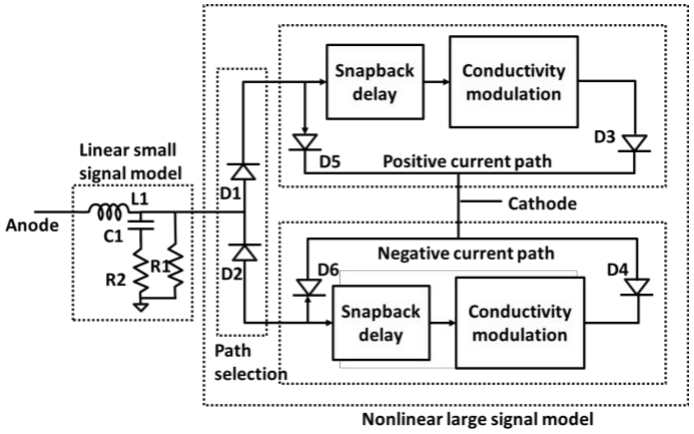

Figure 1. SEED model framework for TVS devices.

2. SEED SIMULATIONS

Ensuring an IC does not fail during a race condition, where the on-chip diode turns on and prevents the TVS from turning on and protecting the diode, is an important part of evaluating the quality of the ESD protection strategy. To predict race conditions and to understand the effects of passive impedances between the external TVS and the on-chip diode and the effects of ESD pulse rise time, it is essential to model the TVS device transient response accurately. Several improvements to the TVS and diode models

from [11] are implemented and tested in the following section. A silicon based ESD protection device (NExperia PUSB3FR4) for ultra high-speed interfaces was used as the external TVS protection and a unidirectional silicon based ESD protection device (NExperia PESD5V0L1USF) was used to represent the on-chip protection diode inside the IC.

2.1. SEED MODEL IMPROVEMENTS

Improvements were made to the portions of the device model responsible for conductivity modulation, snapback delay, and its quasi-static IV device behavior.

2.1.1. Quasi-static IV. For a non-snapback diode, the quasi-static IV characteristics can be represented using a modified PN junction model with diodes D3 and D4 as shown in Figure 1. For the external TVS, the snapback behavior needs to be accurately modeled to show the threshold voltage above which the TVS starts to turn on. Small errors in the turn-on threshold for either the diode or TVS were found to substantially change the simulation result during a race condition.

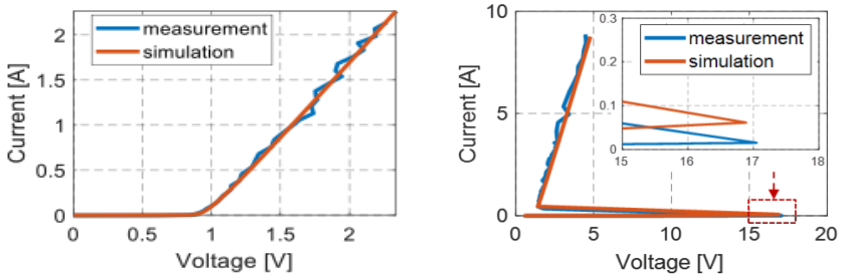

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Figure 2. Quasi-static IV characteristic for the on-chip diode and the external TVS device. (a) IV curve for on-chip diode. (b) IV curve for external TVS.

Fine tuning the model to accurately capture the IV curve at the turn-on point is crucial to achieve accurate results. The quasi-static IV for the on-chip diode and the external TVS after fine tuning of the model are shown in Figure 2.

2.1.2. Conductivity Modulation. The conductivity modulation model predicts the "overshoot" in the TVS or diode voltage beyond the voltage predicted by the quasi-static IV curves and the inductance associated with the small signal model. Conductivity modulation results from limitations in the rate of change of carrier concentrations in the device (overshoot also occurs from parasitic inductance which is accounted for separately in the small-signal model block). The model of conductivity modulation in [11] used only the components shown in black in Figure 3. This circuit allows for a delay in the turn-on behavior of the diode but causes a relatively fast transition between the case where the diode is "off" and not conducting to the case where it is "on". The sudden change in state can cause stability issues in the simulation.

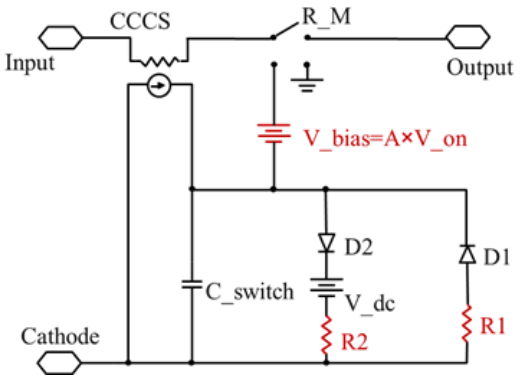

Figure 3. Conductivity modulation model.

The resistors R1 and R2 were added to the model as shown in Figure 3 to avoid none convergence that occurs in rare circumstances. The bias voltage was added to allow

for better tuning of the variable resistance of the voltage-controlled switch and allows a smooth transition of the diode from an “off” to an “on” state where its behavior is dominated by its quasi-static characteristics. The switch resistance transition behavior before and after adding the additional components is shown in Figure 4 (a). The corresponding transient response of the on-chip diode during a TLP event is shown in Figure 4 (b)(c).

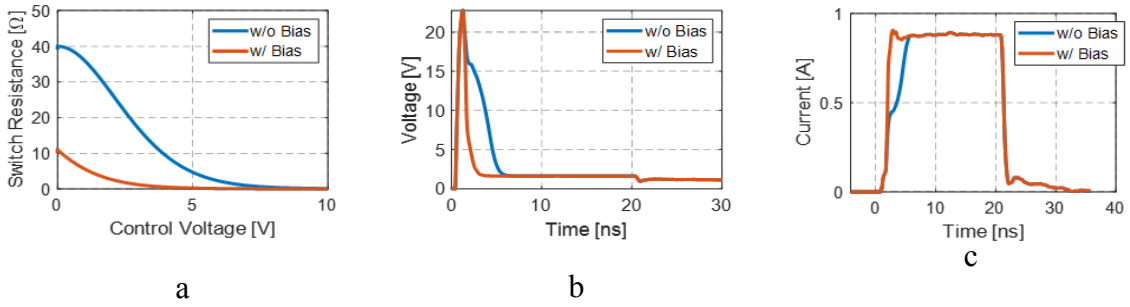

Figure 4. Impact of the bias voltage on the on-chip diode conductivity modulation model. (a) Switch resistance as a function of control voltage with/without a bias voltage. (b) Transient voltage waveform. (c) Transient current waveform.

2.1.3. Snapback Delay. A similar methodology was used to improve the snapback delay model as shown in Figure 5. An additional voltage-controlled switch and a RC integration circuit was added to further expand the ability to tune the turn-on time and resistance of the switch. The change in the switch resistance with the control voltage is shown in Figure 6 (a). The effect of the additional switch and the RC circuit on the transient waveforms are shown in Figure 6 (b)(c). As before, creating a smooth transition in the switch resistance improved the accuracy and stability of simulations using the device model.

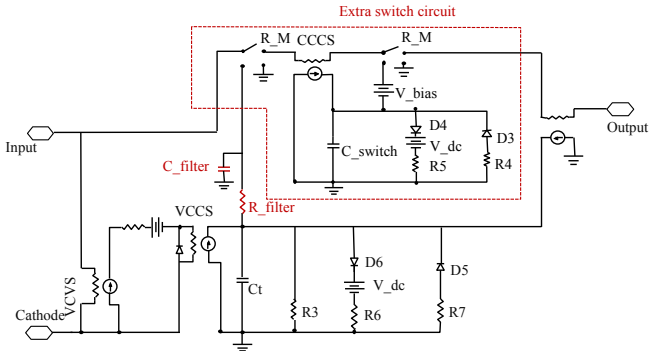

Figure 5. Snapback delay model.

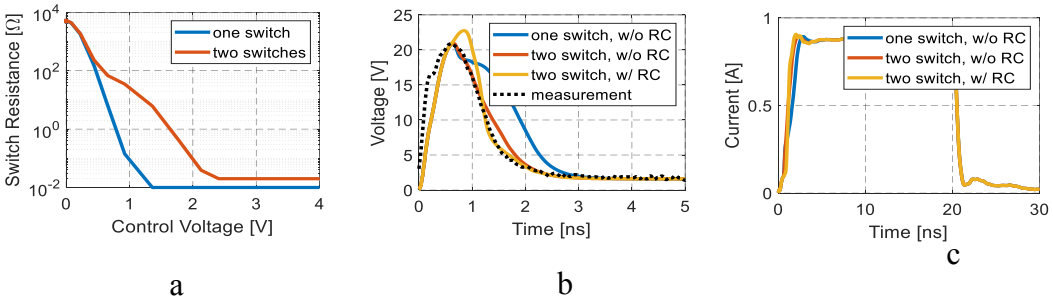

Figure 6. Effect of adding additional voltage-controlled switch and RC circuit to snapback delay model for the external TVS; The TLP voltage was 60V. (a) Switch resistance as a function of control voltage with/without added voltage-controlled switch. (b) Transient voltage waveform. (c) Transient current waveform.

2.2. TRANSIENT RESPONSE OF TVS AND DIODE

The transient current and voltage waveforms for the TVS (NExperia PUSB3FR4) and on-chip diodes (NExperia PESD5V0L1USF) are shown in Figure 7 and Figure 8 when reacting to TLP pulses of different magnitudes. A TLP was used as an excitation source because of its good repeatability and because of the ease of changing its rise time using low pass filters. The on-chip diode turns on for each of the waveforms in Figure 7, as they are above its 0.7 V turn-on voltage. The external TVS does not turn on until the

TLP source voltage is above 28 V. The simulation models do a reasonably good job of predicting both the transient and steady state voltage and current levels for the on-chip diode and the external TVS.

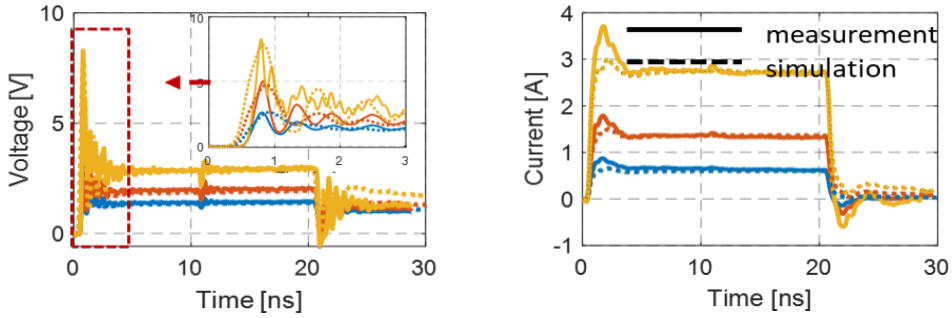

Figure 7. Transient waveforms for the on-chip diode for different applied TLP voltage levels. The color indicates the TLP voltage: blue: 19 V, orange: 42 V, yellow: 84 V. (a) Transient voltage waveform. (b) Transient current waveform.

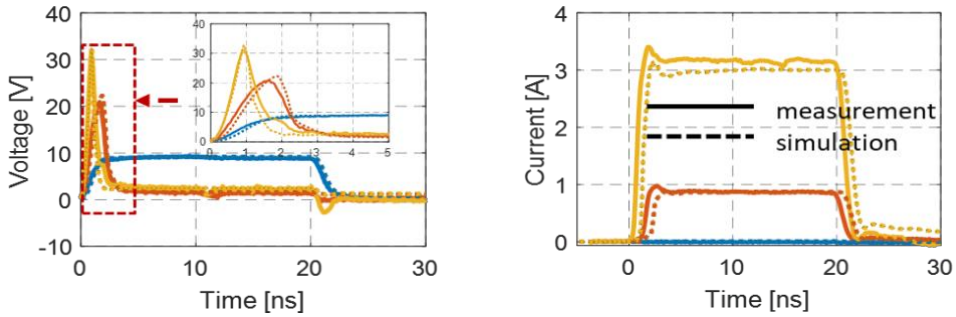

Figure 8. Transient waveforms for the external TVS for different applied TLP voltage levels. The color indicates the TLP voltage: blue: 9 V, orange: 28 V, yellow: 93 V. The TVS does not turn for less than a 28 V TLP voltage. (a) Transient voltage waveform. (b) Transient current waveform.

3. IN-SYSTEM TRANSIENT RESPONSE

Once good models of the TVS and on-chip diode were created, these models were used to investigate the interaction between the devices when used together in a system, the impact of adding passive impedances between them, and the impact of the pulse rise time.

3.1. MEASUREMENT SETUP

A test board was built that simulates a typical I/O configuration consisting of an on-chip diode and an external TVS. The board allows for measurement of the voltage and the current associated with each device. Current is measured using inductive probes integrated into the PCB which have been used in previous studies [11]. The PCB layout was improved over [11] by reducing the length of the inductive probes from 4 mm to 2.5 mm to better capture high-frequency components, and by "shielding" the probe components from the TVS and trace by placing them on the other side of the board (Figure 9). The induced voltage measured by the loop probe was converted to current using the reconstruction process discussed in [11], only the transfer impedance from the input port to the probe output was used in the reconstruction. Here the full S-parameter matrix was used, as including the reflection coefficient further improves the accuracy. The accuracy was demonstrated by comparing the reconstructed current with a direct measurement of current at a matched termination at the end of the board. The difference between the current found using the integrated loop probe and the current found at the matched termination was less than 5% for a 20ns TLP pulse.

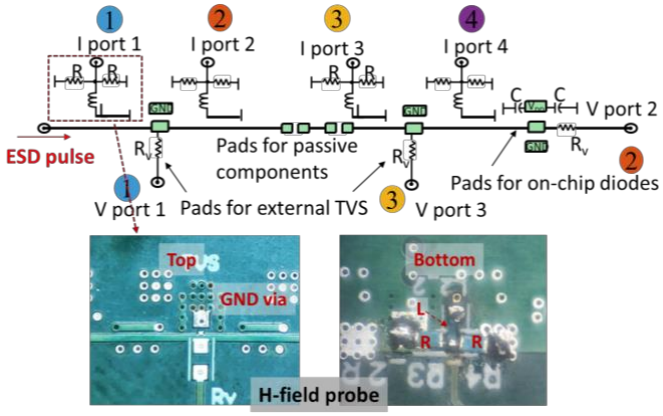

Figure 9. The test board allows for device current and voltage measurements.

3.2. CIRCUIT SIMULATION

Figure 10 shows a simplified circuit diagram for the test board. It is worthwhile to note that the microstrip trace between the TVS and the on-chip diode must be modeled as a lossy transmission line. This transmission line impacts both the level and delay of the reflections between the devices and is critical for accurate SEED model results.

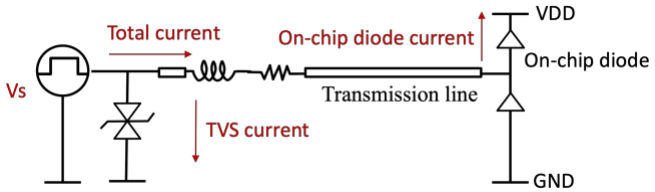

Figure 10. Circuit diagram for the test board and TLP source. The added resistance and inductance were varied among experiments.

Example waveforms are shown in Figure 11 for a 45 V TLP. The simulation accuracy is improved using the revised SEED model compared to the results in [11], especially for the first 0~5 ns when the transient response is dominated by the

conductivity modulation and snapback delay model. The quasi-static current matches the measurements within 5%. Similar performance was observed at other TLP levels.

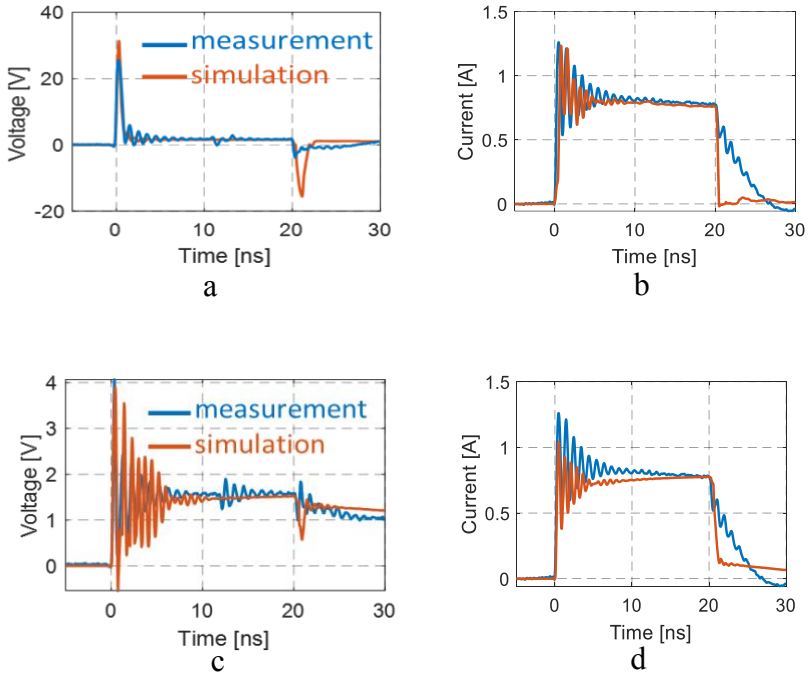

Figure 11. Transient waveforms for the external TVS and the on-chip diode when a 45 V TLP was applied to the test board in Figure 9. (a) Voltage at external TVS. (b) Current through external TVS. (c) Voltage at on-chip diode. (d) Current through on-chip diode.

3.3. IMPACT OF TLP RISE TIME

The peak voltage on the trace is positively correlated with the derivative of current as a result of the parasitic inductance of the devices. The rise time of the ESD pulses will thus play a significant role in the transient response of the system and the turn-on behavior of the TVS. Ultimately, the designer wants to limit the current flowing into the on-chip diode.

Figure 12 shows the on-chip diode quasi-static current at different TLP voltage levels and different TLP pulse rise times. The measured data were obtained by increasing the TLP voltage from 13 V to 93 V in 5 V steps. The quasi-static current through the on-chip diode current starts to drop when the TVS turns on. The point where the TVS turns on is highly dependent on the TLP pulse rise time, since the voltage across the on-chip diode inductance goes up with the rise time. For example, in the case where there are no components between the external TVS and the on-chip diode, the TVS turns on with a 28 V TLP voltage with a pulse rise time of 0.4 ns, but does not turn on until the TLP voltage exceeds 83 V for a pulse rise time of 5 ns. For the slower pulse rise time the on-chip diode current can reach as high as 2.6 A, which may damage the IC. For the faster pulse the current is limited to 1 A. Figure 13 shows examples of the transient waveforms for different excitation rise times at the same TLP voltage level for the case when there are no components placed between the external TVS and the on-chip diode. A low pass filter between the TLP source and the board varies the rise time from 0.4 ns to 5 ns while the TLP voltage level remains at 65 V. The TVS turns on for rise times less than 5 ns and does not turn on for the 5 ns rise-time pulse. The on-chip diode current is much higher for the slow-rise time pulse than for the other cases. The simulation accurately predicts the measured results.

3.4. IMPACT OF COMPONENTS BETWEEN THE TVS AND ON-CHIP DIODE

Series resistance or inductance between the TVS and on-chip diode contributes to the development of voltage at the external TVS and will thus help ensure an earlier turn-on of the TVS. Figures 12 and 14 show the impact of placing different values of

resistance or inductance between the TVS and diode. The component values were selected to be comparable to the parasitic inductance or resistance of a signal line or comparable to the inductance of a common-mode choke widely used for USB 3.0 I/O interfaces. Results show the impact of the components both as a function of the TLP voltage and of the TLP rise time.

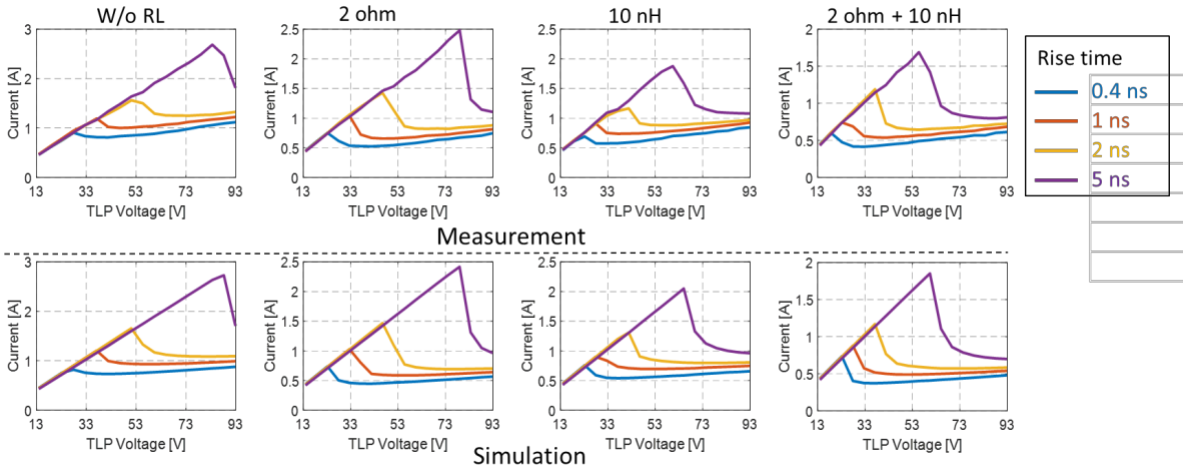

Figure 12. Quasi-static current through the on-chip diode as a function of rise time and TLP voltage. Rise time varies from 0.4 ns to 5 ns.

As expected, adding resistance or inductance allows the external TVS to turn on for a lower TLP voltage, thus reducing the worst-case current flowing to the on-chip diode. Adding these components also resulted in lower diode currents even at voltages where they are not required to turn on the TVS. For example, for the 5 nS rise-time, the turn on voltage was reduced from 83 V with no components to 53 V when a 2 ohm resistor and 10 nH inductor were between the TVS and diode. An example of transient waveform is shown in Figure 15 when the TLP rise time was 0.4 ns. The current through

the on-chip diode was reduced by 50% when a 2 ohm resistor and 10 nH inductor were added between the TVS and diode. Depending on the rise time, the worst-case diode current was reduced by 60-70% by adding both resistance and inductance. The current for TLP voltages above the point where the TVS is firmly turned on (e.g. above 50 V for a 1 ns rise time) were reduced by 50-60%.

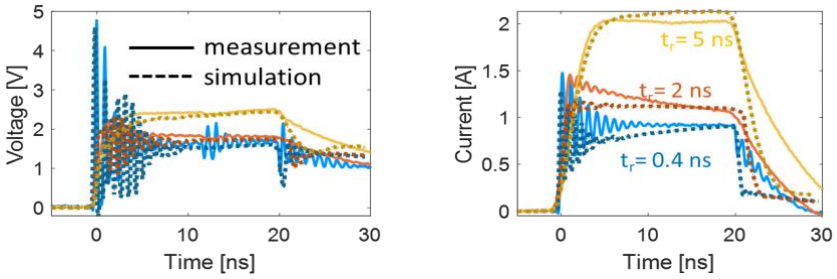

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Figure 13. Transient voltage and current for the on-chip diode when applying 65 V TLPs with different rise times (no passive components added). (a) Voltage at the on-chip diode. (b) Current through the on-chip diode.

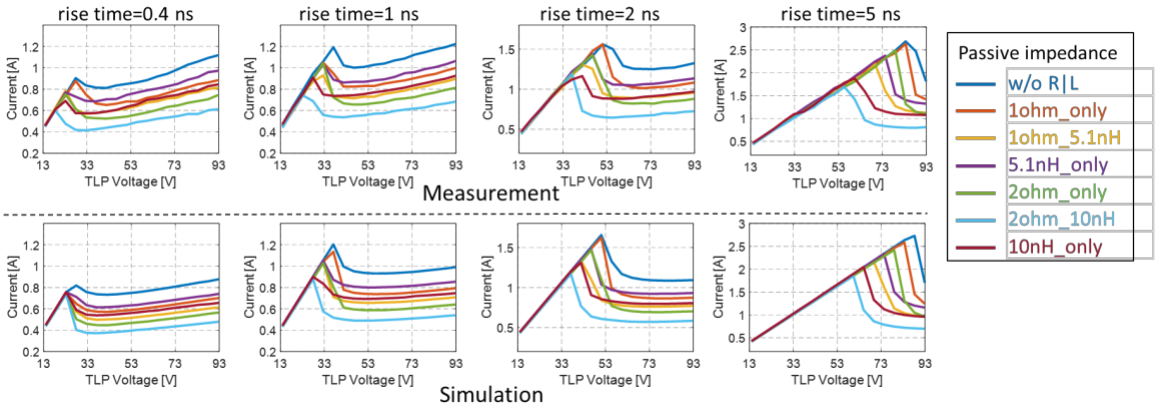

Figure 14. Quasi-static current for the on-chip diode Different passive impedance between the external TVS and the on-chip diode.

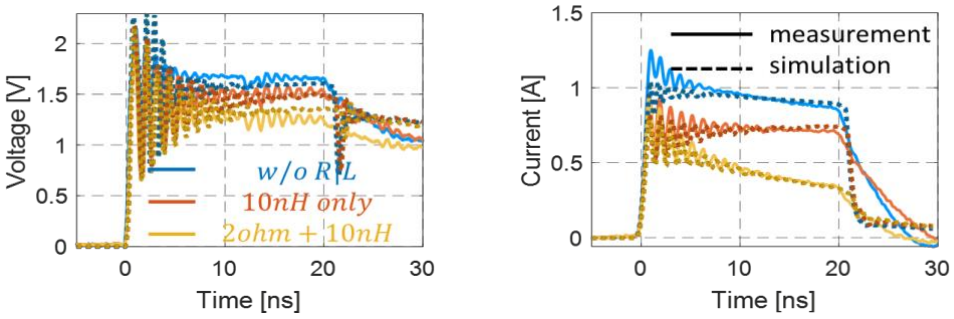

Figure 15. Transient waveform for the on-chip diode with different passive impedances between the external TVS and the on-chip diode. The TLP voltage was 45 V. (a) Voltage at on-chip diode. (b) Current through on-chip diode.

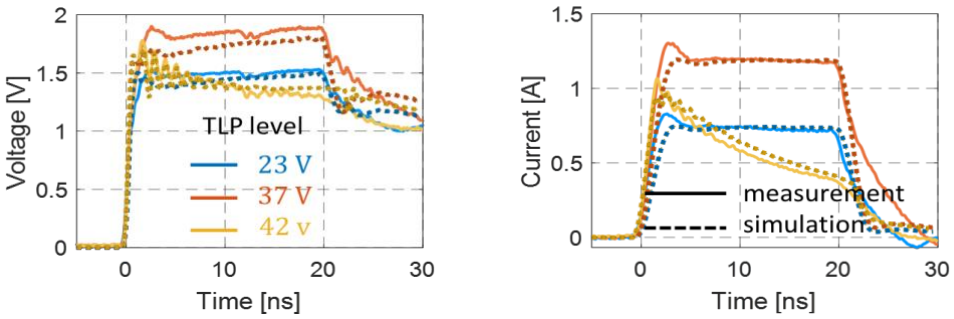

Figure16. Transient waveform for the on-chip at different TLP voltage. (a) Voltage at the on-chip diode. (b) Current through the on-chip diode.

Figures 12 and 14 show that the on-chip diode current increases with the TLP voltage until the external TVS turns on. At that point, the diode current quickly drops for a higher TLP voltage before slowly rising again. Figure 16 shows a case where the on-chip diode quasi-static current is the same for both a 23 V and 42 V TLP, and is higher for a 37 V TLP. The fact that higher diode currents may be seen for lower TLP voltages

is worth noting, as it means that passing the highest TLP voltage test does not guarantee failures may not occur at lower levels.

4. DISCUSSION

Accurately measuring the on-board current and voltage waveforms during rapidly changing transients was a challenge. The modified PCB design improves the measurement accuracy of the integrated loop probes, especially for the first 0-5 ns of the ESD pulse. To improve results, we provided an electric field shield between the trace and the probe, used a shorter coupling stub trace, and placed all other probe components on the bottom side of the board to reduce the direct coupling from the trace to other portions of the probe circuitry. Results were also improved by using a more accurate calibration process than in [11] which used only the transfer impedance of the probe. Here, the full 2-port S-parameter matrix between the trace and the probe was used in the deconvolution process to determine trace current. These modifications to the measurement process were required to get a good match between measurements and simulations.

The simulation model presented in [11] is able to determine the TLP voltage and on-chip diode current when the external TVS starts to turn on, but there are noticeable discrepancies between the measured and simulated transient waveforms, especially for the first 0~5 ns of the ESD pulse. These discrepancies are due to the insufficient accuracy of the SEED model. The modeling framework was improved here using additional switching components to allow finer tuning of the model, and to prevent instability issues during simulations. A smooth turn-on transition is particularly important when there is

substantial interactions between the TVS and diode through reflections along the trace transmission line. Very small errors in the model could lead to large errors in the simulation of the system which includes both the TVS and diode. The simulated transient waveforms match the measured diode and TVS voltage and currents within 10%. The TLP voltage level and the diode current when the external TVS starts to turn on matches the measurements within 20%.

Added resistance or inductance can significantly improve the turn-on of the TVS and decrease the worst-case current seen by the on-chip diode. While even a 2-ohm resistance can have a substantial impact on performance, signal integrity issues should be carefully considered before adding any impedances between the devices.

Filtering of the signal on the USB line can also have an impact on TVS turn on. To demonstrate, two low pass filters with different topologies but same frequency response were placed between the external TVS and the on-chip diode. Figure 17 shows the frequency response of the filters. The peak current and quasi-static current versus the TLP input voltage are compared in simulation for the different filters in Figure 18. Similar to adding other impedances between the TVS and diode, the external TVS turns on at a lower voltage level when adding the filters since the inductance of the filter increases the peak voltage at the TVS. The worst-case current through the on-chip diode is reduced by 20% using the T filter. Although the pi filter has a similar frequency response as the T filter, it reduces the peak current by less (10%) than the T filter because of its lower overall inductance.

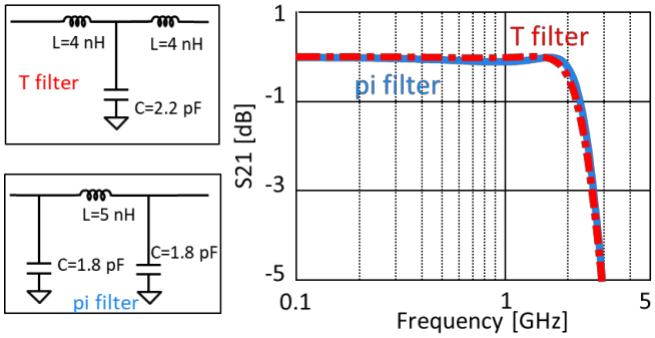

Figure 17. T filter and pi filter circuit and their frequency response.

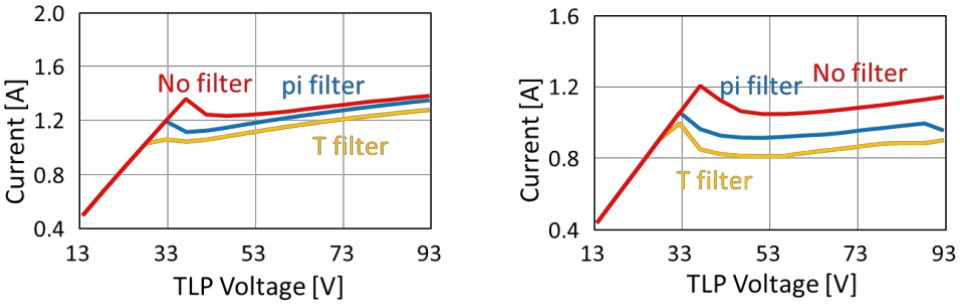

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Figure 18. Peak current and quasi-static current through the on-chip diode as a function of TLP voltage and the filter configuration placed between the external TVS and the on-chip diode. (a) Impacts on the peak current. (b) Impacts on the quasi-static current.

The location of the TVS relative to the IC has been reported to have a strong impact on the TVS behavior [16]. To test this possibility, the distance between the TVS and the on-chip diode was studied in simulation. The diode peak current and quasi-static current versus the TLP voltage is compared in Figure 19 for distances of 2.5, 4.5, and 6.5 cm. The closer the TVS to the on-chip diode, the higher the TLP voltage before the TVS turns on. When the TVS is placed 2.5 cm away from the on chip diode, the external TVS does not turn on until the TLP voltage exceeds 76 V. When the TVS is placed 2.5 cm

away the worst case diode current is roughly twice as high as at 6.5 cm. The current peak reaches 2.9 A which indicates a higher risk of damage to the IC.

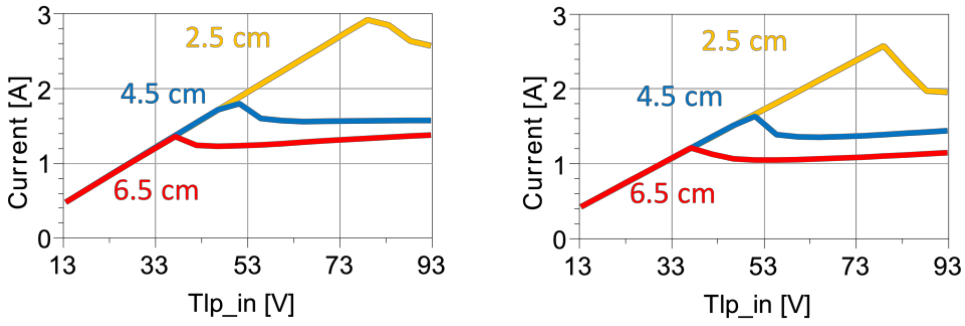

Figure 19. Peak current and quasi-static current through the on-chip diode as a function of the distance between the TVS and diode and the TLP voltage. (a) Peak current (b) Quasi-static current.

5. CONCLUSION

The transient response of an external TVS and on-chip diode placed together in a configuration typical of a high-speed signal I/O interface was studied through measurements and simulation. The SEED models of the TVS and diode were improved by smoothing the transition of the device from “off” to “on” at the end of the conductivity modulation or the start of snapback in order to obtain stable simulations. Improvements to the test board to limit transient coupling to the on-board current probe and improvements to the calibration process were made to enhance the accuracy transient voltage and current measurements. The SEED models presented here accurately predicted the current and voltage associated with the devices for a wide range of TLP

voltages and rise times, and when adding passive components between the TVS and diode.

Careful selection of the TVS protection device is critical for ESD design. Adding components to provide an additional impedance between the external TVS and the on-chip diode can significantly improve the ability of the TVS to protect the IC. The modeling process outlined here can help the design engineer to intelligently select protection devices and other components to maximize protection against a range of transient events while also ensuring the signal integrity of the design. Models may also be used to predict what conditions (e.g. rise-times and voltages) may cause the worst-case current at the diode so that testing and protection schemes may be adjusted accordingly.

Results demonstrate the importance of a thorough simulation strategy as the on-chip diode may be stressed more at a lower test voltage than a higher test voltage when a race condition between the TVS and on-chip diode occurs. For example, in one case shown here the on-chip diode current was 2.5 times higher at a lower test voltage than the highest voltage under test. These race conditions become more important for slow rise time events that may be seen in-practice but are not part of standard test protocols.

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SECTION

2. CONCLUSIONS

The three topics discussed in this dissertation are intended to help the designer to have a better understanding of the real life risk for the electronic devices. Simulation methodology including the circuit simulation, full-wave simulation and the SEED modeling are efficient to get an early design guidance to prevent the damage to the devices.

The experimental investigation into spark distances, current rise times and the modeling of the spark resistance showed that sparks guided along plastic surfaces can bridge distances two to three times longer than the distances predicted by Paschen's law. In spite of the longer spark path, a strongly reduced rise time was observed for sparks along plastic surfaces comparing discharges at the same voltage. It is suggested that the seam structure of the plastic enclosure for the electronic system be carefully designed to increase the voltage at which ESD will penetrate into the system by providing detour paths or paths against the electrostatic field to allow placing the electronics closer to the enclosure.

The ESD current for the wearable device in brush-by scenario can reach values twice as high as the current specified in the IEC standard. This is caused by the much lower impedance caused by having a body close to a metal structure such as a door frame which can leads to a higher risk. Soft failure testing on a DUT provides additional evidence that the brush-by scenario may endanger wearable equipment.

The SEED modeling helps the designer with the diode selection and layout design for the high speed I/O signal lines. Results demonstrate the importance of a thorough simulation strategy as the on-chip diode may be stressed more at a lower test voltage than a higher test voltage when a race condition between the TVS and on-chip diode occurs.

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