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Characterizing and modeling methods for power converters

Anfeng Huang

Department: Electrical and Computer Engineering

CHARACTERIZING AND MODELING METHODS FOR POWER CONVERTERS

by

ANFENG HUANG

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Approved by:

Chulsoon Hwang, Advisor
Jun Fan, Co-Advisor
Victor Khilkevich
Daryl Beetner
Richard Brow

PUBLICATION DISSERTATION OPTION

This dissertation consists of the following four articles, formatted in the style used by the Missouri University of Science and Technology.

Paper I: found on pages 9-35; Transient Behavior Model of Current-Mode Buck Converters for Power Distribution Network Design, has been submitted to in IEEE Transactions on Power Electronics.

Paper II: Pages 36-45; Fixture Design for Parasitic Capacitances of MOSFETs for EMI Applications, will be submitted to 2022 Asia-Pacific International Symposium on Electromagnetic Compatibility.

Paper III: Pages 46-75; Impedance Converter Based Probe Characterization Method for Magnetic Materials Loss Measurement, has been accepted by IEEE Journal of Emerging and Selected Topics in Power Electronics (2021).

Paper IV: Pages 76-101; Improved Current Shut Characterization Method for Ferrite Loss Characterization, is conditionally accepted with major revisions in in IEEE Transactions on Power Electronics.

ABSTRACT

Stable power delivery is becoming increasingly important in modern electronic devices, especially in applications with stringent requirements of its form factor. With the evolution of technology, the switching frequency in a power converter is pushed to a higher frequency range, e.g., several MHz or even higher, to decrease its size. However, the loss generated in the converter increases drastically due to the high switching frequency. In addition, a wide-band feedback controller is required to accommodate the high switching frequency in the converter. We focus on the characterization or modeling of the feedback control circuits and critical components in a switching power converter.

A transient-simulation-oriented averaged continuous-time model is proposed to evaluate the transient output noise of a buck converter. The proposed modeling method is developed with time-domain waveforms, which enables a generalized modeling framework for current-mode controllers with constant and nonconstant switching frequencies.

In this work, we mainly focus on characterization for two types of components: the switching components, including Si MOSFETs and GaN High-electron-mobility transistor (HEMT), and the magnetic core in an inductor.

For the characterization of switching components, a set of test fixtures are designed to characterize the equivalent circuit of Si MOSFETs and GaN HEMTs. The frequency-dependent behaviors of Si MOSFETs are observed, which invalidate the conventional modeling methods for MOSFETs, especially for radiated emission (RE) prediction.

For the characterization of magnetic cores, two different probe calibration methods are demonstrated. Accurate phase discrepancy characterization is allowed with the proposed method, which overcomes the main limitation in the conventional two-winding method. In addition, the proposed method supports wide-band loss measurement without resonance tuning, which supports core loss measurement for non-sinusoidal excitation.

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1. INTRODUCTION

1.1. DC-DC CONVERTERS IN MODERN ELECTRONIC DEVICES

Power Distribution Networks (PDNs) are critical parts of modern electronic devices, which extends from the voltage regulator module [1, 2] (VRM , typically consists of one or multiple DC-DC converters) through the printed-circuit-board (PCB) [3, 4, 5] to the dies of ICs[6, 7], as illustrated in Figure 1.1.

1.1.1. Power Noise of a Power Distribution Network. Therefore, the power noise generated in a real device is influenced by all the PDNs of DC-DC converters, PCBs and ICs. Due to the complexity of PDNs in real products, the quality of a PDN is typically evaluated and interpreted according to its frequency-domain response, i.e., output impedance. Correspondingly, the concept of target impedance has been developed as an engineering criterion in designs.

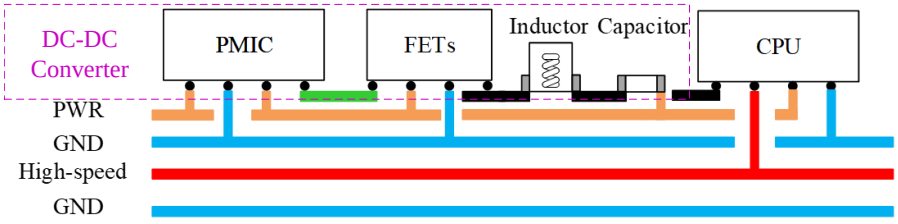


Figure 1.1. A typical onboard end-to-end power distribution network.

The PDNs in the high frequency range (above 10 MHz) can be related to the physical structures of PCBs and chips, e.g., the capacitance between power planes, parasitic inductance related to traces and bonding wires. The output impedance of a system-level PDN is shown in Figure 1. Thus, the PCB-level and chip-level PDNs can be modeled as combinations of linear circuit elements, e.g., partial-element equivalent circuit (PEEC) method. However, the DC-DC converters, which dominate the low-frequency impedance or long-term time-domain response (Figure 1.3) of a system-level PDN, are active circuits

with feedback controllers. The impedance concept provides good physical insights while not being accurate in describing its transient behavior, as the output impedance of a DC-DC converter is hard to define, demonstrated in Figure 1.4.

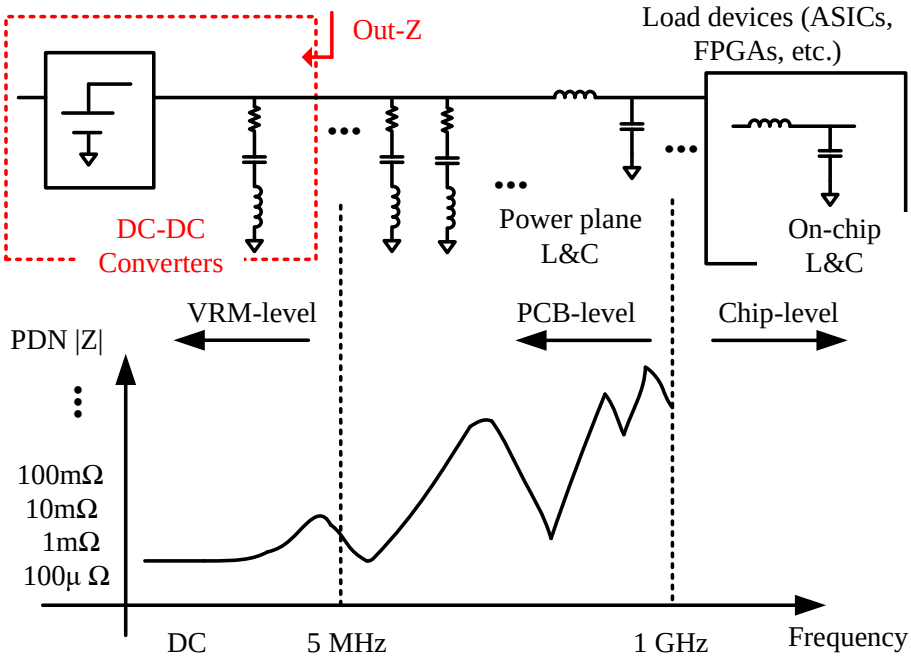


Figure 1.2. Impedance curve of a typical end-to-end PDN platform.

Nowadays, the requirement for a higher speed communication link leads to a lower power supply voltage (lower than 2 V) in chips as it provides faster logic transition [8, 9]. In addition, the power assumption of the microprocessors can be minimized by reducing the supply voltage V_{dd} [10]. However, lower V_{dd} leads to a higher supply current, and the maximum current consumed by a CPU can reach hundreds of Amps[11]. Moreover, due to high clock frequencies, the microprocessors' load transition speeds also increase drastically. The slope of load current change can reach several Amps in nanoseconds range, which imposes additional challenges in modern power converters under transient loading conditions. Stringent load line specification is then defined by the manufacturers, e.g., VR specification for Intel microprocessors [12, 13].

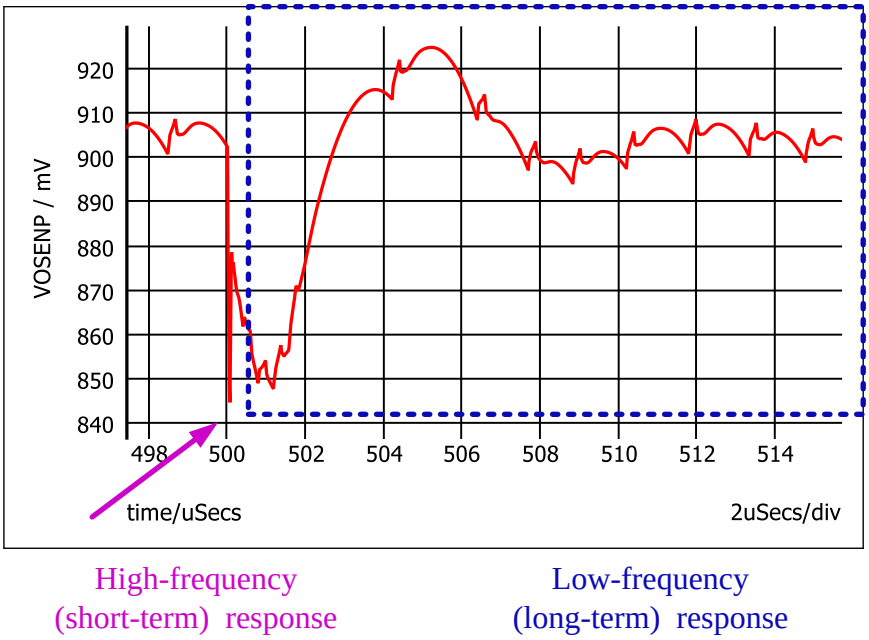


Figure 1.3. Time-domain response of a simulated end-to-end PDN, the low frequency response of the PDN is determined by the VRM, i.e., a buck converter.

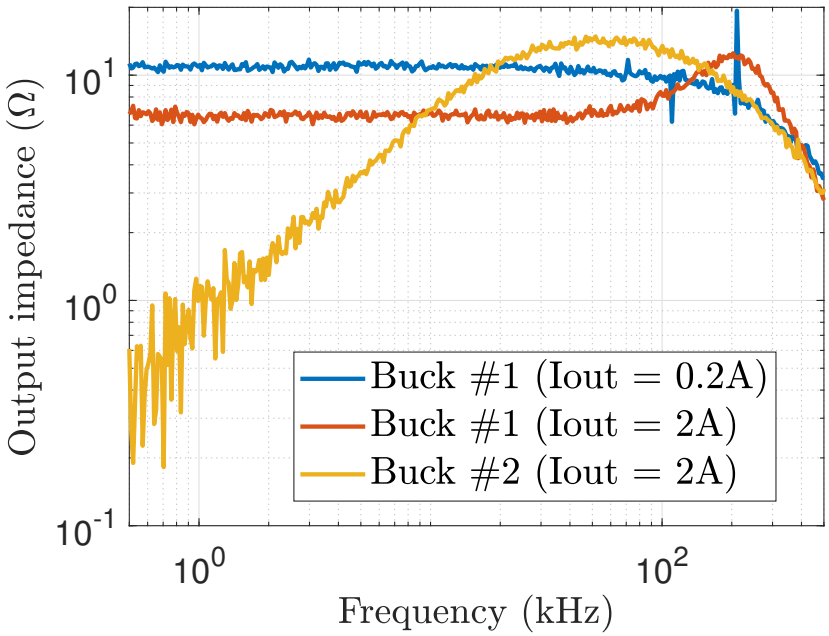


Figure 1.4. The measured output impedance of two buck converters.

To meet the tight ripple requirement of high-performance application-specific integrated circuits and CPUs, advanced control technologies are proposed, which can limit the power noise to 30 mV [14] with a load current change in hundreds of Amps range within μs. As the result, a practical topology-based circuit model is required to reproduce the response of a converter. However, those technologies are top secrets that are well-protected by the manufacturers. Simulation models are typically provided in an encrypted format, which are black boxes for PI engineers. Trail-and-error-based tuning is still the most widely used method in real PI design to optimize the response of a DC-DC converter. In addition, the long simulation time of a VRM is another concern when a detailed model is provided by the vendor. The total elapsed time of each simulation can reach several hours when the end-to-end PDN is integrated into the model. The complexity of modern DC-DC converters is growing progressively which brings in huge troubles for PI engineers to understand. A more user-friendly modeling framework, which can protect the vendor's intellectual property while providing physical understandings for PI engineers, is required.

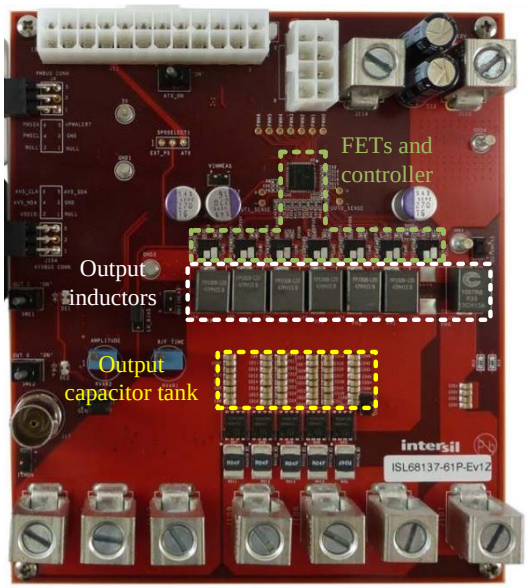


Figure 1.5. Evaluation board of a multi-phase buck converter (Intersil, ISL68137), which supports a continuous output current up to 270 A.

1.1.2. Inductors in the DC-DC Converters. Except for the complicated feedback controllers, the continuous pursuit for a higher power density and efficiency instigates extra issues in the design of converters. With emerging of wide-bandgap semiconductors (SiC and GaN), pushing the switching frequency to dozens or even hundreds of MHz range becomes possible[15, 16]. The required inductance can be greatly reduced with a higher switching frequency, and the form factor of a DC-DC converter can be reduced accordingly [17, 18, 19].

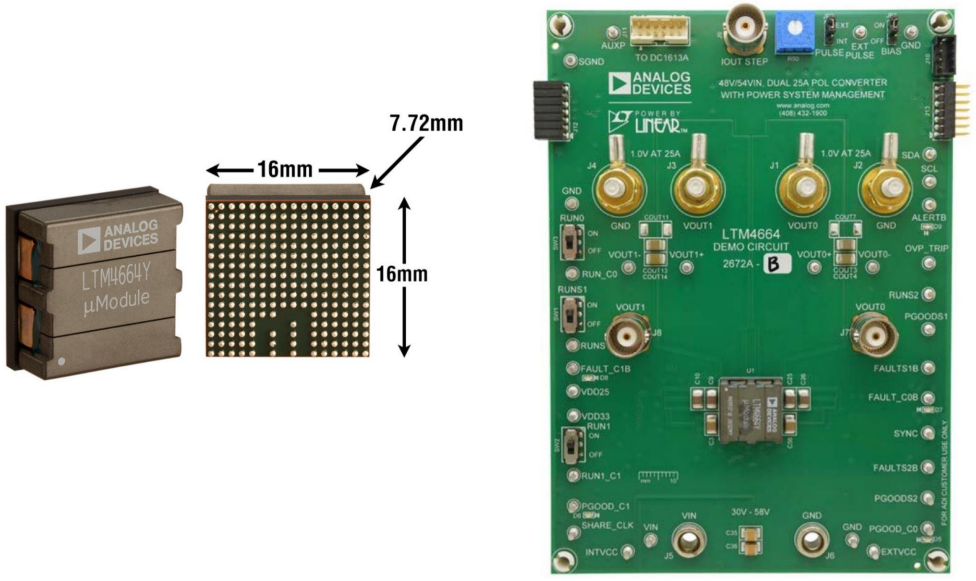


Figure 1.6. Photo of a fully integrated buck converter (Analog Device, LTM4664).

Nevertheless, the magnetic materials hinder the further miniature of converters, which are important for the converter's efficiency and power density [17, 20, 21]. The cores are implemented with highly-nonlinear materials, whose loss is dependent on many factors, e.g, amplitude and frequency of excitation, waveforms, DC bias, and temperature. They fulfill the requirement of large DC current, multi-phase converters are developed, and large inductors are used to avoid over-saturation. It is worth noting that due to the non-linearity of the core loss and the dependence on so many factors, predicting the core loss under all conditions is almost not possible. Massive measurements are required to

obtain accurate core loss under different operations. Thermal and electrical [22] methods have been developed for core loss characterization; however, all of them have their own weakness, especially for massive tests.

In the future, the whole VRM can be even integrated into a single chip. For instance, the μModule series fully integrated buck converter (Analog Device) can provide an output current up to 100A, where the majority of the space is occupied by the inductor and magnetic core. Reducing the size of a huge inductor and pushing the performance of a core to its limit is worth further investigation.

1.1.3. EMI Issues in Switching Converters. Near-field noise and electromagnetic interference (EMI) issues are emerging problems coming along with the evolutions of DC-DC converters. Unwanted high-frequency noise is generated by the converters due to the switching nature of the buck converter. The fast charging voltage (dv/dt) and current (di/dt) at the switching node of a switching converter make it a potentially effective radiator.

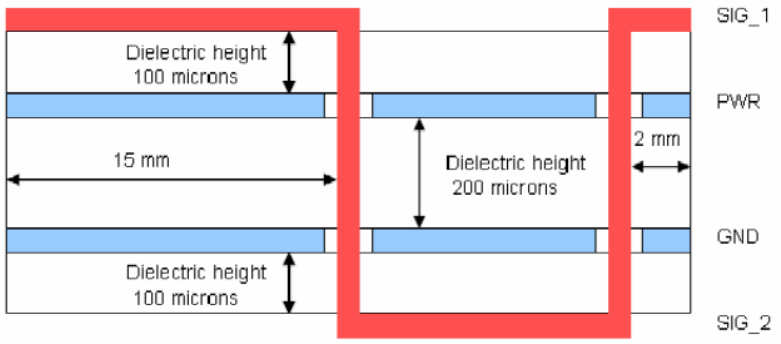


Figure 1.7. Typical coupling path between a power-net and a high-speed trace.

The frequency of the noise can be as high as 300 MHz [9] and can be easily coupled to nearby high-speed signal traces [8]. It is worth noting that, the modeling of switching noise is not included in ordinary PDN design, where the buck converters are evaluated only up to several MHz as we have mentioned.

Figure 1.7 illustrates a typical scenario where the high-frequency noise generated by a switching converter can couple to the nearby high-speed trace through the vias. The power/ground planes in PDNs act like cavity resonators at high frequencies which present a high impedance path to the return displacement current at resonant frequencies. The energy can be easily coupled to interconnect discontinuities, e.g. vias. A demonstration of the coupled noise can be found in Figure 1.8.

Figure 1.8. Noise coupled from a buck converter to nearby high-speed traces.

To predict the EMI noise generated by a switching converter, a detailed and accurate simulation model is required. The actual structure of the PCB, equivalent circuits of MOSFETs and gate driver, and even the physical dimensions of the chip package are required. The model may be implemented if tremendous efforts are applied, the computational expense can be intolerable. In summary, the requirement of high frequency and power density switching in future applications imposes new challenges in circuit design and EMI issues.

1.2. CONTENTS AND CONTRIBUTIONS

The outlines and contributions of this dissertation are summarized.

In the first paper, a transient simulation-oriented average modeling method for current-mode (CM) buck converters is developed. Compared with the existing models, the contributions of the article are highlighted as follows:

First, the utilization of time-domain waveforms enables a generalized modeling framework for CM controllers with constant and nonconstant switching frequencies. Second, nn efficient two-step parameter extraction flow is developed with the help of the proposed modeling technique. An accurate equivalent model can be efficiently implemented based on simulation (from an encrypted model) or measurement results.

In the following paper, the characterization methods for critical components in power converters are discussed. The measurement methods for parasitic capacitances of a MOSFET and the corresponding test fixtures are presented. Additionally, the frequency-dependent behavior is reported for the first time.

In the last two papers, the challenges in core loss characterization are discussed, and two-probe characterization based methods are proposed to release the requirement for resonance tuning in real practices.

PAPER

I. TRANSIENT BEHAVIOR MODEL OF CURRENT-MODE BUCK CONVERTERS FOR POWER DISTRIBUTION NETWORK DESIGN

ABSTRACT

Accurate power noise simulation is critical in the development of modern electronic devices. However, the widely used target impedance fails to predict the low-frequency noise generated in a device due to the existence of the DC-DC converter, whose output impedance can change under different loading conditions. A physical circuit model is then desired to replicate the behavior of a voltage regulator module (VRM), and the average technique is an efficient method to estimate the noise of a pulse-width-modulated (PWM) converter. With the emergence of converters with adaptive on-time (AOT) controllers, more complex averaging methods are required, but none of them supports transient simulation. A general, efficient and accurate modeling technique is presented in the paper, whose framework supports both current-mode PWM and AOT controllers. In addition, a novel two-step parameter extraction method is proposed, which can be used to evaluate the equivalent values of internal feedback parameters of an encrypted simulation model or from measurement. The modeling method is validated by both simulation and measurement.

Keywords: Power distribution network, average model, buck converter, transient simulation

1. INTRODUCTION

Design and optimization for power distribution networks (PDNs) are critical for state-of-the-art applications such as laptops and smartphones. The PDN is designed to maintain a constant supply voltage for the chips and keep it within a narrow tolerance band [1, 2, 3]. The demand for low-voltage operation of a high-speed digital interface is increasing due to the faster logic transition [4, 5]; however, the noise margin is also compromised. Evaluating the quality of a PDN at the design stage is becoming increasingly important.

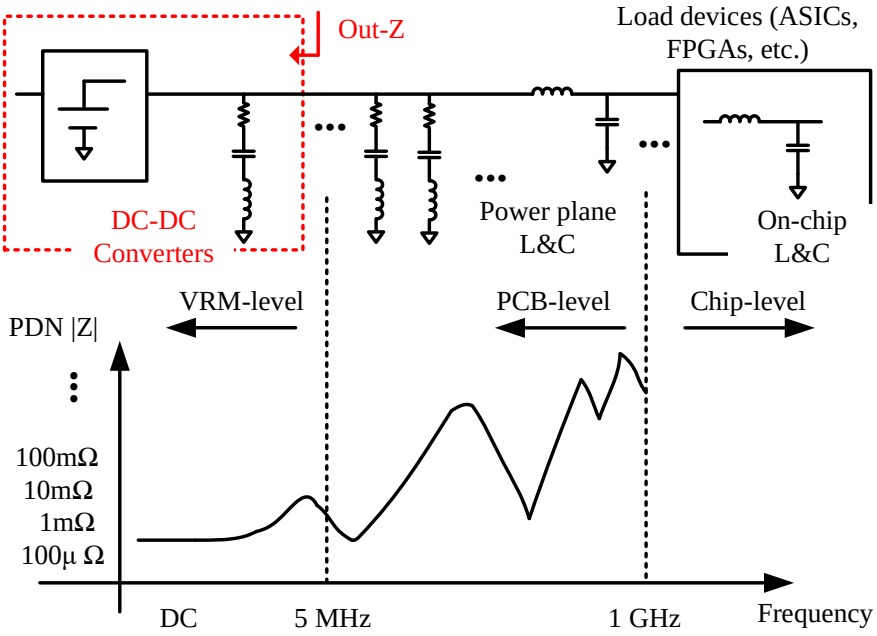


Figure 1. Impedance curve of a typical end-to-end PDN platform.

To ensure limited voltage fluctuation under different loading conditions, the target impedance has been developed as a common criterion for engineers [7], and a typical system-level PDN is demonstrated in Figure 1. However, the feedback circuits inside a VRM and the limitations in the practical measurement hinder the utilization of the impedance concept to predict its transient behavior, as demonstrated in Figure 2. The first buck converter has a load-line compensation function, and the measured output impedance is output current

dependent. The impedance of buck # 2 is approximately 400 $\mu\Omega$ at 500 Hz and is even smaller in the lower frequency range. Therefore, transient simulation still serves as the gold standard for power noise evaluation.

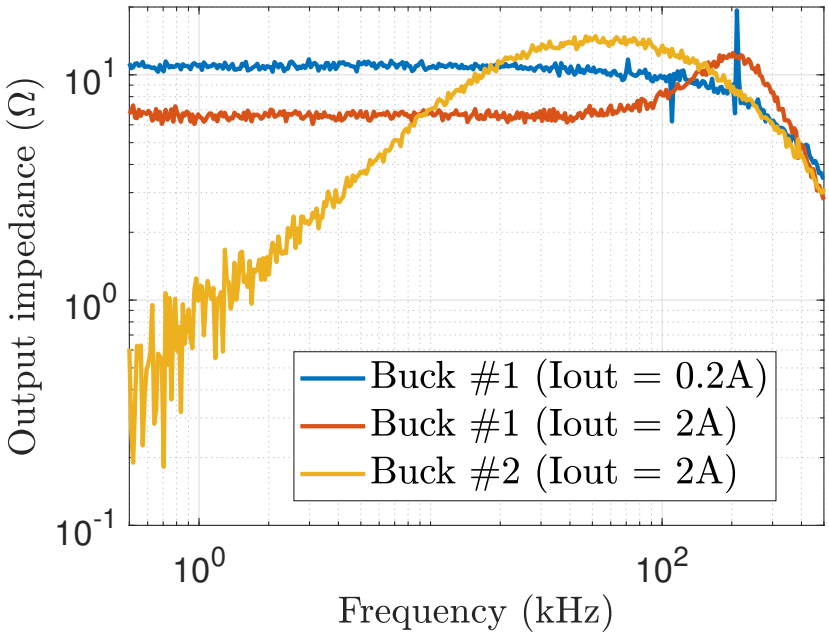


Figure 2. Measured output impedance of two buck converters.

The most conventional method for evaluating the noise generated by a PDN is performing the transient simulation with an accurate SPICE model, which includes all components in the switching power converter and parasitic components in the PCB and the chip. Nevertheless, the model of a switching converter is typically provided in the encrypted format and is locked to a certain simulation tool. In addition, tremendous efforts are required to link the PDNs of a PCB and a chip to that of the converter, as S-parameter blocks are the most widely used format to describe the PCB and chip-level PDNs. It is worth noting that many power electronics-oriented SPICE solvers cannot properly handle the cosimulation[8]. The long elapsed time of the simulation is another concern when a detailed SPICE model is provided. A simplified yet accurate model is required for efficient evaluation and optimization of an end-to-end PDN at the design stage.

Average-value technique[9, 10, 11, 12, 13] has been developed as a solution to reveal the complicated physics behind the circuit. In particular, the modeling method is preferred due to its simplicity and has been successfully applied in the modeling of buck converters with constant switching frequency. Essentially, the "sample and hold" effect is included in the model, and thus, the frequency response of the buck converter can be estimated. Even though the ripples in current and voltage waveforms are not explicitly represented, the response due to the feedback controller can be well reproduced by the per-cycle average technique. Additionally, the absence of ON/OFF switching provides a better convergence capability and a faster simulation speed. Even though these models are typically implemented for design purposes and represented by the Laplace transform, several transient-simulation-oriented average models are developed to replicate the time-domain behavior of a buck converter [12, 14, 15]. Both steady-state and transient-state behaviors, e.g., DC load regulation and over/undershoot of output voltage, can be accurately predicted.

Recently, AOT controllers have been increasingly used due to their feasibility of high-bandwidth design capability and high efficiency [16, 17]. The AOT controller has a smaller switching delay than an ordinary PWM controller and is suitable for CPU applications due to its fast response [18]. Nevertheless, traditional averaging techniques are hard to directly apply due to the frequency variant nature of the controller. The describing function (DF) is one of the solutions to model the nonconstant frequency operation in the converter, and several small-signal models [11, 19, 20, 21] have been successfully implemented based on this idea. Similar to the previous models for the PWM controller, those models are proposed for design purposes. To the best of the authors' knowledge, none of those models provide transient simulation capability.

With the higher integration level in VRM design, complicated feedback circuits, including current and voltage feedback loops and slope compensation, are integrated into a chip and not disclosed to users due to intellectual property (IP) concerns. The models

provided by the manufacturers are not suitable for power integrity applications, as we have mentioned. Thus, developing a parameter extraction technique that can be used to determine the equivalent parameters of internal feedback loops is also desired.

This paper provides a transient simulation-oriented average modeling method for current-mode (CM) buck converters. Compared with the existing models, the contributions of the article are highlighted as follows:

1. The utilization of time-domain waveforms enables a generalized modeling framework for CM controllers with constant and nonconstant switching frequencies.

2. An efficient two-step parameter extraction flow is developed with the help of the proposed modeling technique. An accurate equivalent model can be efficiently implemented based on simulation (from an encrypted model) or measurement results.

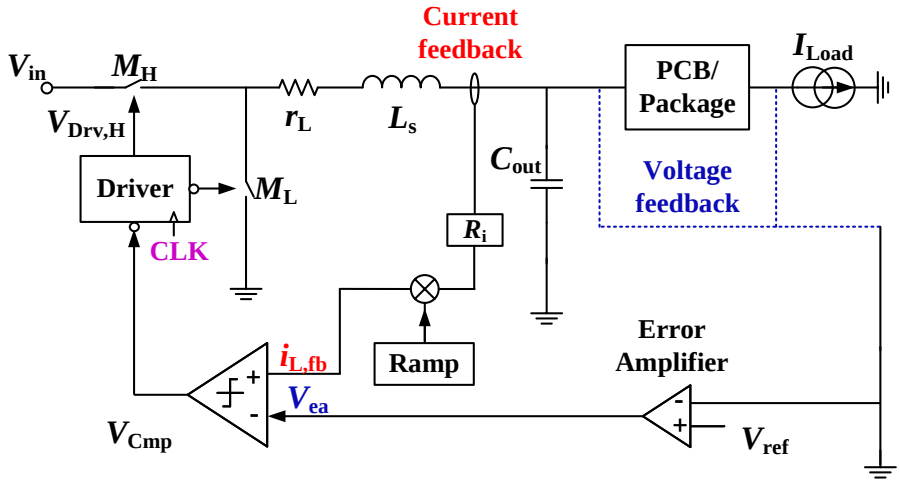


Figure 3. Circuit diagram of the CM converter with a PWM controller.

2. BUCK CONVERTERS WITH CURRENT MODE CONTROL

2.1. TOPOLOGIES OF CM BUCK CONVERTERS

The control mode of a converter can be mainly divided into voltage and current modes. The fast response of the current feedback loop reduces the feedback delay and enables a simpler type II compensator design. In addition, the CM controller is naturally

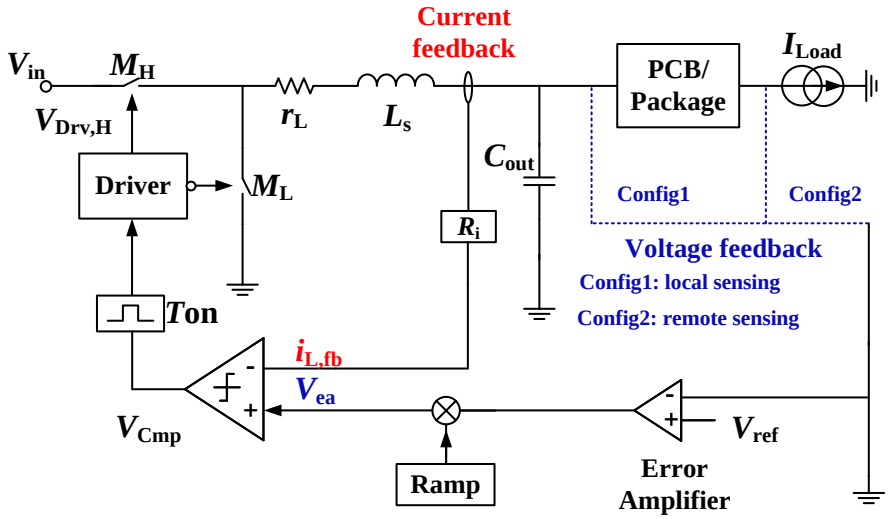


Figure 4. Circuit diagram of the CM converter with an AOT controller.

suitable for multiphase design, as accurate current sharing is achievable. In this section, the topologies of buck converters with CM controllers are illustrated in Figure 4 and Figure 3, and the AOT controller is used to exemplify the operation principle of the converter.

The converter consists of a synchronized step-down power stage and an AOT controller with dual feedback loops. The feedback controller is primarily implemented by a comparator with injected slope compensation, an inductor current sensor, a remote voltage sensor, a voltage loop error amplifier, and an internal voltage reference. An adaptive on-time generator is triggered by the comparator and controls the on-off states of two MOSFETs in the power stage. Depending on whether the inductor current i_L reaches zero during each switching cycle, the converter may operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

The critical waveforms in the feedback circuit are shown in Figure 5. The current loop feedback signal $i_{L,fb}$ and the voltage loop feedback signal V_{ea} are connected to the inverting and noninverting pins of the comparator, respectively. Thus, a short pulse V_{Cmp} will be generated when V_{ea} is larger than $i_{L,fb}$. The on-timer is then activated by V_{Cmp}, and the high-side MOSFET M_H is turned on during T_{on}. Meanwhile, the inductor current

ramps up as the inductor is energized by input voltage V_{in}. The low side MOSFET M_L is turned on, and the inductor current decreases once T_{on} is expired. The off-time ends when V_{Cmp} triggers the next on-time cycle.

The on-time of the AOT controller is typically determined by the nominal switching frequency, input, and output voltage of the converter [22]:

$$T_{on} = \frac{V_{out} F_{nom}}{V_{in}}, \tag{1}$$

where V_{out} is the output voltage and F_{nom} is the nominal switching frequency of the buck converter.

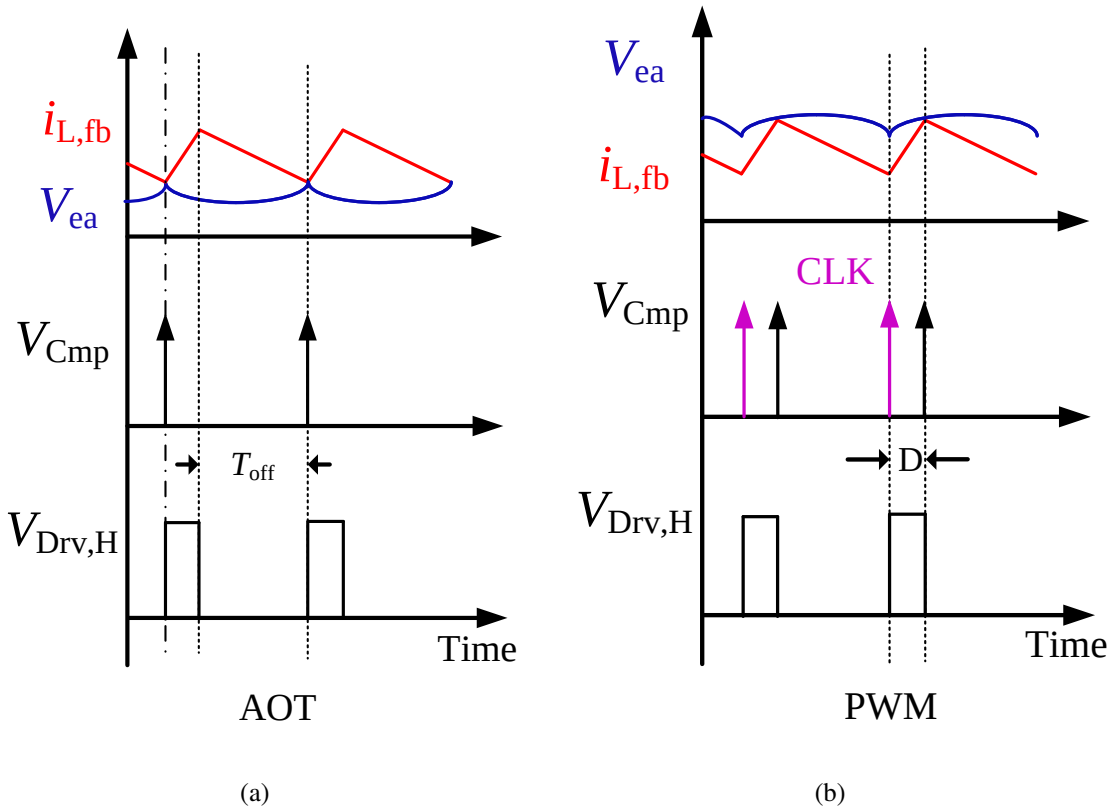


Figure 5. Critical waveforms (CCM operation) in the feedback circuits of the (a) AOT controller; (b) PWM controller.

2.2. DIFFERENCES BETWEEN AOT AND PWM CONTROLLERS

As demonstrated in Figure 3 and Figure 4 , the circuit diagrams of the CM buck converters with the AOT and PWM controllers are very similar, except for the comparator and gate driver. Due to the deployment of the adaptive on-timer, the gate driving signal will expire automatically, and only one trigger signal is required to activate the timer. As a consequence, the switching frequency of the AOT controller is not a constant value. Additionally, a fixed reference clock is provided in a PWM controller, and the turn-off timing of the gate driver is controlled by the comparator. The $i_{L,fb}$ and the V_{ea} are then reversely connected to the comparator, which can control the on-time or duty cycle of the PWM signal.

In summary, the feedback signals are reversely connected to the comparator in the two controllers. The off-time of the gate driving signal is tuned in the AOT controller, and on-time, i.e., the duty cycle, is controlled in the PWM controller.

3. PROPOSED MODELING WAVEFORM-BASED MODELING APPROACH FOR A CM BUCK CONVERTER

Even though the difference in the topology of the two controllers is relatively trivial, the nonconstant switching frequency in the AOT controller invalidates the traditional modeling method for the PWM controller. In this section, a topology and time-domain waveform based modeling method is proposed for CM mode buck converters. The idea from the DF method is adopted to model a system with a nonconstant fundamental frequency. A similar modeling approach was developed and applied to a PWM controller in [15, 23]. The equations are formulated in a time-domain representation, which makes the model naturally suitable for transient simulation. As an add-on feature, the extensibility of the approach is better than that of the traditional frequency method. The same framework can be applied for both the AOT and PWM controllers.

The circuit depicted in Figure 4 can be divided into three subcircuit blocks: the voltage feedback loop, the current feedback loop, and the power stage, which are discussed separately in the rest of the section. We note that the hysteresis in the comparator and dead time in the gate driver are not considered in the model. In addition, only CCM operation is supported at this stage.

3.1. VOLTAGE FEEDBACK LOOP

Figure 6 shows the circuit diagram of a typical type II compensator. The output voltage V_{out} is fed back to the error amplifier and compared with the internal reference voltage V_{REF}.

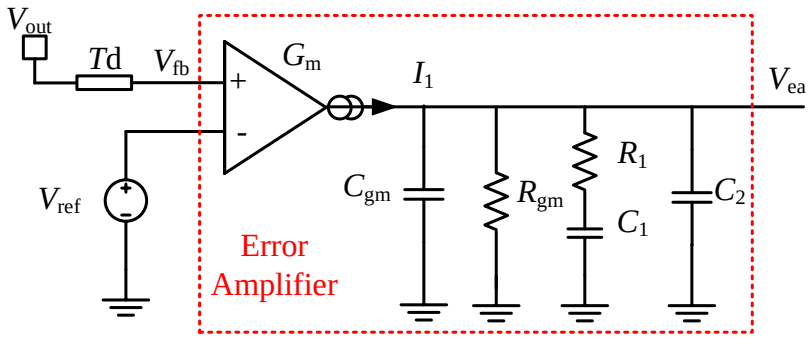


Figure 6. Simplified circuit diagram of an error amplifier.

An operational transconductance amplifier (OTA) is typically used due to its high open-loop gain and bandwidth. Another parameter in this loop is the feedback delay T_d from the instant when V_{out} is sensed to the instant when V_{fb} is updated. The output voltage V_{ea} of the OTA is analyzed in the Laplace domain and formulated as:

$$V_{ea} = G_m(V_{out} - V_{ref})\times \\ (R_1 + \frac{1}{sC_1})//\frac{1}{sC_2}//R_{gm}//\frac{1}{sC_{gm}}e^{-sT_d}, \tag{2}$$

where G_m is the open-loop gain of the OTA. R_1, C_1 and C_2 are compensation components in the error amplifier. R_{gm} and C_{gm} are the internal parasitics of the OTA. The transfer function can be further explicated by deriving locations of the zero and the poles in the circuit.

$$V_{ea} = K_{dc}(V_{out} - V_{ref}) \times \frac{s - f_{z1}}{(s - f_{p0})(s - f_{p1})} \times e^{-sT_d}. \tag{3}$$

The locations of the zero and the poles are $f_{z1} = \frac{1}{2\pi}R_1C_1$, $f_{p0} = \frac{1}{2\pi}R_{gm}(C_{gm} + C_1 + C_2)$, and $f_{p1} = \frac{1}{2\pi}R_1C_2$, respectively. K_{dc} is the DC gain of the error amplifier circuit.

3.2. CURRENT FEEDBACK LOOP

In the buck converter, the voltage feedback loop is typically configured with a narrow bandwidth to achieve accurate DC regulation while the transient recovery speed is sacrificed. Therefore, the current feedback loop is important to speed up the transient response of the converter. R_i represents the total sensing gain of the current feedback loop, and the output signal $i_{L,fb}$ can be formulated as:

$$i_{L,fb} = i_L \cdot R_i. \tag{4}$$

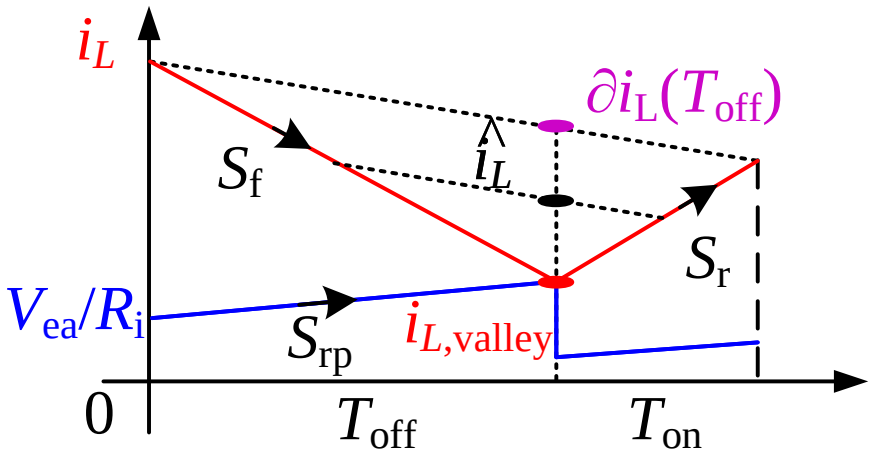


Figure 7. Waveforms of the current feedback loop in the CCM state.

It is worth noting that the switching period of the AOT controller is directly determined by $i_{L,fb}$ and V_{ea}. The derivation of average inductor current $\hat{i_L}$ is important to calculate the switching period T_{sw} in the converter. Due to the off-time modulating nature of the controller, the switching cycle start time is defined as the turn-off transition of high-side switching.

The inductor current is always larger than zero, and the switching period T_{sw} of the AOT controller can be separated into T_{on} and T_{off} periods.

$$T_{sw} = T_{on} + T_{off}. \tag{5}$$

The inductor used in the circuit is typical with a high-quality factor, and the current flows through it can be simplified as a triangular wave. The charging and discharging slopes S_r and S_f are calculated as:

$$S_r = \frac{V_{in} - \hat{i_L}(r_{on,H} + r_L) - V_{out}}{L_s}, \tag{6}$$

$$S_f = \frac{-\hat{i_L}(r_{on,L} + r_L) - V_{out}}{L_s}, \tag{7}$$

where r_L and L_s are the equivalent series resistance (ESR) and inductance of the output inductor. In this model, we assume that a linear slope compensation circuit is deployed whose rising slope is S_{rp}. In addition, the ramp generator is reset at the crossing moment of V_{ea} and $i_{L,fb}$, i.e., turn-on transition of the high-side switch, as depicted in Figure 7.

The minimum value of the inductor current in one cycle $i_{L,Valley}$ can be expressed as:

$$i_{L,Valley} = i_L(T_{off}) = \frac{1}{R_i}(V_{ea} + T_{off}S_{rp}). \tag{8}$$

Linear interpolation is then applied to the inductor current regarding $i_L(0)$ and $i_L(T_{sw})$,

$$\begin{aligned} \partial i_L(t) &= (i_L(T_{sw}) - i_L(0)) \times \frac{t}{T_{sw}} \\ &= (S_r T_{on} + S_f T_{off}) \times \frac{t}{T_{sw}}. \end{aligned} \tag{9}$$

The average inductor current $\hat{i_L}$ is defined as:

$$\hat{i_L} = i_{L,Valley} + 0.5 \cdot (\partial i_L(T_{off}) - i_{L,Valley}). \tag{10}$$

An equation with the independent variable T_{sw} can be constructed by substituting (5), (8) and (9) into (10):

$$\hat{i_L} - i_{L,Valley} R_i = -0.5\ S_f T_{off} + 0.5\ (i_L(0) - \partial i_L(T_{off})). \tag{11}$$

The switching period of the AOT controller in the CCM state can be solved by

$$T_{sw} = \frac{-R_i D_s T_{on}^2}{2\hat{i_L} R_i - R_i D_s T_{on} - 2V_{ea} - 2Ramp}, \tag{12}$$

where the difference between rising and falling slopes is defined as $D_s = D_s = S_r - S_f$, and $Ramp$ is formulated as:

$$Ramp = S_{rp}(T_{sw} - T_{on}). \tag{13}$$

3.3. POWER STAGE

The power stage includes the half-bridge inverter and the LC filter of the buck converter. The switching node voltage V_{SW} and the inductor current i_L are shown in Figure 8.

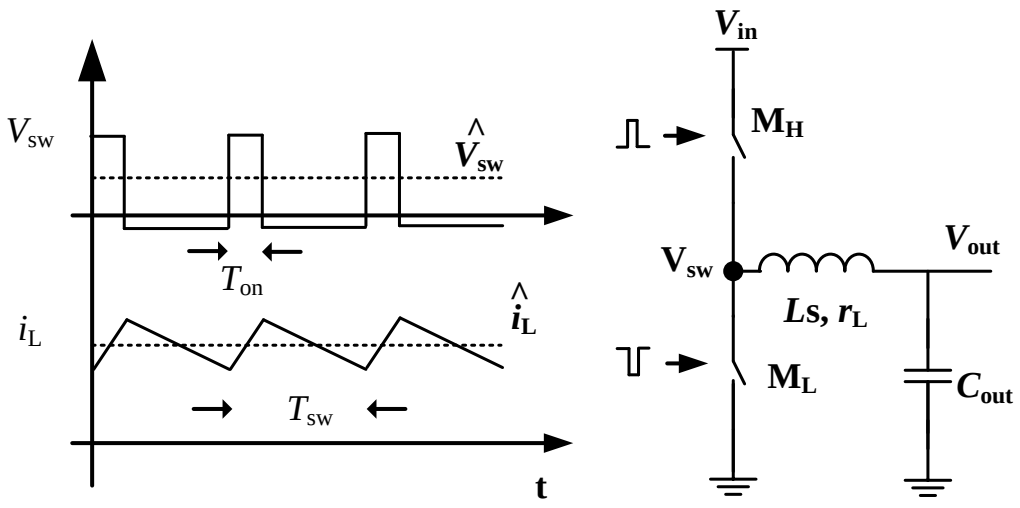


Figure 8. Power stage waveforms, including the LC filter and the half-bridge inverter.

In the CCM state, the conduction current is always larger than zero, and a pair of complementary pulse signals are generated to drive the two MOSFETs M_H and M_L. A triangle shape inductor current is thereby generated. Within each switching cycle, the average inductor current is denoted as $\hat{i_L}$. The average voltage of the switching node is calculated as:

$$\hat{V_{sw}} = \frac{T_{on}}{T_{sw}}(V_{in} - \hat{i_L} r_{on,H}) - (1 - \frac{T_{on}}{T_{sw}})\hat{i_L} r_{on,L}, \tag{14}$$

where $r_{on,H}$ and $r_{on,L}$ are the resistances of M_H and M_L, respectively. T_{sw} denotes the switching period of the buck converter, which is determined by both voltage and current feedback loops.

A droop voltage is induced between the inductor due to its equivalent series resistance (ESR) r_L, and the output voltage for the next cycle can be directly calculated as:

$$V_{out} = \hat{V_{sw}} - \hat{i_L} r_L. \tag{15}$$

3.4. KEY PARAMETERS AND MODEL IMPLEMENTATION

Table 1 lists all the key parameters that are required to implement the average model, which can be divided into two groups: system parameters and device parameters. The system parameters are related to the off-chip components and circuits, and they are typically configurable and accessible to the users. The device parameters are defined as the internal parameters of the chip, and many of those parameters are not accessible due to intellectual property protection.

The proposed average buck converter model can be fully described when the values of all parameters are provided.

The behavior of the buck converter is described by analytical equations, and thus, the model is implemented by the combination of RLC components and dependent sources. In addition, it is currently built in the Keysight Advanced Design System (ADS) and can be translated to different circuit simulators, e.g., Pspice and Hspice.

Table 1. Key parameters of the proposed model

Category	Parameter	Description
System Parameters	V_{in}	Input voltage.
	F_{nom}	Nominal switching frequency.
	C_{out}	Capacitance of output capacitor.
	L_s,r_L	Inductance and its ESR.
Device Parameters (Accessible)	$r_{on,H}$, $r_{on,L}$	On resistances of high and low side MOSFETs
	V_{ref}	Reference voltage.
Device Parameters (Integrated)	K_{dc}	DC gain of EA.
	f_{p0}, f_{p1}, f_{z1}	Zero and poles of EA.
	T_d	Remote sensing delay.
	S_{rp}	Slope of ramp compensation.
	R_i	Current sensing gain.

4. SIMULATION VALIDATION

In this section, the simulated results are presented to validate the proposed average model. A circuit model is implemented in Simplis for comparison. The parameters used in the simulations are $V_{in} = 5\,\text{V}$, $F_{nom} = 600\,\text{kHz}$, $C_{out} = 542\,\mu\text{F}$, $L_s = 500\,\text{nH}$, $r_L = 1\,m\Omega$, $r_{on,H} = 10\,m\Omega$, $r_{on,L} = 3\,m\Omega$, $V_{ref} = 0.9\,\text{V}$, $K_{dc} = 200$, $f_{p0} = 400\,\text{Hz}$, $f_{p1} = 1\,\text{MHz}$, $f_{z1} = 16.7\,\text{kHz}$, $T_d = 20\,\text{ns}$, $S_{rp} = 240\,\text{V/ms}$, and $R_i = 0.2\,\text{V/A}$.

Figure 9 and Figure 10 illustrate the load transient responses of the two models from 0.5 A to 5A and vice versa. Both rise and fall time is configured as 1 μs. The recovery time and voltage drop simulated by the two models are well matched. Due to the cycle-by-cycle averaging of the model, on-off switching is not generated in the model. The difference between the two models is brought by the missing ripple, which is limited to 2 mV in the test case.

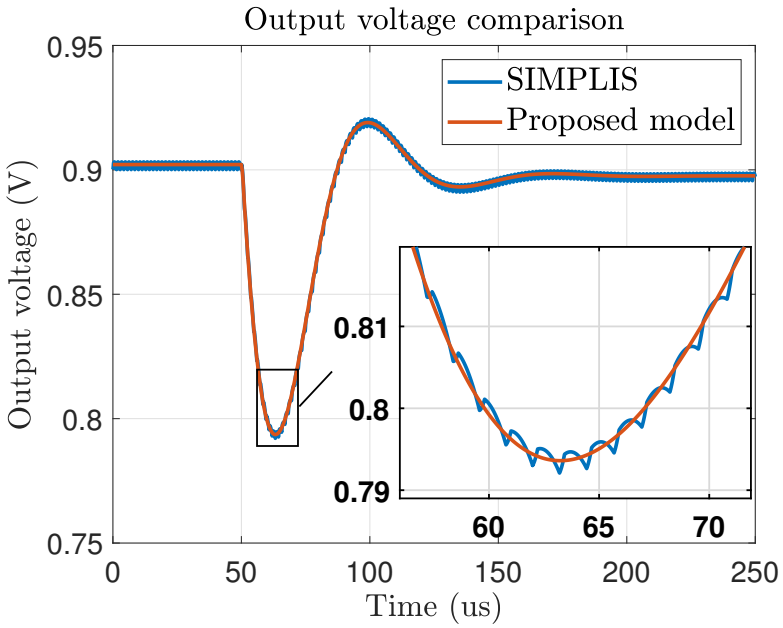


Figure 9. Transient response of the output voltage with ramp-up load, from 0.5 A to 5 A (rise time: 1 us).

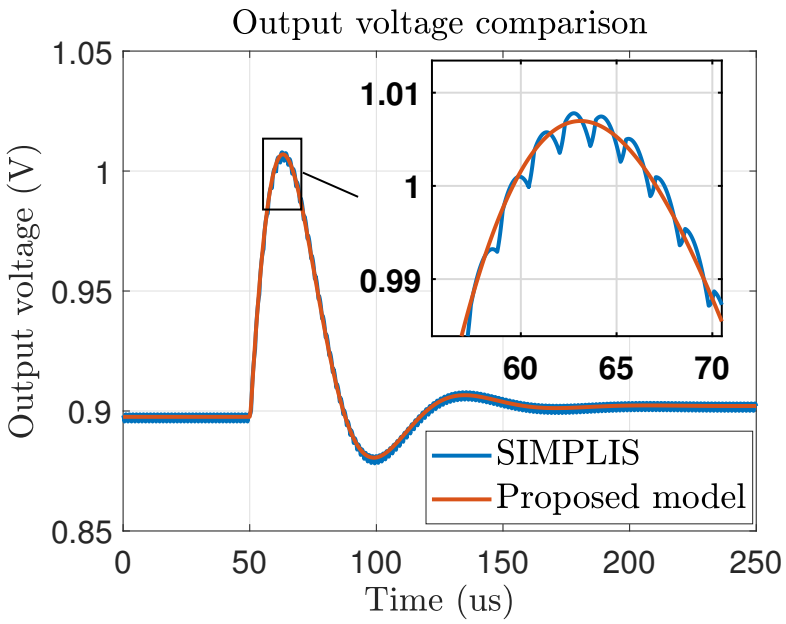


Figure 10. Transient response of the output voltage with ramp-down load, from 5 A to 0.5 A (fall time: 1 us).

As discussed previously, the frequency variant nature of the AOT controller is the main challenge in Laplace transformation-based modeling. With the time-domain modeling technique, the change in switching period and on-time can be captured, as shown in Figure 11. The T_{sw} and T_{on} during the transient state can be well predicted by the proposed model, and the errors are limited to 0.5%. The well-matched results further validate the proposed modeling methodology.

Finally, the comparison of output voltage when the parasitic components of PCB are demonstrated in Figure 12. The configuration of the output capacitor in the simulation models is replaced by that of a real product, and the parasitics of a remote sensing trace are included in the model. The extra spike due to those parasitic inductances can also be captured by the model. This indicates that the model can be used to predict power noise in a realistic application. In addition, the influence of different internal feedback parameters, e.g., the rising slope of ramp compensation and zeros and poles of the error amplifier, can be simulated by the proposed model.

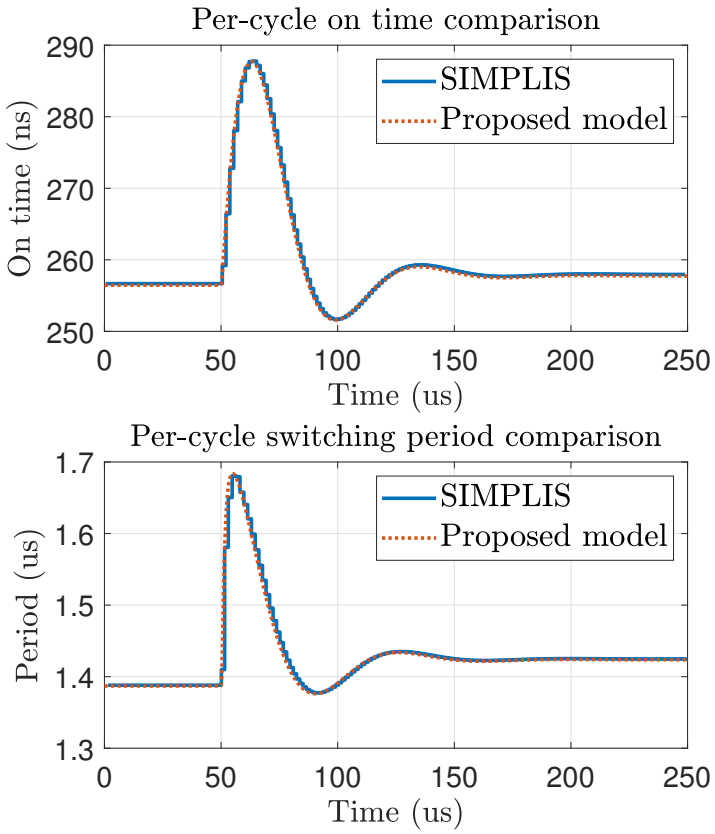


Figure 11. Comparison of T_{sw} and T_{on} under ramp-down loading conditions, where the load current drops from 5 A to 0.5 An in 1us.

5. TWO-STEP PARAMETER EXTRACTION METHOD

As a modern VRM reaches higher integration levels, its internal circuits are becoming increasingly complicated. The exact feedback configurations and slope compensation circuits are not accessible to users. With the help of the time-domain modeling methodology, the trial-and-error approach is used to determine all the unknown parameters[15, 23]. However, the tuning process is extremely tedious and time-consuming, as 7 or more parameters are coupled together.

A novel two-step method is proposed to extract the parameters of internal circuits and replicate the time-domain behavior of a CM buck converter. The seven unknowns are separated into DC (K_{dc}, S_{rp} and R_i) and AC parameters (f_{p0}, f_{p1}, f_{p1} and T_d). The initial

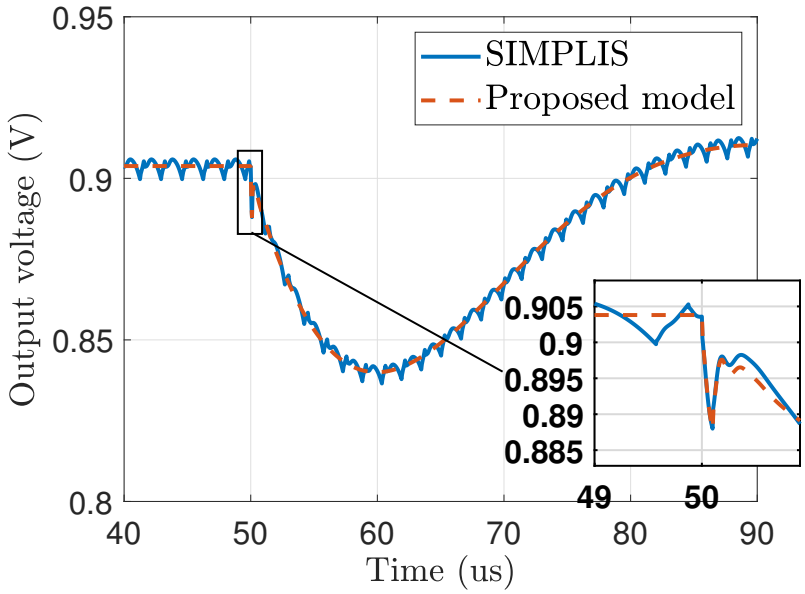


Figure 12. Comparison of output voltages simulated by two models.

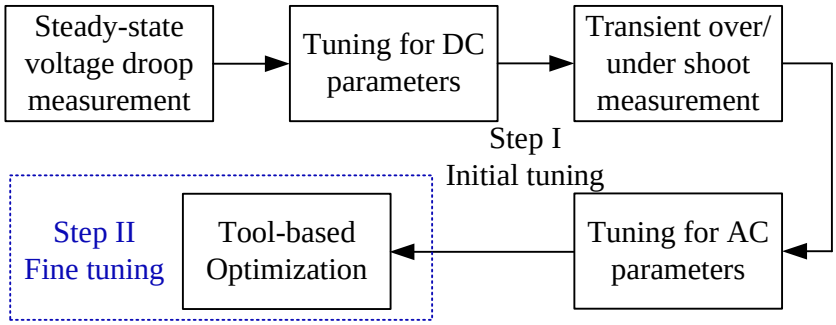


Figure 13. The flow of the two-step parameter extraction.

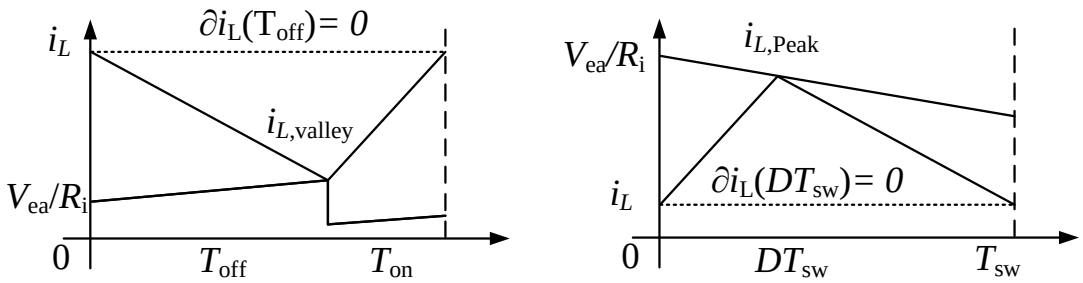


Figure 14. Waveforms of the current feedback loop under steady-state conditions (a)in the AOT controller, (b) in the PWM controller.

values of all seven variables can be efficiently extracted from measurement or simulation, and fine-tuning can be applied to further optimize the parameters. The tuning process for the AOT controller is exemplified in this section, as shown in Figure 13.

5.1. INITIAL TUNING

5.1.1. DC Parameters. The modeling technique demonstrated in Section III provides the simulation capability for both transient and steady-state operation of a buck converter, and the model can be greatly simplified when it is used to describe behaviors in the steady state. The output voltage of the error amplifier V_{ea} can be simplified, as only its DC gain needs to be considered. Eliminating the AC terms in (3), the V_{ea} can be formulated as:

$$V_{ea} = K_{dc}(V_{out} - V_{ref}). \tag{16}$$

It is well known that the per-cycle derivative of the inductor current is zero in the steady state, as shown in Figure 14. The ∂i_L can be simplified as:

$$\partial i_L = i_L(T_{sw}) - i_L(0) = 0. \tag{17}$$

The per-cycle average inductor current can then be formulated as:

$$\hat{i_L} = i_{L,Valley} - 0.5 S_f T_{off}. \tag{18}$$

The equation can be expanded as:

$$\hat{i_L} R_i - (V_{ea} + S_{rp} T_{off}) + 0.5 R_i S_f T_{off} = 0. \tag{19}$$

The steady state V_{out} can be obtained by substituting (16) into (19).

$$V_{out} = \frac{\hat{i_L} R_i + 0.5 T_{off} R_i S_f - S_{rp} T_{off}}{K_{dc}} + V_{ref}. \tag{20}$$

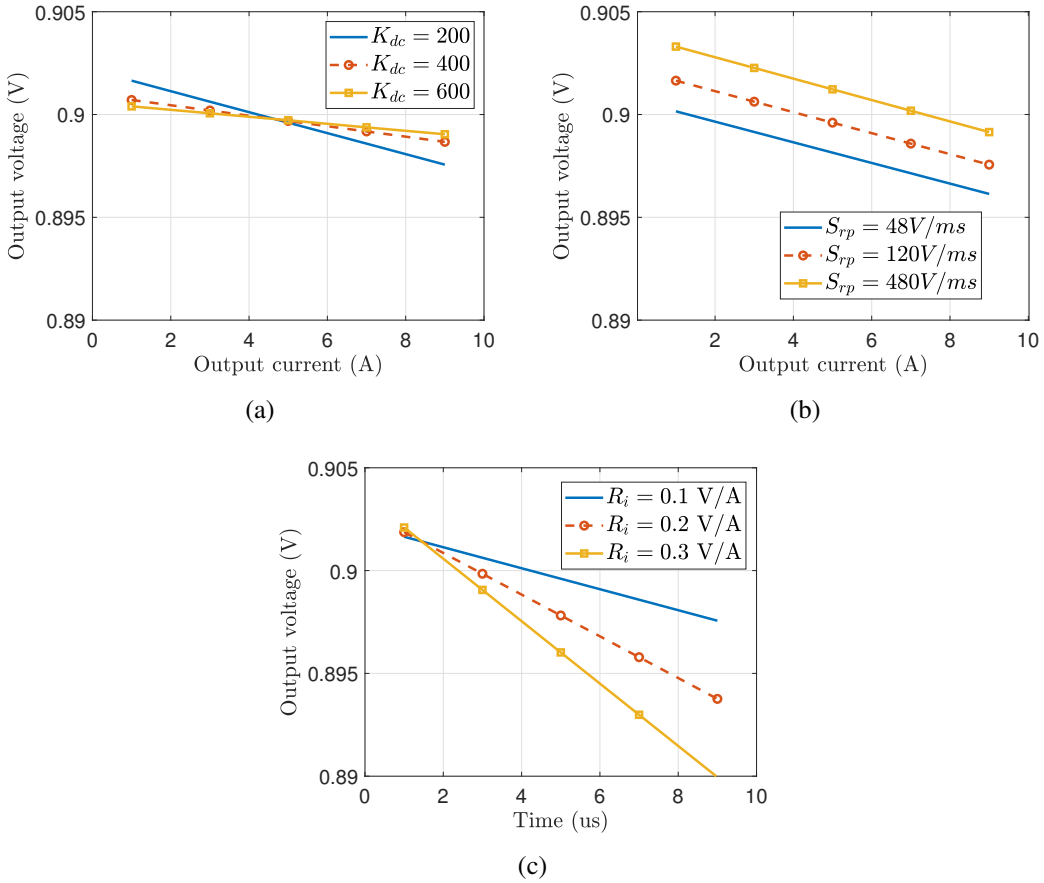


Figure 15. Impacts of DC parameters (a) K_{dc}; (b) S_{rp}; (c) R_i.

It can be seen that the steady state output voltage of a CM buck with an AOT controller is only determined by DC parameters (K_{dc}, S_{rp} and R_i), and the influences of them are illustrated in Figure 15, and Table 2. It is worth noting that the same parameter tuning strategy can be applied to a CM buck converter with a PWM controller. The critical waveform of the current feedback loop is shown in Figure 1.14(b). The steady-state per-cycle

inductor current can be simplified.

$$\hat{i_L} = i_{L,Peak} - 0.5 S_r D T_{sw}. \tag{21}$$

where D is the duty cycle of the PWM signal. Similarly, the V_{out} can be expressed as:

$$V_{out} = \frac{\hat{i_L} R_i - 0.5 D S_r T_{sw} + D R_i S_{rp} T_{sw}}{K_{dc} R_i} + V_{ref}. \tag{22}$$

Table 2. Influence of DC parameters

Parameter	Trend	offset	Slope
K_{dc}	↑	N/A	↓
	↓	N/A	↑
S_{rp}	↑	↑	-
	↓	↓	-
R_i	↑	N/A	↑
	↓	N/A	↓

5.1.2. AC Parameters. The rest of the unknown parameters are treated as AC parameters that can be characterized by the transient response. The voltage droop and overshoot recovery are mainly affected by these AC parameters, and the influence of AC parameters is under ramp-up loading conditions.

The first voltage droop and the ringing frequency during recovery are mainly dominated by f_{p0}; see Figure 1.16(a). The f_{z1} can be further determined by fitting the recovery slope (see Figure 1.16(b). It is worth noting that f_{p1} only has minor impacts on the voltage droop, and the simulation result is not attached. It is suggested to set f_{p1} to twice the switching frequency according to general design guidelines. The tuning for control delay T_d by observing the ringing amplitude is depicted in Figure 1.16(c). Default parameters are $K_{dc} = 200$, $f_{p0} = 400\,\text{Hz}$, $f_{p2} = 1\,\text{MHz}$, $f_{z1} = 16.7\,\text{kHz}$, $T_d = 0\,n\text{s}$, $S_{rp} = 240\,\text{V/ms}$, and $R_i = 0.1\,\text{V/A}$.

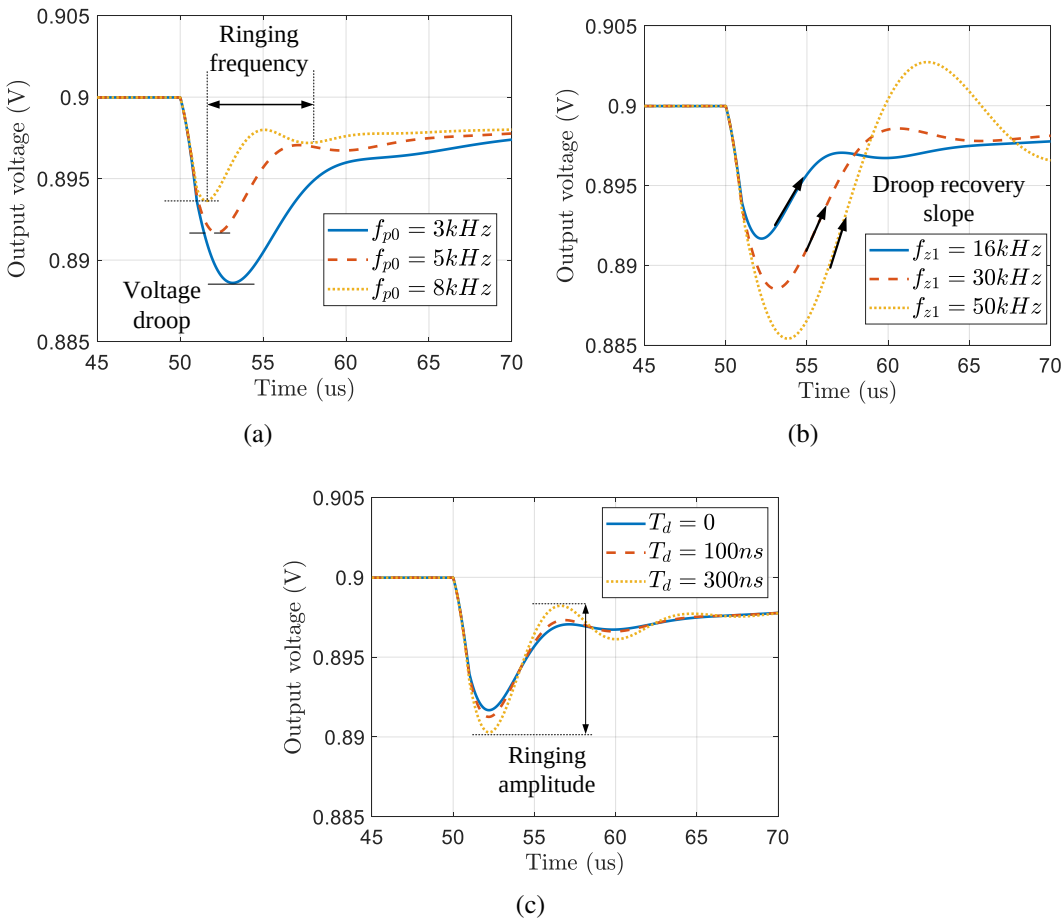


Figure 16. Impacts of AC parameters (a) f_{p0}; (b) f_{z1}; (c) T_d.

5.2. FINE-TUNING

The simulated voltage waveform based on the initial values can achieve a relatively good correlation with the measured result. The fine-tuning step only works as an optional process to further improve the accuracy. The ADS built-in optimization tool is used here to further adjust the parameters simultaneously based on the initial values obtained from the previous step.

6. MEASUREMENT VALIDATION ON A PRACTICAL EVALUATION

The proposed modeling and parameter extraction methods are performed on a buck converter with the AOT controller, which is different from the model used in the simulation. The configuration and photograph of the measurement setup are plotted in Figure 1.17(a). The input voltage is configured as 3 V by a DC power supply (Agilent E3648A). An electric load (Kikusui PLZ164WA) is used to control the current extracted from the converter. Both the output voltage and current are monitored by an oscilloscope (R&S RTO1024).

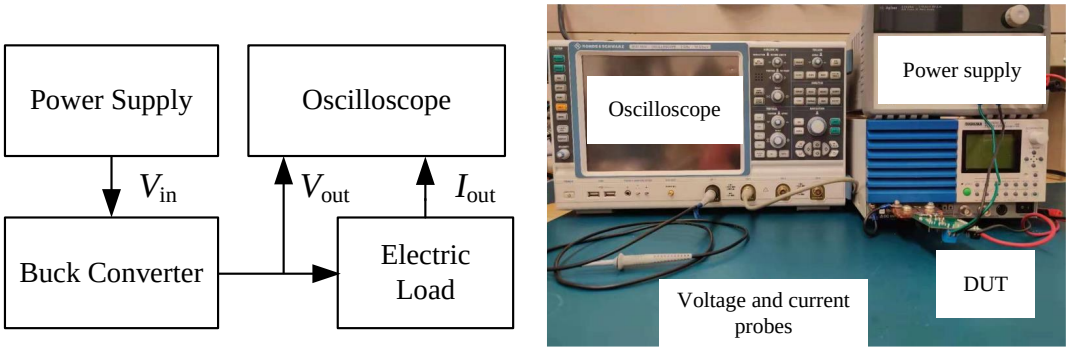
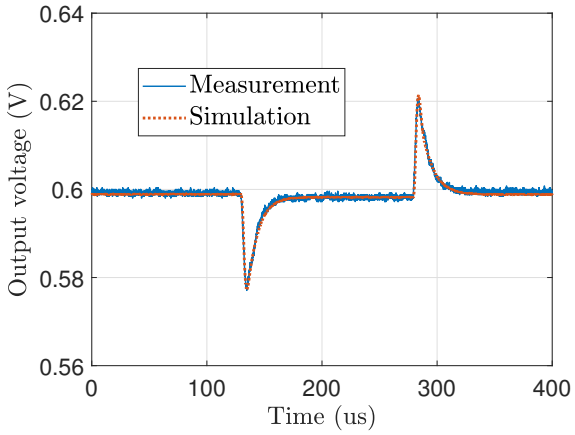


Figure 17. Measurement setup of the validation.

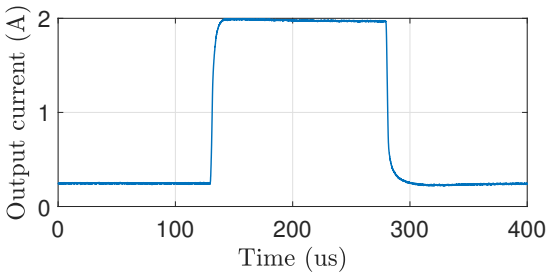
The voltage reference is configured as 0.6 V, and the switching frequency is configured as 600 kHz. The output inductor is 250 nH with a 2.2 mΩ ESR, and the total output capacitance of the X7R ceramic capacitors is 118 μF considering the derate effect. In addition, the converter is configured in forced CCM mode.

Figure 18 comparse the measured and simulated output voltages under different transient loads. The load amplitudes are from 0.25 A to 2 A, respectively. In addition, both rise and fall times are configured as 2μs. The simulated and measured results have good correlations for both of the conditions. The maximum differences in the output voltage are limited to ±1.8 mV. This validates both the time-domain modeling approach and the parameter extraction flow. The well-matched results demonstrate the capability of the proposed model, the model can be applied in the early design stage of an electronic

device when the vendor's model has not been provided. Additionally, the proposed two-step parameter extraction method facilitates the calibration process of the model, enables an efficient system-level power noise evaluation.



(a)



(b)

Figure 18. (a) Comparison of simulated and measured output voltage; (b) the output current extracted by the slammer board; the high and low levels of current are 0.25 A and 2 A, respectively.

7. CONCLUSION

A transient-simulation-oriented average model is proposed for CM buck converters. Both PWM and AOT converters can be divided into three subcircuits and modeled separately. The main contribution of the paper is providing a framework that can model controllers with constant and nonconstant switching frequencies. The proposed model is verified by both simulation and measurement. In addition to the modeling methodology,

the model can also serve as a platform to extract the internal parameters of the controller when the vendor's model is not provided in the early design stage. In addition, the model supports cosimulation with PCB parasitics, which enables an end-to-end PDN evaluation for real products.

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II. FIXTURE DESIGN FOR PARASITIC CAPACITANCES OF MOSFETS FOR EMI APPLICATIONS

ABSTRACT

Due to the fast-switching nature of modern power converters, up to hundreds of MHz of common noise can easily be generated. The characterization of switching components, e.g., Si MOSFETs, is essential for noise reduction. However, limited by the measurement capability of instruments, the voltage-dependent capacitances of high voltage MOSFETs are typically characterized at approximately 1 MHz, which is insufficient for EMI applications. In this paper, the measurement method and the corresponding test fixtures are presented. The bandwidth of capacitances is pushed to 30 MHz and higher , and frequency-dependent capacitances of a MOSFET are observed through measurements.

Keywords: MOSFET, voltage-dependent capacitances

1. INTRODUCTION

Switching power converters are widely used in modern electronic devices due to their high efficiency. However, unwanted high-frequency noise is generated by the converters due to their switching nature. Noise can even be observed at thousands of order harmonics of the switching frequency. With the trend toward higher power density, the switching frequencies of converters are pushed higher and can reach dozens of MHz. Severe electromagnetic interference (EMI) and radio frequency interference (RFI) issues will be generated with the further evolution of power converters [1].

To estimate the noise produced by a switching converter, reliable measurement and modeling techniques are required. The capacitance-voltage ($C - V$) characteristic is one of the most important parameters of MOSFETs, and the simplified equivalent circuit of a MOSFET is plotted in Figure 1. Semiconductor device parameter analyzers, e.g., Keysight

B1505A, have been developed for such measurements. Nevertheless, the frequency of $C - V$ is limited to 5 MHz, which is insufficient for EMI applications. Vector network analyzers (VNAs) have been applied to extend the frequency range in previous research [2]. Limited by the sensitivity of the one-port impedance method, the resolution of capacitance measurement is restricted in the dozens of pF range. Additionally, reconfiguration of the measurement setup is required during the $C - V$ test process, as MOSFETs contain three parasitic capacitors.

As demonstrated in Figure 1, three parasitic capacitances need to be characterized for a MOSFET. Three different configurations are then required to extract those values separately. The configurations have been standardized and can be easily achieved with commercially available instruments [3]. C_{iss}, C_{rss} and C_{oss} can be measured accordingly with the measurement setups shown in Figure 2, Figure 3, and Figure 4. Since the output capacitance (C_{oss}) and input capacitance (C_{iss}) measurements are simply performed, only the reverse transfer capacitance (C_{rss}) measurement will be discussed in this paper.

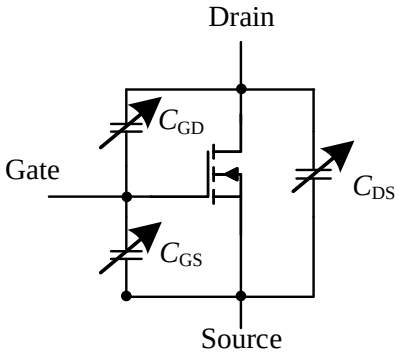

Figure 1. Simplified circuits of a MOSFET containing three junction capacitances.

In this work, considerations in the $C - V$ test are discussed regarding the sensitivity of different impedance characterization methods. In addition, two sets of test fixtures are designed for MOSFETs with a standard 5 × 6 mm footprint. The proposed fixture can

greatly reduce the efforts spent on setup configuration. The original contribution of the paper includes the demonstration of frequency-dependent capacitances of Si MOSFETs, which invalidates the modeling method of a commercially available model.

2. $C - V$ MEASUREMENT METHOD AND PRACTICAL CONSIDERATIONS

Figure 3 shows that the floating current generated by C_{DS} is not detected by the impedance analyzer (IA), as the AC guard provides an alternative current path. It is important to understand that the AC guard is a circuit unique to the autobalancing bridge and that it is connected to the shields of the four-terminal pair connectors. Therefore, C_{rss} can only be measured by an autobalancing bridge IA.

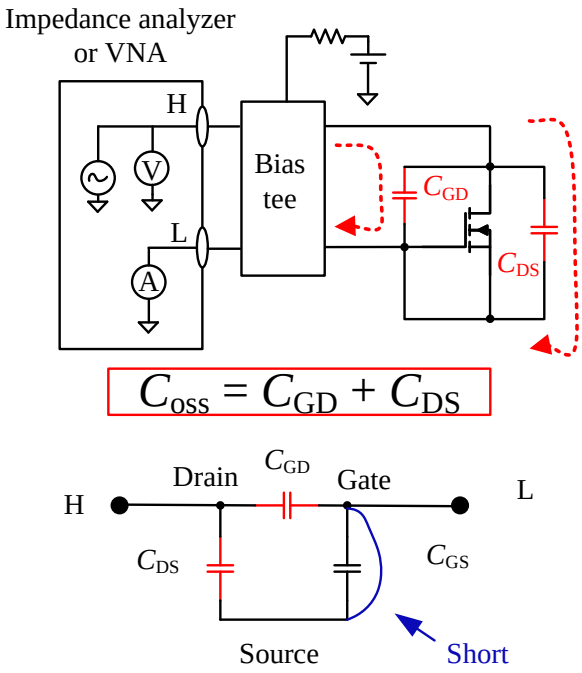

Figure 2. Configurations and equivalent circuits with an autobalancing bridge impedance analyzer for C_{oss} measurement.

The junction capacitances can be calculated with the measured capacitances through the following equations:

$$C_{GS} = C_{iss} - C_{rss}, \tag{1}$$

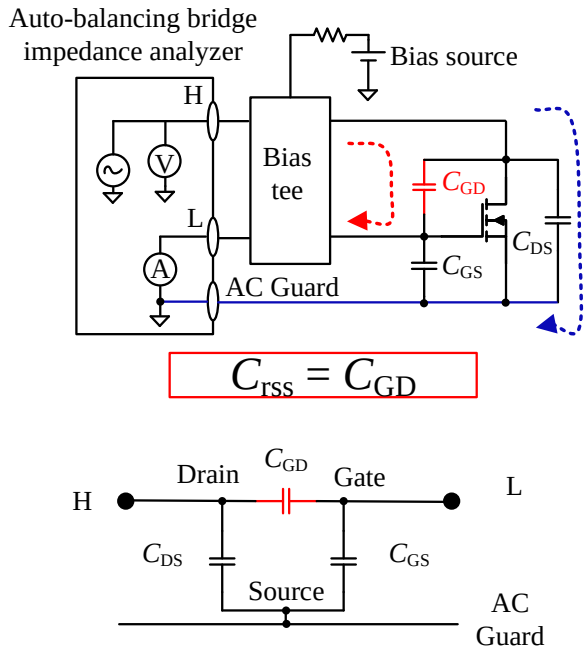

Figure 3. Configurations and equivalent circuits with an autobalancing bridge impedance analyzer for C_{rss} measurement.

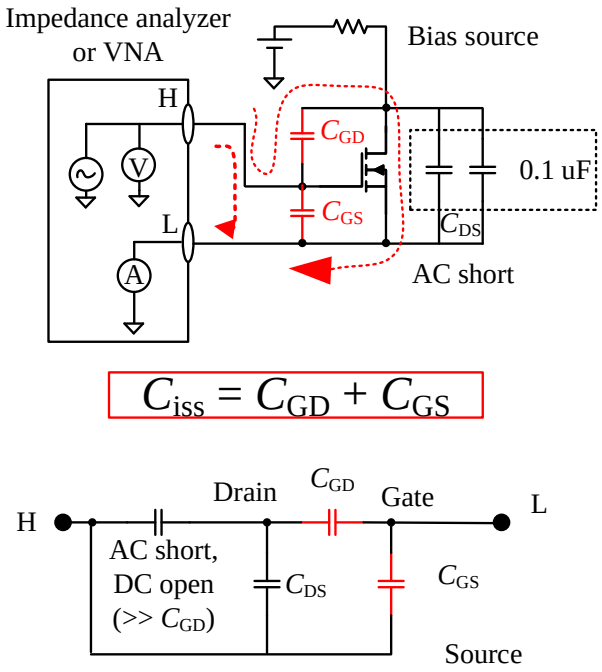

Figure 4. Configurations and equivalent circuits with an autobalancing bridge impedance analyzer for C_{iss} measurement.

$$C_{GD} = C_{rss}, \tag{2}$$

$$C_{DS} = C_{oss} - C_{rss}. \tag{3}$$

However, autobalancing bridge IAs bring peculiar advantages in $C - V$ measurements. The operation frequency of such IAs is limited to several MHz, especially when a high bias voltage is expected in the measurement. As an example, the E4990A IA (Keysight) can operate up to 120 MHz, but the bandwidth of its bias fixtures is no more than 2 MHz (model: 16065A and 16065C). RF instruments, e.g., a VNA or an RF IA, are required to extend the measurement to dozens of MHz or even higher frequency ranges. We note that an RF-IV IA enables accurate measurements over a broad range from 1/10 times lower impedance to 10 times higher impedance than the network analyzer method [4], as plotted in Figure 5.

Table 1 lists the parasitic capacitances of several 600 V MOSFETs, whose capacitances can be as low as 0.5 pF. Thus, the RF-IV impedance analyzer are preferred in the characterization of MOSFETs.

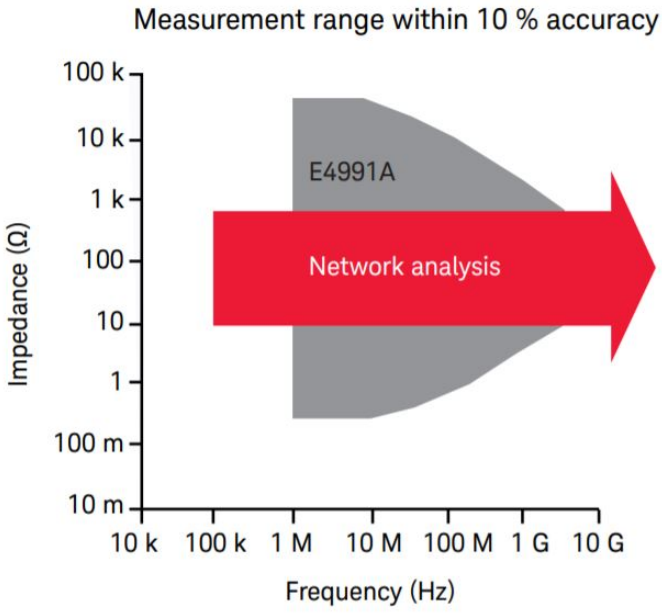

Figure 5. Comparison of 10% impedance measurement accuracy range of a VNA and an RF IV IA.

Table 1. Parasitic capacitances extracted from the datasheet under a 100 V drain-source voltage.

Model	Cgs (pF)	Cgd (pF)	Cds (pF)
IPLK70R600P7	360	0.5	9
IPLK70R2K0P7	130	0.5	3
AONS660A70F	898.6	1.4	21.6
AONS1R1A70	459.6	1.4	14.6

3. FIXTURE DESIGN AND MEASUREMENT VALIDATION

3.1. CONSIDERATIONS IN THE FIXTURE DESIGN

In this section, fixtures for $C - V$ measurements are presented to accommodate different interconnects of the autobalancing bridge IA (Kelvin connection) and the RF-IV IA (coaxial connector). A modular design is applied in the fixture design, and an external bias tee (Model: Keysight 16065A, ±200 V) is used. as shown in Figure 6. C_{rss} and C_{oss} can be directly measured with a daughterboard.

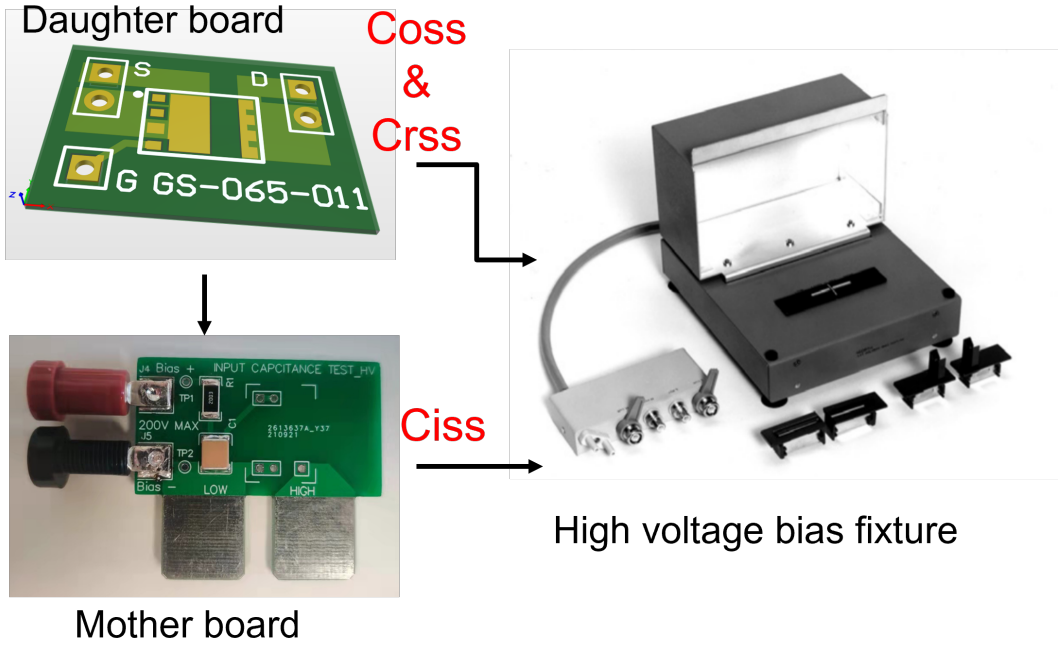

Figure 6. Fixtures for an autobalancing bridge IA.

A motherboard is designed to measure C_{iss}, the bias voltage can be applied through banana connectors, and the daughterboard can be directly installed on the motherboard. Limited by the bias tee, the maximum bias voltage and the maximum frequency are limited to 200 V and 2 MHz, respectively.

The operation frequency can be extended to 30 MHz and above with high-frequency fixtures. It is worth noting that the parasitic inductance should be minimized to extend the operation frequency, and the height between the signal plane and its return plane is configured to be 0.2 mm in this design. The inductance can be further reduced by using a smaller height, but the maximum bias voltage that can be applied will be compromised if the internal bias-tee is used in the measurement. The bias voltage can be increased with an external high voltage bias tee.

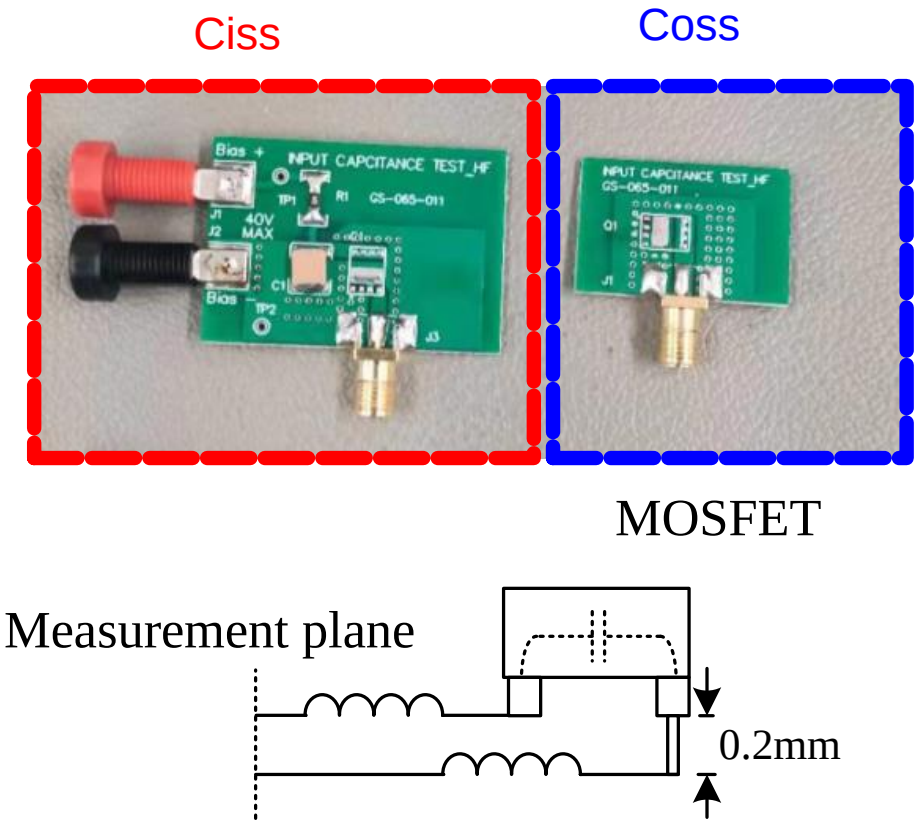

Figure 7. Fixtures for an RF-IV IA or a VNA.

3.2. EXPERIMENTAL VERIFICATION

To validate the designed test fixtures, a Si MOSFET (model: Infineon IPLK70R2K0P7) is tested with an autobalancing bridge IA. The discrepancies between the measured capacitances and those provided by the datasheet are within 5%. However, the capacitances, especially C_{rss}, exhibit frequency-dependent characteristics.

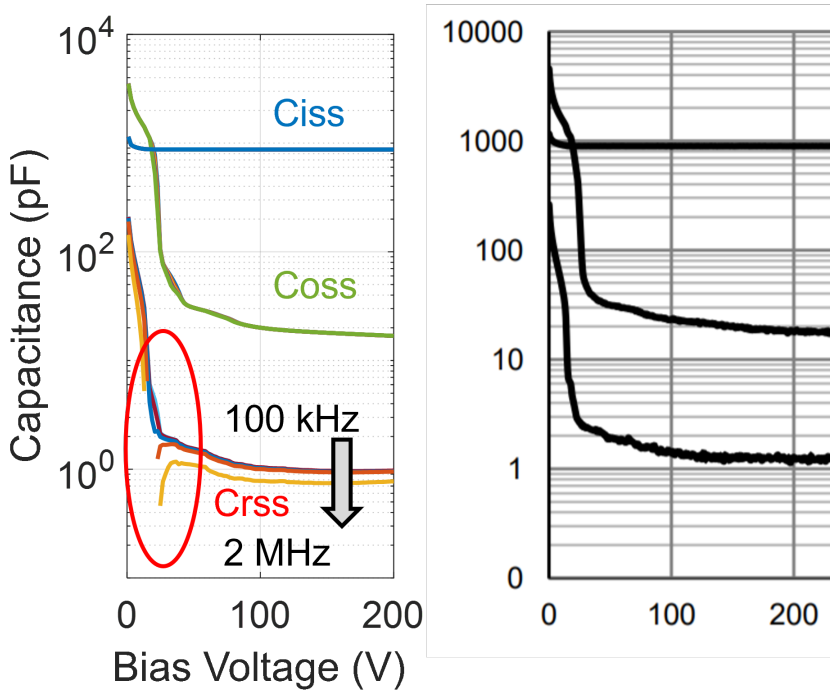

Figure 8. Comparison of parasitic capacitances (IA model: HP4194A) obtained from the measurement and datasheet.

To further validate the frequency-related behavior, the same MOSFET is measured by an RF-IV IA, and the measured C_{oss} is demonstrated. The excitation frequency is swept from 1 - 30 MHz, and the bias voltage is configured between 0 - 40 V. Similarly, the capacitance is non-constant among different excitation frequencies. It is worth noting that the phase of the measured capacitance shows a highly unstable phase when the bias voltage is approximately 30 V.

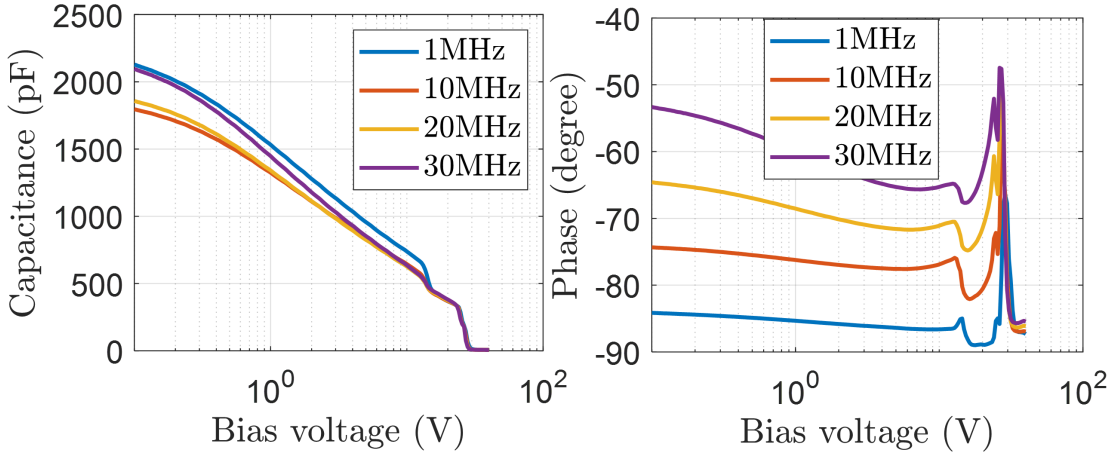

Figure 9. Measured C_{oss} (IA model: HP4294A, 1 MHz - 1.8 GHz) under different excitation frequencies.

Finally, C_{oss} extracted from its SPICE model is illustrated for comparison. The voltage-dependent capacitance is captured by the model; however, the simulated capacitance is frequency-independent. Additionally, the capacitance contains a negative resistance according to its phase information.

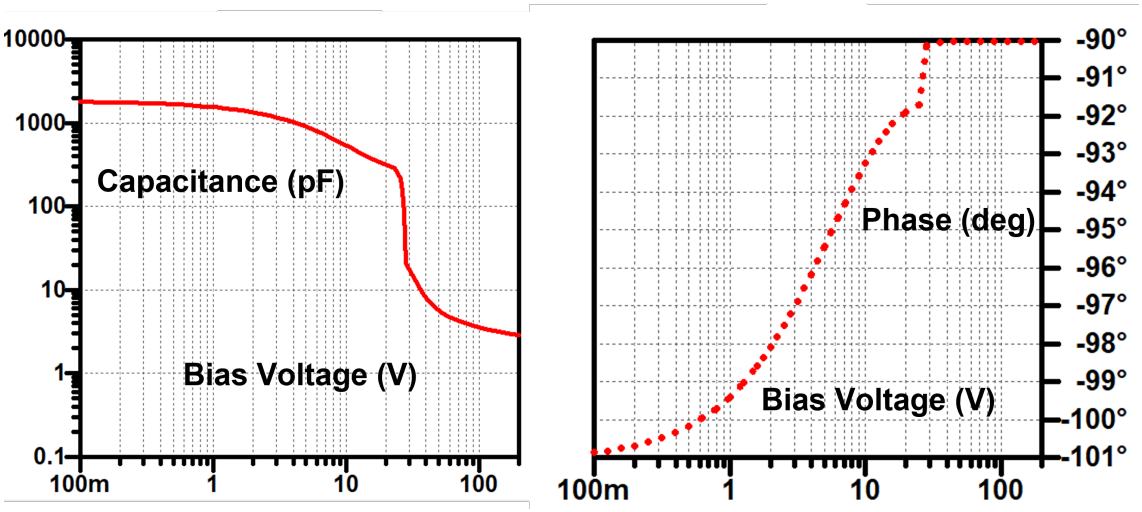

Figure 10. Simulated C_{oss} of IPLK70R2K0P7. The simulation model is provided by the manufacturer.

4. CONCLUSION

The measurement methods and considerations of Si MOSFETs in real practice are discussed in this paper. Two sets of fixtures are designed to facilitate measurements when specialized instruments are not available. The frequency-dependent capacitances of Si MOSFET are captured with the proposed fixture, while the behavior is not shown in the SPICE model. Fundamental modifications are required in the modeling of MOSFETs to enable the next order-of-magnitude improvement for EMC applications.

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III. IMPEDANCE CONVERTER BASED PROBE CHARACTERIZATION METHOD FOR MAGNETIC MATERIALS LOSS MEASUREMENT

ABSTRACT

As an essential component in power applications, magnetic cores and their design play an important role in achieving high efficiency and high power density. Accurate measurement of the core loss is important for inductor and power converter optimization. Loss measurement depends on exactly determining the phase angle between the voltage and the current. However, measurement errors can be introduced due to the discrepancies in propagation delays in the voltage and current sensors. In addition, the propagation delay is frequency dependent, but has a large influence in the MHz range and above. Previously, several methods have been proposed to compensate for this discrepancy but they are time consuming and can result in large measurement errors.

In this paper, a characterization method for ferrite loss based on a vector network analyzer and an impedance converter is proposed to accurately measure the phase discrepancies between voltage and current sensors. The proposed method is experimentally verified up to 15 MHz with a three-coil test setup.

Keywords: Ferrite loss characterization, Phase discrepancy, VNA, Impedance converter

1. INTRODUCTION

Magnetic components (e.g., inductors and transformers) are critical components in power electronics applications [1, 2, 3, 4]. Due to their high permeability, ferrites are used to reduce the physical dimension of these passive components. However, ferrites are nonlinear. Losses can be influenced by the temperature, frequency and magnetic flux

density [5, 6, 7, 8]. To optimize the performance of inductors and transformers with respect to loss, size, power density and thermal characteristics, accurate loss measurements for these magnetic materials are essential.

Among the existing methods, the dual-winding measurement method [9, 10, 11] is the most widely used as the conduction loss of windings can be excluded from the measurement. However, the accuracy of this method is sensitive to the phase error between the voltage and current measurements. Typically, the main discrepancy is caused by imbalanced propagation delays between probes or the phase shift of a nonideal current sensing resistor. As discussed in [11], the phase shift of a 0.2 Ω sensing resistor with a 1 nH parasitic inductor can reach 8.9° at 5 MHz, and a measurement error larger than 100% can be generated by this level of phase error.

To eliminate the error caused by the phase discrepancy, several methods exist, including the phase difference cancellation method and the probe characterization method.

The error can be almost neglected if the phase difference between the voltage current and current waveforms is perfectly canceled, which can be achieved with an additional capacitor [9, 10] or inductor [10]. Accurate core loss can be characterized by these techniques; however, perfect phase cancellation can only be achieved at a single frequency, which makes the tuning process burdensome. In addition, due to the nonlinearity of magnetic material, the permeability of the core can change with excitation level. The compensation reactance needs to be changed with the excitation level even for a single frequency as the inductance value of the inductor can change. The requirement for perfect resonance compensation makes this method time consuming and cumbersome. An improved partial cancellation method is proposed in [11], which enables accurate core loss characterization without fine-tuning. Although perfect cancellation is not required, different cancellation factors are required for different devices under test (DUTs). Automatic core loss measurement is still challenging for the method.

The simplicity of core loss measurement can be greatly improved if the probes can be rigorously characterized. This avoids a tedious reactance tuning process and allows standardized core loss characterization without changing the compensation parameters. A ferrite loss characterization method was implemented with voltage, current probes and an impedance analyzer [12]. The phase error can be compensated during the calibration process. However, only "THRU" calibration can be applied which cannot eliminate all the effects of probes and parasitics. Moreover, the characterization process is hard to be applied to modern commercial active probes due to the limitation of the probe-to-instrument interface. Besides, the method is invalidated when the core sample is operating in the non-linear region, as impedance analyzers are designed for linear components.

In this paper, an impedance converter-based in-house probe is proposed to address these challenges. The wide-band phase shift and attenuation of the probe can be characterized by a VNA, which provides a constant compensation factor for different measurement configurations. Thus, the core loss can be accurately measured with an ordinary dual-winding measurement setup without extra compensation components. The proposed method is validated by an air-core three-coil system up to 15 MHz. This paper is organized as follows. In Section II, the phase discrepancy introduced core loss measurement error is analyzed, and the in-ideal performance of a commercial active probe is demonstrated. The proposed impedance converter based in-house probe and its characterization method are discussed in Sections II and III. Section IV validates the proposed method for several cores with different materials. In Sections V and VI, the error analysis and conclusion are provided, respectively.

2. OVERVIEW OF THE DUAL-WINDING METHOD

2.1. SENSITIVITY TO PHASE DISCREPANCY

Figure 1 shows an equivalent circuit for a general dual-winding measurement setup. The DUT carries two windings with identical turn numbers, and the two windings serve exciting and sensing purposes separately. R_{w1}, R_{w2}, L_M, L_{w1} and L_{w2} correspond to the equivalent series resistances (ESRs) and the magnetizing and leakage inductances of the winding wires. R_{Core} represents the core loss, which includes hysteresis, eddy current and residual loss in the magnetic material. The mutual resistance due to the proximity effect in the windings should also be considered [13, 14], which is denoted as R_{wm}.

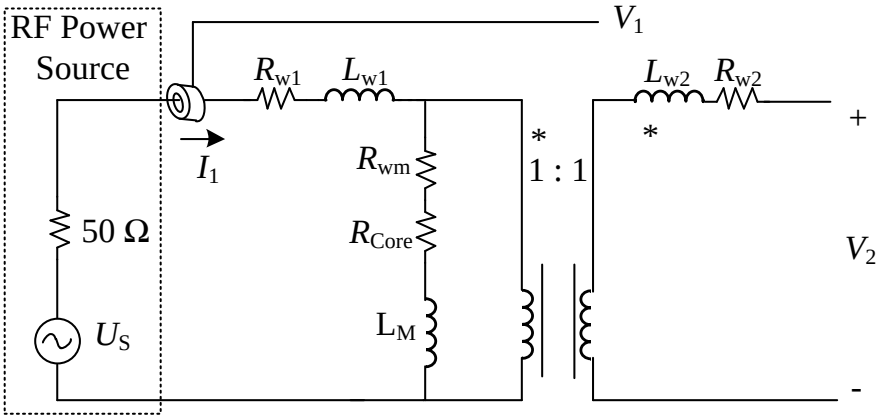


Figure 1. Equivalent circuit for the dual-winding measurement setup.

The loss generated by core and mutual-winding resistance can be characterized by measuring the primary winding current I_1 and the open circuit voltage V_2 of the secondary winding. It can be formulated as

$$\begin{aligned} P_{Mutual} &= \frac{1}{T}\int_0^T V_2 \cdot I_1 dt \\ &= \frac{1}{T}\int_0^T V_2 \cdot \frac{V_1}{Z_t} dt. \end{aligned} \tag{1}$$

where Z_t is the I-V transfer impedance of the current sensor and T denotes the period of the excitation signal. The mutual winding loss R_{wm} can be extracted and cancelled and the core loss can be expressed as

$$P_{Core} = P_{Mutual} - \int_0^T I_1^2 R_{wm}. \tag{2}$$

The phase difference between V_2 and I_1 is close to 90° in a low loss transformer. Thus, propagation delay between the voltage and current probes is one of the main error sources in ferrite loss characterization. The sensitivity of loss measurement has been well-discussed in [9] and can be formulated as

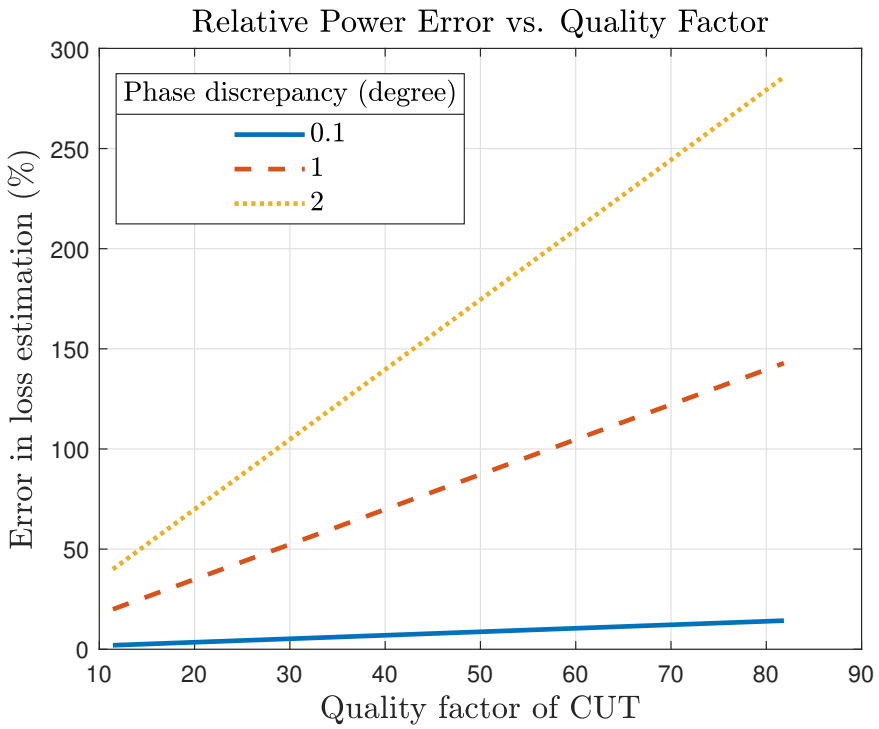


Figure 2. Error vs. Q factor for different phase discrepancy levels.

$$\begin{aligned} P_{error} &= tan(\theta) \cdot \Delta\theta \\ &= Q \cdot \Delta\theta \end{aligned} \tag{3}$$

where θ represents the phase difference between the voltage and current waveforms and $\Delta\theta$ is the phase shift discrepancy between the voltage and current sensors. Q is the quality factor of the ferrite core under test (CUT) and is expressed as

$$Q = \frac{\omega L_M}{R_{Core}} \tag{4}$$

Figure 2 shows the error in the loss measurement caused by the phase discrepancy between probes.

The measurement error increases with the quality factor of the CUT in a fixed measurement setup. A phase discrepancy of 1° can produce 100% error for a coil with a Q factor larger than 60, while the Q factor can even reach 80 in real measurement. As a result, the phase discrepancy can generate a large measurement error in the hundreds of kHz range and above. Moreover, the phase shift of a probe is typically brought by the propagation delay of its cable and the internal amplifier, which is larger under a high frequency range. As an example, a propagation delay of 28 ns generates a 1° phase shift at 100 kHz, and the phase shift is 10 times larger, i.e., 10° at 1 MHz. Therefore, it is essential to compensate for the phase discrepancy especially for high-frequency and low-loss applications.

2.2. CHALLENGES IN CHARACTERIZATION FOR COMMERCIAL PROBES

Most electric ferrite characterization methods [10, 11, 12, 15] were developed based on commercial active probes, which provide high input impedance and consistency of propagation delay between different units. However, the vendors only provide data under limited operating conditions, e.g., the propagation delay from probe tip to output is provided for a Tektronix P6251. Extra delay can be introduced by an external probe tip, and the exact value of the delay is not provided.

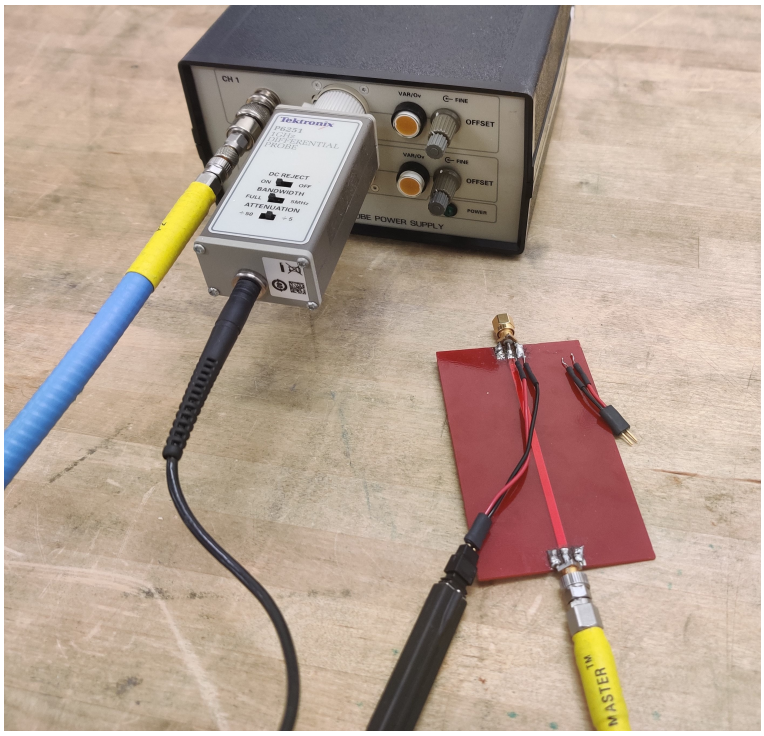


Figure 3. Photograph of the current probe.

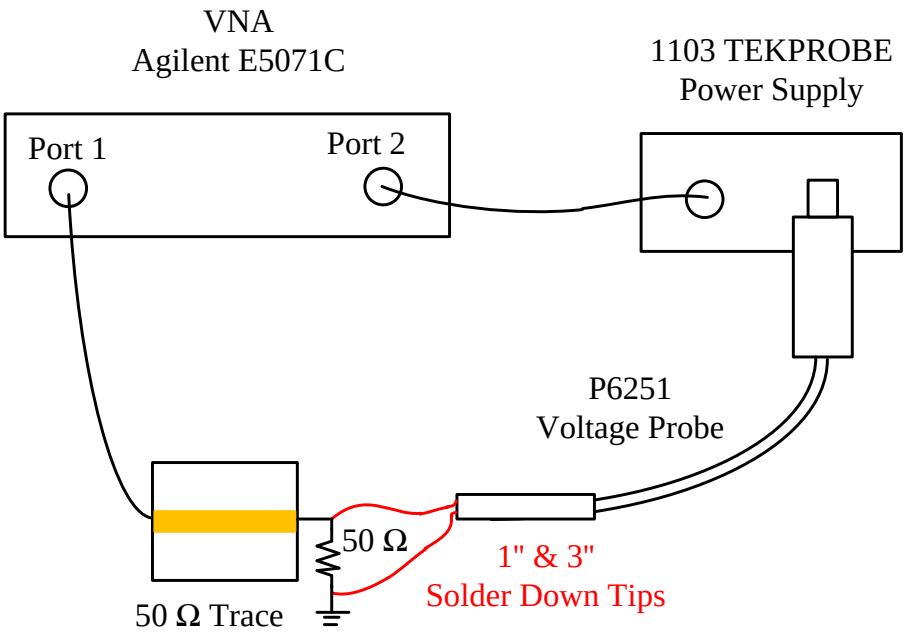


Figure 4. Gain and phase of the transfer function for the current probe.

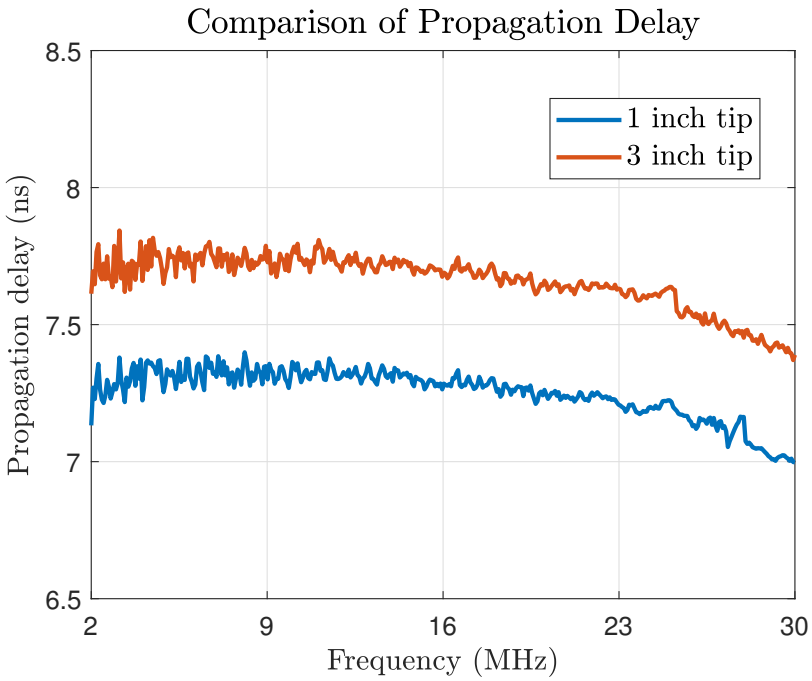


Figure 5. Measured propagation delays of P6251 with different solder tips.

A VNA is an instrument that measures the wide-band network parameters of electric devices and has been widely used for probe characterization. Due to the various probe-to-instrument interfaces defined by different manufacturers, using a VNA to measure the electric performance of active probes can be difficult. Fortunately, active probes with a TekProbe interface can be powered by its probe power supply (TekProbe power supply 1103) and connected to any instrument with 50 Ω input impedance. The propagation delay and attenuation of an active voltage probe can be directly extracted from S_{21} measurement, which are formulated as

$$Attenuation = 1/mag(S_{21}), \tag{5}$$

$$T_d = \frac{\Delta Phase(S_{21})}{\Delta\omega}, \tag{6}$$

where ω is the frequency of S_{21}.

The propagation delays and attenuation are measured with the same trace, coax cables and 50 Ω terminator, as shown in Figure 5. A ~ 300 ps difference in delay is observed, which is brought by the difference in tip length. The delay due to the probe tip is not provided by the vendor. In addition, the propagation delays are not constant values even in the 2 to 30 MHz range. Applying delay data provided by the vendor in probe compensation can introduce unacceptable error, especially in high frequency applications [15]. Even though the measurement accuracy is less sensitive to attenuation error voltage, the non-constant attenuation will introduce extra error.

In summary, commercial probes cannot provide a constant propagation delay among operating bandwidths. A large measurement error can be generated if the frequency-dependent propagation delay is not captured and compensated.

3. IMPLEMENTATION AND CHARACTERIZATION METHODS FOR THE VOLTAGE PROBE

A probe can be characterized using a VNA as demonstrated in Section II. An impedance converter is designed that allows the attachment of high-impedance passive probes to a VNA and gets rid of the limitation of commercial probes. The design considerations for the probing system are also discussed.

3.1. IMPLEMENTATION FOR IMPEDANCE CONVERTER-BASED PROBE

A passive voltage probe is typically connected to a 1 MΩ input channel of an oscilloscope, the equivalent circuit of both probe, and scope is illustrated in Figure 6.

The passive voltage probe can be modeled as the combination of a parallel RC circuit and a transmission line. The probe tip resistance R_P is typically 9 MΩ which gives a 10:1 diving ratio with the scope's 1 MΩ input resistance R_S. At dozens of kHz and above, the same dividing ratio is achieved by the capacitances of the probe tip C_P (typical value: 10 pF), transmission line C_{TL} and scope channel C_S (typical value: 15 ~ 30 pF).

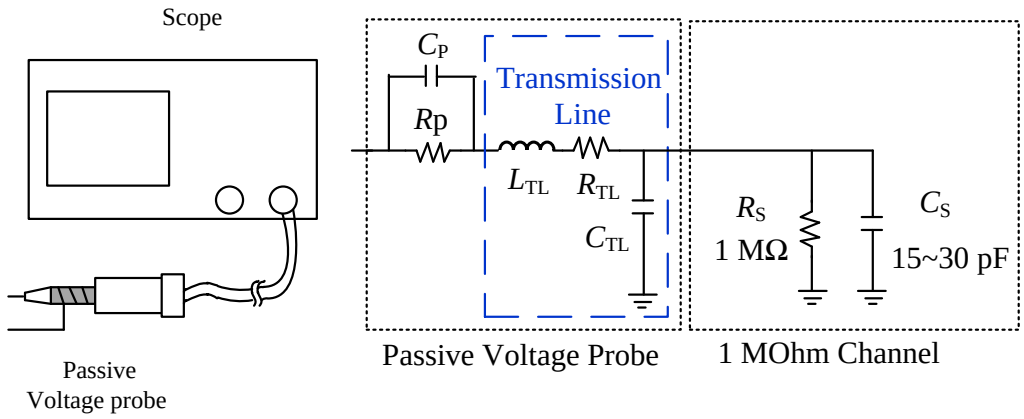


Figure 6. Equivalent circuit of a probe connected to a 1 MΩ channel.

The impedance converter is then designed to reproduce the input impedance of a 1 MΩ channel of the scope. It consists of an operational amplifier and a parallel RC network. The input-output voltage transfer function of the combined voltage probe and impedance converter TF_{VP} can be measured by a VNA. The measurement setup and equivalent circuit of the probing system are demonstrated in Figure 7 and Figure 8, respectively.

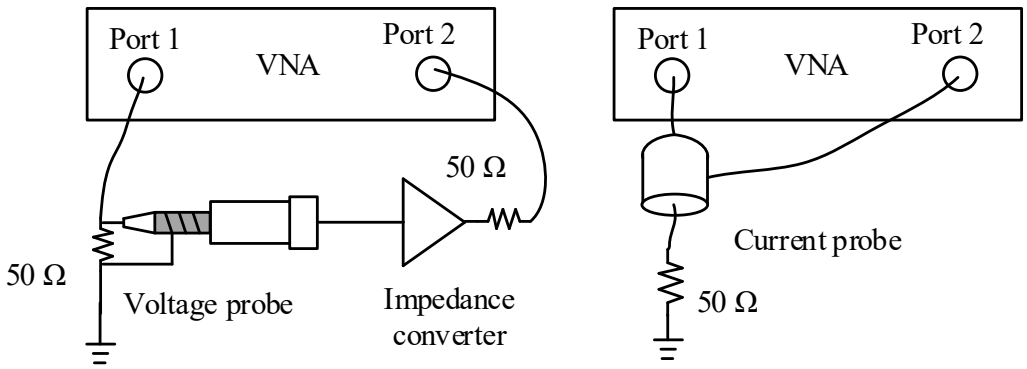


Figure 7. Characterization setups for voltage probing system and current probe.

As demonstrated in Figure 8, V_1 is the voltage source generated by port 1 with a 50 Ω source impedance. Port 1 is terminated with a 50 Ω load; therefore, V_{P1} is denoted as the output voltage of port 1 and is measured by the voltage measurement circuit.

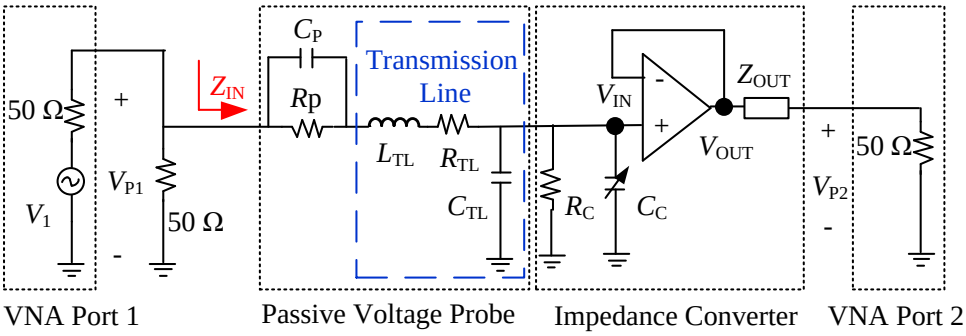


Figure 8. Equivalent circuit for the voltage probing system characterization setup.

To calculate the transfer function of the voltage measurement circuit, the input impedance of the probe needs to be calculated first as:

$$Z_{IN}(\omega) = (\frac{1}{j\omega C_P}//R_P) + j\omega L_{TL} + R_{TL} + (\frac{1}{j\omega(C_C + C_{TL})}//R_C). \tag{7}$$

We note that L_{TL} and R_{TL} are in the range of nH and hundreds of ohms and, thus can be neglected. In addition, in the frequency range of interest (< 30 MHz), $Z_{IN} >> 50\Omega$; therefore, the signal picked up by the voltage probe V_{P1} is given by

$$V_{P1} = V_1 \cdot \frac{(50\Omega//Z_P)}{50\Omega + (50\Omega//Z_P)} \approx (\frac{V_1}{2}). \tag{8}$$

The output of the voltage probe is connected to the impedance converter and the input signal of the impedance converter V_{IN} can be easily found as:

$$V_{IN} = V_{P1}\frac{Z_C//Z_{CTL}}{Z_P} \tag{9}$$

where Z_C and Z_{CTL} are the input impedances of the impedance converter and the parasitic capacitance of the transmission line, respectively.

$$Z_C = R_C//\frac{1}{j\omega C_C} \tag{10}$$

$$Z_{CTL} = \frac{1}{j\omega C_{CTL}}. \tag{11}$$

Due to the negative feedback provided by the amplifier, $V_{OUT} = V_{IN}$. The voltage V_{P2} induced on port 2 can be written as

$$V_{P2} = V_{OUT} \cdot \frac{50\Omega}{Z_{OUT} + 50\Omega}. \tag{12}$$

The output impedance of the converter is configured to be 50 Ω for impedance matching.

Finally, the transfer function of the combined voltage probe and impedance converter $TF_{VP}(\omega)$ can be related by the two port voltages V_{P1} and V_{P2} as:

$$TF_{VP}(\omega) = \frac{V_{P2}}{V_{P1}} = \frac{Z_C // Z_{CTL}}{2Z_P} = S_{21VP}. \tag{13}$$

The transfer function TF_{VP} contains both attenuation and phase information among the whole measurement frequency range.

3.2. CHARACTERIZATION FOR A CURRENT PROBE

The characterization method for the current probe is well known[16], and the measurement setup is depicted in Figure 7. The current-voltage transfer function of the probe TF_{CP} at different source frequencies ω can be expressed as:

$$TF_{CP}(\omega) = S_{21CP} \times 50. \tag{14}$$

3.3. MEASUREMENT PROCEDURE

As the measured phase shift discrepancy is frequency dependent, the fast Fourier transform (FFT) is applied to the measured time domain voltage and current waveforms. After compensation is performed in the frequency domain, the loss can be calculated.

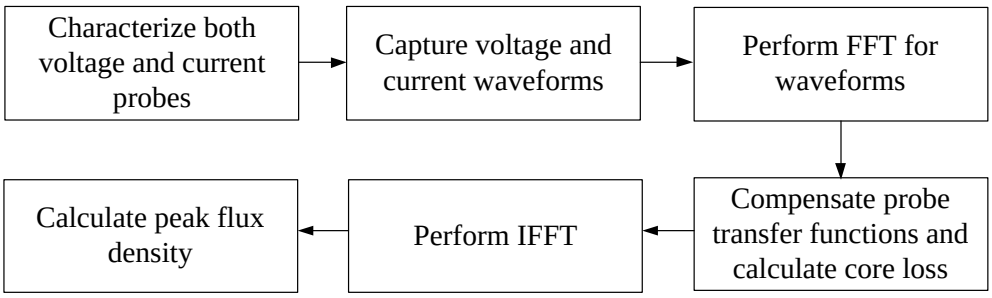


Figure 9. Flowchart for the proposed method.

Then, the inverse fast Fourier transform (IFFT) is applied for the voltage waveforms and the compensated peak flux density is obtained. The flowchart of the proposed measurement method is shown in Figure 9.

3.4. DESIGN CONSIDERATIONS FOR THE VOLTAGE PROBING SYSTEM

Despite the benefits introduced by the impedance converter, there are still limitations in the designed voltage probing system. First, the high-speed operational amplifiers have a limited voltage output swing (typically less than 10 V), and an extra attenuator is required for high flux measurement cases. Second, the input impedance of passive probes is not sufficient for high-frequency applications [10]. The two issues can be solved by introducing another attenuating capacitor into the probing system, as shown in Figure 10.

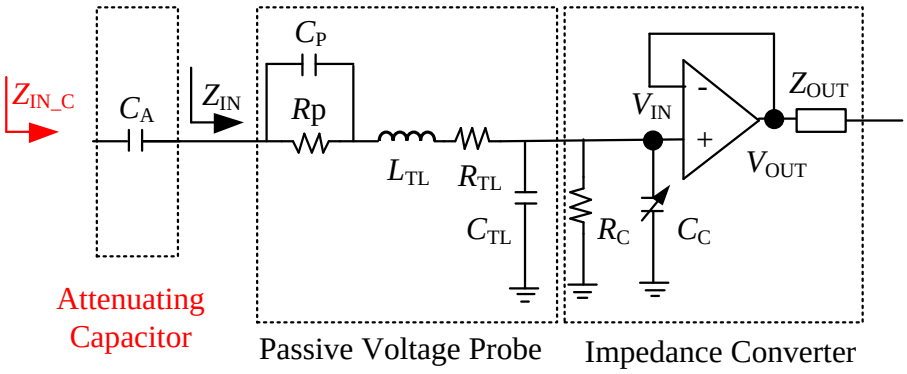


Figure 10. Equivalent circuit model with the attenuating capacitor.

The total input impedance of the probing system Z_{IN_C} with the attenuating capacitor C_A is expressed as

$$Z_{IN\_C} = \frac{1}{j\omega C_A} // Z_{IN}. \tag{15}$$

In addition, the extra attenuation ratio AR generated by C_A, it can be formulated as

$$AR = \frac{Z_{IN}}{Z_{IN\_C}}. \tag{16}$$

In summary, both the input impedance and maximum input voltage of the probing system can be extended with an extra attenuating capacitor.

4. CHARACTERIZATION OF THE VOLTAGE PROBING SYSTEM AND CURRENT PROBE

4.1. VOLTAGE PROBING SYSTEM

Figure 11 shows the prototype of the impedance converter and the voltage probe. The impedance converter is built with an operational amplifier (Analog Device ADA4817-1) and a passive probe (R&S RT-ZP10). R_C is configured as 1 MΩ and C_C is a tunable capacitor whose capacitance value ranges between 1-30 pF. This configuration provides an attenuation ratio of 20, i.e., 26 dB.

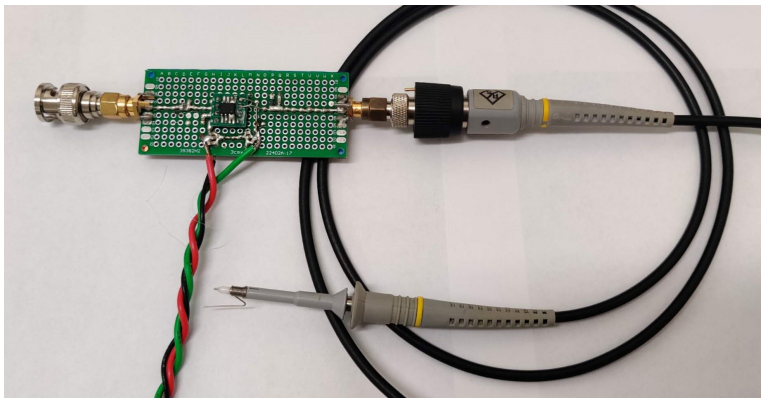
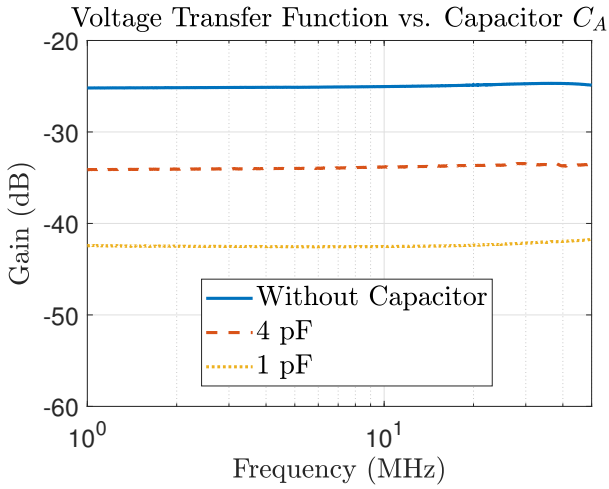
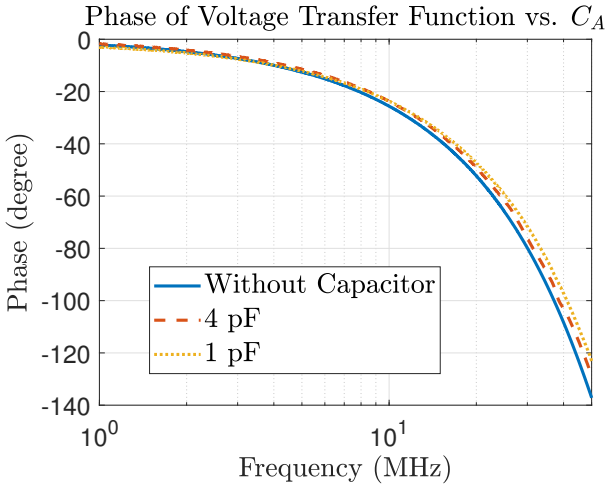


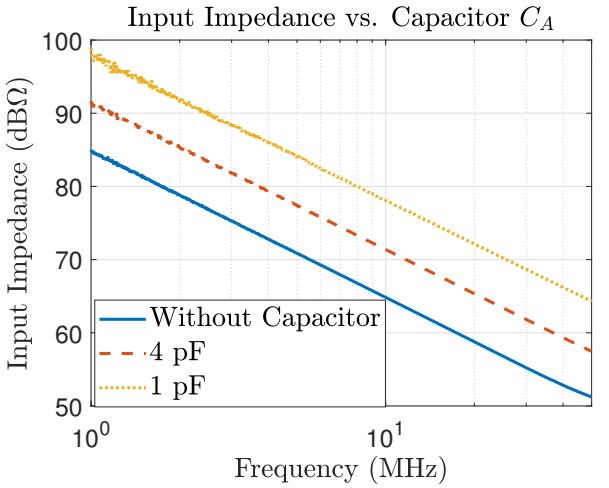
Figure 11. Prototype of the impedance converter and the passive voltage probe.



(a) Gain of the voltage transfer function.



(b) Phase of the voltage transfer function.



(c) Input Impedance of the voltage probe.

Figure 12. Influence of C_A on the voltage measurement circuit.

To verify the proposed equivalent circuit of the voltage probe, the input impedance and the transfer functions are measured for the cases where C_A is not added, C_A = 4 pF and C_A = 1 pF. The measurement setup is demonstrated in Figure 7.

The measured gain and phase values of the voltage transfer function for three cases are shown in Figure 1.12(a) and 1.12(b), respectively. The calculated gains with a capacitance of 4 pF and 1 pF are -36 dB and -46 dB, respectively, which agrees well with the measured results. Smooth voltage transfer functions are obtained up to 50 MHz from the current design and can be extended to a higher frequency with better control of parasitics in the amplifier board.

The input impedance Z_{IN_C} also increases with external capacitor C_A, which is verified in Figure 1.12(c). The input impedance is measured directly by the VNA. The input impedance of the voltage probe decreases at a rate of 20 dB/dec, which validates the capacitor-based circuit model. In addition, the capacitances extracted from the measurement are 8.9 pF, 3.6 pF and 2 pF when C_A is not added, while the expected capacitances are 10 pF, 2.8 pF and 1 pF, respectively.

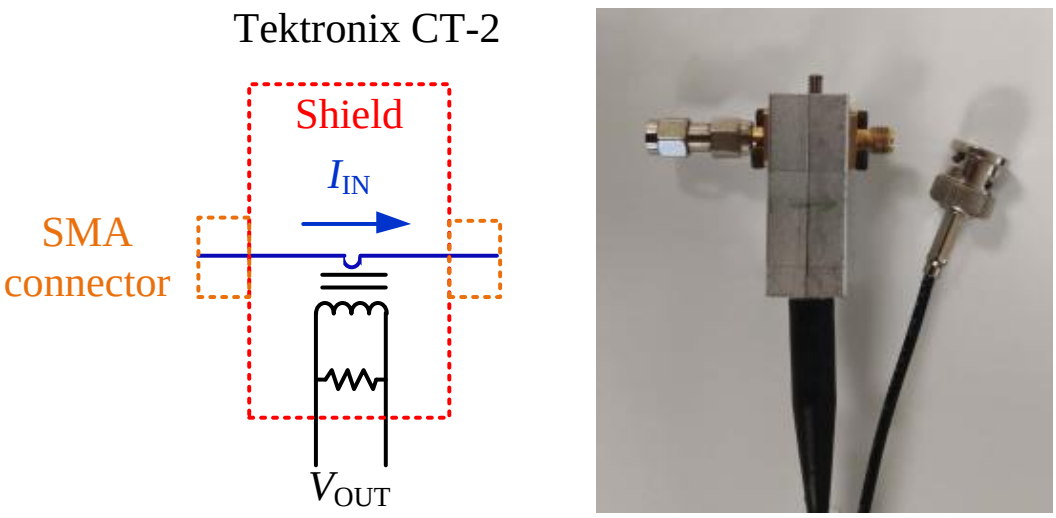


Figure 13. Photograph of the current probe.

4.2. CURRENT PROBE CHARACTERIZATION

The current probe (Tektronix CT-2 with P6041 probe cable) and its transfer function are shown in Fig 14. Two SMA connectors are connected in series and installed on the current probe so that the probe can be directly connected to other instruments using coaxial connectors. The current I_{IN} flowing through the probe can be measured by the output voltage V_{out}.

We note that the gain of the current probe is approximately a constant value up to 50 MHz, while the phase shift can reach 20° at 10 MHz. This phase shift is due to the propagation delay of the current probe and its cable.

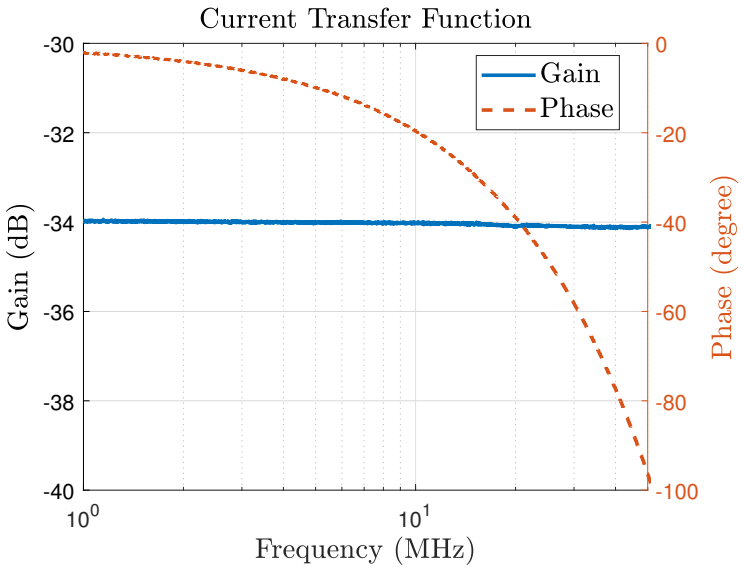


Figure 14. Gain and phase of the transfer function for the current probe.

5. EXPERIMENTAL VALIDATION

5.1. CORE LOSS CHARACTERIZATION

To verify the proposed characterization method, an experiment was built as shown in Figure 15.

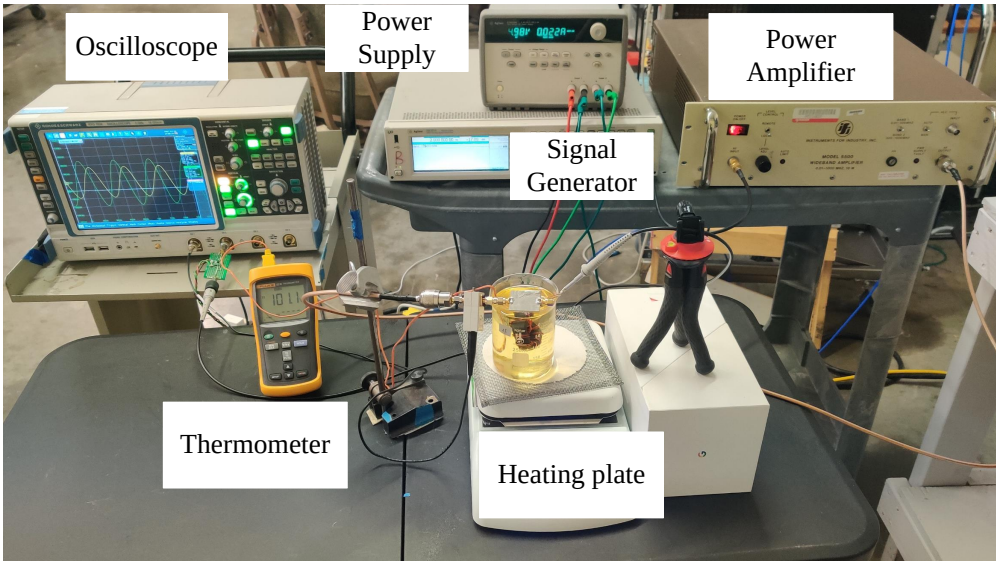
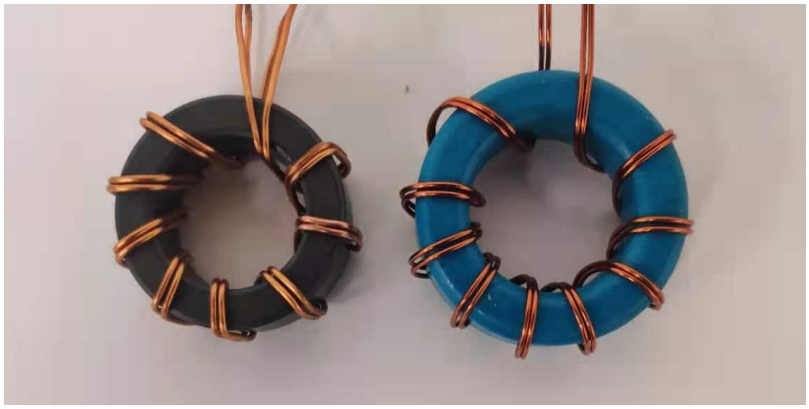


Figure 15. Photograph of the core characterization setup.

It consists of a signal generator (Agilent N5181A), a power supply (Agilent E3648A), a power amplifier (Instruments for industry 5500) and an oscilloscope (R&S RTO1024, 10 GS/s with 2 GHz bandwidth).

In addition, the ferrite core is immersed in the oil bath on a hot plate, and its temperature is supervised by a thermocouple. The setup supports high temperature core loss measurement up to 100° C without largely influencing the temperature of voltage and current probes. C_A is configured to be ~1-pF to increase the input impedance of the voltage probe. We note that two capacitors (2.1 pF, Murata, dielectric: C0G, voltage rating: 200 V) are connected in series to avoid capacitance variation due to the high voltage level.

Two different cores from TDK (R41.8/26.2/12.5N97) and Fair-Rite (T36/23/13-61) were characterized separately. Figure 12 shows the CUT samples made with 7 turns of AWG 24 copper wires. The losses measured by the in-house probe and P6251 (Tektronix, with a 1-inch solder down tip) are compared. Both commercial and in-house probes are compensated with the transfer functions measured by the VNA (Agilent E5071C).



Fair-Rite 61 TDK N97

Figure 16. Toroid samples with bifilar windings.

5.1.1. Measurement Results for Fair-rite 61. The measured core losses are compared with the datasheet results, as shown in Figure 17. The excitation frequency was set to 2 MHz, and the core losses at 25° C were measured. The losses measured by the in-house and the Tek P6251 are well matched, where the differences between two probes are within 3%. In addition, the errors are within 8% if we assume the manufacturer's loss measurement results are accurate. However, the loss due to mutual winding is not included and will be discussed in the next section.

5.1.2. Measurement Results for TDK N97. To demonstrate the measurement accuracy of the proposed method, the core loss of the TDK N97 core is measured under 700 kHz excitation.

The measured core losses are compared with those given by the datasheet in Figure 18. Similar to the previous measurement results, the discrepancy between the measurement results and the datasheet is less than 10%, which further validates the proposed probe characterization method.

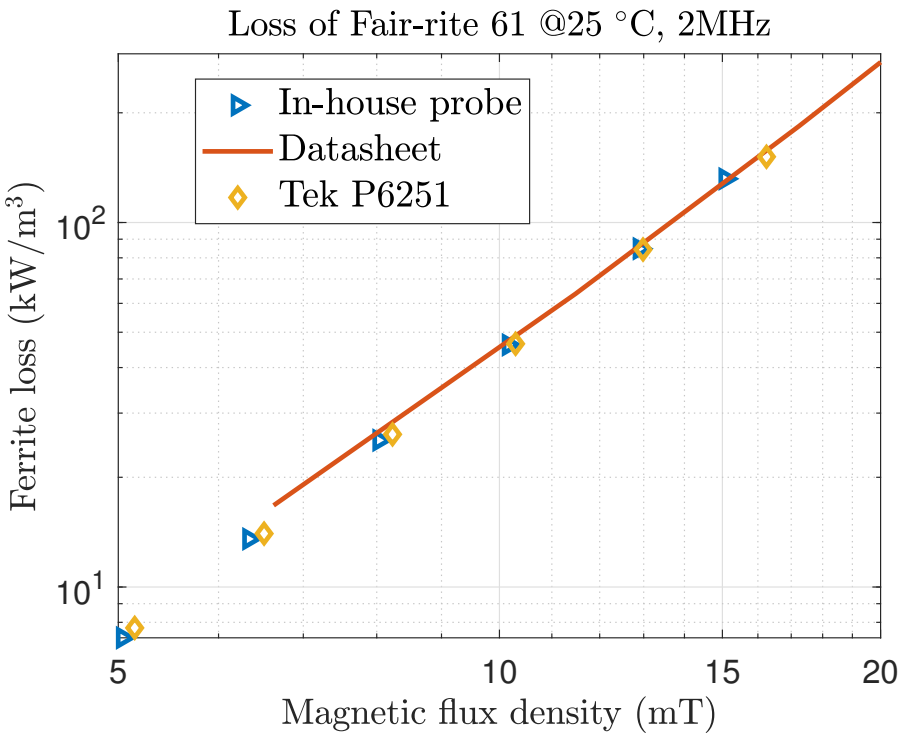


Figure 17. Core loss comparison between proposed method and datasheet.

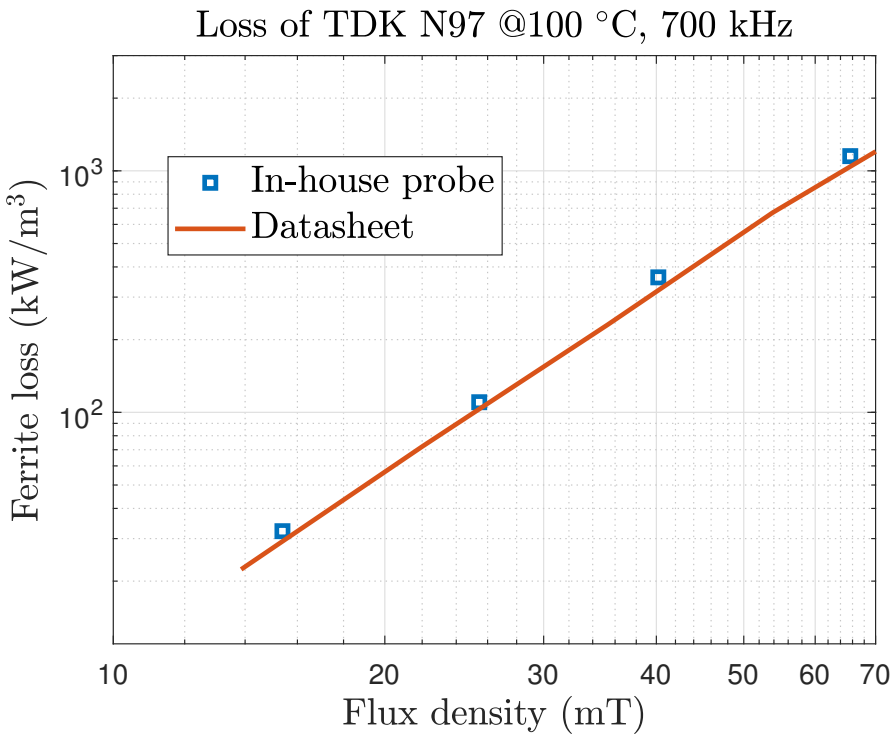


Figure 18. Core loss comparison between the proposed method and the datasheet.

5.2. CHARACTERIZATION OF MUTUAL IMPEDANCE OF A THREE-COIL SYSTEM

Due to the lack of a reference method for core loss characterization, validations performed with cores are not strong supports for the proposed method. A three-coil system with an air core is then developed for further validation. The experimental setup is depicted in Figure 19. The coil module consists of a primary, a secondary and a loading coil. According to [17], the mutual impedance Z_M between the primary and secondary coils can be expressed as:

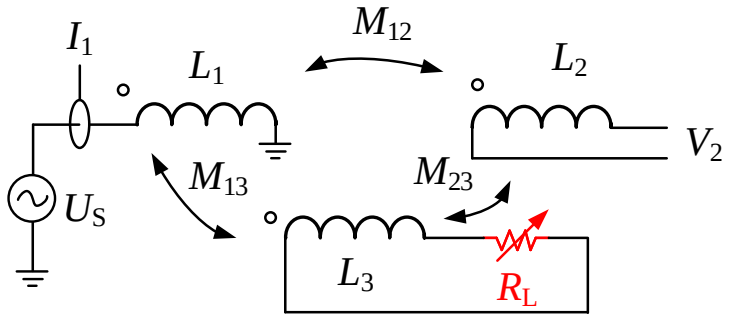


Figure 19. Equivalent circuit of the three-coil system.

The L_1, L_2 and L_3 correspond to self-inductance of the primary, secondary and loading coil. M_{12}, M_{13} and M_{22} represent the mutual inductance, R_L is the load resistance which is used to control the mutual impedance.

$$Z_M = \frac{V_2}{I_1} = \frac{\omega^2(M_{12}L_3 - M_{13}M_{23} - j\omega M_{12}R_L)}{R_L + j\omega L_3}, \tag{17}$$

where V_2 is the open circuit voltage of the secondary coil and I_1 is the input current of the primary coil. Due to the mutual coupling between three coils, Z_M can be controlled by the value of the load resistor R_L. We note that the three coils are assembled without a magnetic core and Z_M is a constant value under different excitation levels. Therefore, the Z_M measured by a VNA is compared with that measured by the setup shown in Figure 15.

Figure 20. Three-coil system prototype.

Figure 21 compares the phases of Z_M measured by different instruments. The phase changes with the load resistance R_L which validates the three-coil structure. In addition, the phase error between the two methods is limited to 0.2° in the frequency range of 2 to 15 MHz.

6. DISCUSSION

To ensure the accuracy of the proposed measurement method, it is necessary to identify and analyze various error sources in the system, including the influence of mutual resistance, measurement repeatability, loop size of the voltage probe, and linear region of probes .

6.1. INFLUENCE OF MUTUAL RESISTANCE

As discussed in [13, 14], the mutual resistance between primary and secondary windings is another main error source in core loss characterization. Unlike leakage winding loss, mutual resistance loss cannot be removed by the two-winding measurement method and thus can introduce significant error at high frequencies.

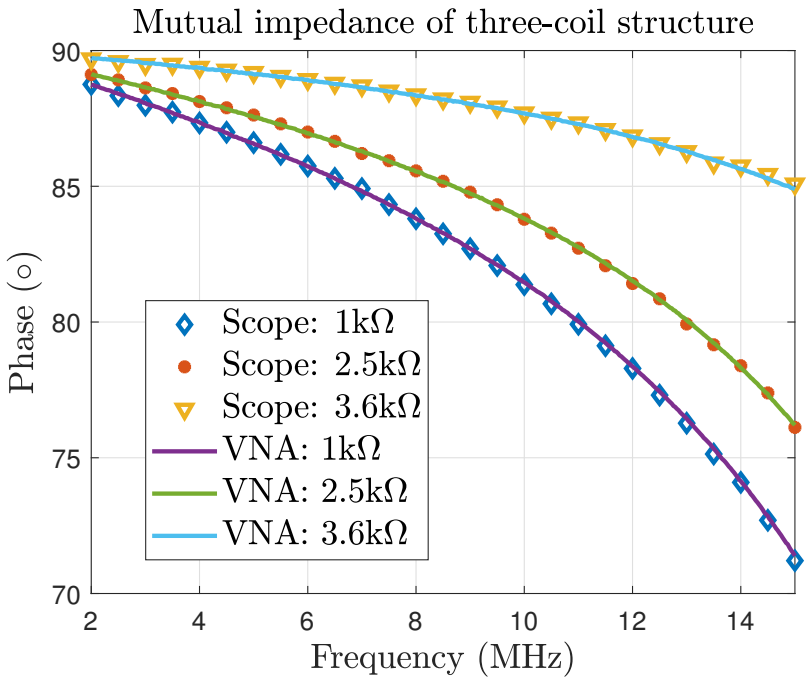


Figure 21. Comparison of mutual impedance measured by VNA and scope under different loading resistances.

The small signal core and mutual winding resistance of the Fair-Rite 61 sample are characterized by the VNA according to measurement method proposed in [13]. The excitation current of VNA was configured as ~ 2 mA, and the extracted mutual resistance was ~ 75 mΩ at 2 MHz, which is much smaller than the equivalent core resistance. The mutual winding loss can be neglected.

6.2. MEASUREMENT REPEATABILITY

The largest advantage of the proposed method is that the voltage and current probes are characterized before core loss measurement, and no tuning process is required during the test.

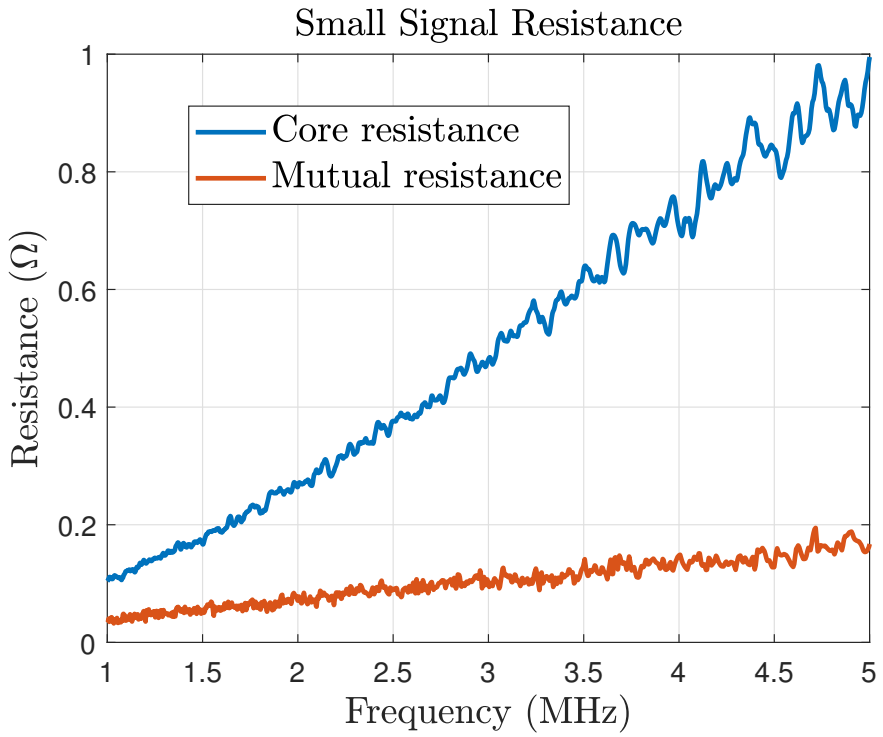


Figure 22. Extracted small signal core and mutual winding resistances. The output power of the VNA was configured as -10 dBm.

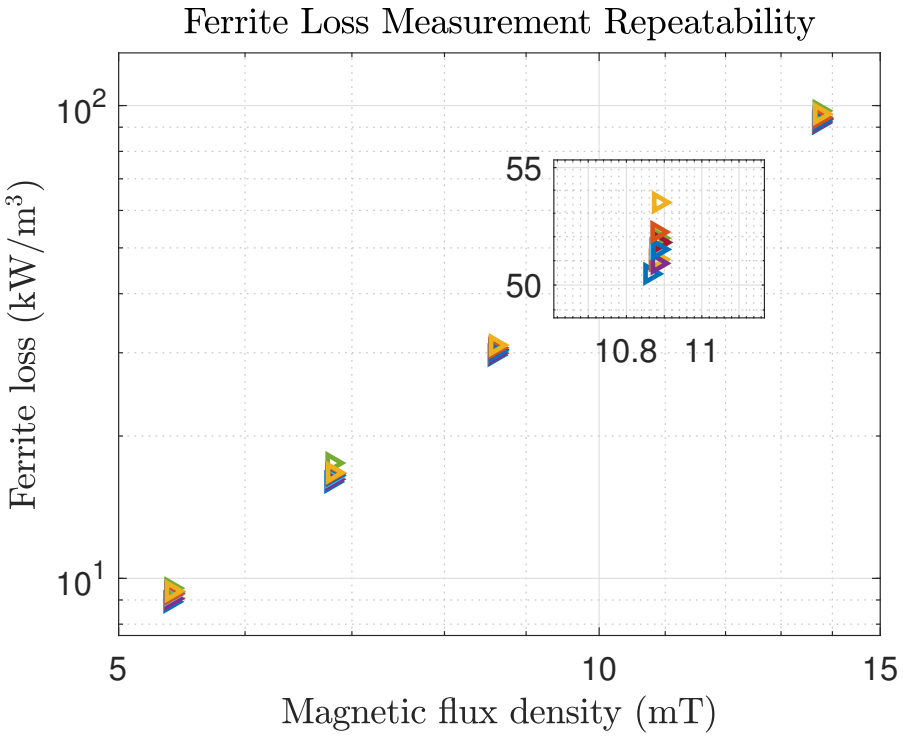


Figure 23. Measurement repeatability of the proposed method.

Repeatability of the measurement results is essential for the proposed method, as the positioning of the probes can potentially introduce uncertainty into the measurement results. Therefore, the results of 10 measurements are shown in Figure 23, where both the voltage and current probes are removed and reconnected to the circuit. The variation of the results is within 6%.

6.3. ERROR CAUSED BY LOOP DIFFERENT LOOP SIZES OF PICK-UP STRUCTURE

The input impedance of a voltage probe can be simplified as a capacitor as we demonstrated in Figure 12. But the parasitic inductance of the pick-up structure, that comes from the probe and installation of the DUT, can introduce extra error in the voltage measurement.

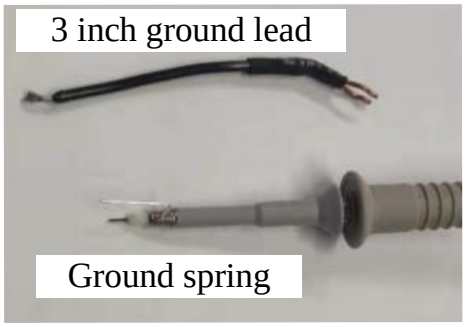


Figure 24. Photograph of different grounding structures.

To evaluate the error brought by the loop size, the differences in transfer functions measured with two ground structures are illustrated in Figure 25.

The comparison is performed without an external capacitor C_A, which is the case can be most affected by the parasitic inductance. Due to the larger loop size formed by the tip and 3-inch ground lead, extra attenuation and phase delay are introduced. We note that the phase difference is limited to 0.1° and the difference in gain is within 1% below 20 MHz.

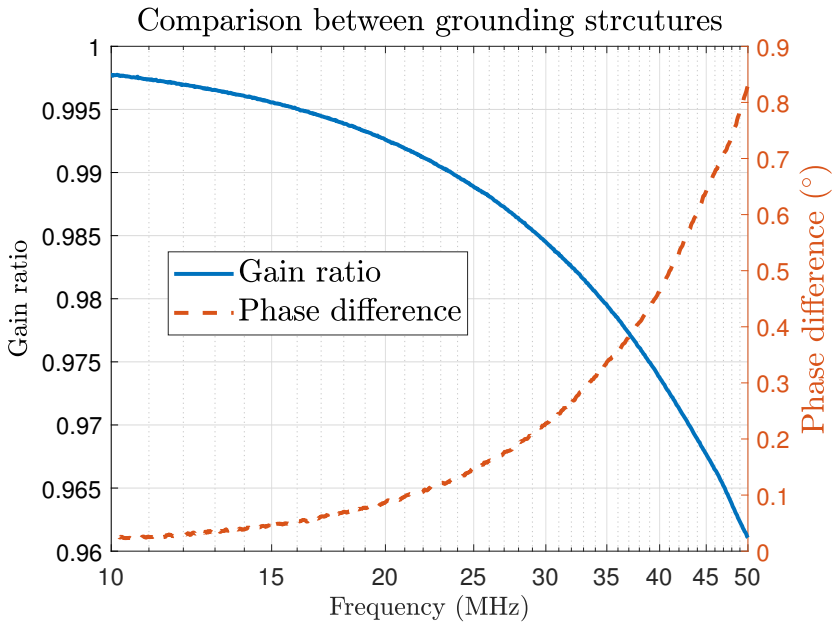


Figure 25. Gain ratio and phase difference between the ground spring and the 3 inch ground lead.

Despite the error is almost negligible below 20 MHz, consistency of the measurement loop between probe characterization and real measurement is still suggested to eliminate the possible error.

6.4. LINEAR REGION OF PROBES

The saturation of both voltage probe and current probes should be avoided. The linear operating region of the voltage probing system can be evaluated by the voltage transfer curve, which is defined as the ratio between input and output voltage. The same concept can be applied for the current probe or referring to the data from the manufacturer.

The output signal of the proposed voltage probing system is measured by a spectrum analyzer (R&S FSV30) under sinusoidal excitation, as shown in Figure 26. The input voltage is controlled by the signal generator and the frequency is configured as 2 MHz. We note that the input voltage is measured separately with a reference active voltage probe (Tektronix: P6251).

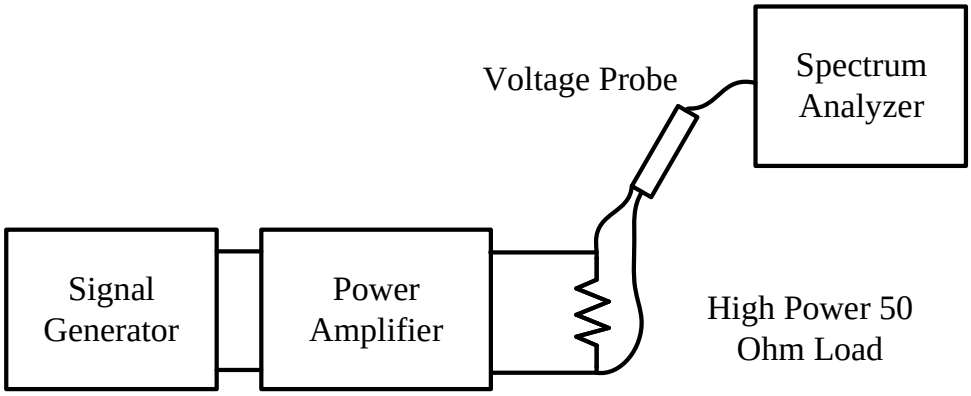


Figure 26. Measurement setup for the voltage transfer curve of voltage probing system.

Table 1. THD of the active probe.

THD of output voltage (%)	0.41	0.62	0.69	0.86	2.39	6.9
Output Voltage (V)	0.76	0.95	1.21	1.52	1.71	1.88

The measured voltage transfer curves of the in-house active probe are shown and plotted against an ideal one. As the gain of the internal amplifier is a constant value, the boundary compression point can be defined according to the output voltage. For this example, the probing system can be regarded as a linear system when the output voltage is less than 1.6 V, as shown in Figure 27. In addition, the total harmonic distortion of the probing system can be limited to 1% when the output voltage is below the threshold voltage. In summary, a higher attenuation should be applied to the probe once its output voltage is larger than 1.6 V. The THD of the probe (without external capacitors) is listed in Table1.

7. CONCLUSION

This paper proposes an impedance converter-based probe characterization method for core loss characterization. The in-house active probe eliminates the constraint of the complex probe-to-instrument interface in commercial probes, and the VNA-based probe characterization method can be applied. DUT-free probe compensation is then allowed

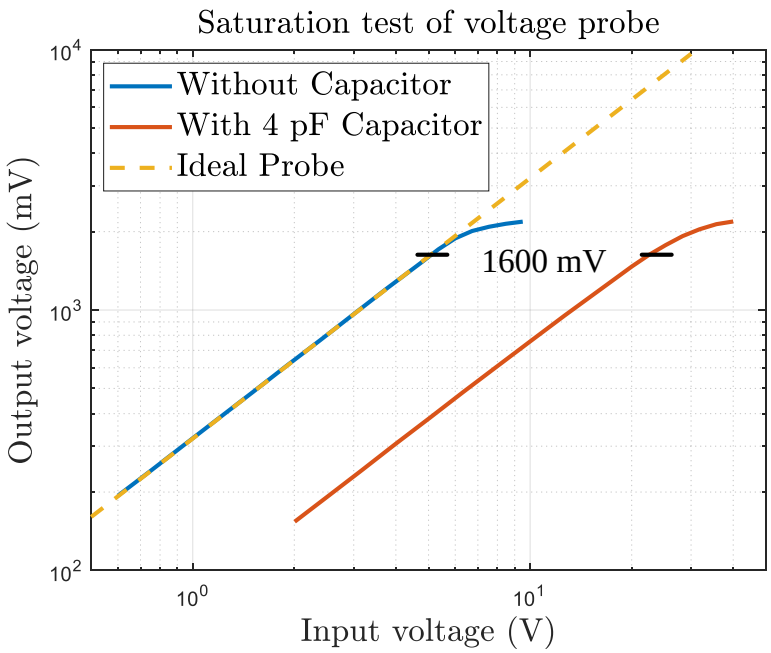


Figure 27. Voltage transfer curve of the voltage probing system with different configurations.

without extra phase cancellation components, which enables a fast and accurate core loss characterization. The proposed method is experimentally validated by a linear three-coil system with controllable mutual impedance. It demonstrates that the error in phase is limited to 0.2° compared with a VNA below 15 MHz. In addition, the core loss error between measurement results and data from the datasheet is below 10%.

Possible sources of error using this method are analyzed. In particular, the linear operating regions of probes are evaluated which overcomes the limitation of the small-signal measurement of a VNA.

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IV. IMPROVED CURRENT SHUT CHARACTERIZATION METHOD FOR FERRITE LOSS CHARACTERIZATION

ABSTRACT

With the increasing switching frequencies and power densities in modern power converters, magnetic core losses are becoming more essential for efficiency and thermal optimization. Traditionally, the two-winding method suffers from sensitivity to phase error in practical measurements; this is mainly brought by the unknown phase shift of a current-sensing resistor. Several methods have been developed to characterize the phase shift of a current shunt resistor; however, the load effects of oscilloscopes are neglected. As a result, the corresponding phase shift can be significantly underestimated. To solve this problem, this paper proposes an improved method for phase shift extraction of a current shunt. For validation, this paper considers a comparison between a resistor and a current probe. The measurement results validate the proposed method (up to 50 MHz). In addition, a shunt resistor implemented with a coaxial resistor array is designed with a phase shift of 0.1° at 16 MHz.

Keywords: Core loss, two-port resistor, current-to-voltage impedance, coaxial resistor

1. INTRODUCTION

Power converters with high efficiency and power density are increasingly pursued in modern consumer electronics. The switching frequency in a converter is then pushed to a higher range. However, a magnetic device, e.g., a transformer or an inductor, is one of the limiting factors in further improving power density. Therefore, accurate ferrite loss characterization is desired for the optimization of power converters in terms of cost, form factor and efficiency.

Various methods [1, 2, 3, 4, 5, 6, 7] have been developed for ferrite loss measurement, and the dual-winding method [4, 5, 6, 7] is the most widely used approach, as shown in Figure 1, where U_s is the excitation of the winding, and R_{w1}, R_{w2}, L_{w1} and L_{w2} correspond to the series equivalent resistors (ESRs) and the leakage inductances of the winding wires. L_M is the magnetizing inductance, R_{mw} is the mutual winding loss and R_{Core} is the corresponding core loss. The turn ratio of windings is defined as $N_1 : N_2$.

Although extra efforts are required to compensate for the mutual winding loss [7], this method is regarded as the reference method for core loss characterization due to its simplicity and accuracy. However, this method suffers from sensitivity to phase errors in current and voltage measurements. A 1° phase error can result in 100% error in ferrite loss measurement[5]. It is worth noting that the dominant sources of error come from the phase shift of the current sensor, which is brought by the propagation delay of a current probe or the parasitic inductance of a sensing resistor.

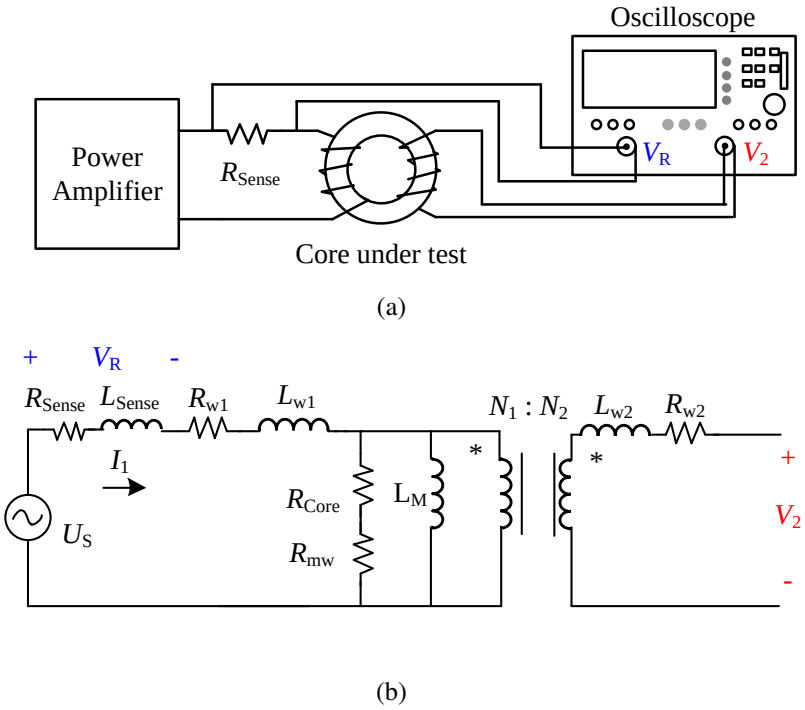


Figure 1. Measurement setup and its equivalent circuits.

Capacitive and inductive phase cancellation methods have been proposed to overcome the drawbacks of the original two-winding method. The phase difference between the voltage and current decreases from nearly 90° to nearly 0° with a capacitor or an inductor [5]. The measurement becomes much less sensitive to phase error. This type of method provides the highest accuracy among all the existing methods. However, perfect cancellation requires fine-tuning, and the characterization process is difficult to automate. Additionally, it is only applicable to applications with sinusoidal excitation.

Hence, there is an interest in developing methods based on calibrating the probes rather than cancelling the phase difference between the voltage and current waveforms. This challenge can be addressed through probe characterization with a vector network analyzer or a gain/phase analyzer [8]. The phase compensation can also be achieved with a high-quality capacitor [9]. However, the main limitation of the above methods is the negligence of the possible nonlinearity of a current probe. Current probes are fabricated with magnetic cores, and the phase shift of a current probe can change with the level of excitation, especially under DC bias. The saturation issue can be solved by using Rogowski coils, nevertheless, the phase shift of a Rogowski coil can be influenced by the probing position[10]. The positional error is hard to eliminate in the real applications.

Several ferrite loss characterization methods have been developed based on resistors due to their simple electrical property [4, 5, 11]. Resistive current sensors or shunts use the Ohm's law for a direct current-to-voltage conversion, however, the ESL of an ordinary two-terminal resistor is typically in nH range and can introduce tremendous error. The ESL of a resistor can be measured by an impedance analyzer [5] while the reproducibility of the ESL is extremely weak due to landing of probes. The inconsistent contact between a resistor and a probe can either add or subtract series inductance to the device under test (DUT) [12]. Despite being a simple linear component, the phase shift of a resistor is almost unpredictable when it's installed on a board. Therefore, state-of-art current shunts are implemented with coax connectors [13], which greatly improve the reproducibility of

probe-to-resistor connection. In addition, the parasitic inductance of a current shunt can be reduced with a coaxial resistor array. Its phase shift is controlled within 1° in dozens of MHz range. Nevertheless, the induced phase error is still intolerable without proper phase compensation, especially when the given material has low permeability and a high-quality factor.

The two-port measurement technique [14] is the reference method for low impedance measurement, and the transfer impedance, i.e., Z_{21}, is used to define the impedance of a current shunt. However, such a definition is only valid when the input impedance of the detector is infinitely large. A large error is generated if the loading effect of a measurement instrument is non-negligible. Therefore, the current-to-voltage impedance Z_{iv} of the current shunt cannot be represented by its transfer impedance Z_{21}.

The main original contribution of the paper involves rigorous modeling, derivation and experimental verification of the Z_{iv} of a two-port resistor when it is connected to a 50 Ω detector. Additionally, a coaxial current shunt prototype is built, and the phase shift is controlled within 0.1° below 16 MHz. This paper is organized as follows: the characterization method is discussed in Section II. In Section III, the modified core loss measurement setup and the associated post-processes are demonstrated. Measurements are utilized in Section IV to verify the consistency of the transfer functions under a high current input. Furthermore, an improved two-port resistor design with a circular resistor array is demonstrated and verified in Section V. Section VI concludes this paper.

2. IMPLEMENTATION AND CHARACTERIZATION OF A TWO-PORT RESISTOR

2.1. DESIGN CONSIDERATIONS AND IMPLEMENTATION OF THE PROTOTYPE

The structure of the proposed two-port resistor is demonstrated in Figure 2, which consists of a shunted chip resistor (2010 thin film, 1.2Ω), a 1-inch transmission line and two coaxial connectors. Compared with existing current shunts with only one coaxial connector, the two-port desin possesses two advantages. First, the resistor configuration remains the same for both impedance characterization and core loss measurement, which improves the fidelity of impedance characterization. Second, the conventional two-port impedance measurement method can be applied and directly compared with the proposed method.

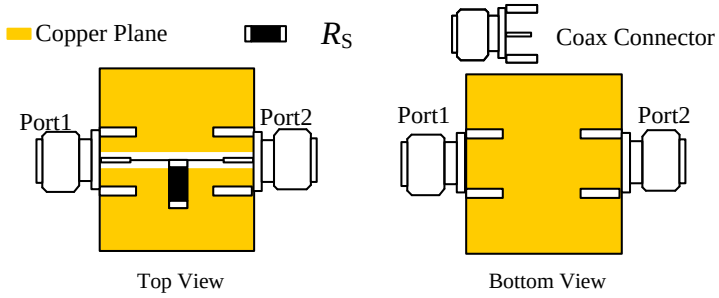
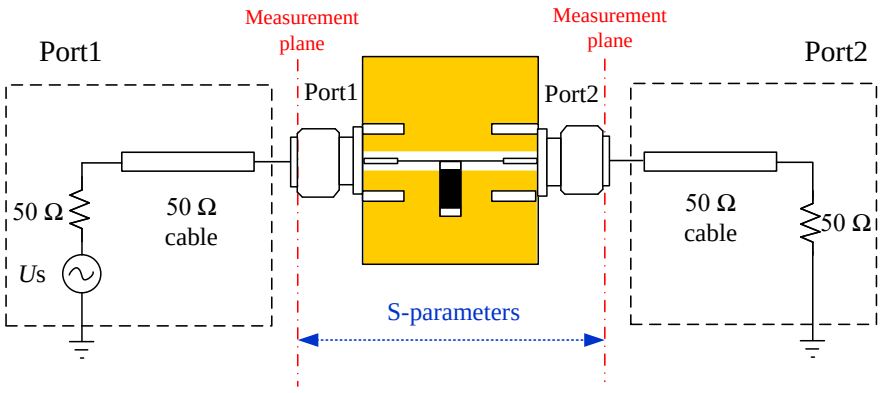


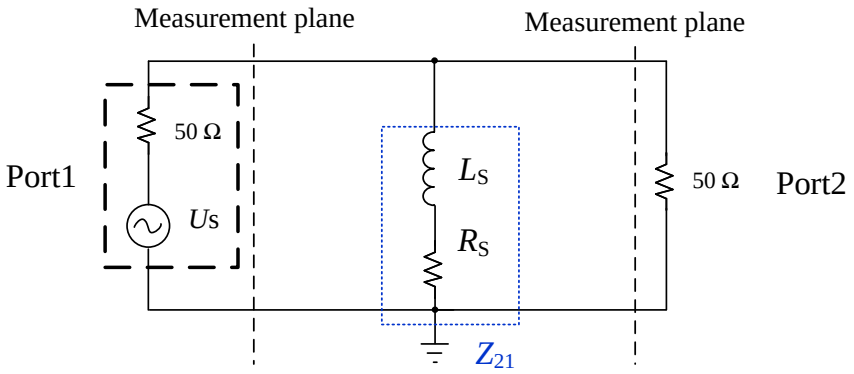
Figure 2. Diagram of the proposed two-port resistor with SMA coaxial connectors.

2.2. ELECTRICAL MODEL OF THE PROTOTYPE AND ITS CHARACTERIZATION METHOD

The two-port resistor can be directly characterized by a VNA because coaxial connectors are used, as demonstrated in Figure 1.3(a). In the measurement, port 1 is configured as the transmitter with an internal voltage source U_s, and port 2 is set as the receiver. The port impedance of both ports is 50 Ω. The calibration is performed to the end of connectors which removes the influence of cables and adapters.



(a)



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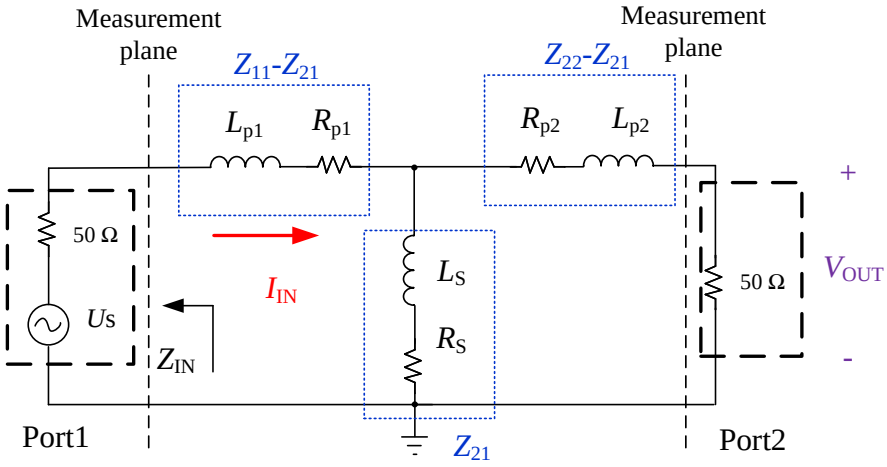


(c)

Figure 3. Equivalent circuits and measurement setup of the resistor.

2.2.1. Conventional Impedance Characterization Method. The equivalent circuit of the conventional method is shown in Figure 1.3(b). Only the transfer impedance Z_{21} is extracted from the measurement, which consists of the ESR R_S and ESL L_S of the sensing resistor. Parasitics of the fixture are considered in the improved method, where L_{P1}, R_{P1} and L_{P2}, R_{P2} are the ESLs and ESRs of the test fixture. The current-to-voltage impedance Z_{iv} of the current shunt is approximated as the transfer impedance Z_{21}, which can be formulated as [14]:

$$Z_{iv} \approx Z_{21} = 25\frac{S_{21}}{1 - S_{21}}. \tag{1}$$

It is worth noting that Z_{iv} equals Z_{21} only if the input impedance of the detector is infinitely large. Typically, the utilized measurement instrument has an input impedance of 50 Ω, and the corresponding loading effects cannot be neglected in dozens of MHz ranges and above. Additionally, the parasitic inductances and resistances of the test fixture are also neglected in the method.

2.2.2. Improved Current-to-Voltage Impedance Characterization Method. To correctly model the current-to-voltage impedance Z_{iv} of the structure, both parasitics components of fixture and a 50 Ω load should be considered, as shown in Figure 1.3(c). Z_{iv} is defined as the ratio between hte induced voltage V_{OUT} across the 50 Ω load and the input current I_{IN}, which is expressed as:

$$Z_{iv} = \frac{V_{OUT}}{I_{IN}}. \tag{2}$$

The Z-parameters matrix can be calculated according to the measured S-parameters obtained by a VNA[15]. Figure 1.3(c) depicts the equivalent circuit represented by the Z-parameters.

In this circuit, ω represents the source frequency. After the Z-parameters are obtained from the S-parameters, the input impedance Z_{IN} of the two port circuit can be expressed as follows [15]

$$\begin{aligned} Z_{IN} &= Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_0} \\ &= Z_{11} - \frac{Z_{21}^2}{Z_{22} + Z_0}. \end{aligned} \tag{3}$$

Then, the input current can be calculated accordingly:

$$I_{IN} = \frac{U_S}{Z_0 + Z_{IN}}. \tag{4}$$

The voltage V_{21} across the mutual impedance Z_{21} can then be formulated as

$$V_{21} = U_S - I_{IN}(Z_0 + Z_{11} - Z_{21}). \tag{5}$$

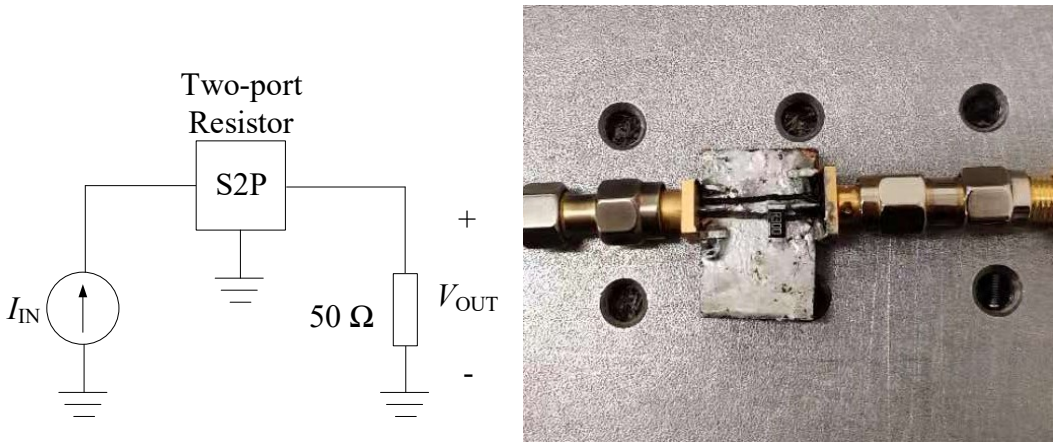
The output voltage V_{OUT} at the receiver with a 50Ω impedance can be obtained as follows:

$$V_{OUT} = V_{21}\frac{Z_0}{Z_0 + Z_{22} - Z_{21}}. \tag{6}$$

The Z_{iv} of the resistor could be calculated by substituting (4) and (6) into (1).

$$Z_{iv} = \frac{Z_0 Z_{21}}{Z_0 + Z_{22}} = 50\frac{Z_{21}}{50 + Z_{22}}. \tag{7}$$

Similar to those of VNAs, the input impedances of high-frequency oscilloscopes can be set to 50 Ω and the Z_{iv} remains the same as it is connected to the scope in the practical core loss measurement setup.



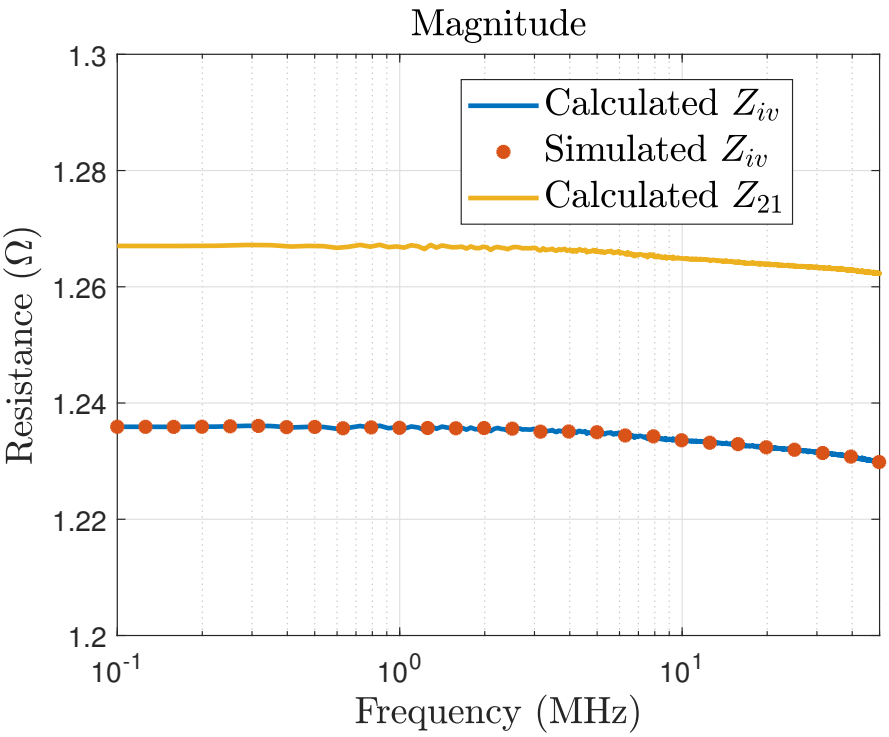
(a) (b)

Figure 4. (a)Simulation configuration for Z_{iv} extraction; (b) Photograph of the prototype.

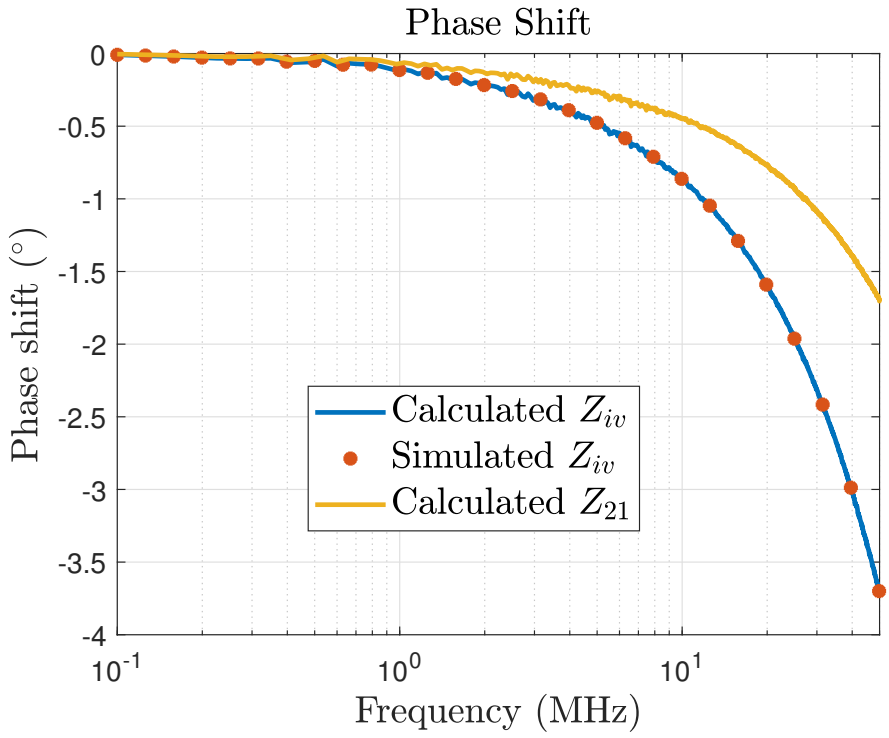
2.3. PROTOTYPE IMPLEMENTATION AND SIMULATION VALIDATION

To verify the proposed impedance extraction method, a simulation model is implemented in Advanced Design System (ADS). The simulation setup is shown in Figure 1.4(a). The first port is excited by an AC current source I_{IN}, and the second port is terminated with a 50 Ω resistor, which represents the input impedance of an oscilloscope. The "S2P" block represents the two-port S-parameters of the prototype that are measured by a VNA (Model: Agilent E5071C), which is illustrated in Figure 1.4(b).

Figure 5 compares the magnitudes and phases of the impedance with different definitions. The simulated and calculated Z_{iv} value represent the results obtained from the simulation and according to (7), respectively. The magnitudes and phases are well matched, which validates the Z_{iv} calculation method. Additionally, a 2% discrepancy is observed in the magnitudes calculated for Z_{iv} and Z_{21}. This disagreement is brought by the loading effect of 50 Ω. More importantly, the 50 Ω load introduces a $\sim 0.5°$ error in the phase at only 10 MHz. Significant errors will be generated at higher frequencies.



(a) Amplitude of Z_{iv} and Z_{21}.



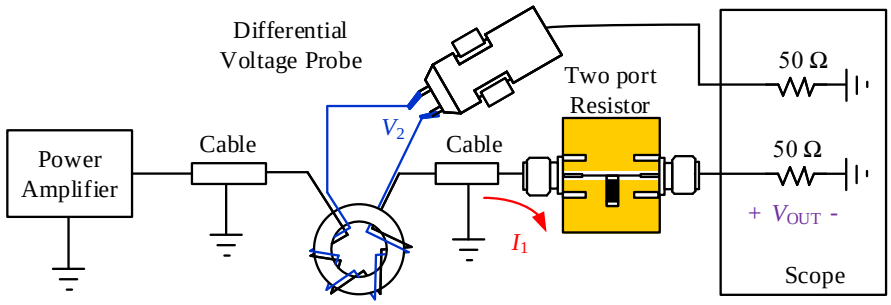
(b) Phase of Z_{iv} and Z_{21}.

Figure 5. Verification of Z_{iv}.

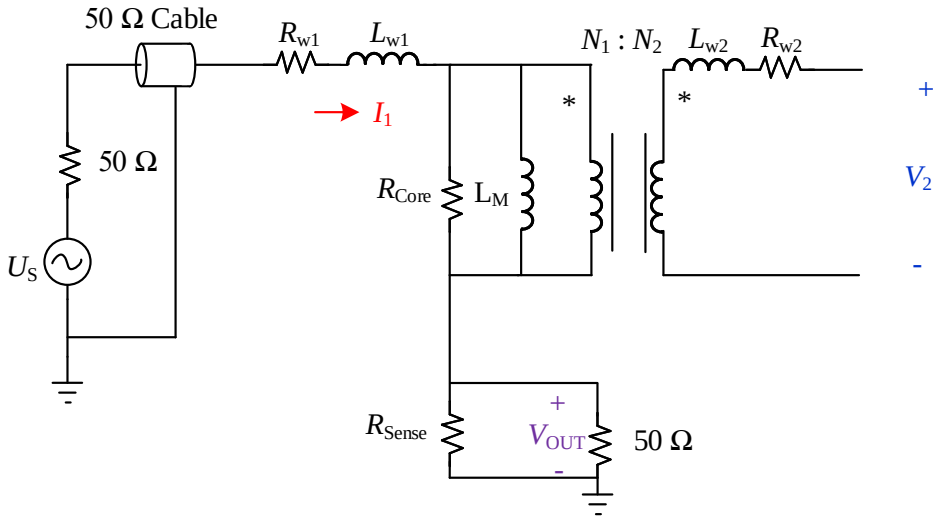
3. CORE LOSS MEASUREMENT SETUP AND ERROR ANALYSIS DUE TO THE INPUT IMPEDANCE OF AN OSCILLOSCOPE

3.1. MEASUREMENT SETUP AND CALCULATION FLOW

In this section, the modified core loss measurement setup and the loss calculation procedures are presented. The measurement configuration and its equivalent circuit are shown in Figure 6.



(a) Diagram of core loss characterization setup with the two-port resistor.



(b) Equivalent circuit of modified core loss measurement setup.

Figure 6. Diagram and equivalent circuit for the modified core loss measurement setup.

The system consists of an RF power amplifier source and a dual-winding transformer; this is the same as the original measurement setup as shown in Figure 1.1(a). We note that the input impedance of the oscilloscope should be set to 50 Ω. Similar to the original setup,

a high impedance voltage probe should be applied for voltage measurement. In addition to the resistor, the propagation delay of the voltage probe should also be obtained. It may be provided by its vendor or could be characterized with a VNA.

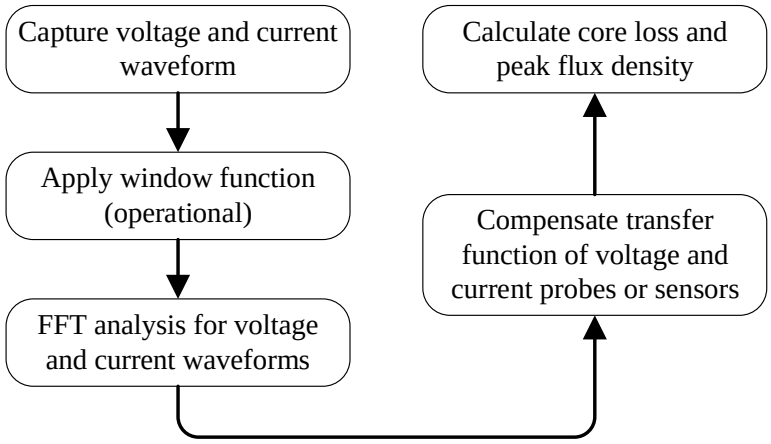


Figure 7. Calculation flow for current sensing compensation and core loss measurement.

Due to the frequency-dependent phase shifts of both voltage and current sensors, frequency-domain analysis and compensation are preferred. Therefore, a fast Fourier transform (FFT) is applied to the measured time-domain voltage and current waveforms. The calculation process for flux density has been well discussed in [16]. The calculation flow for core loss measurement is demonstrated in Figure 7.

3.2. ERROR DUE TO THE INPUT IMPEDANCE OF AN OSCILLOSCOPE

The Z_{iv} of a two-port resistor can be accurately characterized by a VNA; however, the reproducibility of the Z_{iv} is influenced by the nonideal characteristic of the oscilloscope, e.g., ADC interleaving, the RF front-end transfer characteristic and magnitude resolution [17, 18]. Only the input port impedances of real time oscilloscopes (RTO) are discussed in the paper. Errors related to other factors are also important for performance, but they are not treated in this paper and are considered as an additional measurement noise.

The port matches of three RTOs are measured with a VNA (Agilent E5071C). The port impedance versus the frequency is shown in Figure 8. It is clear that the port impedances of oscilloscopes are not exact 50 Ω. The impedance discrepancy between an oscilloscope and the VNA introduces extra phase error into the real measurement. To examine the errors introduced by the input impedance of an oscilloscope, the Z_{iv} of the resistor prototype is evaluated with 48 Ω and 50 Ω resistive loads according to (7). Due to the small impedance of the resistor, i.e. 1.2 Ω, the errors are less than 10 mΩ in terms of magnitude. The errors in phase in comparison with those of the 50 Ω load case are illustrated in Figure 9. As observed from the calculation, the error increases with frequency but is limited to 0.1° at 50 MHz. However, it should be emphasized that port impedance mismatches can introduce intolerable errors at hundreds of MHz, which is the main limitation of the proposed method.

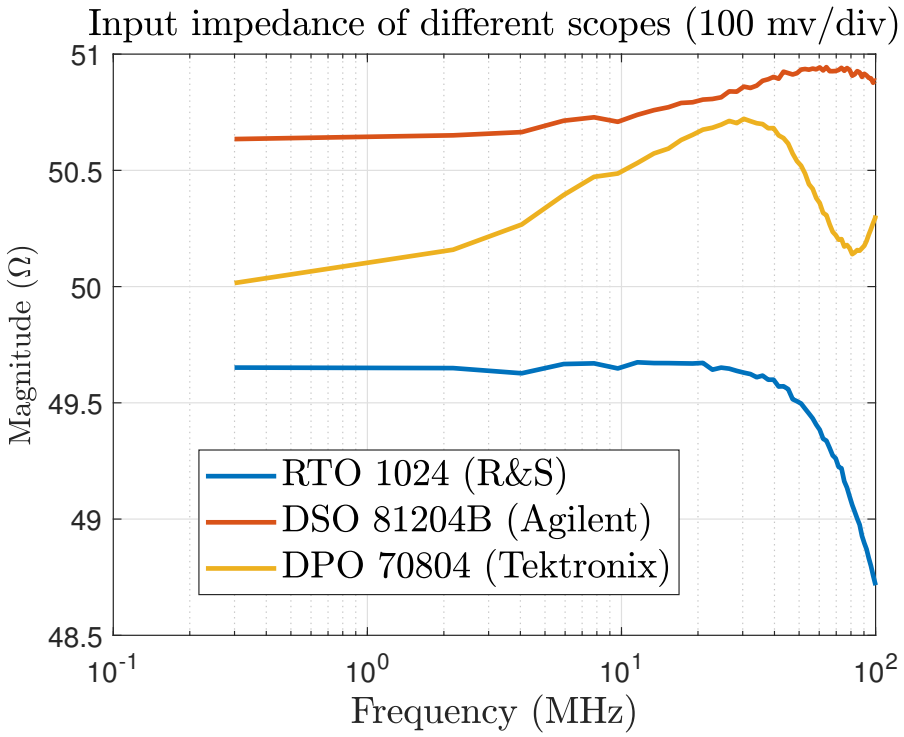


Figure 8. Port impedance versus frequency for different oscilloscopes.

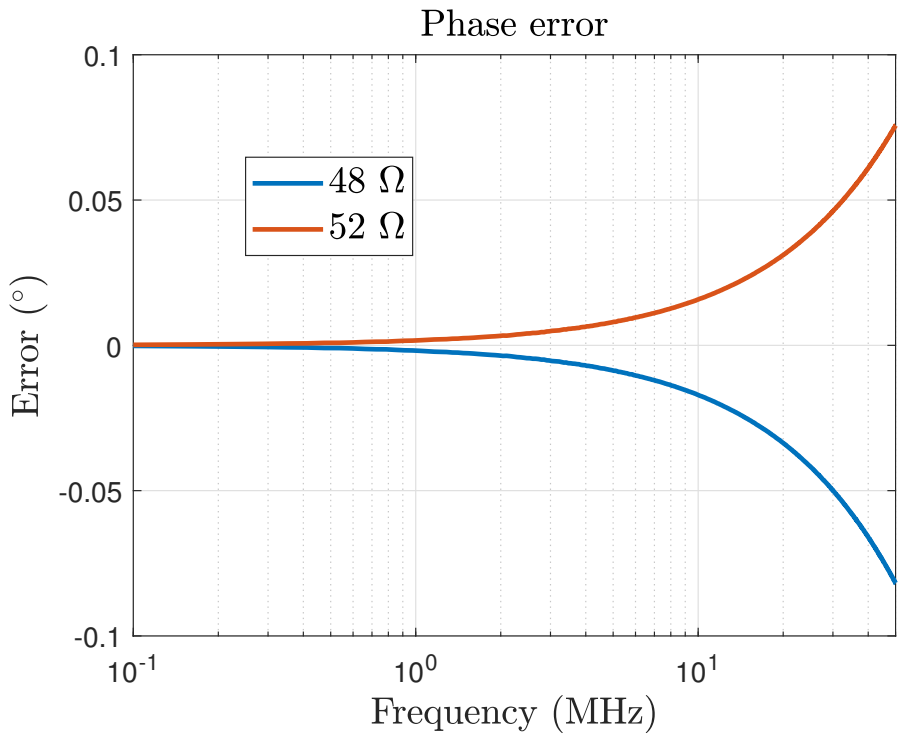


Figure 9. Phase error induced with different load impedances.

4. EXPERIMENTAL VALIDATION

The main source of error in the proposed method is the consistency of Z_{iv} when the resistor is connected to different instruments. To further validate the reproducibility of the proposed resistor characterization method, a current probe is used as a reference as its transfer impedance Z_{ct} can also be characterized by a VNA. It should be emphasized that the comparison is performed under a low-current excitation, and the current probe can be treated as a linear component .

The small-signal transfer impedance Z_{ct} of a current probe is well defined and can be characterized according to [19].

$$Z_{ct} = 50 \cdot S_{21}. \tag{8}$$

4.1. MEASUREMENT VALIDATION WITH A CURRENT PROBE

4.1.1. Configuration of the Measurement Setup. The experimental configuration is depicted in Figure 10. It consists of a high power source, i.e., a signal generator (Agilent N5181A) and a power amplifier (Amplifier research 100W1000). The power source is terminated by the resistor prototype, and the output port of the prototype is connected to an oscilloscope (R&S RTO1024, 10 GS/s with a 2 GHz bandwidth). A current probe (Tektronix CT-2 with a P6041 probe cable) is inserted between the power source and the resistor for comparison. The input current is set to approximately 0.25 A (peak value). According to the datasheet, the current probe can measure continuous current up to 4A (peak value) without saturation [20].

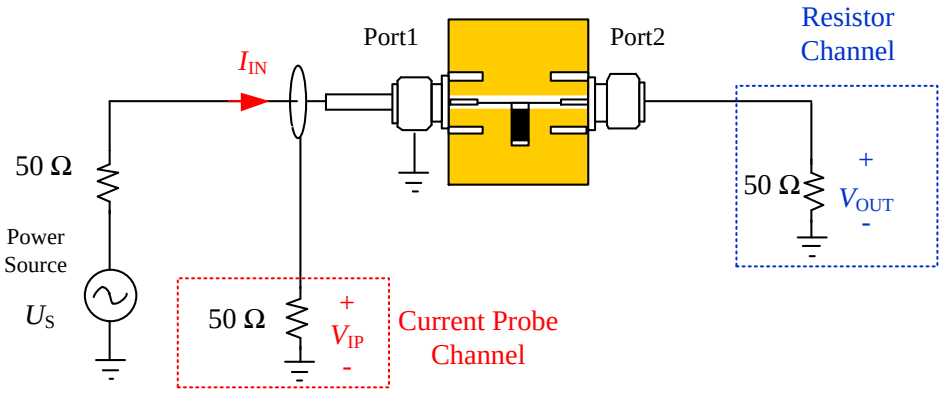


Figure 10. Measurement setup of the validation.

V_{IP} and V_{OUT} are the outputs of the current probe and the two-port resistor, respectively. To compare the characterization results measured by the VNA and scope, current ratio R_{Scope} is defined, which can be expressed as follows:

$$R_{Scope} = \frac{V_{IP}(\omega)}{V_{OUT}(\omega)} = \frac{I_{IN} Z_{ctScope}}{I_{IN} Z_{ivScope}} = \frac{Z_{ctScope}}{Z_{ivScope}}. \tag{9}$$

We note that the time-domain waveforms are transformed into the frequency domain by the FFT. The ratio describes the difference between the current-to-voltage impedances of the current probe and the two-port resistor. A ratio R_{VNA} can be calculated according to (7) and (8), which can be measured by a VNA.

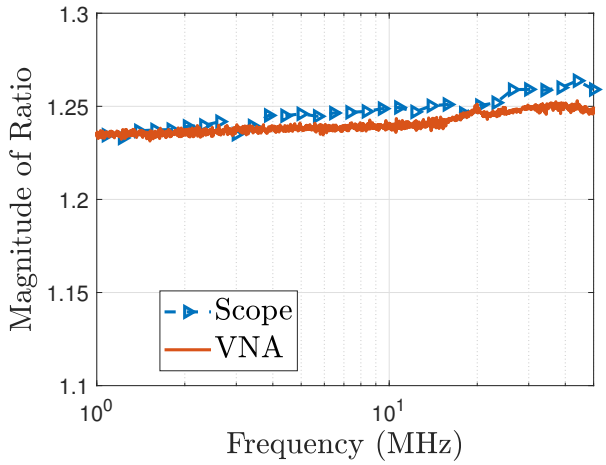
$$R_{VNA} = \frac{Z_{ct}}{Z_{iv}}. \tag{10}$$

4.1.2. Results Comparison. Figure 11 compares the ratios measured by an oscilloscope and a VNA. The discrepancy in magnitude is 1.5% at most (up to 50 MHz). Additionally, the phase shift differences are smaller than 0.3° among the frequencies of interest. In particular, the error is limited to 0.1° below 16 MHz. Assuming that the quality factor of the core under study is 100, the measurement error due to the phase shift is approximately 15% [5]. We note that resonance compensation is not required in the proposed method, so it can be expanded for applications with nonsinusoidal excitation. However, it's suggested that the resonance method should be applied for cores with quality factors greater than 100.

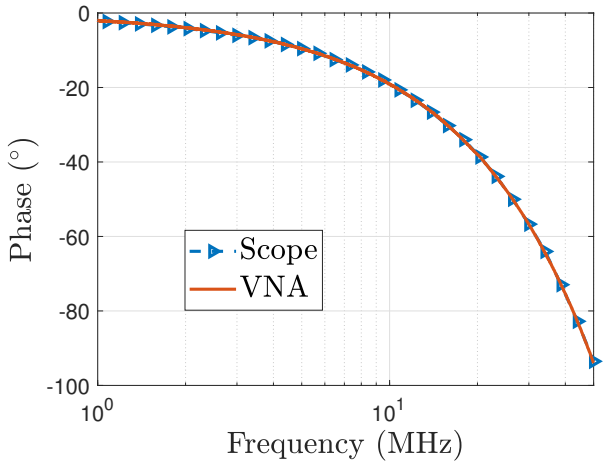
In addition, the strong agreement between the results measured by the oscilloscope and the VNA not only prove our resistor characterization method but also indicate that resistor characterization can be performed on a less expensive instrument (i.e. an oscilloscope instead of a VNA) if a reference current probe is available. Nevertheless, the VNA-based method is still preferred because it provides a better signal-to-noise ratio and requires much less testing time.

4.2. EXPERIMENTAL VALIDATION WITH MAGNETIC CORES

To further validate the proposed two-port resistor and compensation method, the core loss of the commercial high-frequency and high-power magnetic material 61 (NiZn) from Fair-Rite is tested. The outer diameter, inner diameter and height of the core are 35.5



(a)



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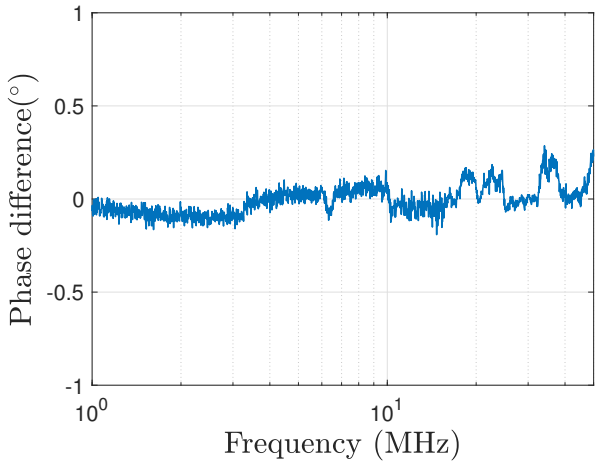


(c)

Figure 11. Comparison of the measured R_{Scope} and R_{VNA}; (a) Magnitude; (b) Phase; (c) Phase difference.

mm, 23 mm and 12.7 mm, respectively. Figure 12 shows the core under test and the 8-turn bifilar winding it carries. The ferrite loss measurement setup is demonstrated in Figure 6. In addition, the ferrite core is immersed in an oil bath, and its temperature is kept reasonably at an ambient level. The voltage induced across the secondary winding is measured by a differential probe (Tektronix P6251 and Tekprobe power supply 1103). We note that the phase shift of the probe is characterized by a VNA. The configuration of the measurement setup is depicted in Figure 13.

Figure 12. Toroid samples with bifilar windings.

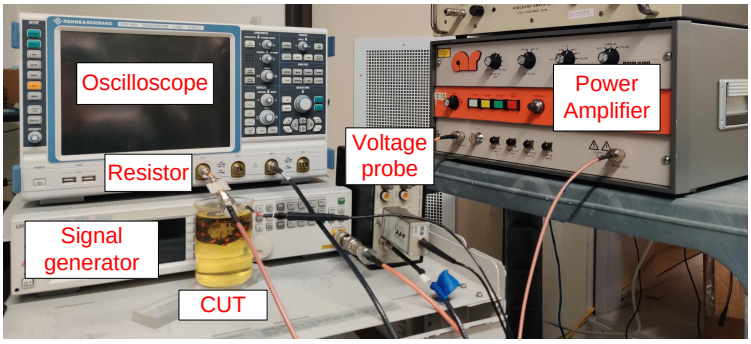


Figure 13. Measurement setup for the ferrite core.

The core loss is measured under sinusoidal excitation with a 2 MHz frequency, and the results are compared with those measured by the CT-2 current probe and datasheet. The comparisons are demonstrated in Figure 14. This shows that the results measured by the current probe and the proposed two-port resistor are well matched, as expected (with

an error $\Delta < 10\%$). In this paper, we focus on eliminating the phase discrepancies among probes. The measurement errors introduced by the temperature, mutual-winding loss and parasitic capacitances are not within the scope of our study.

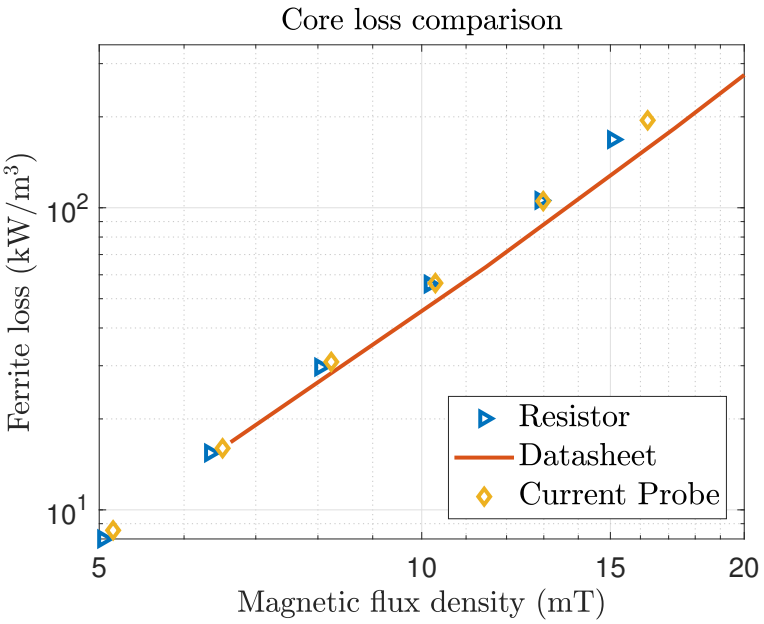


Figure 14. Toroid samples with bifilar windings.

5. TWO-PORT RESISTOR WITH A COAXIAL RESISTOR ARRAY

The phase shift induced by a current probe or two-port resistor has been discussed and validated by the measurements in Section 4.1. Nevertheless, either an expensive VNA or a current probe with known phase shifts is still required. A two-port resistor with a quasi-zero phase shift is desired to eliminate the process of resistor characterization. An effective approach for increasing bandwidth is to place several resistors in parallel and connect the sensing wire in the center region where the flux density is weakest [21].

5.1. DESIGN AND IMPLEMENTATION OF A TWO-PORT RESISTOR WITH A CIRCULAR RESISTOR ARRAY

The placement of a circular resistor can almost cancel the mutual flux coupling. A diagram of the two-port coaxial resistor is demonstrated in Figure 15.

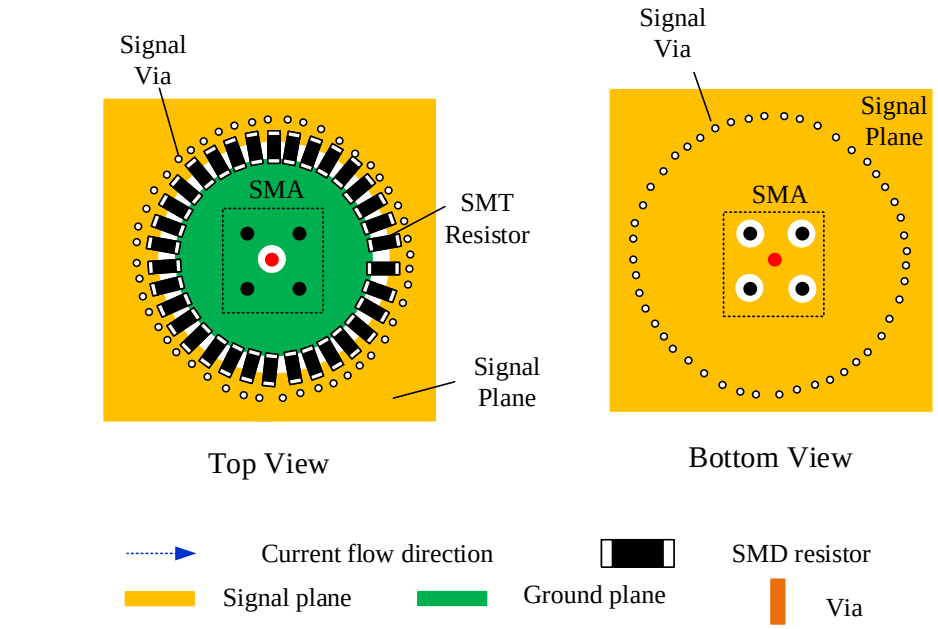
5.1.1. Structure of the Two-Port Resistor with a Circular Array. Small surface-mounted resistors are soldered on the top layer of the PCB board. The current flows from the inner conductor of the SMA connector on the top side through the bottom plane of the printed circuit board. The SMA connector at the bottom is pin-to-pin connected to the connector at the top side, and the voltage generated across the resistor array can be directly measured at the port. Due to the 50 Ω load of the second port, the majority of the current returns back to the connector shell through vias, resistors and the copper plane on the top layer. It is worth noting that the height difference H_D between the two planes is the most critical parameter for reducing the loop size, i.e., the parasitic inductance of the series. The top two layers of a 4-layer PCB are used, as H_D can be configured to 0.1 mm in practical PCB fabrication scenarios.

5.2. SIMULATION AND MEASUREMENT VALIDATION OF THE RESISTOR

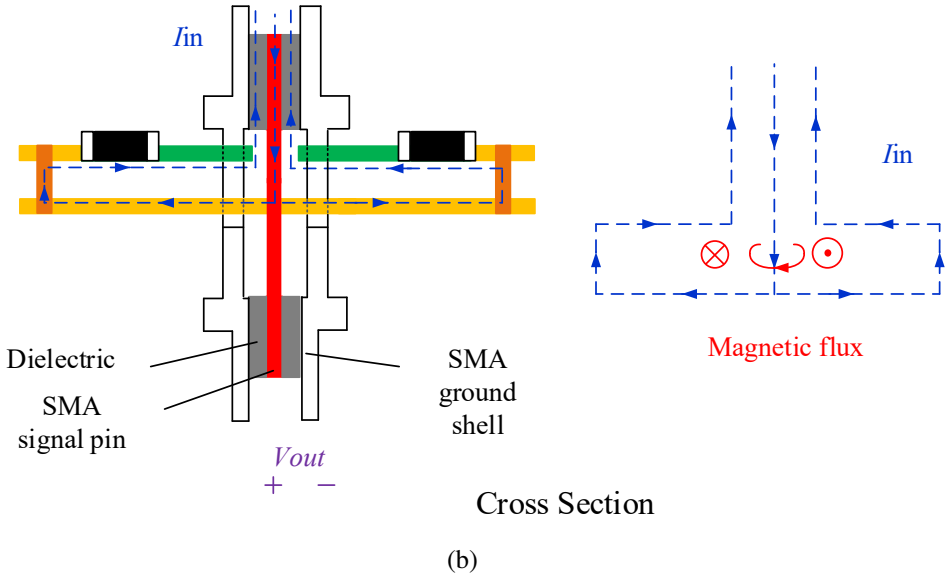
To validate the proposed structure, a prototype is illustrated in Figure 16. It is built with 20 parallel surface-mounted resistors (resistance: 22Ω, package: 0805), and two surface-mounted and soldered SMA connectors are used (model: Molex 0732511350). The dimensions of the prototype are presented in Table 1.

Table 1. Physical dimensions of the improved two-port resistor.

Symbol	Description	Value
D_{Via}	Diameter of shorting via	0.2 mm
R_{Via}	Radius of circular pattern of via	7.4 mm
R_{Re}	Radius of circular pattern of SMT resistor	6.1 mm
H_{C1}	Thickness of top-layer copper foil	1 oz
H_{C2}	Thickness of bottom-layer copper foil	0.5 oz
H_D	Thickness of dielectric between copper layers	0.1 mm



(a) Top and bottom views of the proposed structure; only a quarter of the resistor is illustrated.



(b)

Figure 15. (a) Top and bottom views of the proposed resistor; (b) Cross section of the proposed resistor and its current flow direction.

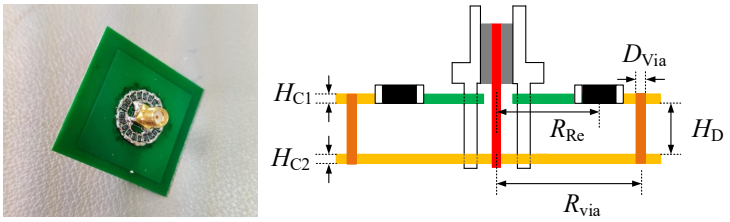


Figure 16. Photograph of the two-port resistor and its labeled dimensions.

In addition to measurement, a simulation model is also implemented in a full-wave electromagnetic field simulator (Ansys HFSS), which is demonstrated in Figure 17. In the simulation, the current is injected through lumped ports across the inner conductor and the outer shell of the SMA connector. Resistors are represented by lumped elements with 1.5 nH of series inductance, as measured by a VNA with the two-port series method [22].

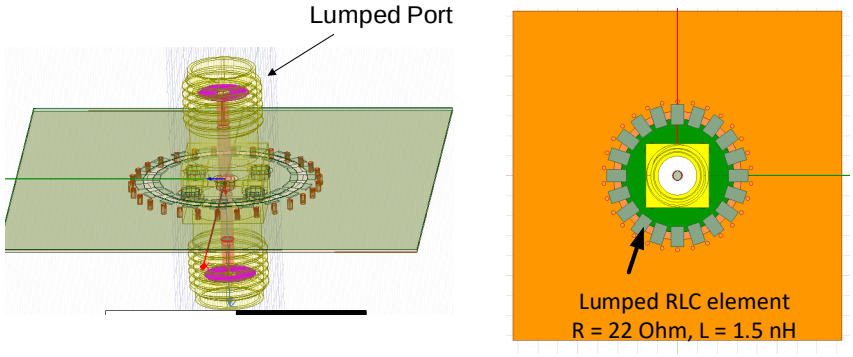


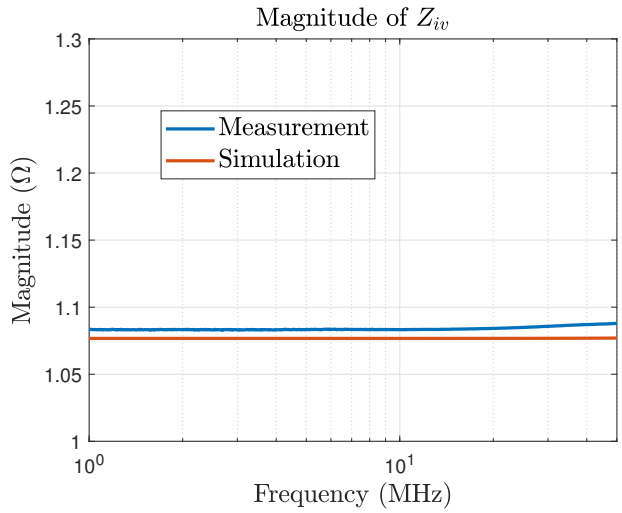
Figure 17. Full wave simulation model and its settings.

As shown in Figure 18, the simulated and measured magnitudes agree well with an approximately 1% difference. Furthermore, the phase shifts also have a strong correlation, where the maximum discrepancy is less than 0.1° below 50 MHz. Additionally, the phase shift of the coaxial prototype is within 0.1° below 16 MHz; this can be treated as an ideal resistor below the frequency range.

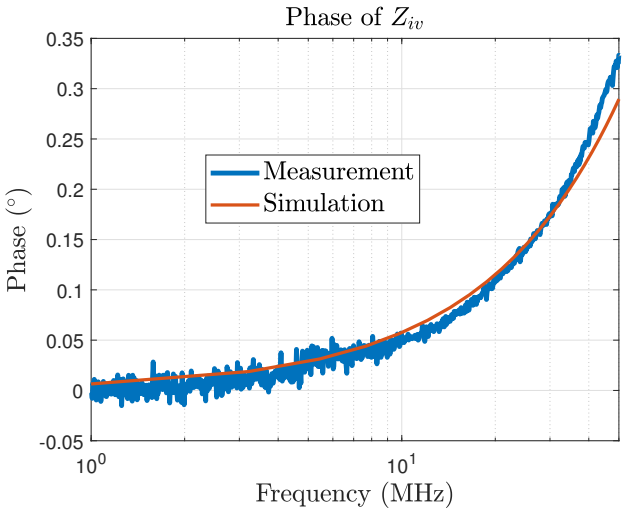
5.3. INFLUENCE OF THE H_D

As we have explained, the most critical parameter in the resistor design is the height difference between the top and bottom planes. The simulation model of the proposed resistor is verified by the above measurement process and can be used to investigate the influence of H_D. The value of H_D is swept in the simulation, and the parasitic inductances extracted at 10 MHz according to (1) are demonstrated in Table 2. It is worth noting that

the inductance of our prototype is ~ 40 pH according to (1), which is 4 times smaller than that of an existing design [13]. H_D is configured as approximately 1 mm, which results in parasitic inductance.



(a)



(b)

Figure 18. Comparison of the simulated and measured transfer impedance prototypes.

Table 2. Extracted parasitic inductance versus H_D.

H_D (mm)	Inductance (pH)
0.1	38
0.3	84
0.5	121

6. CONCLUSION

This paper rigorously illustrates the loading effects of the 50 Ohm detector on the well-known two-port impedance extraction method. The corresponding error is analyzed as well. Furthermore, a revised method is demonstrated to correctly calculate the current-to-voltage impedance of a two-port resistor. The proposed method is experimentally verified up to 50 MHz and can be applied for core loss measurement applications.

The design of an improved current shunt with a coaxial resistor array is exemplified. The parasitic inductance of the prototype presented in the paper is 3 times smaller than that of the state-of-art design. As a benchmark, a 3D simulation model is developed to verify the measurement results. In addition, the main limiting factor in existing current shunt designs is shown through simulation.

However, considerable efforts are required to extend the proposed method to higher frequencies due to the nonideal characteristics of oscilloscopes, e.g., ADC interleaving, impedance mismatches, and front-to-end traits.

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SECTION

2. SUMMARY AND CONCLUSIONS

With the rapid development of power converters, there are serious design challenges in the electronic systems. The characterization and modeling techniques developed in the dissertation are powerful tools for engineers in real applications. In the first paper, a novel topology-based equivalent model is developed to reveal the complex physics behind a feedback controller. The proposed time-domain modeling method is integrated the traditional frequency-domain averaging concept, unique advantages are provided thereby. First, the model is naturally suitable for transient simulation, and the simulation speed is significantly faster than then traditional SPICE model. Second, the framework of the model is applicable to controllers with non-constant operation frequency, which is not achievable in the conventional modeling method. In addition to the modeling method itself, the model can be used to extract the equivalent parameters of a controller, when vendor's model is not applicable in the early design stage. In the second paper, two sets of test fixtures are designed to evaluate the parasitic capacitances of MOSFETs. The fixtures can extend the operation frequency to at least 30 MHz. It is worth noting, the state-of-art modeling method for MOSFETs is invalidated by the designed fixture, as the frequency-dependent behaviors are captured.

In the third and forth papers, two different probe characterization-based core loss measurement methods are developed. By introducing the characterization concept, the tedious reactance tuning procedure in conventional practices are not required. Accurate core loss characterization is experimentally verified up to 10 MHz, and can be extended to higher frequencies. In addition, the limits in phase measurement of state-of-art instruments are discussed in the paper.

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VITA

Anfeng Huang was born in Guilin, Guangxi, China. He received a Bachelor of Science and a Master of Science in Electrical Engineering from the Xidian University, Xi'an, China in July 2014 and July 2017, respectively. He then joined the EMC Laboratory in the Missouri University of Science and Technology, Rolla, MO, USA. He received a Doctor of Philosophy in Electrical Engineering from the Missouri University of Science and Technology in May 2022.

His research interests included the modeling of power distribution network and EMI in power eletronics, magnetic integrity, and electromagnetic interference. He was the recipient of the IEEE James C. Klouda Memorial Scholarship in 2021.