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Analysis and modeling of power supply induced jitter for high speed driver and low dropout voltage regulator

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ANALYSIS AND MODELING OF POWER SUPPLY INDUCED JITTER FOR HIGH SPEED DRIVER AND LOW DROPOUT VOLTAGE REGULATOR

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ABSTRACT

With the scaling of power supply voltage levels and improving trans-conductance of drivers, the sensitivity of drivers to power supply induced delays has increased. The power supply induced jitter (PSIJ) has become one of the major concerns for high-speed system. In this work, the PSIJ analysis and modeling method are proposed for high speed drivers and the system with on-die low dropout (LDO) voltage regulator. In addition, a jitter-aware target impedance concept is proposed for power distribution network (PDN) design to correlate the PSIJ with PDN parasitic.

The proposed PSIJ analysis model is based on the driver power supply rejection ratio (PSRR) response, transition edge slope and the propagation delay. It is demonstrated that the proposed model can be generalized for different type of drivers. Following the proposed PSIJ model, a method for improving the PSIJ simulation accuracy in the input/output buffer information (IBIS) model is also proposed. A PSIJ analysis method is also proposed for system with on-die LDO. The approach relies on separate analysis of the LDO block PSRR response and the buffer block PSIJ sensitivity. This procedure allows designer to evaluate the system PSIJ with fewer and faster simulations.

For the jitter-aware target impedance, a systematic procedure to develop the target impedance curves is formulated and developed for common CMOS buffer circuits. Given the transient IC switching current and the jitter specification, multiple target impedance curves can be defined for a specific circuit. The proposed design procedure can largely relieve over-constrain in the PDN designed based on the original target impedance definition.

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1. INTRODUCTION

1.1. MOTIVATION

The timing budget for today's I/O interfaces become tighter as the transition speed of I/O keeps on increasing. Along with the continuously decreasing of unit interval, the requirements for allowable jitter also become more restrict and the jitter prediction becomes more important. In addition, with the scaling of power supply voltage levels and improving trans-conductance of drivers, the sensitivity of drivers to power supply induced delays has increased [1]. The power supply induced jitter (PSIJ) has become one of the major concerns for high-speed system [2-9].

1.1.1. PSIJ Sensitivity Analysis. The on-die circuits' power voltage is supplied by the power distribution network (PDN), which connects the off-chip power supply with the on-die power and ground terminals. A typical PDN equivalent circuit is shown in Figure 1.1. For a practical PDN, the parasitic inductance and resistance will always exhibit. When currents are consumed at the on-die power net due to the on-die circuit switching, as a result of the non-ideal PDN, the on-die power rail voltage will generate fluctuation. The supply voltage fluctuation can cause significant delay change in the transmitters and receivers, as illustrated in Figure 1.2. For PSIJ characterization, the PSIJ sensitivity can be extracted from transistor level simulation [5]. The obtained PSIJ sensitivity spectrum can be applied to calculate the total PSIJ if the power supply noise spectrum is known.

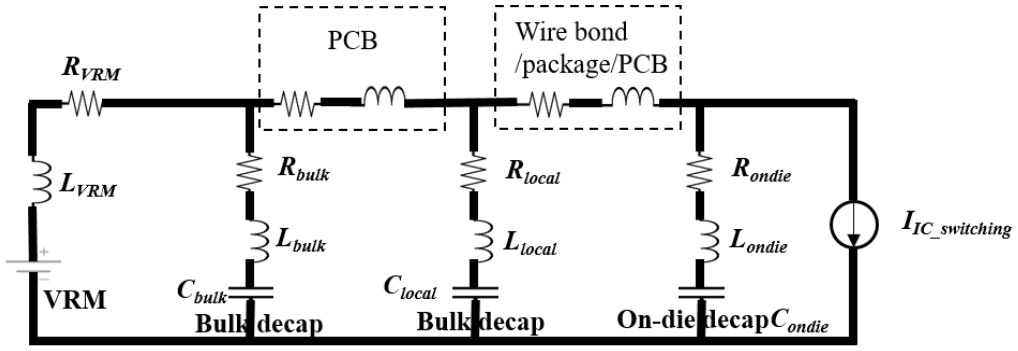


Figure 1.1 A Typical PDN Equivalent Circuit.

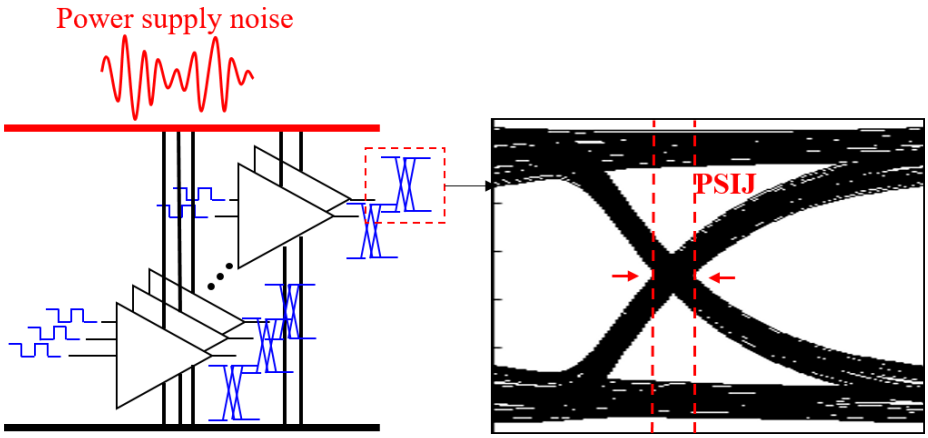


Figure 1.2 PSIJ as a Result of Power Supply Noise.

The PSIJ sensitivity for inverter type of buffers has been widely studied [2,5-8] , as these buffers are frequently inserted in clock and timing circuits and the corresponding delays account for a large percentage of critical timing nets in the design [6]. The other type of drivers are also implemented in many designs [9] and the PSIJ sensitivity for these drivers are also important. For the PSIJ sensitivity derivation, some treat the inverter type of buffers as voltage controlled delay line (VCDL) [6, 8] and the PSIJ

sensitivity can be easily derived with the form of a sinc function. A numerical method is proposed to estimate PSIJ for a current mode differential driver using a root-finding approach by classical Newton's method [10]. Some works have provided analytical method based on the piecewise transistor linear model using transient analysis [2, 7]. The jitter is estimated as the ratio of the output voltage ripple versus the switching edge slope.

In this research, a generalized PSIJ sensitivity model based on power supply rejection ratio (PSRR) response is proposed. The output voltage ripple to the power rail voltage ripple relationship could be easily established through the PSRR response in the frequency domain, allowing easier derivation while maintaining some physical insights.

1.1.2. Driver PSIJ with On-Die Low-Dropout Voltage Regulator. On-board voltage regulator (VRM) is usually applied to generate different necessary power voltage levels for different technology ICs. In addition, a power management IC is often used to efficiently manage power consumption. However, the on-board VRM tends to occupy a large space on board and the physical distance to the on-die circuit is large, resulting high parasitic inductance and resistance. To solve this issue, an on-die low-dropout (LDO) voltage regulator is often applied in common practice to suppress noise coupling from off-chip to on-chip. In addition, the application of on-die LDO helps to reduce the physical distance to the current-consuming IC, thus reducing PDN parasitic [11-13]. This is helpful for reducing the generated on-die power voltage fluctuation. Even with the on-die LDO, the PSIJ performance analysis could still be important due to the continuously tightened timing margin.

Usually, a transient simulation of the entire system will be performed to analyze the PSIJ performance [14]. In this research, a methodology for PSIJ analysis of high

speed output buffer with on-die LDO is proposed. The approach depends on the stand-alone analysis of the LDO block and the buffer block. Assuming the power noise is small, the LDO power supply rejection ratio (PSRR) response and the PSIJ sensitivity can be treated as linear functions. Then the PSIJ sensitivity of the entire system can be obtained by multiplying the LDO PSRR with driver PSIJ sensitivity.

1.1.3. PSIJ Simulation in Behavior Model. Predicting the jitter induced by power noise fluctuations is important for signal and power integrity analysis [2-4]. In many cases, it is difficult to obtain Simulation Program with Integrated Circuit Emphasis (SPICE) model from semiconductor vendor for simulation investigation. Alternatively, the input/output buffer specification (IBIS) model has been widely applied in various signal and power integrity analysis with the purpose to protect the intellectual property. The power-aware IBIS model has been developed to include the non-ideal power/ground effect [15]. The capability to simulate the simultaneous switching noise (SSN) is improved. On the other hand, it is desired to incorporate a better capability to analyze the power supply induced jitter (PSIJ) in IBIS model.

In the power-aware IBIS model, additional data tables to describe the model buffer power characteristics are introduced. Besides sets of I-V (current-voltage) tables represent the I_{ds} (drain-source current) versus V_{ds} (drain-source voltage) characteristic of the pull-down and pull-up transistors, I-V tables describe the I_{ds} versus V_{gs} (gate-source voltage) characteristic of the transistors are also included. In addition, the pre-driver current consumption on the power rail node is added through I-t (current-time) tables for better simultaneous switching noise (SSN) simulation. With these additional tabulated data, the switching coefficient K_u and K_d are modified only as a function of the power rail

voltage. An IBIS-like behavior modeling method for PSIJ is also proposed [16]. This method requires another sets of C-V (capacitance-voltage) tables.

In this research, the switching coefficient K_u and K_d are modified as a function of both time and power rail voltage. No additional tabulated data is required. Moreover, the time averaged effect of power rail voltage to the buffer output switching edge is considered. This is an essential factor for improving the PSIJ simulation accuracy.

1.1.4. PDN Design with PSIJ Consideration. Since the power noise could lead to reduced noise margin, large voltage variations, jitter and other signal integrity issues that could lead to system design failure, to tackle this issue, traditionally, the maximum allowable voltage ripple on the power rail is specified and the target impedance is defined to limit the level of supply voltage fluctuation. Usually, the target impedance concept is defined from frequency domain directly. The value of target impedance curve magnitude is defined by the allowable voltage perturbation divided by the amount of IC current and then extended to the entire frequency range of interest. Then the PDN design objective is to achieve a PDN impedance magnitude lower than the target impedance value. For a practical PDN design, the impedance is hardly a flat line but will be frequency dependent [17]. The applied decoupling capacitors serve to lower the impedance targeting different frequency ranges. On the other hand, various type of parasitic inductance will bring the PDN impedance up with the increase of frequency. An improved concept of target impedance is proposed in [17], [18] to link the time domain maximum allowable voltage ripple with PDN impedance, given the known transient IC current. This concept helps to relieve over-constrain at higher frequency range in the PDN design.

In this research, an improved target impedance concept with jitter specification is proposed to provide a PDN design guideline that can link to the PSIJ directly. Establishing target impedance with jitter specification is the reverse problem of the PSIJ analysis. Given the IC switching current and a known PDN design, the PSIJ can be analytically derived. Reciprocally, the guidelines (target impedance) for PDN design can be alternatively developed from the given IC switching current and the jitter specification

1.2. ORGANIZATION

This dissertation is organized as follows. In Section 2, the analysis and modeling of PSIJ sensitivity of transmitters will be discussed. A generalized PSIJ sensitivity model based on PSRR response is proposed. The obtained PSIJ sensitivity expressions are validated through the comparison with transistor level circuit simulation for both the magnitude and phase. A methodology for PSIJ analysis of high speed output buffer with on-die LDO is also proposed. The proposed analysis method is validated through HSPICE simulation of the entire system. A new behavior model is proposed to improve PSIJ simulation accuracy for IBIS model. An algorithm to implement the proposed IBIS model as a spice sub-circuit netlist is developed. The improved accuracy for PSIJ simulation is validated through transistor level HSPICE simulation. In Section 3, the improved target impedance concept with jitter specification is proposed. The PSIJ relationship with PDN R-L-C parameters for inverter type of drivers is derived from the time domain voltage ripple to PDN R-L-C parameters relationship and time domain voltage ripple to jitter transfer relationship. The correlation between PSIJ and PDN R-L-C parameters and the application of the proposed target impedance concept is validated

through HSPICE simulation and measurement. An in-house designed IC is taped out for the measurement validation. A method to characterize the driver PSIJ sensitivity from off-chip environment is also proposed and validated. In Section 4, the contents of the previous sections are summarized. In addition, the main contributions of this research are specified and the future work directions are identified.

2. ANALYSIS AND MODELING OF PSIJ SENSITIVITY OF TRANSMITTERS

2.1. A GENERALIZED PSIJ MODEL BASED ON PSRR RESPONSE

The PSRR based PSIJ analysis model will be discussed and validated.

2.1.1. PSRR Based PSIJ Sensitivity Model. Conceptually, the PSIJ sensitivity can be written as the ratio of the output time interval error (TIE) Δt to the voltage ripple level on the power rail ΔV_{dd}, when a single frequency sinusoidal noise exhibits on the power rail. This ratio can be reformed into the ratio of PSRR to switching edge slope [19] as expressed in:

$$\frac{\Delta t}{\Delta V_{dd}} = \frac{\Delta V_o / \Delta V_{dd}}{\Delta V_o / \Delta t} = \frac{PSRR}{Slope} \tag{1}$$

where ΔV_o is the variation of output voltage. This concept can also be derived from the decomposed multiple output voltage transition edges as illustrated in Figure 2.1. The two low to high transition edges are the minimum and maximum propagation delay cases corresponding to the maximum and minimum of a sinusoidal power voltage fluctuation. At half of nominal power rail voltage V_{dd0}, the timing difference between the two edges is jitter Δt. The multiple output transition edges can be decomposed into a large signal portion, where the transition happens with power rail voltage V_{dd0}, and a small signal portion, which is introduced by the power rail voltage fluctuation [2, 3]. At half V_{dd0}, the slope can be determined from the large signal portion and the variation of output voltage ΔV_o can be extracted from the small signal portion. The jitter can then be estimated as $\Delta t = \Delta V_o / \text{Slope}$.

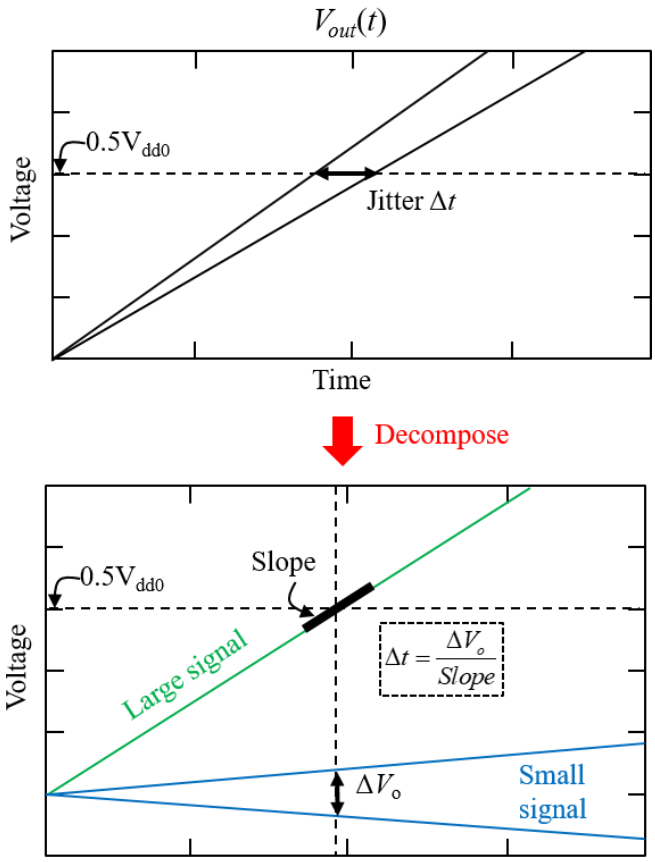
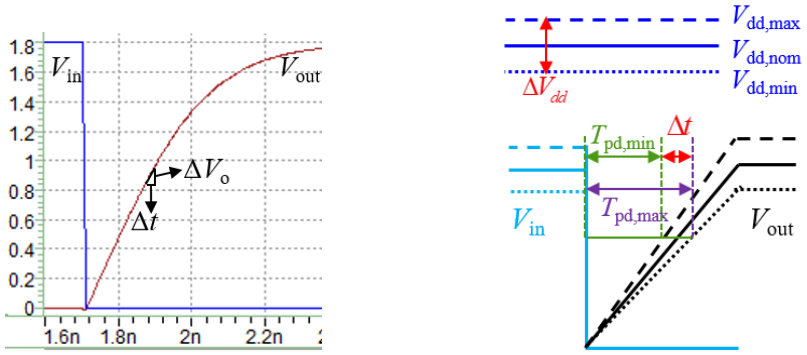


Figure 2.1 Jitter Derivation from Decomposed Multiple Output Voltage Transition Edges.

The frequency domain PSRR response *PSRR*(ω) can be separated into a DC portion $PSRR_{DC}$ and the normalized frequency dependency portion *PSRR*'(ω) as:

$$\frac{PSRR(\omega)}{Slope} = \frac{PSRR_{DC} \cdot PSRR'(\omega)}{Slope} = \frac{\Delta V_o / \Delta V_{dd}\big|_{DC}}{\Delta V_o / \Delta t\big|_{DC}} PSRR'(\omega) = \left.\frac{\Delta t}{\Delta V_{dd}}\right|_{DC} PSRR'(\omega) \quad (2)$$

where ω is the angular frequency. Since the jitter is evaluated at half V_{dd0}, it is a common practice to extract the slope of the transition edge near this voltage level [20], as illustrated in Figure 2.2(a).



a b

Figure 2.2 Rising Edge Slope Estimation. a) Direct Estimation. b) From DC Delay Change Test.

By taking a small variation of output voltage and recording the corresponding timing difference, the slope of the rising edge can be calculated. However, in practice, the rising edge is not a perfect straight line and the output edge slope during propagation delay time range will not be a constant. Applying the slope value read from output edge near half V_{dd0} can lead to inaccurate PSIJ sensitivity results, as the slope effect during the entire propagation delay time range is neglected. In order to obtain a slope value that can give a better result for PSIJ sensitivity estimation, the slope is extracted from the driver delay change test under different power rail voltage level at DC, as depicted in Figure 2.2(b). With maximum power rail voltage level $V_{dd,max}$, the corresponding propagation delay of the driver will be the smallest $T_{pd,min}$. With minimum power voltage $V_{dd,min}$, the propagation delay is $T_{pd,max}$. The ratio of the variation in power voltage ΔV_{dd} to the corresponding variation of propagation delay Δt is related to slope as:

$$\frac{PSRR_{DC}}{Slope} = \frac{\Delta V_{dd}}{\Delta t}\bigg|_{DC} = \frac{V_{dd.\max} - V_{dd.\min}}{T_{pd,\max} - T_{pd,\min}} \tag{3}$$

which is the inverse of the DC jitter sensitivity $(T_{pd,max}- T_{pd,min})/(V_{dd,max}- V_{dd,min})$.

As previously mentioned, the noise presented on the power rail will influence the output switching edge during the entire time range of the driver propagation delay T_{p0}, as illustrated in Figure 2.3. If the period of the sinusoidal noise on the power rail is the same as the propagation delay of the driver, regardless of the actual value of the power rail noise at the time when output voltage is half V_{dd0}, the output switching edge delay time will not change. This is because the time averaged effect of the noise at this specific frequency is zero during the time range of the propagation delay. For the PSIJ sensitivity derivation, this effect should be taken into consideration.

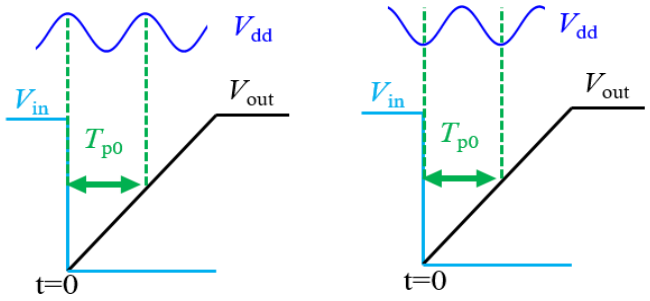


Figure 2.3 Power Noise Time Averaged Effect during Propagation Delay.

Based on the above discussion, the PSIJ sensitivity formulation can be derived. Substitute (3) into (2) and take the time harmonic form of $PSRR(\omega)$ for the time averaged effect consideration, the PSIJ sensitivity is expressed as:

$$\begin{aligned} PSIJsensitivity(f) &= \int_0^{T_{p0}} \frac{PSRR(\omega)\cdot e^{j\omega t}}{Slope\cdot T_{p0}} dt \\ &= \frac{PSRR_{DC}}{Slope} PSRR'(2\pi f) e^{j\pi f T_{p0}} \sin c(\pi f T_{p0}) \end{aligned} \tag{4}$$

where *f* is the frequency. From (4), it can be observed that the PSIJ sensitivity is related to the DC jitter sensitivity and the frequency dependency originates from the normalized PSRR response and the time averaged effect induced sinc function portion.

In this work, the proposed model will be applied for the PSIJ analysis for the three different drivers as shown in Figure 2.4. For different type of drivers, the PSIJ sensitivity frequency dependency are expected to be different. Since the driver PSIJ sensitivity frequency behavior is related to the PSRR response and the propagation delay, the different PSIJ sensitivity frequency behavior can be understood by the analysis of PSRR response and equivalent RC delay of the circuit, as illustrated in Figure 2.5.

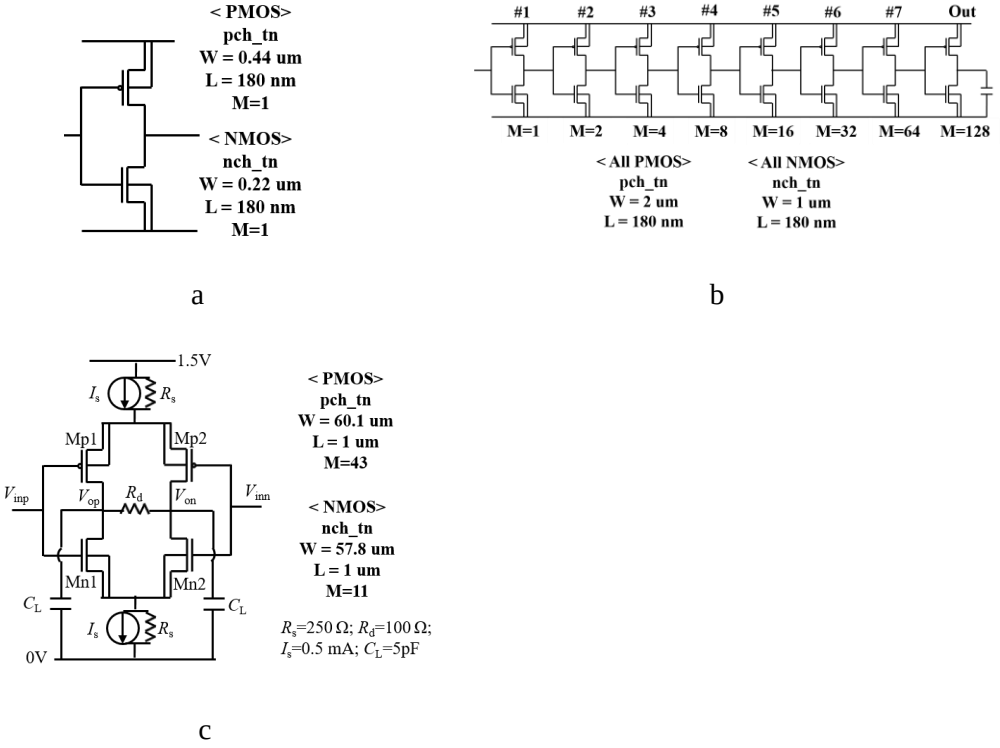
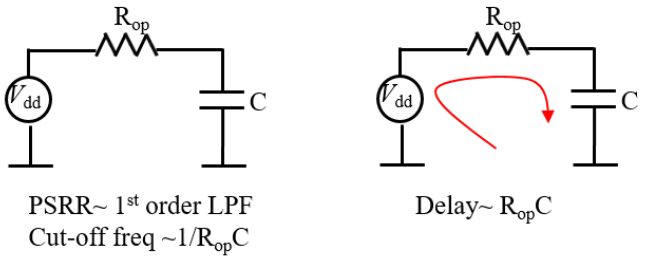


Figure 2.4 Tested Drivers. a) Inverter. b) Inverter Chain. c) Current Mode Differential Driver.



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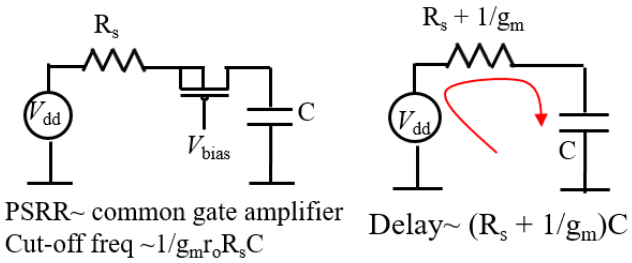


b

Figure 2.5 Comparison of Frequency Dependency Due to PSRR and Propagation Delay. a) Inverter. b) Differential Driver.

The analysis for single stage inverter is shown in Figure 2.5(a). The PMOS can be regarded as a resistor when looking at the rising edge case. The PSRR analysis is close to the analysis for a first order low pass filter, with a cutoff frequency around $1/R_{op}C$, where R_{op} is the turn on resistance of PMOS. For the output delay of the inverter, it can be roughly estimated as $R_{op}C$ and the corresponding frequency is the null frequency for the sinc function portion. In this case, the propagation delay related frequency roll-off is faster than the PSRR related frequency roll-off. As a result, the PSIJ sensitivity frequency dependency is dominated by the propagation delay related time averaged effect. For inverter chain, as the propagation delay is a linear accumulation of delay of each stage

[7], the null frequency for the sinc function portion will be even smaller than the cutoff frequency of the PSRR response.

The analysis for current mode differential driver is shown in Figure 2.5(b). For the designed driver, the transistors will have some amplification effects. For the simplest estimation, the PSRR analysis can be regarded as the analysis for a common gate amplifier. The cutoff frequency can be estimated as $1/g_m r_o R_s C$ [21], where g_m is the PMOS trans-conductance, r_o is the PMOS output resistance and R_s is the current source resistance. On the other hand, for the delay estimation, the transistor can be regarded as a resistor with value of $1/g_m$. So the propagation delay is roughly estimated as $(R_s+1/g_m)C$. In general, $g_m r_o R_s C$ is larger than $(R_s+1/g_m)C$ [21]. In consequence, the PSRR response will have smaller cutoff frequency and the PSRR frequency dependency will roll off faster than the propagation delay related sinc function frequency dependency.

2.1.2. Validation on Different Drivers. The proposed method is validated on different type of drivers.

2.1.2.1. Inverter. The proposed PSRR based PSIJ sensitivity model is firstly applied for a single stage inverter. The design parameters for the single stage inverter is shown in Figure 2.4 (a). To obtain the PSRR response of the inverter, the circuit needs to be set to a proper DC status. For a single stage inverter, the power rail noise voltage will mainly influence the low to high transition. If the input switching edge transition time is assumed to be negligible, when the output transits from low to high, the input will always be low. For the PSRR simulation, the input will be set to zero as plotted in Figure 2.6. The nominal power rail voltage for this inverter is 1.8V and a sinusoidal source with 50mV amplitude is served as the noise source. The load capacitance for the test is set to

20fF. By conducting AC simulation and obtain the ratio of the output voltage to the amplitude of sinusoidal noise, the PSRR response for the output rising edge case is obtained.

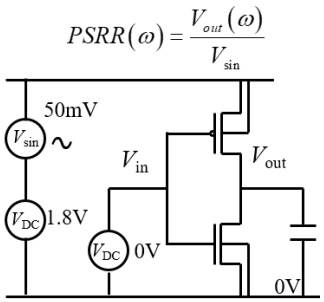


Figure 2.6 PSRR Simulation Test for Single Stage Inverter.

The simulated PSRR magnitude and phase for the inverter is shown in Figure 2.7. At low frequency range, the magnitude of PSRR is one and at higher frequency range, the PSRR begins to fall off. This is because for the PSRR simulation setup, the NMOS is set to off and PMOS is in linear region. At low frequency range, the PMOS is regarded as a resistor and the loading capacitor can be treated as open. As a result, the output will have the same amplitude as the input. With the increase of the frequency, the capacitor will start to take effect and the output voltage will begin to fall off.

To validate the proposed PSIJ sensitivity expression (4), HSPICE simulation is conducted to obtain the reference PSIJ sensitivity values at different frequencies. The simulation setup for jitter extraction is depicted in Figure 2.8(a). In order to obtain both the magnitude and phase information, the TIE sequence is extracted as illustrated in Figure 2.8(b). The TIE is calculated by subtracting actual output edge switching time

from the ideal output edge switching. The obtained TIE value for each edge is plotted in time domain with respect to the input edge switching time, as in the derivation of (4), the time of input edge switching is treated as zero during the integration process. The extracted TIE sequence for the case with 100MHz power noise is shown in Figure 2.9, from which the magnitude and phase of the PSIJ can be acquired. The comparison of the PSIJ sensitivity magnitude and phase results obtained from the PSRR based model and HSPICE simulation are shown in Figure 2.10(a) and (b), respectively. The proposed PSIJ sensitivity model exhibits reasonably good estimation accuracy compared to the simulation results.

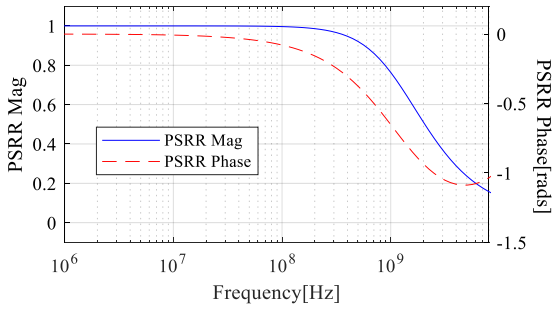


Figure 2.7 PSRR Simulation Result for Single Stage Inverter.

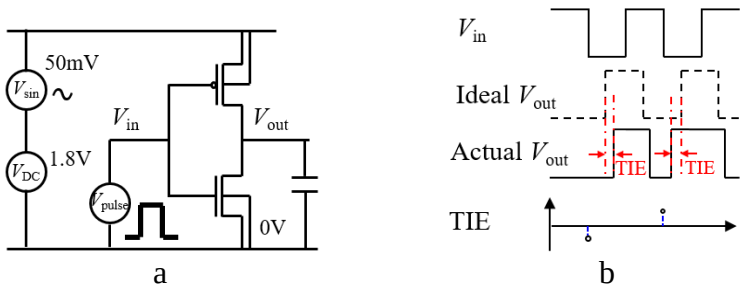


Figure 2.8 Simulation Setup for Jitter Extraction. a) Setup. b) Extraction of TIE Sequence.

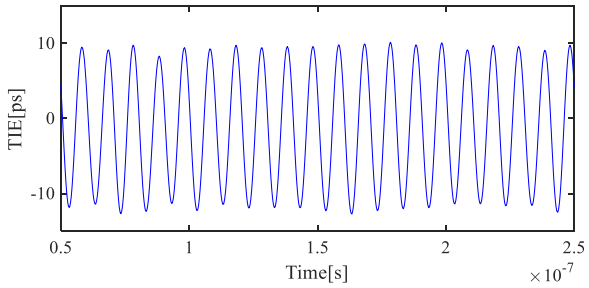
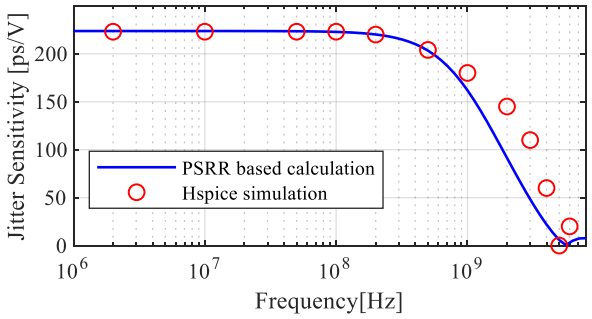
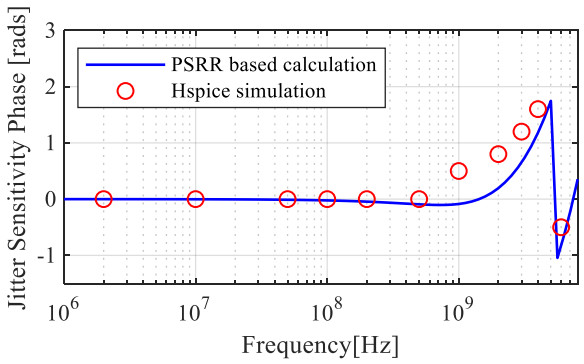


Figure 2.9 Extracted TIE Sequence for the Case with 100 MHz Power Noise.



a



b

Figure 2.10 Single Stage Inverter PSIJ Sensitivity Results Comparison between PSRR Based Model and HSPICE Simulation. a) Magnitude. b) Phase.

2.1.2.2. Inverter chain. The equation (4) can also be applied for inverter chain PSIJ sensitivity analysis with proper modification on the PSRR response and slope portion. Since each stage in the inverter chain will have their own PSRR response and slope, which will all contribute to the total PSIJ, the form of (4) needs to be adjusted accordingly. For the inverter chain, the total PSIJ at the final output stage can be obtained from the linear accumulation of local PSIJ at each stage [7], as illustrated in Figure 2.11. Since the switching edge directions are opposite for the odd and even number stages in the inverter chain, the polarity of induced jitter for the adjacent stages will be opposite, as the slopes of rising and falling edges are opposite in sign.

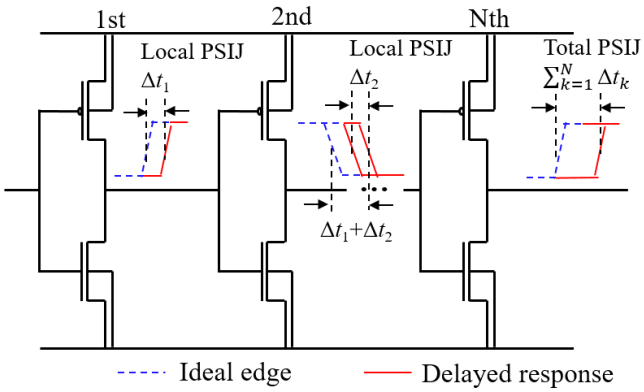
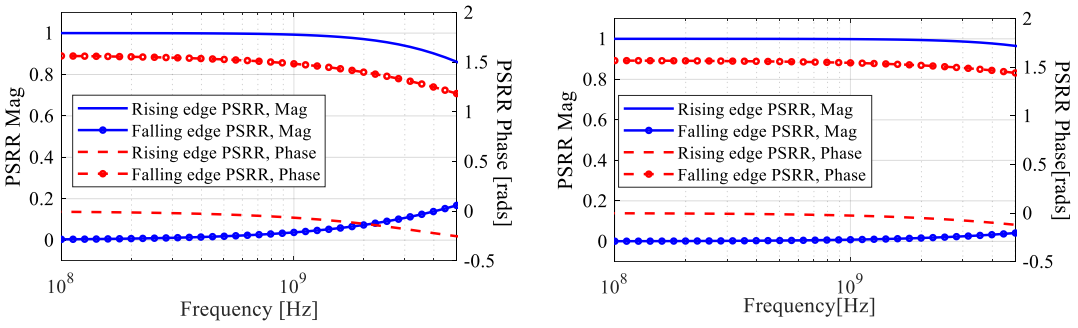


Figure 2.11 Inverter Chain Total PSIJ as Sum of Each Stage Local PSIJ.

The design parameters for the tested inverter chain is shown in Figure 2.4(b). The loading capacitance at the last stage is 10fF. This is an eight stage inverter chain where each stage size is increased at the same factor of 2. For each stage, PMOS is twice the size of NMOS. For the inverter chain designed in this fashion, besides the last output stage, the propagation delay of #1 to #7 stages will be almost the same and the rising and

falling edge propagation delays will also be very similar. In addition, the PSRR response of #1 to #7 stages are almost identical.

For each stage, the PSRR response for the rising edge case can be obtained by setting the input of each stage as low. The PSRR response for the falling edge case can be extracted by setting the input of each stage as high. The PSRR response of each stage for both the rising and falling edges in the inverter chain are summarized in Figure 2.12. The PSRR response for #1 to #7 stages are identical and are plotted in Figure 2.12(a) while the last stage PSRR response is shown in Figure 2.12(b).



a b

Figure 2.12 PSRR for Each stage in Inverter Chain. a) #1-#7 Stages. b) Output Stage.

For the inverter chain output rising edge case, the total jitter can be calculated by the linear summation of the local PSIJ as:

$$\left.\frac{PSRR_{DC}}{Slope}\right|_{\#1-\#7}\left(3\cdot PSRR'(\omega)_{rise}-4\cdot PSRR'(\omega)_{fall}\right)$$
$$+\left.\frac{PSRR_{DC}}{Slope}\right|_{Vout} PSRR'(\omega)_{rise}\Big|_{Vout} \quad (5)$$
$$=\left.\frac{PSRR_{DC}}{Slope}\right|_{\#1-\#7} A_{R\_\#1-\#7}'(\omega)+\left.\frac{PSRR_{DC}}{Slope}\right|_{Vout} A_{R\_Vout}'(\omega)$$

The local PSIJ of each stage is expressed as the form of the DC performance portion multiply with the normalized frequency dependency portion as shown in (2). Since the #1 to #7 stages share the same PSRR and rising/falling edge characteristics, the DC performance portion are the same and is written as $PSRR_{DC}/\text{Slope}|_{\#1\text{-}\#7}$. On the other hand, the DC performance portion for the final stage is different and is expressed as $PSRR_{DC}/\text{Slope}|_{Vout}$. For the case where the final output stage is rising, there will be four falling edges and three rising edges in the previous seven stages. All the rising edge stages will have the same normalized PSRR frequency dependency portion $PSRR'(\omega)_{rise,}$ while all the falling edge stages will have the same normalized PSRR frequency dependency portion $PSRR'(\omega)_{fall}$. The normalized PSRR frequency dependency portion for the last output stage is $PSRR'(\omega)_{rise}|_{Vout}$. The signs of local PSIJs for the adjacent stages are opposite and are explicitly expressed since the slope is treated as a magnitude value. For simplification, the normalized frequency dependency portion of the #1 to #7 stages is written as $A_{R\_\#1\text{-}\#7}'(\omega)$ and for the last stage the normalized frequency dependency portion is expressed as $A_{R\_Vout}'(\omega)$.

The DC performance portion can also be estimated by the DC delay change test. The DC performance portions for the #1 to #7 stages can be evaluated together. By recording the DC delay change at the #7 stage of the inverter chain, the DC jitter

sensitivity for the stages from #1 to #7 is written as $(T_{pd,max}- T_{pd,min})/(V_{dd,max}- V_{dd,min})|_{\#1\text{-}\#7}$. Since the PSRR response for the falling edge case is zero at DC, the DC jitter sensitivity is contributed by the three rising edge stages and it can be concluded:

$$\left.\frac{PSRR_{DC}}{Slope}\right|_{\#1-\#7} = \left.\frac{T_{pd\max} - T_{pd\min}}{V_{dd\max} - V_{dd\min}}\right|_{\#1-\#7} \Big/ 3 \tag{6}$$

The DC performance portion for the last stage can be extracted by isolating this stage and treat it as a single stage inverter, keeping the original loading capacitance. The DC performance portion is estimated as the DC jitter sensitivity of the output stage $(T_{pd,max}- T_{pd,min})/(V_{dd,max}- V_{dd,min})|_{Vout}$:

$$\left.\frac{PSRR_{DC}}{Slope}\right|_{Vout} = \left.\frac{1}{Slope}\right|_{Vout} = \left.\frac{T_{pd\max} - T_{pd\min}}{V_{dd\max} - V_{dd\min}}\right|_{Vout} \tag{7}$$

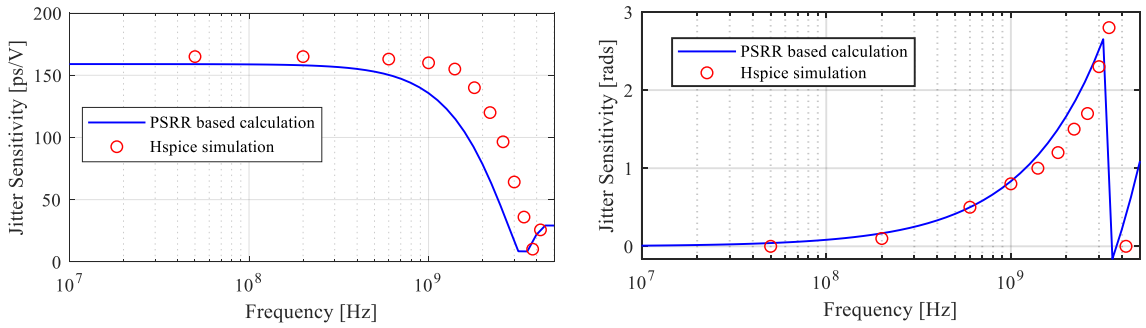
As all the stages in the inverter chain are consecutive in time, the time averaged effect of power rail noise should be considered in the propagation delay time range of the entire chain. Based on the above analysis, the application form of equation (4) for the inverter chain rising edge case is:

$$PSIJsensitivity(f) = \left[\begin{array}{l} \left.\frac{PSRR_{DC}}{Slope}\right|_{\#1-\#7} A_{R\_\#1-\#7}'(2\pi f) \\ + \left.\frac{PSRR_{DC}}{Slope}\right|_{Vout} A_{R\_Vout}'(2\pi f) \end{array}\right] e^{j\pi f T_{pR0}} \sin c\left(\pi f T_{pR0}\right) \tag{8}$$

where T_{pR0} is the inverter chain propagation delay for the rising edge case. The PSIJ sensitivity formulation for the falling edge case can be derived similarly.

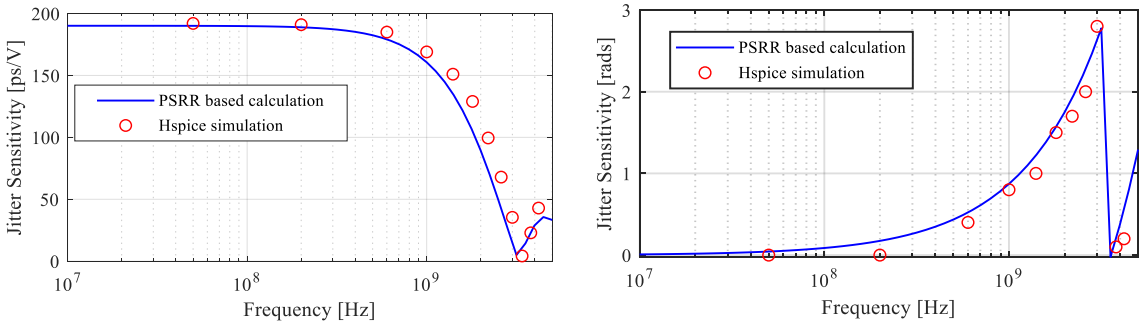
The obtained PSIJ sensitivity expressions for the rising and falling edge cases are validated through HSPICE simulation. For rising edge, the comparison results of PSRR based model and HSPICE simulation for PSIJ sensitivity magnitude and phase are plotted

in Figure 2.13 (a) and (b), respectively. For falling edge, the comparison results of PSRR based model and HSPICE simulation for PSIJ sensitivity magnitude and phase are plotted in Figure 2.14 (a) and (b), respectively. The proposed model can estimate the inverter chain PSIJ sensitivity with reasonably good accuracy for both the magnitude and phase.



a b

Figure 2.13 Inverter Chain Rising Edge PSIJ Sensitivity Results Comparison between PSRR Based Model and HSPICE Simulation. a) Magnitude. b) Phase.



a b

Figure 2.14 Inverter Chain Falling Edge PSIJ Sensitivity Results Comparison between PSRR Based Model and HSPICE Simulation. a) Magnitude. b) Phase.

2.1.2.3. Current mode differential driver. For current mode differential driver PSIJ sensitivity analysis, equation (4) can also be applied with proper modification on the PSRR response and slope portion. The PSRR response and slope of both the positive node and negative node need to be considered for PSIJ analysis. Since the slope of the positive node and negative node may be different, if only differential output PSRR response and slope is considered, the effect of the different slope in the positive and negative node to the PSIJ will be missed.

The design parameters for the current mode differential driver is shown in Figure 2.4(c). The nominal power rail voltage is 1.5V. The voltage levels for the single ended output are designed to be 0.625V for the low state and 0.875V for the high state. The differential output swing will be 500mV.

In order to obtain the PSRR response of the current mode differential driver, the circuit needs to be set to a proper DC status, as the input switching time is assumed to be negligible. The differential driver is switching between two DC statuses. For the case where the positive side input is low and negative side input is high, the magnitude and phase of the PSRR response is plotted in Figure 2.15(a). For the case where the positive side input is high and negative side input is low, the magnitude and phase of the PSRR response is plotted in Figure 2.15(b). At a fixed DC status, the PSRR response for the positive and negative side are different. It should be noted that despite the PSRR response will change for the positive and negative side output when the DC status changes, eventually only two PSRR response will be obtained. As Mp1 and Mp2 are the same and Mn1 and Mn2 are also the same. The PSRR response with larger value is denoted as

$PSRR_{nl}= V_{nl}/V_{sin}$, where V_{sin} is the amplitude of the power rail noise. The PSRR response with smaller value is written as $PSRR_{ns}=V_{ns}/V_{sin}$.

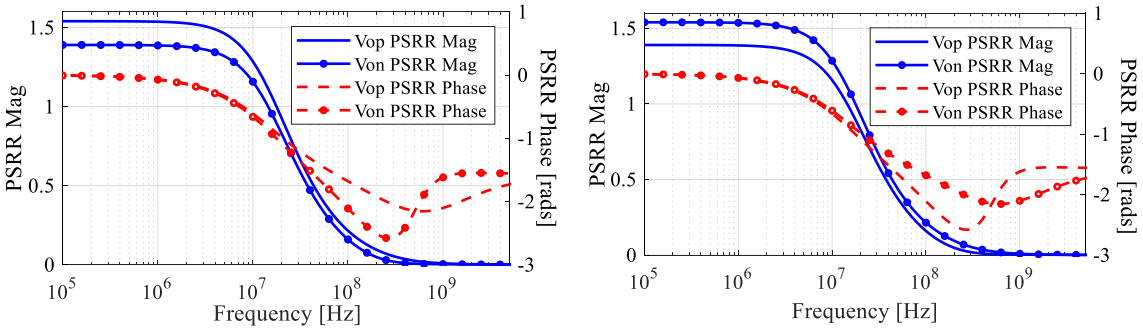


Figure 2.15 PSRR of Differential Driver. a) Positive Input Low, Negative Input High. b) Positive Input High, Negative Input Low.

The process to derive the differential TIE from PSRR response is illustrated in Figure 2.16. The positive and negative node output with ideal power voltage are denoted as *OP* and *ON*, respectively. The voltage value for the low and high states are denoted as V_2 and V_1, respectively. The crossing time location of *OP* and *ON* under the nominal power voltage is denoted as t_c. The crossing voltage level at t_c is represented as V_{cross}. When the power voltage is increased, the changed positive and negative node output are indicated as *OP*' and *ON*', respectively. The difference between the new crossing time location t_c' and the original t_c is the differential output TIE. At the original t_c, *OP*' will increase to V_{pnx} while *ON*' will increase to V_{nnx}. The *OP*' and *ON*' crossing point, *OP*' and t_c crossing point, as well as *ON*' and t_c crossing point has formed a triangle. The length of the triangle vertical edge is V_{pnx}-V_{nnx} and differential TIE will be the height at this edge. The slope of the other two edges in the triangle are *SR* and *SF*, which are the

magnitude of the rising and falling edge slope. From basic geometry theory, the differential TIE can be calculated as $(V_{pnx}-V_{nnx})/(SR+SF)$. For simplicity, the *SR* and *SF* are assumed to be obtained under nominal power voltage. Similarly, the original crossing time t_c, can be expressed as $(V_2-V_1)/(SR+SF)$. From this analysis, it is clearly shown that the differential TIE is related to the PSRR response and the rising/falling edge slopes.

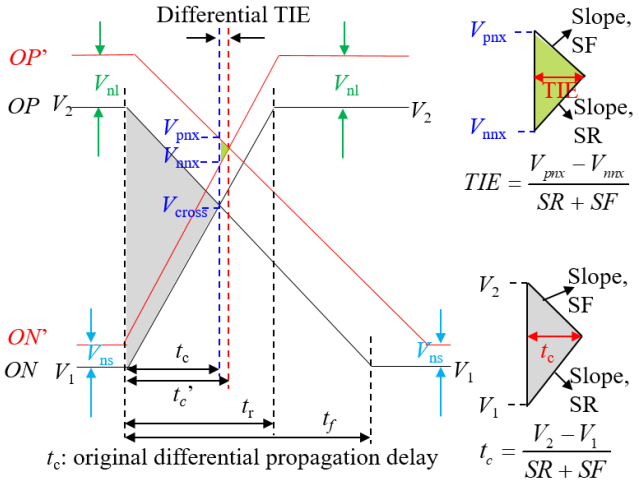


Figure 2.16 Differential Driver Output TIE Analysis Illustration.

The V_{nnx} can be estimated as:

$$V_{nnx} = V_{cross} + V_{ns} + V_{nl}\frac{t_c}{t_r} = V_{cross} + V_{ns} + V_{nl}\frac{SR}{SR+SF} \tag{9}$$

When the power rail voltage is increased, before transition, *ON*' will increase by V_{ns} compared to *ON*. After transition, for the flipped DC status, *ON*' will increase by V_{nl}, compared to *ON*. During the transition, the negative node rising edge slope will also increase due to the PSRR response. At the original crossing time t_c, the voltage increase due to the increase of rising edge slope is estimated as $V_{nl}(t_c/t_r)$, where t_r is the time when

the negative node output changes from V_1 to V_2 and can be written as $(V_2\text{-}V_1)/SR$. Plus the initial increase $V_{ns,}$ V_{nnx} will be $V_{cross}+ V_{ns}+ V_{nl}(t_c/t_r)$.

Similar analysis is carried out for *OP*' and the V_{pnx} is expressed as:

$$V_{pnx} = V_{cross} + V_{nl} + V_{ns}\frac{t_c}{t_f} = V_{cross} + V_{nl} + V_{ns}\frac{SF}{SR+SF} \tag{10}$$

Plug V_{pnx} and V_{nnx} values in the differential TIE expression, normalize to the amplitude of power rail noise, extract the DC performance portion and consider the time averaged effect, the application form of equation (4) for the current mode differential driver is derived as follow:

$$\begin{aligned} &PSIJsensitivity(f) \\ &= \frac{PSRR_{DC}}{SF+SR}\begin{pmatrix}(1-\frac{SR}{SR+SF})PSRR_{nl}'(2\pi f) \\ -(1-\frac{SF}{SR+SF})PSRR_{ns}'(2\pi f)\end{pmatrix} e^{j\pi f T_{p0}}\sin c(\pi f T_{p0}) \end{aligned} \tag{11}$$

T_{p0} is the differential output propagation delay. The DC performance portion is estimated with the differential output DC jitter sensitivity as:

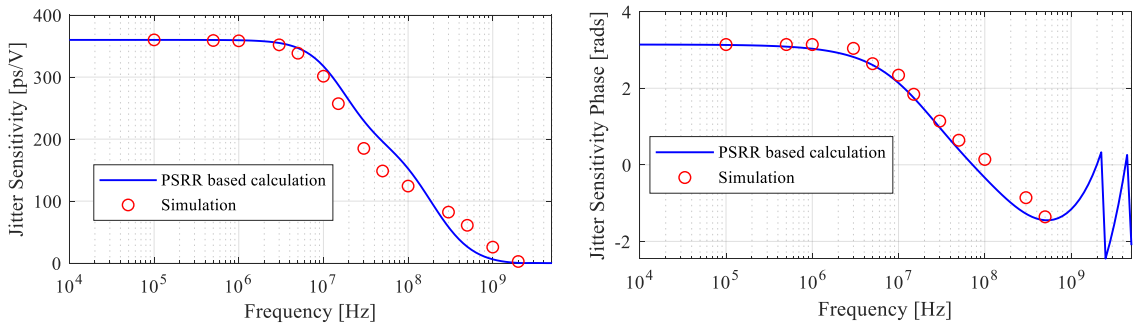
$$\frac{PSRR_{DC}}{SF+SR} = \left|\frac{T_{pd\max} - T_{pd\min}}{V_{dd\max} - V_{dd\min}}\right| \tag{12}$$

The normalized PSRR frequency dependency portion are $PSRR_{nl}$' and $PSRR_{ns}$' for $PSRR_{nl}$ and $PSRR_{ns}$, respectively.

From (11), the influence of PSRR and transition edge slope of the positive and negative nodes can be evaluated. If the PSRR of the negative node and positive node are the same, and the magnitude of *SR* and *SF* are the same, the differential TIE should be zero; If the PSRR responses are the same but the *SR* and *SF* are different, the differential TIE will appear and is proportional to $PSRR(SR\text{-}SF)/(SR+SF)^2$; If the slopes are the same

but the PSRR responses are different, the differential TIE will also exist and is proportional to 0.5($PSRR_{nl}$- $PSRR_{nl}$)/(2Slope).

The PSIJ sensitivity expression for the current mode differential driver is also validated through the comparison with the HSPICE simulation results. The PSIJ sensitivity magnitude and phase are plotted in Figure 2.17(a) and (b), respectively. The results from PSRR based calculation match reasonably well with the one obtained from transistor circuit simulation.



a b

Figure 2.17 Differential Transmitter PSIJ Sensitivity Results Comparison between PSRR Based Model and HSPICE Simulation. a) Differential Output PSIJ Magnitude. b) Differential Output PSIJ Phase.

2.2. ANALYSIS OF PSIJ OF HIGH SPEED OUTPUT BUFFER WITH ON-DIE LDO

As on-die LDO is often applied for high speed output buffer to provide power voltage, the PSIJ of the buffer with LDO is also analyzed.

2.2.1. System PSIJ Sensitivity Analysis Method. The overall block diagram of a typical system is shown in Figure 2.18(a). With the voltage noise presented on the

power rail of the LDO, the PSIJ at the output buffer will be derived. The proposed analysis procedure is shown in Figure 2.18(b). To obtain the PSIJ sensitivity of the system under this scenario, the first step is to acquire the PSRR response of the LDO block. The second step is to derive the buffer PSIJ sensitivity. At last, the system PSIJ sensitivity can be calculated from the product of the LDO PSRR response and buffer PSIJ sensitivity. Assuming the power noise is small, the LDO power supply rejection ratio (PSRR) response and the PSIJ sensitivity can be treated as linear functions.

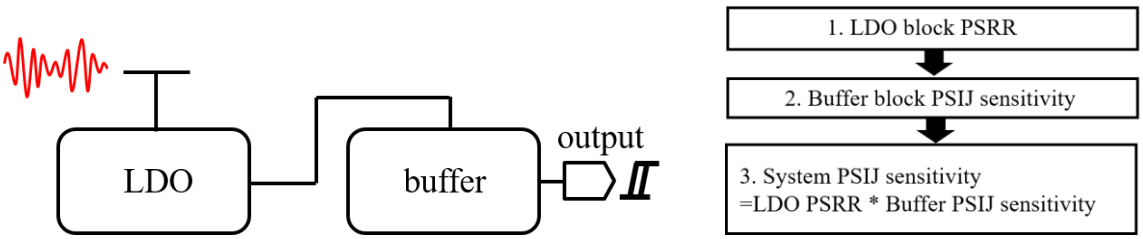


Figure 2.18 System Analysis Method. a) Overall System Block Diagram. b) Proposed Analysis Procedure.

The first step is to simulate the LDO block PSRR response. The design parameters of the on-die LDO is shown in Figure 2.19. The nominal output voltage of the designed LDO is 1.5V. The LDO PSRR response is sensitive to the output load conditions, as the pass transistor current is sensitive to the load parasitic. As a result, the effect of different buffer loads to the LDO PSRR responses should be taken into consideration. The investigated buffers are an inverter chain as shown in Figure 2.4(b) and a current mode differential driver (Tx driver) as shown in Figure 2.4(c).

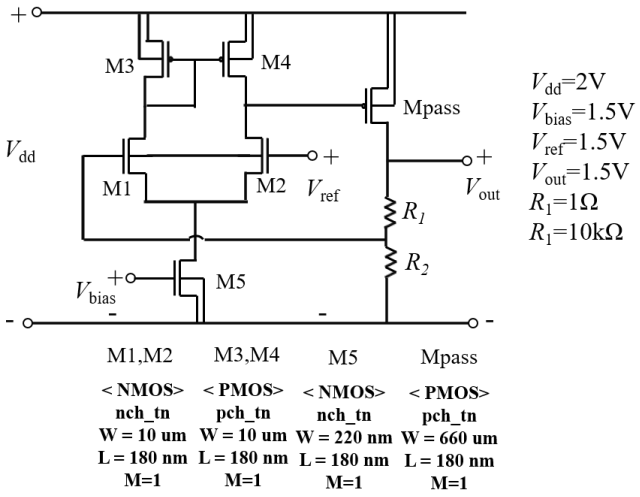


Figure 2.19 Designed LDO Parameters.

To demonstrate the output loading effect to the on-die LDO PSRR response, the simulation setup is shown in Figure 2.20(a). The effect of load resistance, load capacitance and load current to the LDO PSRR response is shown in Figure 2.20(b), (c) and (d), respectively. When different buffers are attached to the LDO output, the equivalent resistive and capacitance loading for the LDO will be changed. So it is necessary to consider the driver loading effect. It can also be shown that the loading current will also influence the PSRR response significantly. This is because the drain source current of the pass transistor will be changed by the loading current, thus changing the equivalent resistance of the pass transistor. As a consequence, when evaluating the LDO PSRR response, the equivalent buffer switching current should be taken into account.

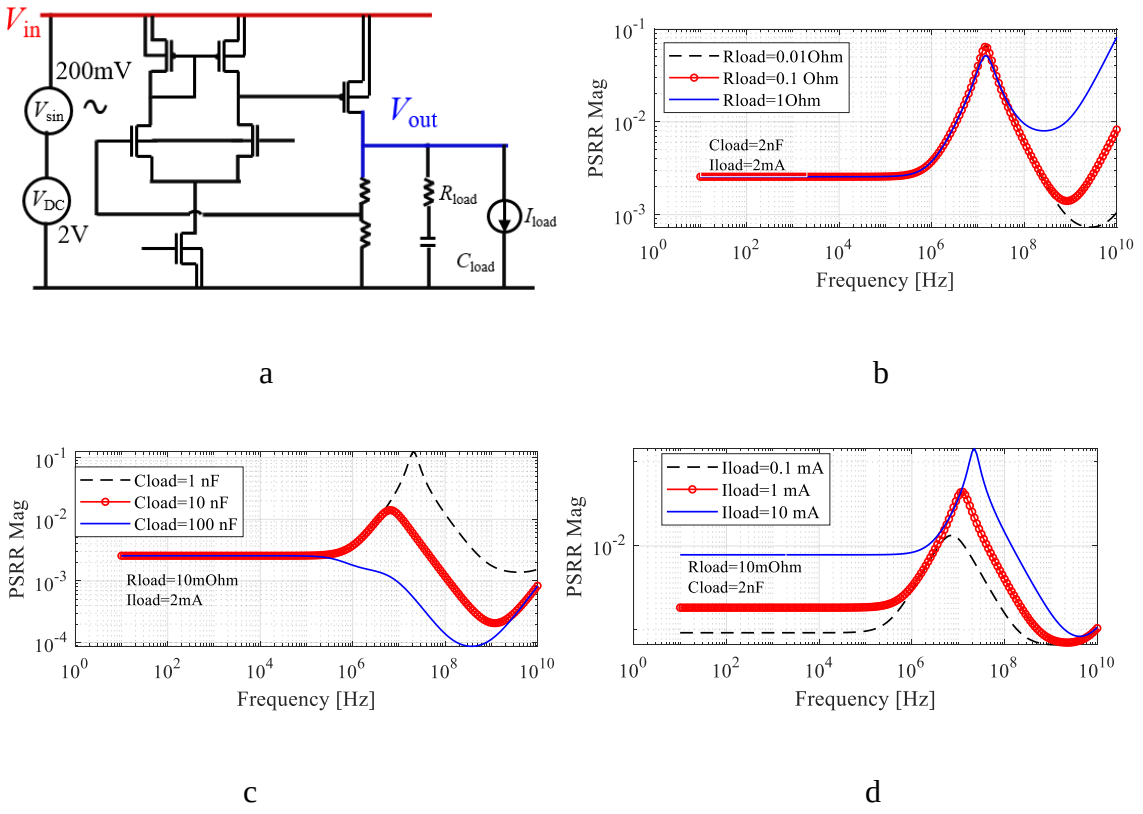


Figure 2.20 Loading Effect to LDO PSRR Response. a) Simulation Setup. b) Load Resistance Effect. c) Load Capacitance Effect. d) Load Current Effect.

In LDO PSRR AC simulation, the buffer power net should be attached to the output of the LDO. The buffer should be set to a certain DC status. However, this can only include the current drawn at the buffer static states. The buffer current consumption during the switching events are neglected. In order to account for the current drawn from power net during driver switching, the switching current on the power net for the inverter chain buffer is shown in Figure 2.21 as an example. For each current peak, the shape is close to a triangle. As there will be two switching events in one period, the averaged equivalent switching current I_{equ_load} is evaluated as:

$$I_{equ\_laod} = \frac{0.5 T_{pulse\_width} I_{peak} * 2}{T_{input\_switching}} \quad (13)$$

where T_{pulse_width} is the width of the triangular switching current pulse. I_{peak} is the peak value of the switching current. $T_{inpu\_switching}$ is the period of the input switching pulse. The extracted equivalent loading current is 0.2mA for the designed inverter chain.

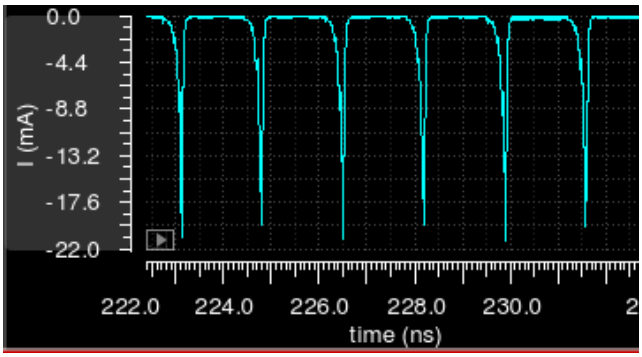


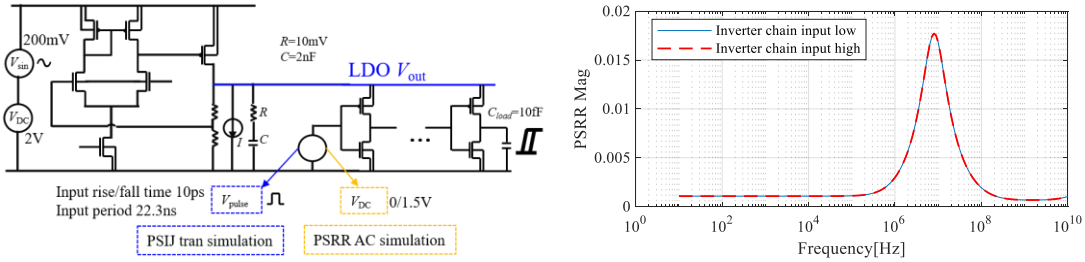
Figure 2.21 Current Drawn on Power Net for Inverter Chain Driver.

The second step for the system PSIJ sensitivity analysis is to obtain the buffer PSIJ sensitivity, which can be obtained by adding a sinusoidal source to the DC power and sweeping the source frequency. With the LDO block PSRR response $PSRR_{LDO}$ and the buffer PSIJ sensitivity $JitterSensitivity_{driver}$, the total system PSIJ sensitivity $JitterSensitivity_{sys}$ can be derived as:

$$JitterSensitivity_{sys} = PSRR_{LDO} \cdot JitterSensitivity_{driver} \quad (14)$$

2.2.2. Simulation Validation. The simulation setup for LDO PSRR response with inverter chain as loading buffer is plotted in Figure 2.22(a). A current source with 0.2mA DC current is used to mimic the current drawn during inverter chain switching. The simulated LDO PSRR response is shown in Figure 2.22(b). The output noise to input

noise amplitude is taken as the PSRR value. Regardless of the inverter chain input status, the PSRR responses are the same.



a b

Figure 2.22 PSRR Response of LDO Block with Inverter Chain Buffer. a) Simulation Setup. b) PSRR Response.

Similar analysis can be carried out for the case where the buffer is a current mode differential driver. The switching current drawn from the power net is shown in Figure 2.23. For this driver, there will be a constant current consumption at the static status. The equivalent loading current during the switching event is about 6uA. On the other hand, as it can be noticed, there will be a DC current always presented on the power rail during the current mode differential driver operation. The simulation setup for LDO block PSRR analysis is shown in Figure 2.24(a). As mentioned before, for PSRR analysis, the current mode differential driver needs to be set to a proper DC status. The input voltage is shown in Figure 2.24(a). The PSRR response of the LDO block is shown in Figure 2.24(b). Regardless of the inverter chain input status, the PSRR responses are the same. The peak location is close to 15MHz.

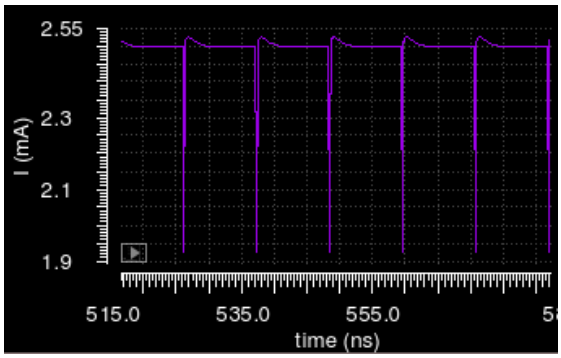
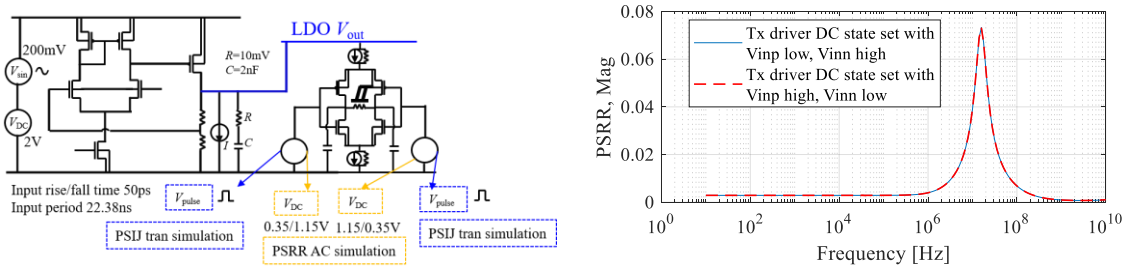


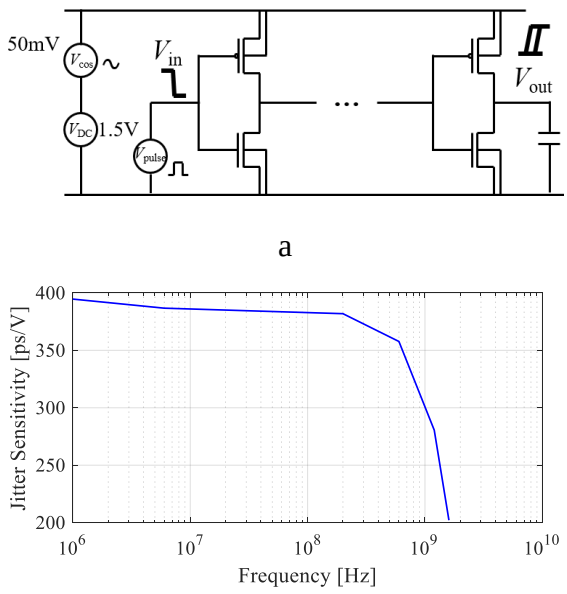
Figure 2.23 Current Drawn on Power Net for Current Mode Differential Driver.



a b

Figure 2.24 PSRR Response of LDO Block with Current Mode Differential Driver. a) Simulation Setup. b) PSRR Response.

For the inverter chain, the PSIJ sensitivity analysis setup is shown in Figure 2.25(a). By sweeping the frequencies of the sinusoidal noise source, the PSIJ sensitivity is extracted as shown in Figure 2.25(b). For the current mode differential driver, the simulation setup for PSIJ sensitivity analysis is shown in Figure 2.26(a). The PSIJ sensitivity is plotted in Figure 2.26(b).



a

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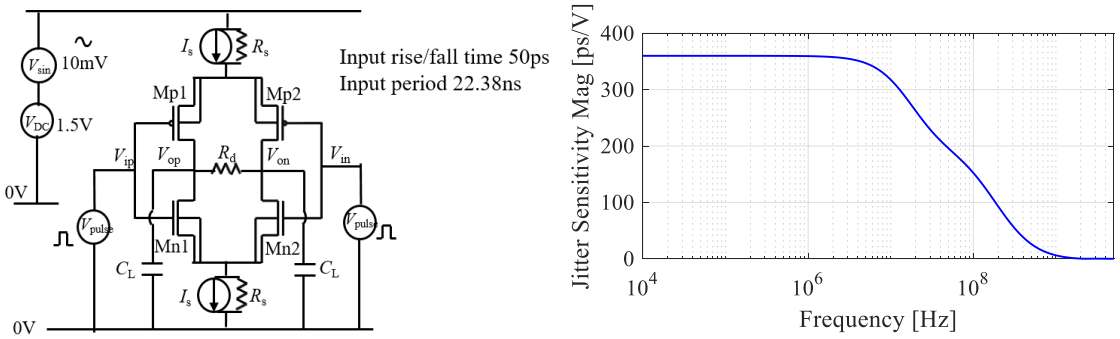
Figure 2.25 PSIJ Sensitivity of Inverter Chain Buffer. a) Simulation Setup. b) PSIJ Sensitivity.



a

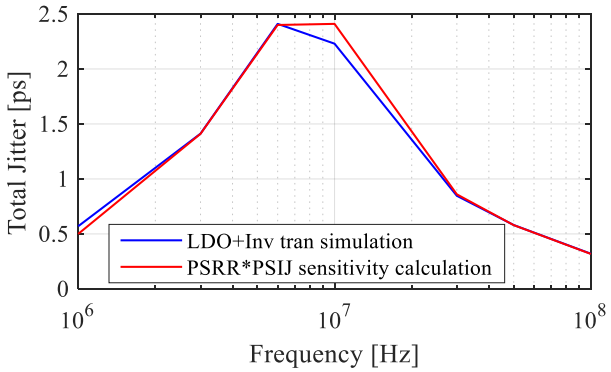
b

Figure 2.26 PSIJ Sensitivity of Current Mode Differential Driver. a) Simulation Setup. b) PSIJ sensitivity.

To validate the proposed method, the transient simulation of the total system is performed to extract the PSIJ sensitivity. The simulation setup for the two buffer cases are the same as in Figure 2.22(a) and 2.24(a). The input of the driver are changed to the switching pulses for the transient simulation. The DC load current is also removed. The comparison of the calculated total system PSIJ sensitivity using (14) and the simulated PSIJ sensitivity from the total system is shown in Figure 2.27. The results for the inverter chain buffer case and the current mode differential driver case are shown in Figure 2.27(a) and (b), respectively. The proposed analysis method can evaluate the total system PSIJ sensitivity with reasonably good accuracy.

From the proposed method, the contribution of different blocks to the total system PSIJ sensitivity properties can be distinguished. With the application of on-die LDO, the system PSIJ has been reduced significantly, due to the power net noise suppression capability of the LDO block. In addition, it can be observed that the peak frequency location in the PSIJ sensitivity of the total system are determined by the LDO block PSRR response. This could be helpful for the design optimization of different blocks to achieve better timing performance of the system.

In addition, it can be noticed that the system PSIJ sensitivity has been reduced compared to the driver only PSIJ sensitivity. It is a demonstration of the advantages for using the on-die LDO. This is because the on-die LDO can reject the noise on the power rail. Since the noise in the output of LDO is reduced, the introduced PSIJ in the buffer using on-die LDO output as power supply is also reduced.



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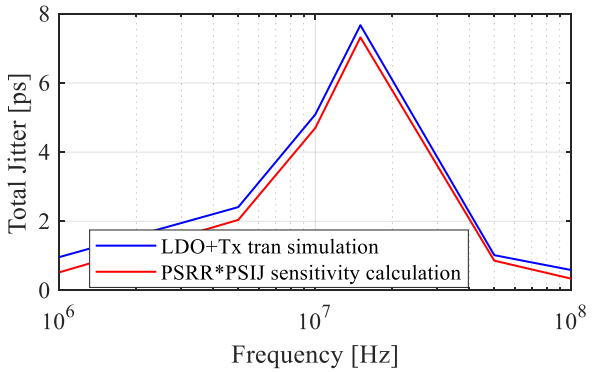


b

Figure 2.27 Total System PSIJ Sensitivity Results Comparison between Total System Transient Simulation and the Proposed Calculation Method. a) Buffer Is an Inverter Chain. b) Buffer Is a Current Mode Differential Driver.

2.3. IMPROVING PSIJ SIMULATION ACCURACY FOR IBIS MODEL

PSIJ simulation is an important part for signal integrity and power integrity analysis. As the SPICE model is not always available from the semiconductor vendors, the IBIS model has been developed. It is desired to improve the PSIJ simulation capability for this kind of behavior model.

2.3.1. Modeling of PSIJ in IBIS Model. The equivalent circuit for a basic IBIS output model is shown in Figure 2.28. It is composed of the pull-up branch, pull-down branch, power clamp branch and ground clamp branch. C_comp is the equivalent output capacitance of the driver. L_pkg, R_pkg and C_pkg are the equivalent inductance, resistance and capacitance for the driver. I_{out} is the total current at the buffer output node and can be calculated from the pull-up, pull-down, power clamp and ground clamp branches currents. I-V tables for pull-up transistor describes the pull-up current I_{pu} relationship with the voltage difference between V_{comp} and the power voltage. I-V tables for pull-down transistor describes the pull-up current I_{pd} relationship with the voltage difference between V_{comp} and the ground voltage. The power clamp I-V table lists I_{pc} versus the voltage difference between V_{comp} and the power voltage. The ground clamp I-V table lists I_{gc} versus the voltage difference between V_{comp} and the ground voltage. Rising and falling waveforms V-t(voltage-time) tables provide the transient information on the value of V_{comp} as a function of time for different loading conditions. The switching coefficient K_u and K_d are used as multiplication factors on the currents I_{pu} and I_{pd}, respectively. The K_u and K_d can be determined with the well-known 2 equations 2 unknowns algorithm:

$$-I_{out1} = K_u I_{pu1} + K_d I_{pd1} + I_{pc1} + I_{gc1} \tag{15}$$

$$-I_{out2} = K_u I_{pu2} + K_d I_{pd2} + I_{pc2} + I_{gc2} \tag{16}$$

where I_{out1}, I_{pu1}, I_{pd1}, I_{pc1}, and I_{gc1} are the currents for a particular load condition, in which case the V_{comp} is V_{comp1}. I_{out2}, I_{pu2}, I_{pd2}, I_{pc2}, and I_{gc2} are the currents for a different load condition, in which case the V_{comp} is V_{comp2}.

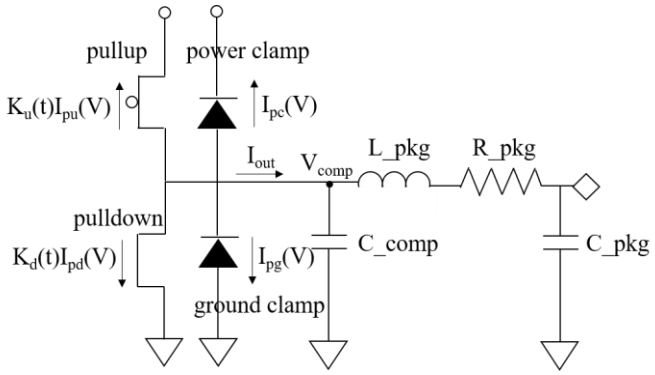


Figure 2.28 IBIS Output Model Structure.

2.3.1.1. Model derivation. As the transition behavior of the buffer is mainly described by the switching coefficient K_u and K_d, to improve the PSIJ simulation accuracy, the switching coefficients are modified as a function of both time and the power rail voltage:

$$K_u(t) = K_{u0}(t) + B_u(t) \cdot \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right] + A_u(t) \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right]^2 \quad (17)$$

$$K_d(t) = K_{d0}(t) + B_d(t) \cdot \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right] + A_d(t) \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right]^2 \quad (18)$$

where $K_{u0}(t)$ and $K_{d0}(t)$ are the extracted switching coefficients with the ideal power voltage V_{cc0}. $B_u(t)$ and $B_d(t)$ are the linear correction coefficients. $A_u(t)$ and $A_d(t)$ are the quadratic correction coefficients. $V_{cc}(t)$ is actual power rail voltage. T_{switch} is the elapsed time since the input switching event happens.

For the proposed modification on the switching coefficients, the correction coefficients $B_u(t)$, $B_d(t)$, $A_u(t)$ and $A_d(t)$ are served to account for the delay change due to

the power rail noise voltage at each time point. It should also be noted that instead of the instantaneous power rail voltage, the time averaged power rail voltage is used. In [22], only the instantaneous power voltage effect is considered. The effect of the time averaged power rail noise on the buffer output switching edge is illustrated in Figure 2.3. The power rail noise can take effect in the entire time range of the buffer output propagation delay. If the period of the sinusoidal power rail noise voltage is the same as the propagation delay, regardless of the actual instantaneous power rail voltage value at the output switching edge, the propagation delay will not change. To model the PSIJ behavior correctly, it is essential to consider the time averaged power rail voltage.

Before the simulation can be performed, the switching coefficients and the corresponding correction coefficients need to be extracted. The switching coefficients at the minimum, typical and maximum DC power rail voltage should be firstly obtained using (15) and (16). The switching coefficients calculated under the typical power rail voltage are noted as $K_{u0}(t)$ and $K_{d0}(t)$. For $B_u(t)$ and $A_u(t)$ used for the pull-up switching coefficient $K_u(t)$, the 2 equations 2 unknowns algorithm can be employed. The pull-up switching coefficient $K_{u\_max}(t)$ at the maximum DC voltage V_{cc_max} and the pull-up switching coefficient $K_{u\_min}(t)$ at the minimum DC voltage V_{cc_min} are written using the form of (17) and have formed the 2 equations:

$$K_{u\_\max}(t) = K_{u0}(t) + B_u(t)(V_{cc\_max} - V_{cc0}) + A_u(t)(V_{cc\_max} - V_{cc0})^2 \qquad (19)$$

$$K_{u\_\min}(t) = K_{u0}(t) + B_u(t)(V_{cc\_\min} - V_{cc0}) + A_u(t)(V_{cc\_\min} - V_{cc0})^2 \qquad (20)$$

The correction coefficients $B_u(t)$ and $A_u(t)$ for the pull-up switching coefficient $K_u(t)$ can then be calculated from (5) and (6). $B_d(t)$ and $A_d(t)$ for the pull-down switching coefficient $K_d(t)$ can be similarly derived.

2.3.1.2. Spice implementation. For most of the open source spice simulators, the IBIS support is not developed. The other way around to apply the IBIS model for system analysis in these simulators is to convert the existing IBIS model into sub-circuit spice netlist [23]. On the other hand, with the converted IBIS model, the IBIS algorithm is explicitly revealed as spice compatible sub-circuit format, allowing easier implementation of the new algorithm and new IBIS model.

The spice implementation process is summarized in Figure 2.29. The first step is to differentiate the rising and falling event from the input. This can be realized by calculating the d*v*/d*t* of the input signal [24], as shown in Figure 2.30(a). This can be realized using an ideal transmission line. The d*v* is the voltage difference between the input port and output port of the transmission line. The d*t* is the delay of the transmission line and is also the simulation time step.

The second step is to calculate the elapsed time after the buffer input switching happens. From the converted d*v*/d*t*, the time at which point the input switching happens is known. This time point value will be held until the next switching event happens, as plotted in Figure 2.30(b). The held time value is also realized with an ideal transmission line. The previous time step time value will be stored in the output port of the ideal transmission line. The special variable "time" in Ngspice, which reflecting the actual simulation time will be utilized [24]. By subtracting the held signal from the variable "time", the elapsed time since every switching event occurs is obtained. At the beginning of every switching event, the held time value can be reset to zero, thus the elapsed time for each switching event can be recorded. The time value is transferred into voltage value.

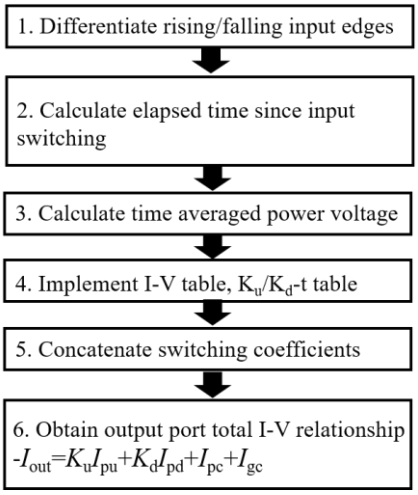
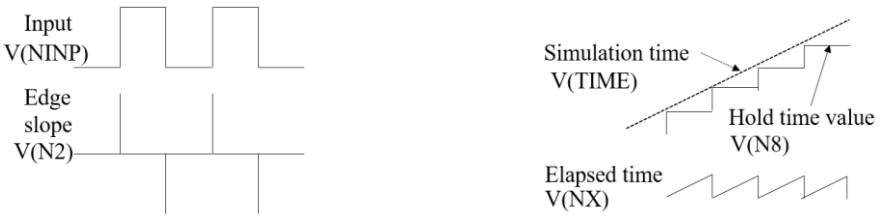


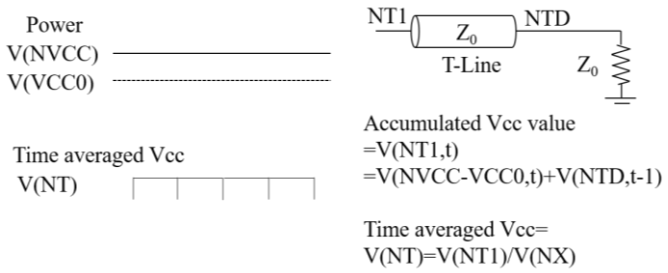
Figure 2.29 Spice Implementation Procedure.



a b

Figure 2.30 Control Signal Calculation. a) Find Switching Edges. b) Obtain Elapsed Time Since Switching Event Happens.

In the third step, the time averaged power rail voltage is implemented. This is one of the most important elements in the proposed new IBIS model. An ideal transmission line with the propagation delay of a single simulation time step is applied, as illustrated in Figure 2.31(a). The far end voltage value sum the power rail voltage at the current time step is fed to the near end of the transmission line. This value is then divided by the elapsed time to obtain the time averaged power rail voltage since the input switches. The corresponding control signals in spice netlist are shown in Figure 2.31(b).



a

```
B8 NT1 0 V...
=(V(NX) > 0.01)?(V(NVCC)*0.001-1.8*0.001+V(NTD)):0.0
B9 NT 0 V=(V(NX) > 0.01)? V(NT1)/V(NX) : 0.0

T3 NT1 0 NTD 0 Z0=50 Td=10p
R3 NTD 0 50
```

b

Figure 2.31 Implementation of Time Averaged Power Rail Noise Voltage for the Proposed Model. a) Obtain Time Averaged Power Rail Voltage. b) Ngspice Sub-Circuit Netlist for Related Control Signals.

For the fourth step, the I-V table and the modified K_u/K_d-t table are converted into spice netlist. I-V table data are realized with the ASRC sources in Ngspice [24], as shown in Figure 2.32(a). For the new IBIS model, the modified K_u-t table is implemented as an ASRC source as depicted in Figure 2.32(b), following expression (17). The switching coefficient $K_{u0}(t)$ under the nominal voltage, the linear correction coefficient $B_u(t)$ and the quadratic correction coefficient $A_u(t)$ are previously calculated offline. The voltage V(1,2) represents the elapsed time. The voltage V(5) represents the time averaged power rail noise voltage. The voltage of V(3,4) represents the switching coefficient $K_u(t)$. Similarly, the K_d-t table can also be written as an ASRC source. The original K_u-t table is also shown for comparison, as plotted in Figure 2.32(c). In the fifth step, the actual switching coefficients will be concatenated from the K_u/K_d-t table data based on the input bit

sequence as illustrated in [24]. At last, the driver output port current voltage relationship can be transformed into the spice netlist form following equation $-I_{out} = K_u I_{pu} + K_d I_{pd} + I_{pc} + I_{gc}$, as demonstrated in [24].

```
* PU BRANCH
.SUBCKT driver_PULLUP_TYP 3 4 1 2
B1 3 4 I =
+ (V(1,2) < -1.800000E0)? 1.514020E2:
+ (V(1,2) < -1.753250E0)? -1.933262E2*V(1,2)-1.965852E2:
...
+ -8.792500E1
.ENDS
```

a

```
* KU COEF RISE
.SUBCKT driver_TYP_KU_R 3 4 1 2 5
B1 3 4 V =
+ (V(1,2) < 0.000000E0)? 0.000000E0:
+ (V(1,2) < 0.003622352)? 12.87944* V(1,2)+0.000000000000·
+ (V(1,2) < 0.007244704)? -0.0000729516*V(1,2)+0.04665411·

... +(0.0000251111959497*V(1,2)+-0.1034584500000000)*V(5) ...
... +(0.0002022823036612*V(1,2)+-0.1034590917761164)*V(5) ...
```

Ku0(t)

Bu(t)

```
+(0.0039680452540881*V(1,2)+-7.5443674999999999)*V(5)*V(5):
+(0.0091645843101826*V(1,2)+-7.5443863236936428)*V(5)*V(5):
```

Au(t)

b

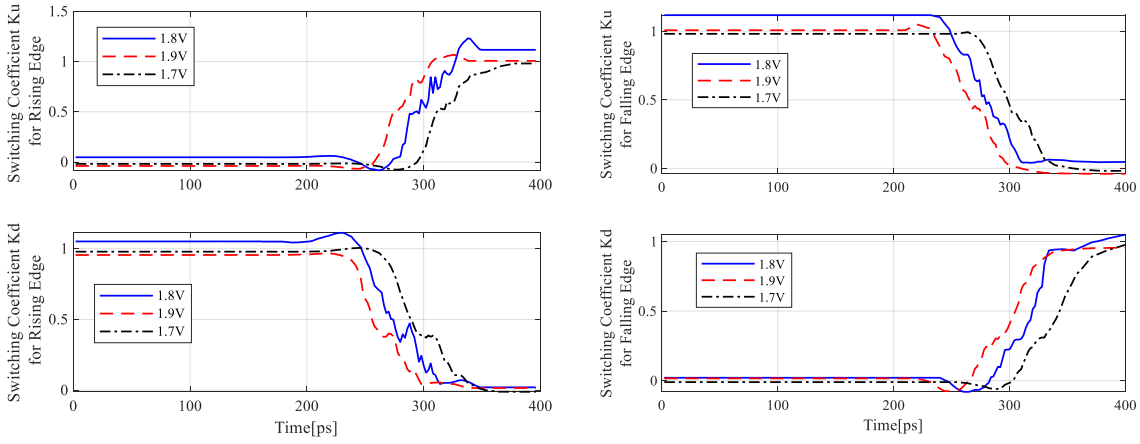
```
* KU COEF RISE
.SUBCKT driver_TYP_KU_R 3 4 1 2
B1 3 4 V =
+ (V(1,2) < 0.000000E0)? 0.000000E0:
+ (V(1,2) < 3.622352E-3)? 1.287944E1 * V(1,2) + 0.000000E0:
+ (V(1,2) < 7.244704E-3)? -7.295161E-5 * V(1,2) + 4.665411E-2:
```

Ku0(t)

c

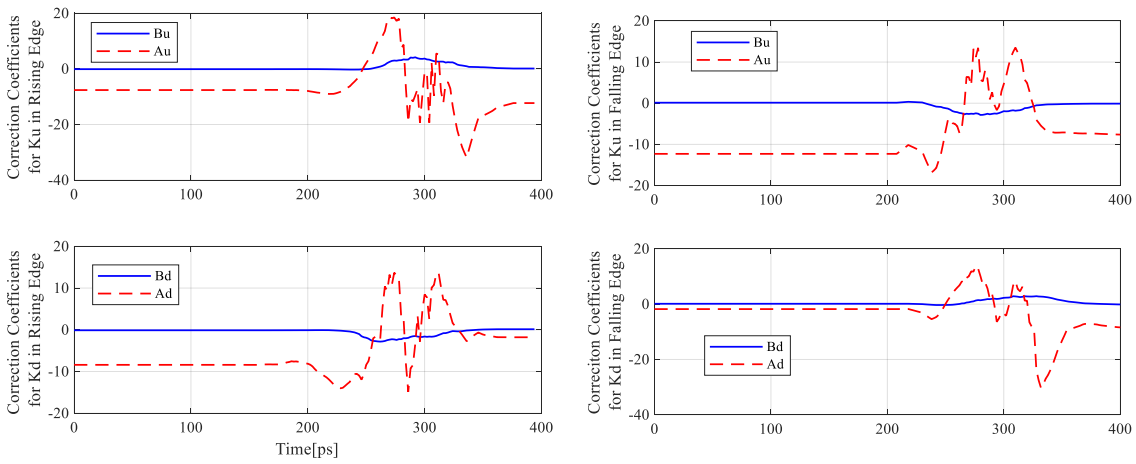
Figure 2.32 Tabulated Data Expressed as Ngspice Sub-Circuit Netlist. a) Implementation in the Proposed Model. b) Implementation in the Original Model.

2.3.2. Model Validation. The proposed new IBIS model is validated on an inverter chain. The design parameters for the inverter chain is shown in Figure 2.4(b). For this circuit, there are no power and ground clamp branches. The C_comp is extracted following the procedure listed in [15], with a value of 0.496pF. The nominal power voltage is 1.8V, while the minimum and maximum power voltages are 1.7V and 1.9V respectively. The extracted switching coefficients at the three different DC power voltages for the rising and falling cases are shown in Figure 2.33(a) and (b), respectively. It can be observed that for the switching coefficients at different DC power voltages, the delay information is embedded. In addition, it is also possible for the switching coefficients to exhibit some ripples, especially at the transition regions. The correction coefficients extracted for the rising and falling cases using (5) and (6) are shown in Figure 2.34(a) and (b), respectively. Three test cases are performed for the proposed new IBIS model.



a b

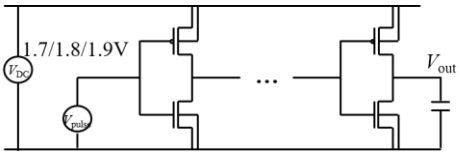
Figure 2.33 Switching Coefficients Ku, Kd. a) Rising Edge. b) Falling Edge.



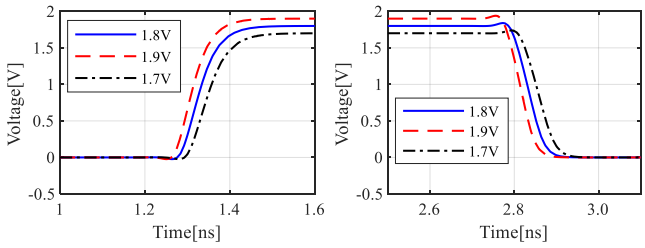
a b

Figure 2.34 Correction Coefficients Bu, Au, Bd, Ad. a) Rising Edge. b) Falling Edge.

The simulation setup for the first test case is shown in Figure 2.35(a). The DC power voltage are set to 1.7V, 1.8V and 1.9V. The transistor level transient simulation results for an output rising and a falling edge obtained using HSPICE are shown in Figure 2.35(b). The input rising switching happens at 1ns, while the input falling switching happens at 2.5ns. The simulation results of the proposed new IBIS model using Ngspice are shown in Figure 2.35(c). The proposed model can correlate with the transistor level circuit model results with reasonably good accuracy. The simulated time averaged power rail noise of the proposed new IBIS model is plotted in Figure 2.35(d), for the corresponding rising and falling cases. It can be shown that the time averaged power noise voltage is -0.1V for 1.7V case, 0V for 1.8V case and 0.1V for 1.9V case. Due to the limitation of the implementation algorithm, at the initial stage of the switching event, the time averaged power noise voltage will need time to rise to the expected value. However, it can still be applied to capture the delay change effect.



a



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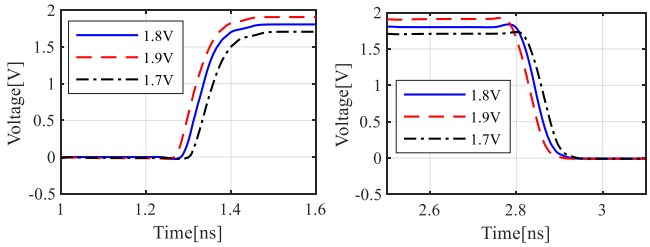
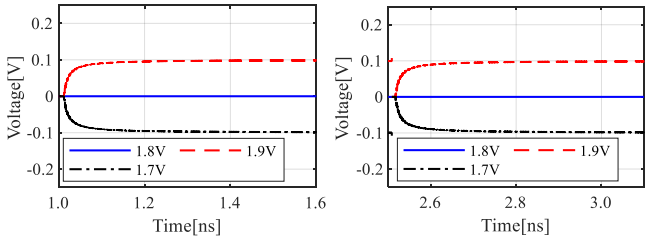


c



d

Figure 2.35 Test Case1. a) Simulation Setup. b) HSPICE Output Results. c) Proposed Model Output Results. d) Proposed Model Time Averaged Power Noise Results.

The HSPICE simulation results of the power-aware IBIS model (version 5.0) for this driver is also plotted in Figure 2.36. It can be observed that the model fails to capture

the delay change caused by the power voltage change. This is because the power-aware IBIS model improves the capability to simulate the non-ideal power effect by considering the gate modulation effect, not the delay change effect. The K_u and K_d are modified as $K_{sspu}(V_{pu})K_u$ and $K_{sspd}(V_{pd})K_d$, where K_{sspu} is the modification ratio depends on V_{pu}, the voltage difference between V_{comp} and power pin. K_{sspd} is the modification ratio depends on V_{pd}, the voltage difference between V_{comp} and ground pin. Since the ratio modification is only depends on the instantaneous power voltage value, the delay change of the buffer cannot be incorporated correctly.

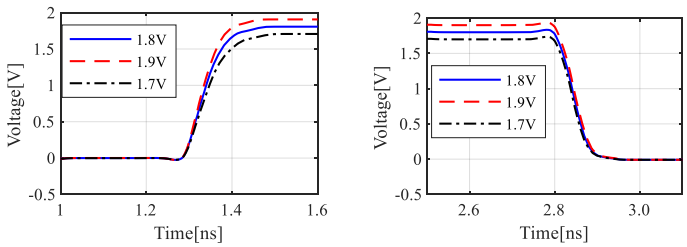


Figure 2.36 Test Case1 Power Aware IBIS Model Results.

The simulation setup for the second test case is shown in Figure 2.37(a). The sinusoidal power rail noise frequency is set to 1MHz with an amplitude of 50 mV. The initial phases are set to 0 and 90 degrees, respectively. The transistor level transient simulation results for the output rising edge are shown in Figure 2.37(b). The simulation results of the proposed new IBIS model are shown in Figure 2.37(c). The proposed model can obtain very similar results as the transistor level circuit model. The simulated time averaged power rail noise of the proposed new IBIS model is plotted in Figure 2.37(d). For the initial phase of 0 degree case, the time averaged power rail noise voltage is close

to zero. As a result, the rising edge waveform is very similar to the no power noise case. For the initial phase of 90 degree case, the time averaged power rail noise voltage is close to 50 mV and the time of output switching event will be moved forward.

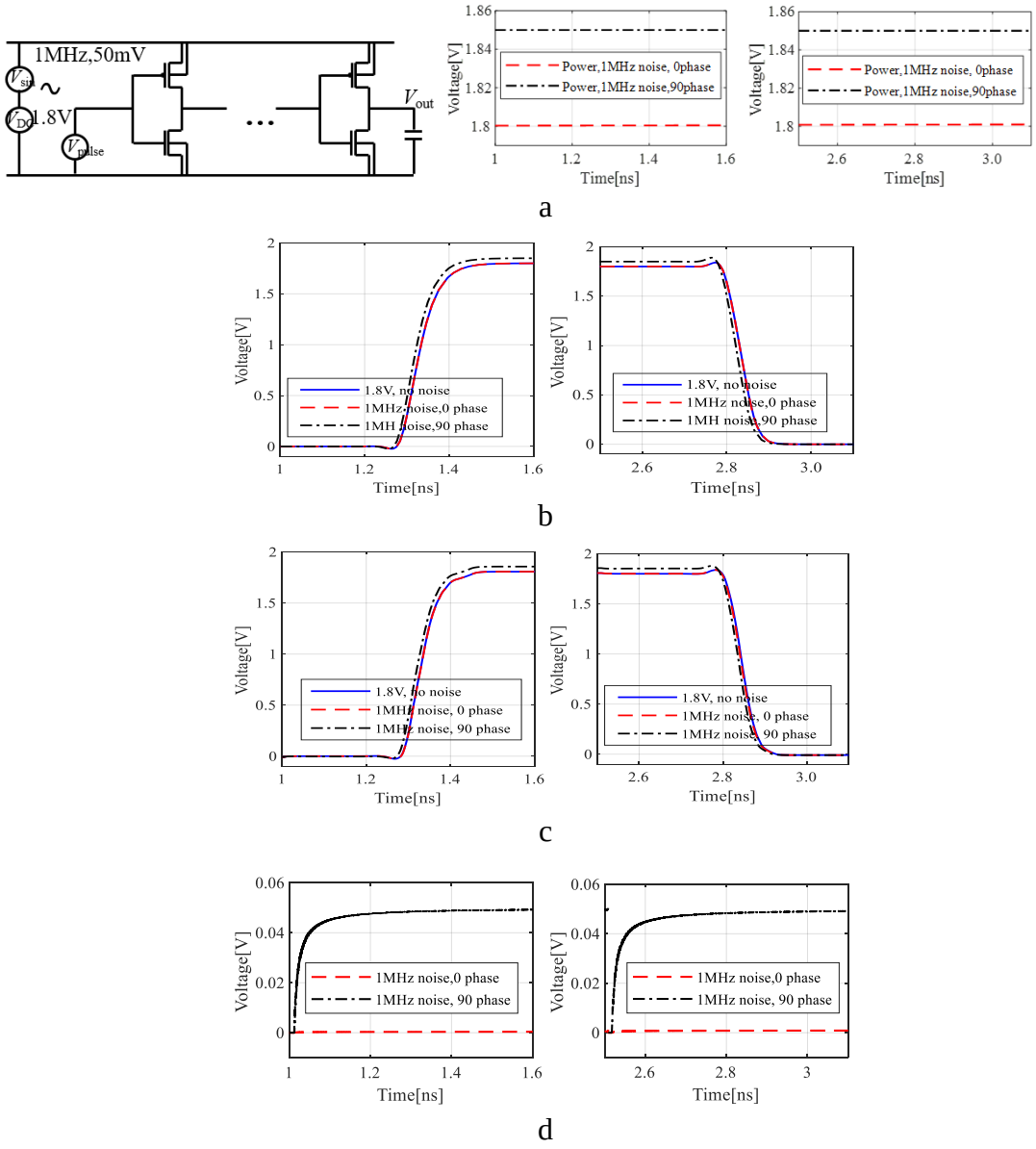
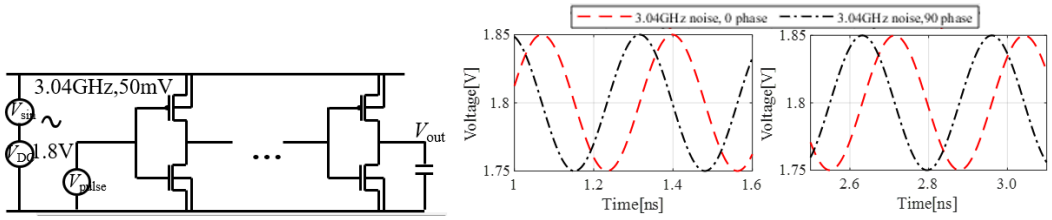
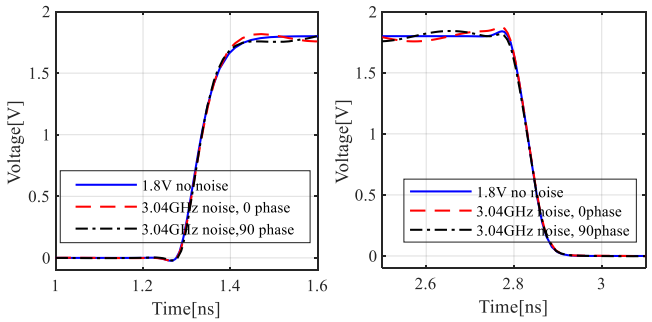


Figure 2.37 Test Case2. a) Simulation Setup. b) Hspice Output Results ;(C) Proposed Model Output Results; (D) Proposed Model Time Averaged Power Noise Results.

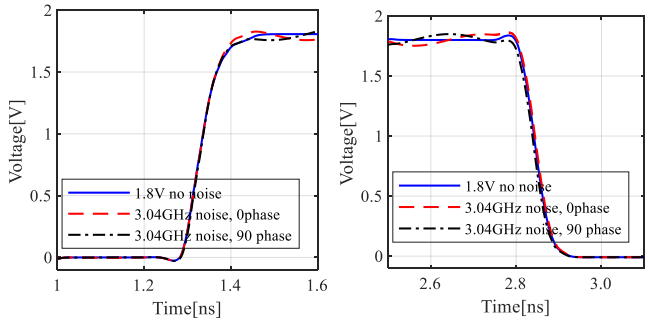
The simulation setup for the third test case is the same as in Figure 2.38(a). The sinusoidal power rail noise frequency is set to 3.04GHz, which has the same period as the propagation delay 329ps. The initial phases are set to 0 and 90 degrees, respectively. The transistor level transient simulation results for the output rising edge are plotted in Figure 2.38(b). The simulation results of the proposed new IBIS model are plotted in Figure 2.38(c). The proposed model shows good correlation with the transistor level circuit model. For this noise frequency, regardless of the initial phase of the power noise, the rising edge location will not change. The simulated time averaged power rail noise of the proposed new IBIS model is plotted in Figure 2.38(d). At 329ps after the input switching happens, the averaged power noise voltage is zero for both the cases.



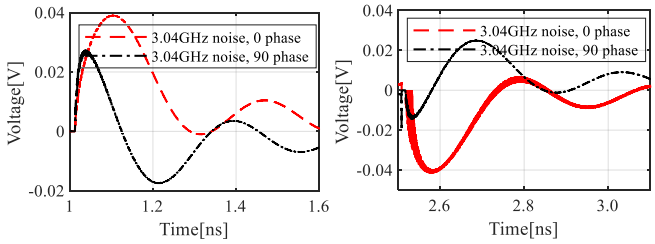
a



b



c



d

Figure 2.38 Test Case3. a) Simulation Setup. b) HSPICE Output Results. c) Proposed Model Output Results. d) Proposed Model Time Averaged Power Noise Results.

3. JITTER-AWARE TARGET IMPEDANCE

3.1. IMPROVED TARGET IMPEDANCE CONCEPT WITH JITTER SPECIFICATION

To assure the performance of high speed buffers, the PDN of the system should be carefully designed [25-35]. Traditionally, the target impedance concept is used to guide the PDN design. In this case, the maximum allowable jitter is used as the design criteria. One of the main intentions to limit the maximum allowable supply voltage fluctuation is to reduce the high speed buffer PSIJ, it will be more informative and straightforward to correlate the PSIJ with PDN design.

3.1.1. Target Impedance with Jitter Specification. To link the target impedance definition with the jitter specification, the jitter and PDN R-L-C parameters relationship should be derived. The time domain voltage ripple to jitter transfer relationship is one of the most critical steps for the derivation. The time domain voltage ripple to PDN parameters relationship is then applied to further link the jitter with PDN R-L-C parameters. Analytical expressions can be derived to associate time domain jitter with PDN R-L-C parameters. Based on these analytical formulations, many groups of PDN R-L-C values can be determined where the jitter specification is satisfied. Each set of these R-L-C values corresponds to a target impedance curve. As long as the designed PDN impedance is lower than either one of these target impedance curves, the jitter requirement can be met.

3.1.1.1. Time domain supply voltage ripple to jitter transfer relationship analytical expressions. Jitter is defined as the peak-to-peak value of the time interval error (TIE) of a signal [2]. To estimate the jitter caused by supply voltage fluctuation, the

continuously-defined time interval error (CTIE) concept is introduced as an alternative to TIE, since CTIE can be analytically calculated [20]. It is applied to describe the time difference between the ideal and the actual edges at any arbitrary switching time as illustrated in Figure 3.1. The TIE can be regarded as a sampled version of CTIE, as the input edge cannot switch continuously in time in a real case. The total time domain jitter can then be estimated by the peak-to-peak value of the CTIE. If there is no fixed phase relationship between the CTIE and the input switching event, it will cover all the possible TIE values indicated by the CTIE curve, as long as the input is switching for long enough time. Thus, the jitter can be derived from the peak-to-peak value of the CTIE.

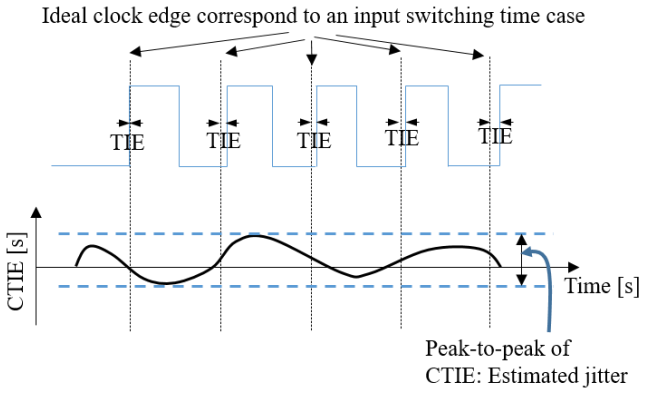


Figure 3.1 CTIE and Jitter Definition.

The PSIJ sensitivity transfer function is usually adopted to describe the transfer relationship from the power voltage noise to jitter. The PSIJ sensitivity value at a specific frequency point describes how much output jitter will be introduced by unit amplitude sinusoidal power noise as illustrated in Figure 3.2. The power rail voltage $V_{dd}(t)$ is fluctuating with amplitude of V_{n0} and has a DC offset level V_{dd0}. The buffer can switch at

any arbitrary time and t_d represents an arbitrary timing offset between the supply voltage fluctuation and buffer switching. The propagation delay between the input signal $V_{in}(t)$ and the output signal $V_{out}(t)$ will vary according to the voltage ripple level at the time of switching. The gray areas indicate the actual propagation delay for each transition, while the dashed vertical lines indicate the ideal output edges. At each arbitrary switching time, the TIE can be evaluated as the time difference between the ideal and actual output edges. The resulting CTIE will also be a single tone signal with the same frequency as the voltage ripple. The jitter caused by the single tone supply voltage ripple is the peak-to-peak value of the corresponding CTIE. By sweeping the sinusoidal wave frequency in the interested frequency range, the PSIJ transfer function can be constructed. Considering the effect of real power supply noise, the frequency domain PSIJ components can be expressed as:

$$PSIJ(f) = \Delta v(f) \cdot PSIJ\_sensitivity(f) \tag{21}$$

where $\Delta v(f)$ is the power rail switching noise in the frequency domain and PSIJ_sensitivity (f) is the power supply noise to jitter transfer function of a specific circuit. In order to obtain total jitter in time domain, the CTIE can be calculated from the convolution of the time domain voltage ripple $\Delta v(t)$ and the time domain supply voltage noise to jitter transfer relationship PSIJ_sensitivity (t) as written in:

$$CTIE\_PSIJ(t) = \Delta v(t) * PSIJ\_sensitivity(t) \tag{22}$$

To summarize, the time domain correspondence of the frequency domain total PSIJ is CTIE. The time domain voltage ripple is easy to understand. The time domain correspondence of the frequency domain PSIJ sensitivity will be discussed in the following content.

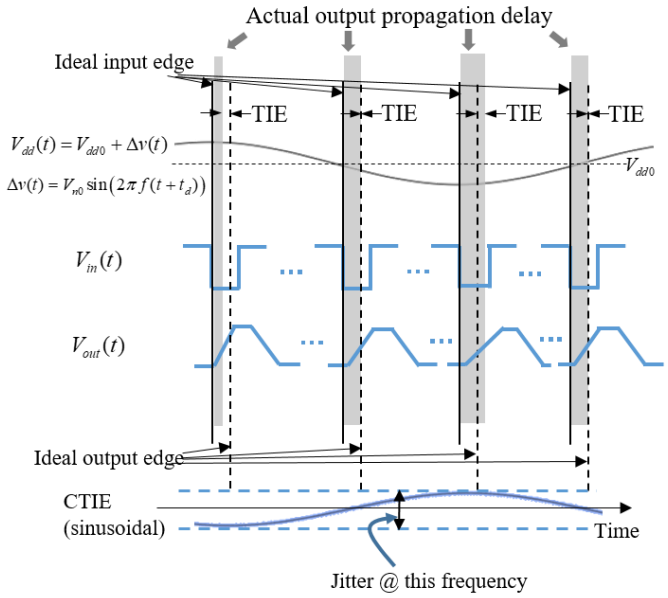


Figure 3.2 Single Tone Power Supply Noise and Resulted CTIE.

For a typical CMOS buffer, either a single stage inverter or an inverter chain, the PSIJ sensitivity transfer function will exhibit in the form of a sinc function [2-4] as expressed in:

$$PSIJ\_sensitivity(f) = \frac{T_{p\max DC} - T_{p\min DC}}{VDD_{\max} - VDD_{\min}} \operatorname{sinc}\left(f \frac{T_{p\max DC} + T_{p\min DC}}{2} \right) \qquad (23)$$

provided that the input rise/fall time is much faster than output rise/fall time. The transfer function is related to the maximum and minimum propagation delay of the buffer (T_{pmaxDC} and T_{pminDC}), as well as the corresponding minimum and maximum DC power voltage (VDD_{max} and VDD_{min}). The deviation magnitudes V_{n0} of VDD_{max} and VDD_{min} to the nominal power voltage V_{dd0} are assumed to be the same.

The inverse Fourier transform of a sinc function is a rectangular pulse as shown in Figure 3.3. If the height of a rectangular pulse $y(t)$ is A_{mag} and the width of the pulse is τ,

then the corresponding frequency domain expression $Y(2\pi f)$ will be $A_{mag}\cdot\tau\cdot \mathrm{sinc}(f\cdot\tau)$. Comparing the expression with (23), it can be observed that $(T_{pmaxDC}-T_{pminDC})/(VDD_{max}-VDD_{min})$ is equal to $A_{mag}\cdot\tau$ and that $(T_{pmaxDC}+T_{pminDC})/2$ is equal to τ. Thus, the time domain voltage ripple to jitter transfer relationship can be expressed as:

$$PSIJ\_sensitivity(t)=\begin{cases}\dfrac{2\left(T_{p\max DC}-T_{p\min DC}\right)}{\left(T_{p\max DC}+T_{p\min DC}\right)\left(VDD_{\max}-VDD_{\min}\right)} & 0\le t\le\dfrac{T_{p\max DC}+T_{p\min DC}}{2}\\ 0 & others\end{cases} \tag{24}$$

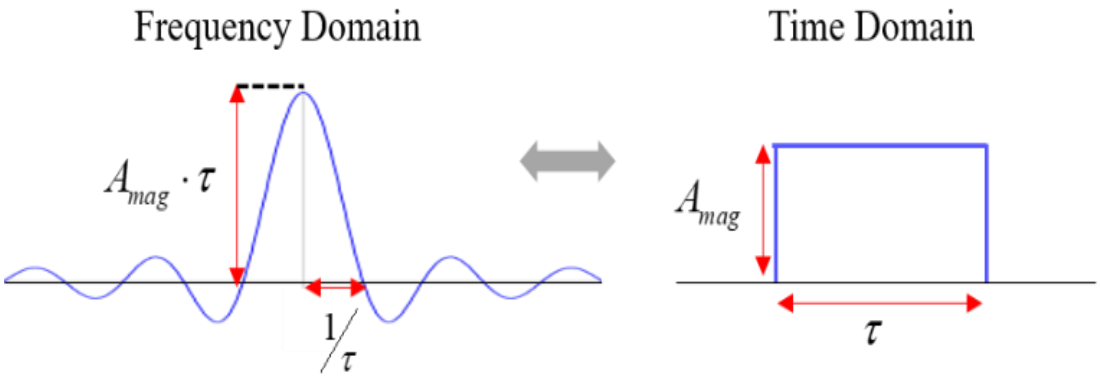


Figure 3.3 Frequency Domain PSIJ Transfer Function vs. Time Domain PSIJ Transfer Relationship.

The pulse width of the PSIJ_sensitivity(t) is determined by the averaged propagation delay $(T_{pmaxDC}+T_{pminDC})/2$. Assuming V_{n0} is much smaller than half of V_{dd0}, the pulse width is roughly the propagation delay of the CMOS buffer with the ideal power rail voltage. The pulse height is determined by the propagation delay variation to DC supply voltage variation ratio and the averaged propagation delay.

The PSIJ_sensitivity(t) can be regarded as the impulse response of a system where the power rail voltage is the system input and the CTIE is the system output as illustrated in Figure 3.4. To demonstrate this impulse response concept, assume an impulse noise voltage is added to the ideal power voltage V_{dd0} and the buffer output is switching from low to high. To evaluate the corresponding CTIE, it is assumed that the buffer can switch at any arbitrary time where t_d denotes an arbitrary timing offset between the impulse noise and buffer switching edge. For an output low-to-high transition, the delay of the transition will be affected by the power rail noise mainly in the time range where the output is rising from the initial voltage to half of V_{dd0} [20]. This time range is the circuit output propagation delay, assuming input falling time is negligible. If the impulse noise voltage appears during the output transition and is in the time scope of propagation delay, the delay of output transition will change. As shown in the illustration, the gray areas denote the range of actual propagation delay, while the dashed vertical lines indicate the ideal output edges. At each arbitrary switching time, the TIE can be evaluated as the time difference between the ideal and actual output edges. The amount of propagation delay change is determined by $2(T_{pmaxDC} - T_{pminDC})/ (VDD_{max} - VDD_{min})/ (T_{pmaxDC} + T_{pminDC})$, which is related to the intrinsic jitter sensitivity of the circuit and the propagation delay.

Conceptually, the CTIE curve induced by this impulse noise voltage is the time domain voltage ripple to jitter transfer function PSIJ_sensitivity(t). It can be summarized that the pulse width of the PSIJ_sensitivity(t) is the propagation delay, as this is the time scope where the impulse noise can take effect. The delay change caused by the impulse noise in the propagation delay time range is a constant value as indicated before and is determined by the circuit's intrinsic jitter sensitivity.

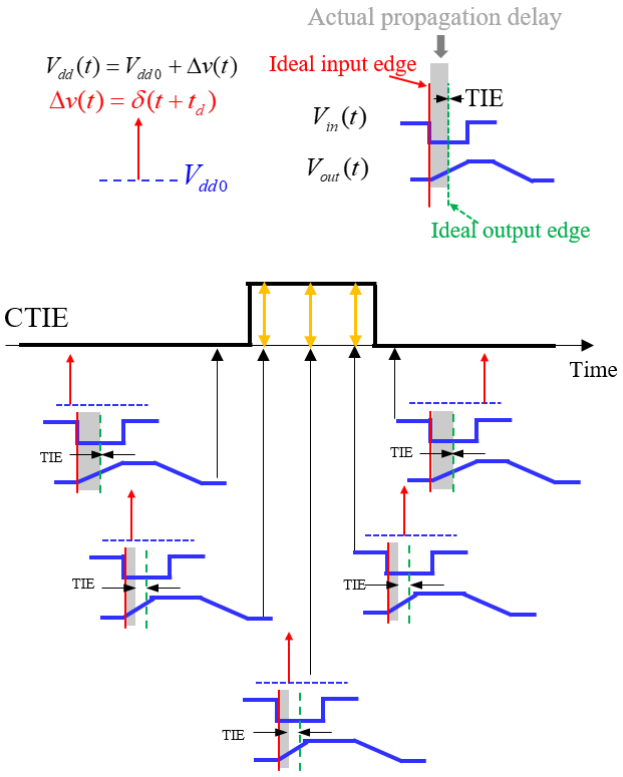


Figure 3.4 Interpretation of Time Domain PSIJ Transfer Relationship as System Impulse Response.

As shown previously, starting from the delay based PSIJ transfer function, the time domain supply voltage ripple to jitter transfer relationship can be derived analytically. The CTIE can then be calculated from (22). This procedure can be applied for either a single stage inverter or an inverter chain, as long as T_{pmaxDC}, T_{pminDC}, VDD_{max} and VDD_{min} are obtained. The CTIE can also be derived directly in time domain by analyzing the output switching edge voltage variation and time variation relationship as illustrated in [3]. The CTIE can be estimated as

$$CTIE\_PSIJ(t) = \frac{\Delta V_{out\_n}(t_{pLH0})}{Slope} \tag{25}$$

where $\Delta V_{out\_n}(t)$ is the variation of the buffer output noise $V_{out\_n}(t)$ and is superimposed on the nominal output $V_{out\_0}(t)$ under ideal power bias and t_{pLH0} represents the nominal propagation delay with ideal bias. Parameter "Slope" is defined as:

$$Slope = \left.\frac{dV_{out\_0}(t)}{dt}\right|_{t=t_{pLH0}} \tag{26}$$

If the supply voltage ripple to output voltage variation transfer relationship can be derived, the time domain voltage ripple to jitter transfer relationship can then be obtained. For a single stage inverter, the voltage ripple to output voltage transfer relationship can be derived analytically, assuming that the single stage buffer is an R-C network [3]. For the inverter chain, there are no simple analytical expressions [7] to describe the supply voltage ripple to output voltage variation transfer relationship. Therefore, this method is only demonstrated for the single stage buffer.

The low-to-high transition for a single stage inverter is demonstrated as the ground is assumed to be ideal [3]. During the transition, the pMOS can be modeled as a resistor *R*, which relates to pMOS turn on resistance, and the load can be modeled as a capacitor *C*. The total supply power voltage is written as:

$$V_{dd}(t) = V_{dd0} + \Delta v(t) \tag{27}$$

The drain current flowing through the pMOS should be equal to the drain current charging the capacitor. This relationship is described by a differential equation

$$C\frac{dV_{out}(t)}{dt} = \frac{V_{dd}(t) - V_{out}(t)}{R} \tag{28}$$

where $V_{out}(t)$ is the output voltage. From the large signal response of (8), the nominal propagation delay is solved as:

$$t_{pLH0} = -RC\ln 0.5 = 0.69RC \tag{29}$$

Parameter "Slope" is then obtained as:

$$Slope = \frac{0.5V_{dd0}}{RC} \tag{30}$$

The small signal response $V_{out\_n}(t)$ is the output voltage noise solved from (8) with the voltage ripple $\Delta v(t)$ as the input. From (25) and (28), the supply voltage ripple to jitter transfer relationship can be derived. It can be noted that if the supply voltage ripple $\Delta v(t)$ is a unit amplitude single frequency sinusoidal wave, then the obtained CTIE from (25) and (28) can be written as a function of frequency as demonstrated in [2]. By sweeping the sinusoidal wave noise frequency, the PSIJ sensitivity transfer function can be constructed. The resulting PSIJ sensitivity from this method is also in the form of a sinc function, which is consistent with the previous propagation-delay based PSIJ sensitivity derivation.

3.1.1.2. Time domain voltage ripple analytical expressions. The typical behavioral model of a PDN is a cascaded R-L-C circuit [35-45], as depicted in Figure 3.5(a). Between the IC and the decoupling capacitors is a series of equivalent inductances and resistances. The inductances mainly correspond to the interconnections, board equivalent inductances and the equivalent series inductance (ESL) of the capacitor package. The resistances mainly come from the IC pin/package contact resistance, interconnections, and the equivalent series resistance (ESR) of the capacitor package. The voltage regulator module (VRM) located at the end of the PDN serves as the ultimate power supply for the IC. The VRM is modeled as an ideal DC power source in series with a resistance and an inductance.

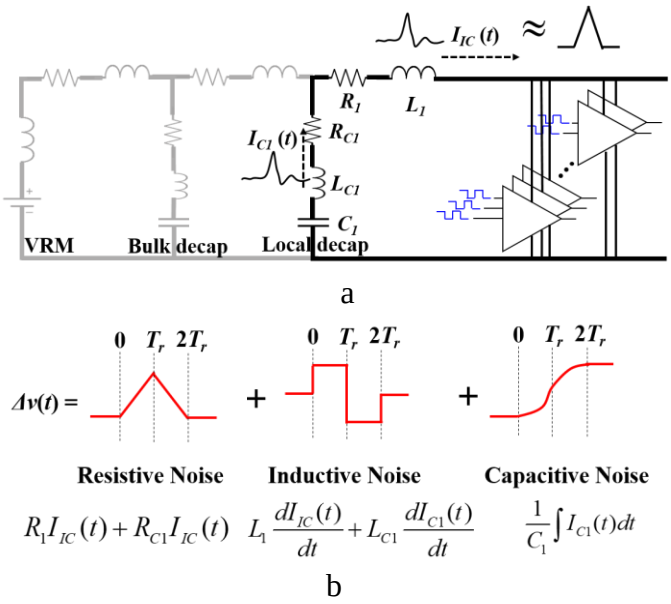


Figure 3.5 PDB Model and Time Domain Voltage Ripple. a) Typical PDN Model with Fast Rise Time Current Pulse. b) Voltage Ripple Components with Fast Rise Time Current Pulse.

The analytical expressions for time domain voltage ripple can be derived by assuming a triangular shaped IC noise switching current [46]. This is generally true for most practical cases [47]. The triangular current pulse can be written as:

$$I_{IC}(t) = \frac{I_p}{T_r}(tu(t) - 2(t - T_r)u(t - T_r) + (t - 2T_r)u(t - 2T_r)) \qquad (31)$$

where I_p is the pulse peak value, T_r is the pulse rise time and $u(t)$ is the step function.

In this study, it is assumed that the rise time of the IC switching current $I_{IC}(t)$ is relatively short and that the charge required can be predominantly provided through the local decoupling capacitor branch. This is one of the most practical operating conditions to be considered [18]. Based on the assumption, the IC switching noise current can be approximated with the high frequency current passing through the local decoupling capacitor $I_{C1}(t)$.

The supply voltage ripple in the aforementioned case is analytically derived as expressed in (32),

$$\begin{aligned}\Delta v(t) &= \left(R_1 I_{IC}(t) + R_{C1} I_{IC}(t)\right) + \left(L_1 \frac{dI_{IC}(t)}{dt} + L_{C1} \frac{dI_{C1}(t)}{dt}\right) \\ &+ \left(\frac{1}{C_1}\int I_{C1}(t)dt\right) \\ &= \frac{I_p}{T_r}(R_1 + R_{C1}) \times \begin{pmatrix} tu(t) - 2(t-T_r)u(t-T_r) \\ +(t-2T_r)u(t-2T_r) \end{pmatrix} \\ &+ \frac{I_p}{T_r}\left(L_1 + L_{C1}\right)\left(u(t) - 2u(t-T_r) + u(t-2T_r)\right) \\ &+ \frac{I_p}{T_r}\frac{1}{2C_1}\begin{pmatrix} t^2u(t) - 2(t-T_r)^2u(t-T_r) \\ +(t-2T_r)^2u(t-2T_r) \end{pmatrix}\end{aligned} \tag{32}$$

as illustrated in [46], where R_1 is the equivalent resistance between the IC and local decoupling capacitor, L_1 is the equivalent inductance between the IC and local decoupling capacitor, R_{C1} is the ESR of the local decoupling capacitor package, L_{C1} is the ESL of the local decoupling package, and C_1 is the local decoupling capacitor. The step function in (32) serves as a switch that remains off until the specified time point has been reached. It is irrelevant during the derivative and integral calculation process.

The three terms on the right-hand side correspond to the noise voltage introduced by the parasitic resistance, parasitic inductance and the capacitor respectively. The shapes of each voltage ripple components are summarized in Figure 3.5(b). The resistive noise voltage is proportional to the triangular current pulse. The inductive noise voltage is in a shape of the derivative of the triangular pulse. The capacitive noise voltage carries the shape of the integration of the triangular pulse.

3.1.1.3. Correlate time domain jitter with PDN R-L-C parameters. By combining the time domain supply voltage ripple to jitter transfer relationship and the time domain voltage ripple analytical expressions, the total time domain jitter can be explicitly correlated with the PDN R-L-C parameters directly.

Considering the simplified PDN model presented in Figure 3.5(a), the local decoupling capacitor is assumed to be large enough to supply the high-frequency switching current; therefore, its contribution to the voltage fluctuation is negligible. In other word, the resonance peak corresponding to the local decoupling branch as illustrated in [46] is assumed to be low enough and the frequency range of interest is mainly at the PDN resistive and inductive region. This assumption is true for most practical designs [17], [18]. In this work, only the contribution from the resistive and inductive parts are considered.

From the propagation delay based PSIJ transfer function, the CTIE can be calculated from (22) as:

$$CTIE\_PSIJ(t) = \int_{-\infty}^{+\infty} \Delta v(\tau) \cdot PSIJ\_sensitivity(t-\tau) d\tau \tag{33}$$

The convolution process for the resistive and inductive parts is illustrated in Figure 3.6. It is assumed that the noise IC current is generated by an aggressor circuit that exhibits longer propagation delay than the victim buffer. Thus, the rise time of the noise IC current is assumed to be longer than the victim buffer propagation delay [47].

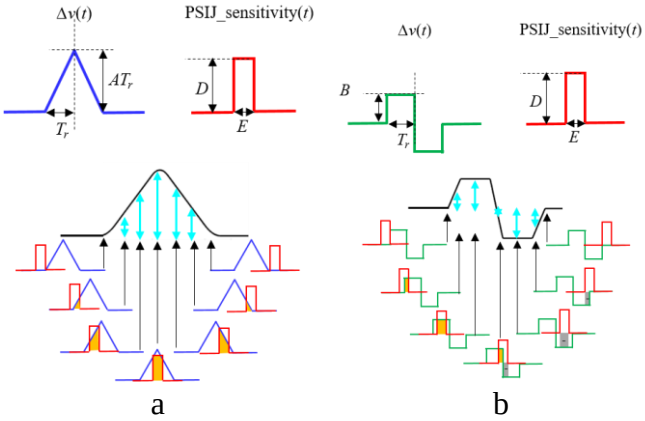


Figure 3.6 Convolution Process Illustration. a) Resistive Noise Convolution. b) Inductive Noise Convolution.

The CTIE contributed by the resistive part is expressed as:

$$CTIE\_PSIJ_R(t)=\begin{cases} AD\dfrac{t^2}{2} & 0\le t\le E<T_r \\ AD\dfrac{t^2-(t-E)^2}{2} & E\le t<T_r \\ AD\dfrac{T_r{}^2-(t-E)^2}{2} & \\ +AD[-\dfrac{t^2-T_r{}^2}{2}+2T_r(t-T_r)] & T_r\le t<T_r+E \\ AD[-\dfrac{t^2-(t-E)^2}{2}+2T_rE] & T_r+E\le t<2T_r \\ AD[-\dfrac{4T_r{}^2-(t-E)^2}{2} & \\ +2T_r(2T_r-t+E)] & 2T_r\le t\le 2T_r+E \end{cases} \tag{34}$$

while the CTIE originating from the inductive part is written as:

$$CTIE\_PSIJ_L(t)=\begin{cases} BDt & 0\le t\le E<T_r \\ BDE & E\le t<T_r \\ BD(2T_r-2t+E) & T_r\le t<T_r+E \\ -BDE & T_r+E\le t<2T_r \\ -BD(2T_r-2t+E) & 2T_r\le t\le 2T_r+E \end{cases} \tag{35}$$

The total CTIE is the sum of the two parts as:

$$CTIE\_PSIJ(t) = CTLE\_PSIJ_R(t) + CTLE\_PSIJ_L(t) \tag{36}$$

where $A = I_p(R_1+R_{C1})/T_r$, $B = I_p(L_1+L_{C1})/T_r$, $E = (T_{pmaxDC}+T_{pminDC})/2$, and $D = (T_{pmaxDC}-T_{pminDC})/(VDD_{max}-VDD_{min})/E$.

There are many R_{PDN} and L_{PDN} combinations that will result in different CTIE curves. The total CTIE under four different R_{PDN} and L_{PDN} combinations is plotted in Figure 3.7. Two extreme cases are demonstrated where there is only resistive part or only inductive part. A case where the inductive part presents but the resistive part dominates is also presented. The other case corresponds to the situation where the resistive part presents but the inductive part dominates.

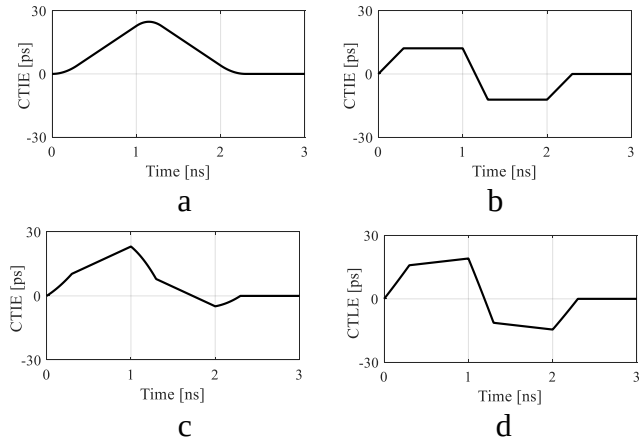


Figure 3.7 CTIE Curve Shape Calculated Using PSIJ Sensitivity Convolution with Different PDN R_{PDN} and L_{PDN} Combinations. a) Pure Resistive. b) Pure Inductive. c) Resistive Dominant ($R_{PDN} > L_{PDN}/T_r$). d) Inductive Dominant ($R_{PDN} < L_{PDN}/T_r$).

To obtain the total jitter, the peak-to-peak value of the CTIE curve should be determined. The starting time of the triangular switching current is set to zero. For the pure resistive case, the maximum CTIE occurs at $T_r+E/2$, which is solved for by setting

the derivative of (34) to zero, since the minimum CTIE happens when time equals zero. For the pure inductive case, the maximum CTIE occurs at T_r and the minimum CTIE occurs at $2T_r$. For simplicity, the peak-to-peak difference of the total CTIE is estimated to be between either CTIE (T_r+E/2) and CTIE (0) or CTIE (T_r) and CTIE ($2T_r$), As a result, the total jitter can be estimated with

$$\begin{aligned} Total\_jitter &\approx \max\left(\begin{matrix}\left|CTIE\_PSIJ(T_r)-CTIE\_PSIJ(2T_r)\right| \\ ,\left|CTIE\_PSIJ(T_r+E/2)-CTIE\_PSIJ(0)\right|\end{matrix}\right) \\ &= \max\left(\left|AD\left(T_rE-E^2\right)+2BDE\right|,\left|AD\left(T_rE-\frac{E^2}{4}\right)\right|\right) \end{aligned} \tag{37}$$

where parameter A and B are correlated with PDN resistance and inductance, respectively.

With this analytical equation, given a jitter specification, many combinations of R_{PDN} and L_{PDN} that will result in the same maximum allowable jitter can be determined. Each of these R_{PDN} and L_{PDN} values can correspond to a target impedance curve. As long as the designed PDN impedance is lower than either one of these target impedance curve, the jitter requirement can be satisfied.

The PSIJ_sensitivity (t) convolution method is suitable for the single stage buffer as well as the buffer chain. From (25), the CTIE of a single stage buffer can be alternatively derived. The small signal response is derived from (28) with the power supply ripple as an input. As mentioned previously, the supply voltage fluctuation can be separated into three components: resistive noise, inductive noise, and capacitive noise, as shown in (22). Correspondingly, the buffer output voltage perturbation $V_{out\_n}(t)$ can also be derived as the sum of three components as:

$$V_{out\_n}(t) = y_1(t) + y_2(t) + y_3(t) \tag{38}$$

where $y_1(t)$ is the small signal response from resistive noise, $y_2(t)$ is the small signal response from inductive noise and $y_3(t)$ is the small signal response from capacitive noise. Similarly, assuming the local decoupling capacitor is large enough to supply the high-frequency switching current, only the resulting noise from the resistive and inductive parts are relevant.

The resistive part in the small signal response of the output voltage is derived as [3]

$$y_1(t) = A\begin{bmatrix} (t + RC(-1 + e^{-t/RC})) \\ -2u(t - T_r)(t - T_r + RC(-1 + e^{-(t-T_r)/RC})) \\ +u(t - 2T_r)(t - 2T_r + RC(-1 + e^{-(t-2T_r)/RC})) \end{bmatrix} \tag{39}$$

where $A=I_p (R_1+R_{C1}) /T_r$. The small signal response of the inductive part is written as:

$$y_2(t) = B\begin{bmatrix} (1 - e^{-t/RC}) - 2u(t - T_r)(1 - e^{-(t-T_r)/RC})) \\ +u(t - 2T_r)(1 - e^{-(t-2T_r)/RC}) \end{bmatrix} \tag{40}$$

where $B=I_p (L_1+L_{C1}) /T_r$.

To obtain the CTIE, the input is assumed to switch at any arbitrary time, thus, the noise variation at the nominal propagation delay time $\Delta V_{out\_n}(t_{pLH0})$ can be estimated to be equal to the total small signal response $V_{out\_n}(t)$. Inserting expressions of $\Delta V_{out\_n}(t_{pLH0})$ into (5), the CTIE of the single stage inverter can be alternatively derived as:

$$\begin{aligned} CTIE\_PSIJ(t) = {} & A\begin{bmatrix} (t + RC(-1 + e^{-t/RC})) \\ -2u(t - T_r)(t - T_r + RC(-1 + e^{-(t-T_r)/RC})) \\ +u(t - 2T_r)(t - 2T_r + RC(-1 + e^{-(t-2T_r)/RC})) \end{bmatrix} \frac{RC}{0.5V_{dd0}} \\ & + B\begin{bmatrix} (1 - e^{-t/RC}) - 2u(t - T_r)(1 - e^{-(t-T_r)/RC})) \\ +u(t - 2T_r)(1 - e^{-(t-2T_r)/RC}) \end{bmatrix} \frac{RC}{0.5V_{dd0}} \end{aligned} \tag{41}$$

The total CTIE is the sum of the CTIE resulting from the resistive and inductive parts as shown on the right hand side of (41). Similarly, the total CTIE under four different R_{PDN} and L_{PDN} combinations are plotted in Figure 3.8. The CTIE curve shape is very similar to the previously derived results using the propagation delay based PSIJ transfer relationship. Since the CTIE curve is calculated with the R-C network model, the resulting curves are smoother. To obtain the total jitter, the peak-to-peak value of the CTIE curve should be determined. The starting time of the triangular switching current is set to zero. For the pure resistive case, the maximum CTIE occurs at – RC*ln(1/(2exp(T_r/RC)-1)), which is solved for by setting the derivative of the second term in (21) equal to zero. Assuming that the buffer propagation delay is shorter than the rise time of the IC triangular current, the time of maximum resistive CTIE can be approximated as T_r+0.69RC/2. For the pure inductive case, the maximum CTIE still happens at T_r, and the minimum CTIE happens at 2T_r. Following the same estimation procedure as in (37), the total jitter can be estimated by

$$Total\_jitter \approx \max\left(\begin{array}{l}\left|CTIE\_PSIJ(T_r)-CTIE\_PSIJ(2T_r)\right|,\\ \left|CTIE\_PSIJ(T_r+\frac{0.69RC}{2})-CTIE\_PSIJ(0)\right|\end{array}\right)$$

$$\approx \max \frac{RC}{0.5V_{dd0}}\left(\begin{array}{l}\left|\left\{\begin{array}{l}AT_r+(2-3\exp(-T_r/RC)\\ +\exp(-2T_r/RC))(B-ARC)\end{array}\right\}\right|,\\ \left|\left\{A\left(T_r+\frac{0.69RC}{2}+RC\left(-1+\exp(-\left(T_r+\frac{0.69RC}{2}\right)/RC)\right)\right)\right\}\right|\end{array}\right) \quad (42)$$

The RC time constant for the single stage buffer can be estimated from propagation delay as RC= t_{pLH0}/0.69. Again, the jitter is correlated with PDN resistance and inductance through parameter A and B, respectively.

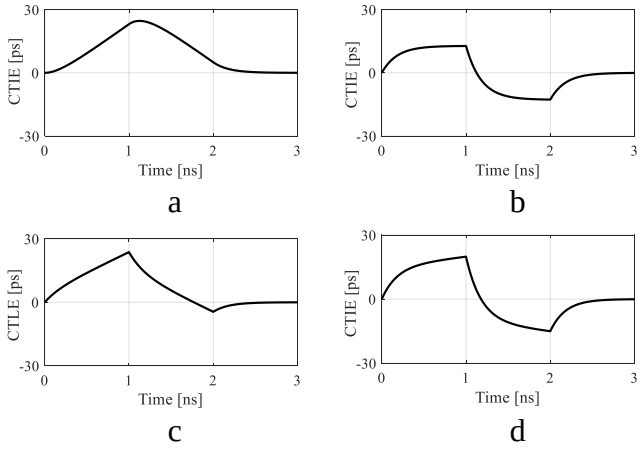


Figure 3.8 CTIE Curve Shape Calculated Using R-C Network Model with Different PDN R_{PDN} and L_{PDN} Combinations. a) Pure Resistive. b) Pure Inductive. c) Resistive Dominant ($R_{PDN} > L_{PDN}/T_r$). d) Inductive Dominant ($R_{PDN} < L_{PDN}/T_r$).

3.1.2. Validation of Target Impedance. With the time domain total jitter correlated with PDN R-L-C parameters through analytical equations, the proposed analytical formulations is firstly validated through HSPICE simulation. Then the application of the improved target impedance concept with jitter specification is demonstrated.

3.1.2.1. Simulation validation of circuit PSIJ transfer function. The jitter correlation with PDN R-L-C parameters are validated for both a single stage inverter and an inverter chain. The width and length of the applied transistors are indicated by W and L, respectively, while M is the multiplication factor. For the inverter chain, each stage has a different multiplication factor, which is increased constantly by the same factor. The two circuits are designed using the 180 nm technology SPICE library as shown in Figure 3.9 and Figure 2.4(b), with an operation voltage of 1.8 V. For the propagation delay based PSIJ transfer relationship method, the PSIJ transfer function of the two circuits are first examined through simulation and compared with the theoretical calculation results

from (23). For the single stage buffer, only the rising edge is considered as the ground is assumed to be ideal. For the buffer chain, both the rising edge and falling edge are considered, as there will always be stages influenced by the power supply noise during switching. The supply voltages, propagation delays, output loading and input signals for the PSIJ sensitivity test of the two circuits are summarized in Table 3.1. By plugging T_{pmaxDC}, T_{pminDC}, VDD_{max} and VDD_{min} into (23), the PSIJ transfer function can be calculated.

Figure 3.9 Designed Single Stage Buffer for Validation.

Table 3.1 Buffer Related Parameters.

Buffer switching edge	Single stage buffer, rising	Inverter chain, rising	Inverter chain, falling
Supply voltage (V)	VDD_{min}=1.7 VDD_{max}=1.9		
T_{pminDC} (ps)	176	274	280
T_{pmaxDC} (ps)	224	307	318
C_{load}	20 fF	10 fF	
Input	Period 3.4 ns, rise/fall time 10 ps		

The real jitter transfer function of the circuits can be obtained through HSPICE simulation. A single frequency sinusoidal wave with 50mV amplitude is imposed on the

ideal dc power supply. Then the resulting jitter at this frequency is measured. By sweeping the sinusoidal noise frequency, the PSIJ transfer function can be obtained. The calculated and simulated PSIJ sensitivity is shown in Figure 3.10. In general, it is validated that for the designed CMOS buffer, the PSIJ transfer function can be estimated as a sinc function with relative accuracy.

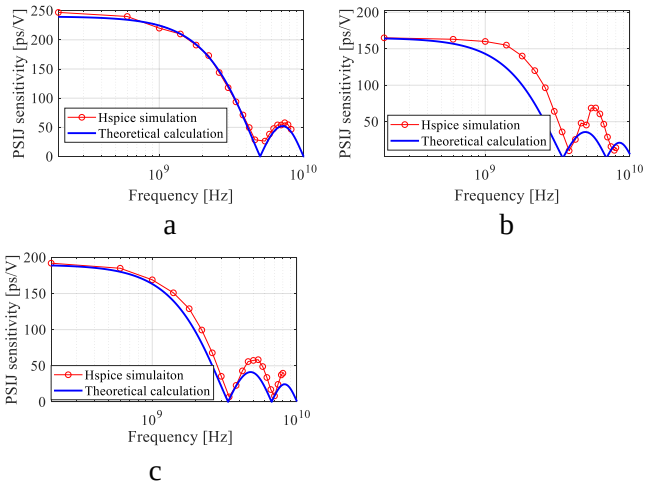


Figure 3.10 PSIJ Transfer Function HSPICE Simulation and Theoretical Calculation Comparison. a) Single Stage Buffer, Rising Edge. b) Inverter Chain, Rising Edge. c) Inverter Chain, Falling Edge.

3.1.2.2. Simulation validation of jitter correlation with PDN R-L-C parameters.

The validation simulation setup is depicted in Figure 3.11. For single stage inverter, the load capacitance is 20 fF. For the inverter chain, the load capacitance is 10 fF. A triangular current source is introduced at the on chip power point. The period of the gate input pulse was 3.4 ns with a rise/fall time of 10 ps, and the period of the IC switching current was 5.69 ns. The rise time T_r of the IC transient current was 1 ns and the peak value I_p was 80 mA.

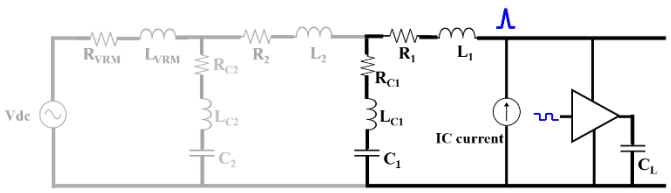


Figure 3.11 Target Impedance with Jitter Specification Validation HSPICE Simulation Setup.

Since the local decoupling branch dominant case is investigated in this work, the related parasitic inductance L_1 and parasitic resistance R_1 are swept to validate (37) and (42). Other components are set to typical values for a PDN model as R_{C1} = 0.01 Ohm, L_{C1} = 0.1 nH, C_1 = 0.08 uF, L_2 = 1 nF, R_2 = 0.01 Ohm, C_2 = 0.8 uF, R_{C2} = 0.01 Ohm, L_{C2} = 0.1 nH, R_{VRM} = 0.1 Ohm and L_{VRM} = 0.1 nH. The L_1 is swept from 0.4 nH to 2 nH with a 0.4 nH step with R_1 set to 0.01 Ohm and R_1 is swept from 0.2 Ohm to 1.4 Ohm with a 0.4 Ohm step with L_1 set to 0.8 nH. The PDN impedance curve with these different R_{PDN} and L_{PDN} combinations are plotted in Figure 3.12. The spectrum of the single IC current pulse and the periodic IC current is shown in Figure 3.13(a) and (b). For a single triangular shaped pulse, the frequency spectrum is the square of a sinc function. Looking at a short time range, the single pulse cut off frequency is higher than the self-resonance frequency for the local decap branch, indicating that the charging will predominantly go through the local decap branch and that the local decap is large enough to provide the charges without introducing obvious voltage ripple. On the other hand, considering the long time range, the periodic transient current is in the frequency range where parasitic inductance and resistance will dominant.

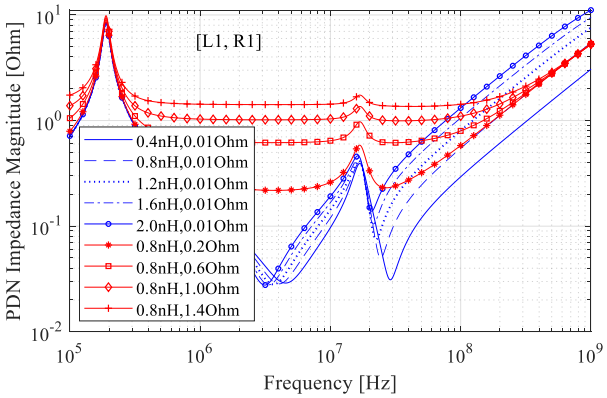


Figure 3.12 Validation Tested PDN Impedance Cases.

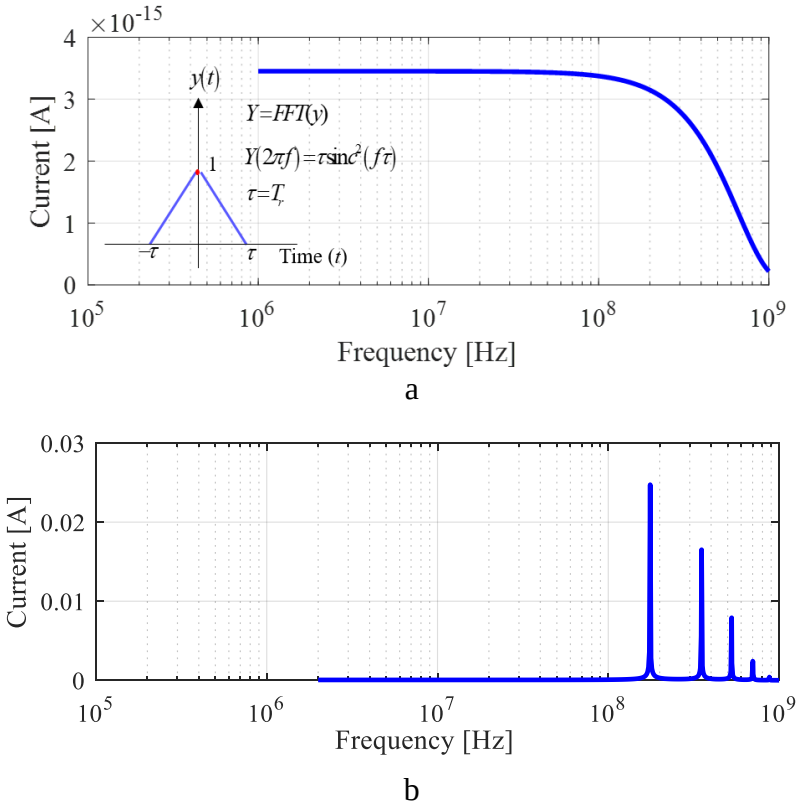
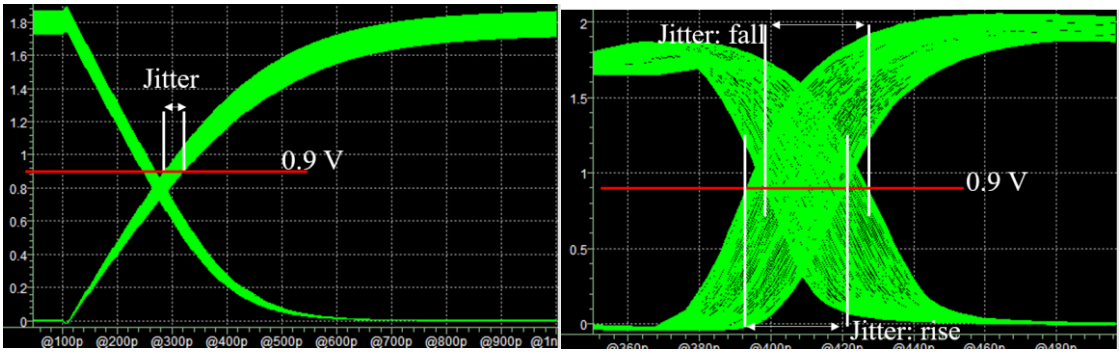


Figure 3.13 IC Current Spectrum. a) Single Current Pulse. b) Periodic Current.

For the single stage inverter and the buffer chain, multiple output transitions obtained from the simulation are overlapped together based on 1 UI length as shown in Figure 3.14(a) and (b). For both the single stage inverter and the buffer chain, the presented results correspond to the case where L_1 = 0.8 nH and R_1=0.01 Ohm. The jitter for single stage buffer rising edge and buffer chain rising/falling edge is measured at half V_{dd0}. As mentioned before, for single stage inverter, since during the output falling period, the PMOS is off, the effect of the power rail voltage to the output jitter is neglected. As a result, only the rising edge jitter of the single stage inverter is evaluated. The simulated jitter and calculated jitter with different R_1 and L_1 values are compared in Figure 3.15(a), (b) and (c) for the single stage buffer rising edge, buffer chain rising and falling edge respectively. For the single stage buffer, both of the proposed methods can evaluate the jitter reasonably close to the simulated values. For the buffer chain, (37) can also give a reasonably good match with the simulation for both the rising and falling edges.



a b

Figure 3.14 Jitter Value Reading Form Simulation. a) Single Stage Buffer, Rising Edge. b) Inverter Chain, Rising and Falling Edge.

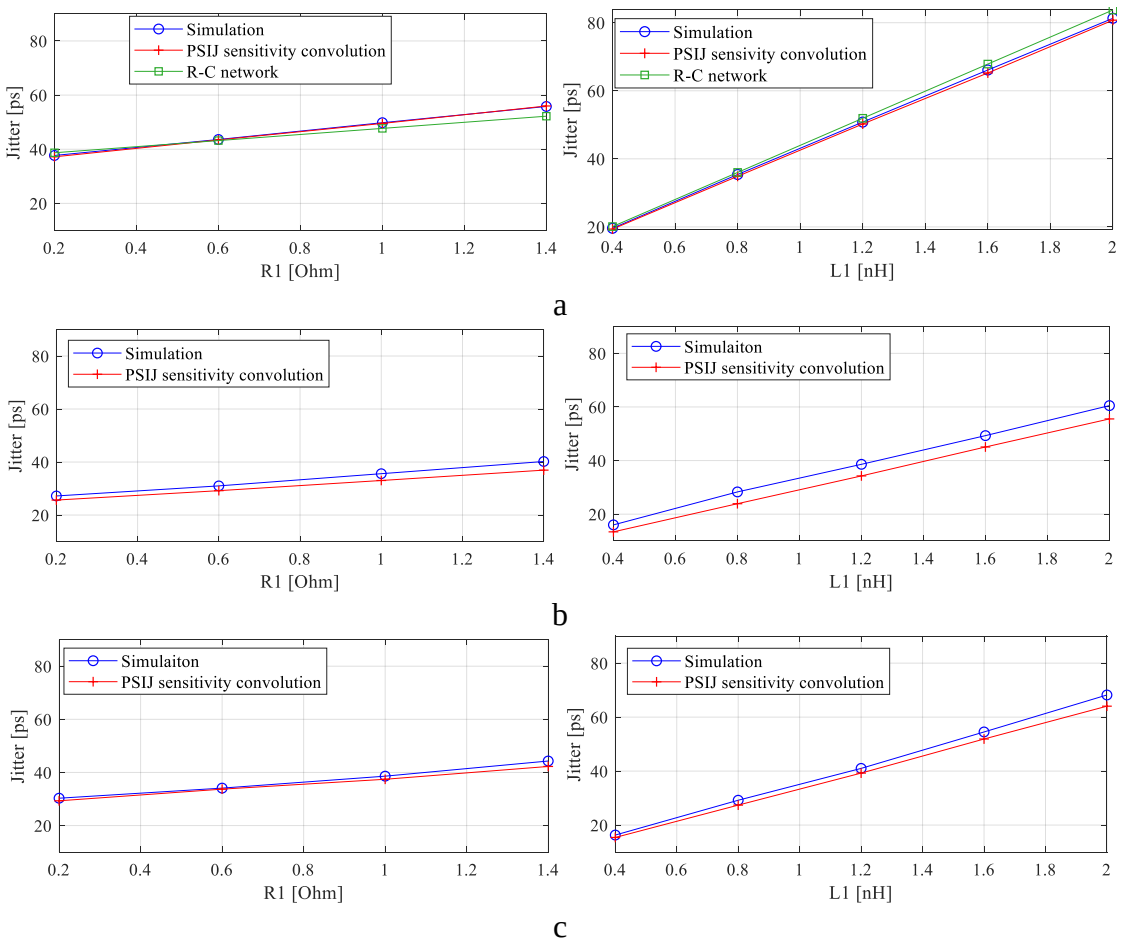


Figure 3.15 Predicted Jitter and HSPICE Simulation Comparison. a) Single Stage Buffer, Rising Edge. b) Inverter Chain, Rising Edge. c) Inverter Chain, Falling Edge.

3.1.2.3. Simulation validation of target impedance with jitter specification. It has been demonstrated that the derived analytical equation can correlate jitter with PDN R-L-C parameters reasonably well for typical CMOS buffers. The improved target impedance definition with jitter specification is demonstrated for both the single stage buffer and the buffer chain. To define the target impedance with jitter requirement, knowledge of IC current is desirable. The IC switching noise current is assumed to have a 1 ns rise time and a peak value of 80 mA. The maximum allowable jitter is set to 40 ps.

For the single stage buffer, since the estimated jitter is fairly close when using both of the proposed methods, the following demonstration is proceeded with the PSIJ transfer relationship method as it can also be applied for the buffer chain. From (37), many R_{PDN} and L_{PDN} combinations can be determined that leading to the same jitter value of 40 ps. The predicted total CTIE under four different R_{PDN} and L_{PDN} combinations are plotted in Figure 3.16. Similarly to previous examples, two extreme cases with pure resistive or pure inductive parasitic for the decap branch are displayed. The resistive and inductance dominant cases for the decap branch are also demonstrated. The total jitter, read from the peak-to-peak value of the CTIE curve, is about 40 ps for each case. The resulting jitter based on the calculated PDN R_{PDN} and L_{PDN} values are validated through simulation as shown in Figure 3.17. It can be shown that, given a jitter specification, the corresponding PDN R-L-C value can be determined.

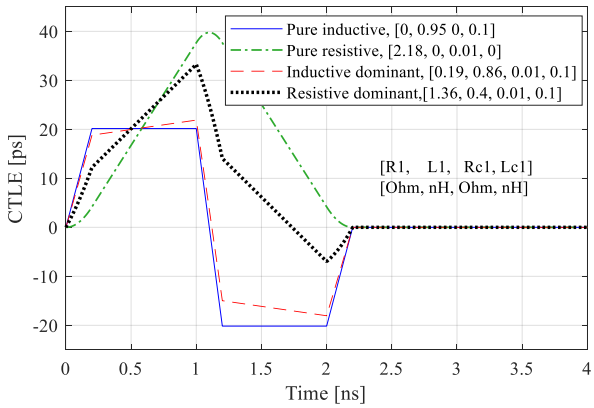


Figure 3.16 CTIE of Four Calculated Cases with the Same Peak-To-Peak Value (40 ps) for Single Stage Inverter.

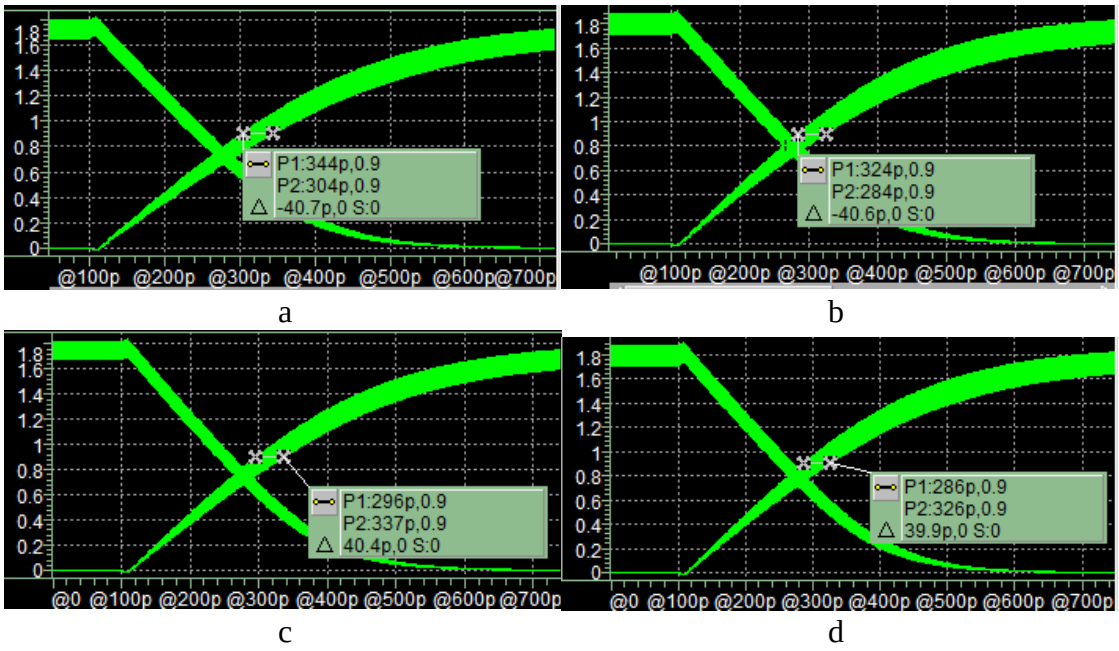


Figure 3.17 Validation of the Predicted Jitter for the Four Cases for Single Stage Inverter. a) Pure Inductive. b) Pure Resistive. c) Inductive Dominant. d) Resistive Dominant.

For these four cases, four target impedance curves corresponding to each case can be defined as shown in Figure 3.18. Since all the target impedance curves generate the same 40 ps jitter at the circuit output, as long as the actual PDN impedance looking from the IC port is lower than one of the target impedance values, the jitter requirement can be fulfilled. The extreme case where only the resistive part presents for the local decap branch puts the most constrain at higher frequency as it is constant at the higher frequency range. The other extreme case where only the inductive part presents for the local decap branch puts the least constrain for the higher frequency range. However, this may be hard to achieve at relatively low frequency ranges. The other cases provide some degree of compromise between the high and low frequency impedance constraints.

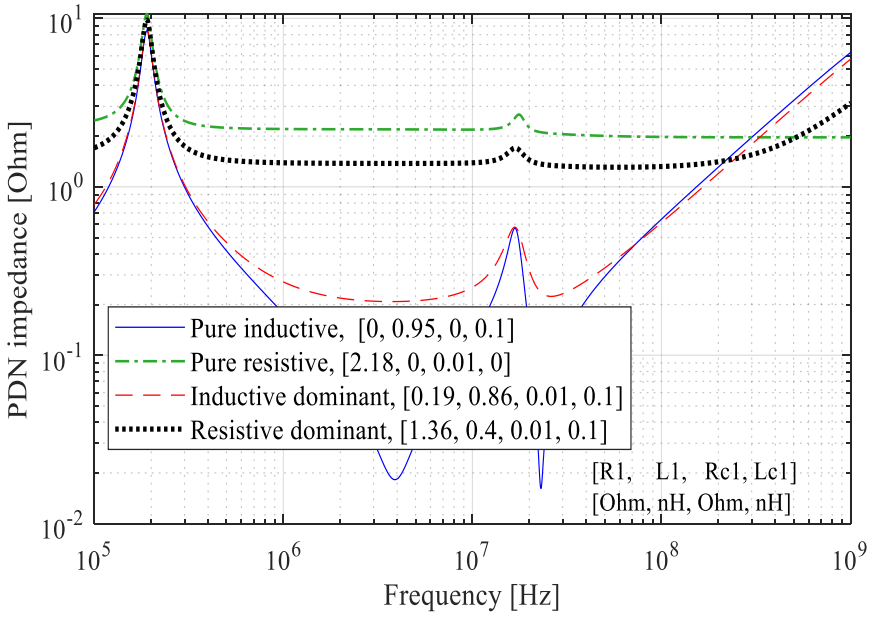


Figure 3.18 Target Impedance Defined Based on Jitter Specification Corresponds to the Four Cases for the Single Stage Buffer.

For the buffer chain, since the falling edge jitter is always slightly larger than the rising edge, as indicated in Figure 3.15(b) and (c), as long as the falling edge is smaller than the requirement the rising edge will also satisfy the specification. From (37), the predicted total CTIE under four different R_{PDN} and L_{PDN} combinations are plotted in Figure 3.19. Again, pure resistive and pure inductive cases are included as extreme boundary cases. The resistive and inductive dominant cases are also presented. Similarly, for these four cases, the total jitter read from the peak to peak value of the CTIE curve is about 40 ps. The resulting jitter values based on the calculated PDN R_{PDN} and L_{PDN} values are validated through simulation as shown in Figure 3.20. In general, even though some cases will have 1 or 2 ps error, the proposed procedure can predict the jitter fairly well and the corresponding PDN R-L-C values can be calculated.

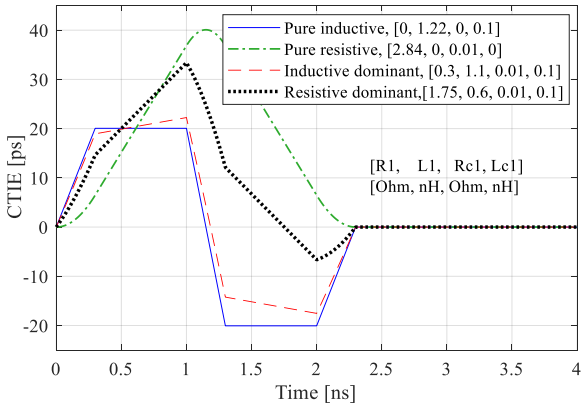


Figure 3.19 CTIE of Four Calculated Cases with the Same Peak-To-Peak Value (40 Ps) for Inverter Chain Falling Edge.

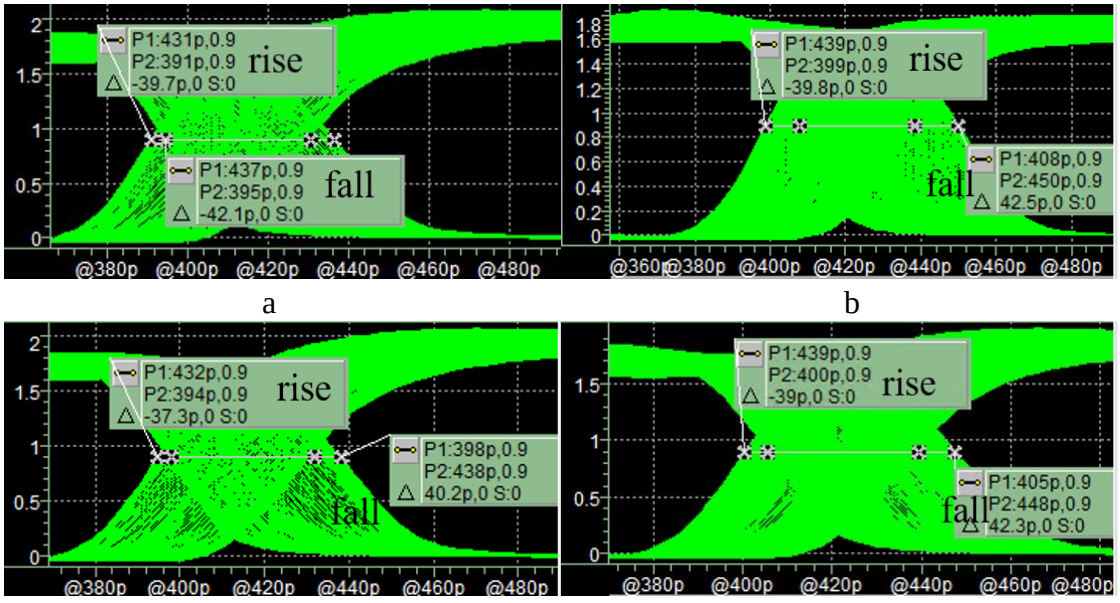


Figure 3.20 Validation of the Predicted Jitter for the Four Cases for Inverter Chain. a) Pure Inductive. b) Pure Resistive. c) Inductive Dominant. d) Resistive Dominant.

Similarly, for the inverter chain, multiple target impedance curves can be defined based on the jitter specification. The target impedance curves for the inverter chain corresponding to the previous four cases are depicted in Figure 3.21. It should also be

noted that for different circuits like the single stage inverter or the buffer chain, the required target impedance settings are different given the same IC switching current and the jitter specification.

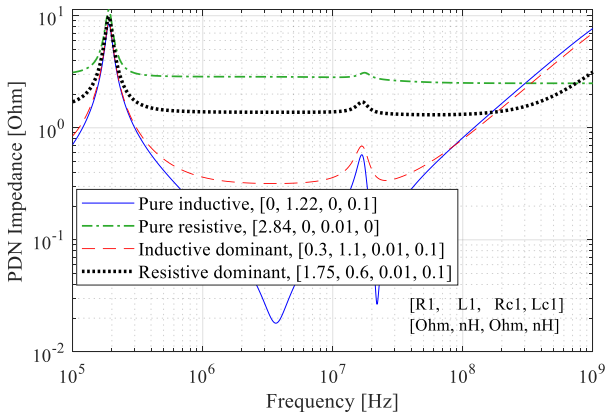


Figure 3.21 Target Impedance Defined Based on Jitter Specification Corresponds to the Four Cases for the Inverter Chain.

With the improved target impedance definition, the PDN design is more flexible since the constraints at high frequencies or low frequencies can be adjusted based on the specific design. Printed circuit board (PCB) designers can easily calculate the two bounding extreme cases and decide the most suitable target impedance curve in between the two extreme cases based on the circuit and jitter requirement. Compared to the previous target impedance definition [17], [18], the proposed target impedance concept can directly relate the buffer output jitter with the PDN design. From Figure 3.18 and Figure 3.21, it can be shown that with the same jitter specification, the bounding target impedance curves (pure resistive and pure inductive) are different for the single stage inverter and inverter chain. If the voltage ripple is applied as specification, the resulting

jitter at the driver output cannot be determined and it will just give the same set of target impedance curves for different buffers. The proposed target impedance concept can provide another level of flexibility with the jitter requirement. The demonstrated power integrity and signal integrity co-analysis method is crucial for a more flexible and cost effective PDN design.

3.2. MEASUREMENT VALIDATION OF PSIJ-PDN CORRELATION

From the proposed jitter-aware target impedance, the essential part is the derivation of the PSIJ-PDN correlation. It is desirable to validate the PSIJ-PDN formulation in a real measurement environment.

3.2.1. Measurement Characterization Procedure. The measurement characterization of PSIJ has been discussed in [48-56]. However, there has not been any demonstration for PSIJ-PDN correlation measurement validation. In this research, the proposed measurement validation procedure is summarized as shown in Figure 3.22.

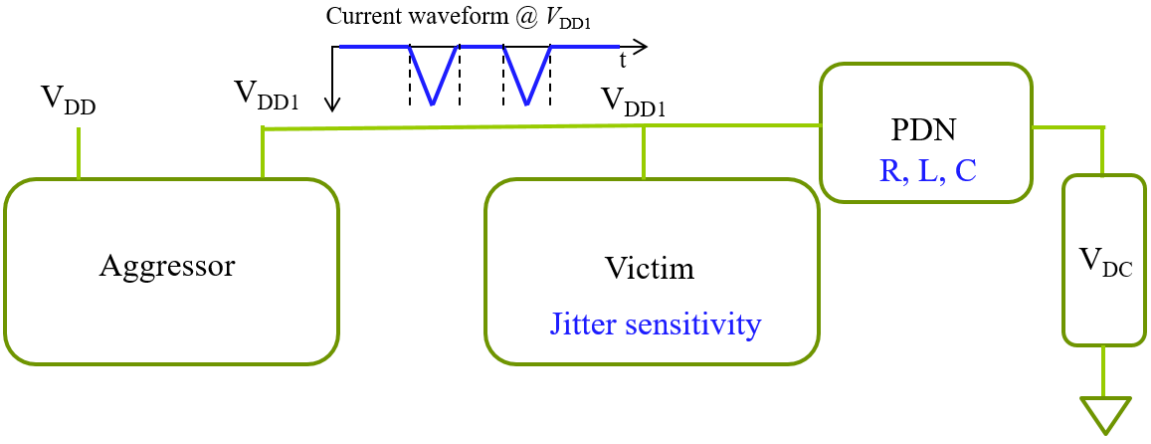


Figure 3.22 PSIJ-PDN Correlation Measurement Procedure.

Firstly, an aggressor circuit is designed that can generate large triangular IC current on the power net of the victim driver. Then on-die PDN characterization will be performed to extract the equivalent R-L-C parameters. Next, the PSIJ sensitivity of the victim driver will be measured. Then the circuit total PSIJ with the aggressor operation will be measured. At last, we will compare the predicted jitter calculated from the PSIJ-PDN formulation with the measured PSIJ.

An in-house designed test IC is used and the chip layout design is shown in Figure 3.23. The aggressor circuit is called the current consuming circuit (CCC) and the victim driver is an inverter chain. The schematic of the inverter chain in plotted in Figure 2.4(b).

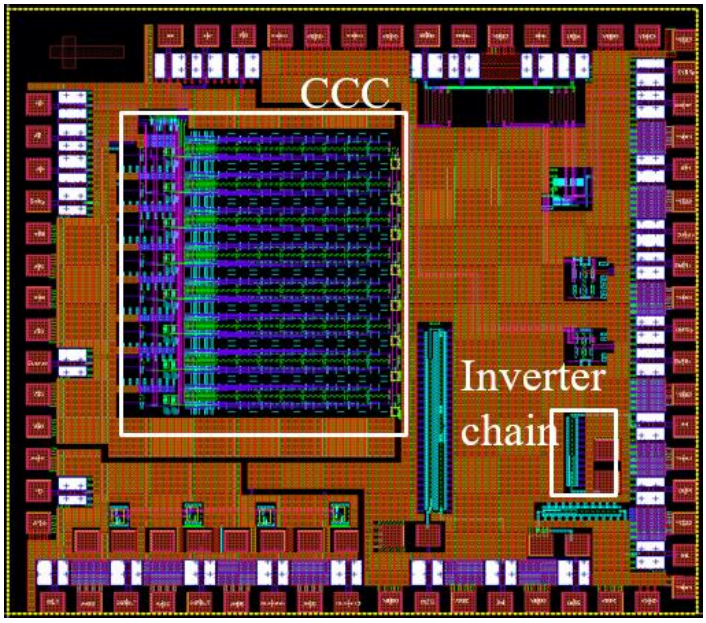


Figure 3.23 Designed Test IC Layout.

The test IC die is wire-bonded to a PCB test board. The designed PCB is plotted in Figure 3.24. The power nets for the aggressor circuit and the victim circuit are separated. The power net for the CCC is denoted as V_{dd}, while the power net for the victim circuit is denoted as V_{dd1}. The CCC control pins are designed to be controlled with on board switch. The decap pins are also designed for the placement of the bulk decoupling capacitors.

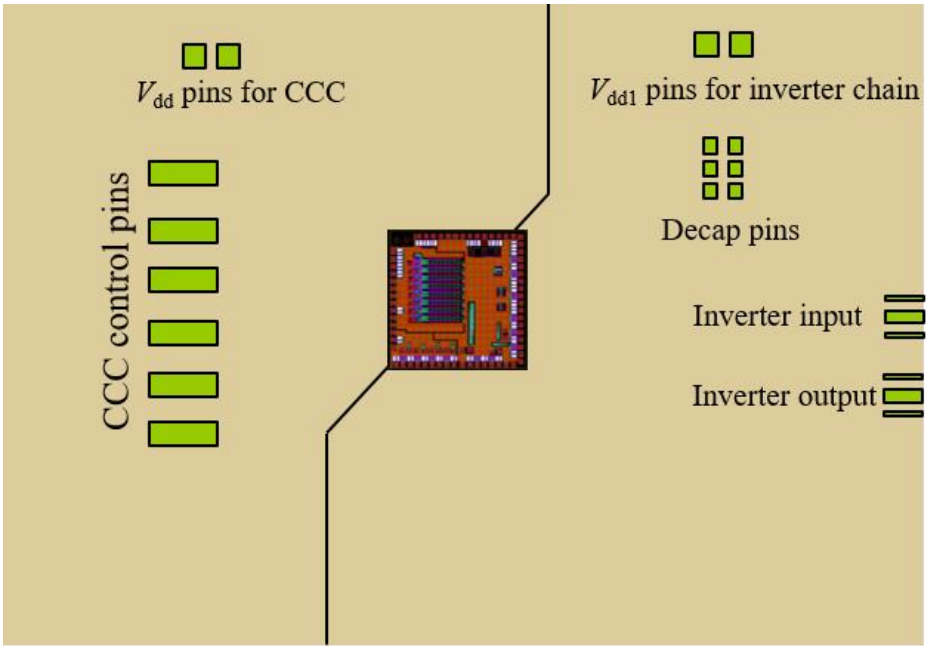


Figure 3.24 Designed PCB for Test IC.

The design block for the CCC and the victim driver are shown in Figure 3.25. The CCC can generate two triangular current pulses in one operating period on the power net of the victim driver. There are 6 control pins. A1 to A3 for current peak amplitude control. R1 to R3 for current rise time control.

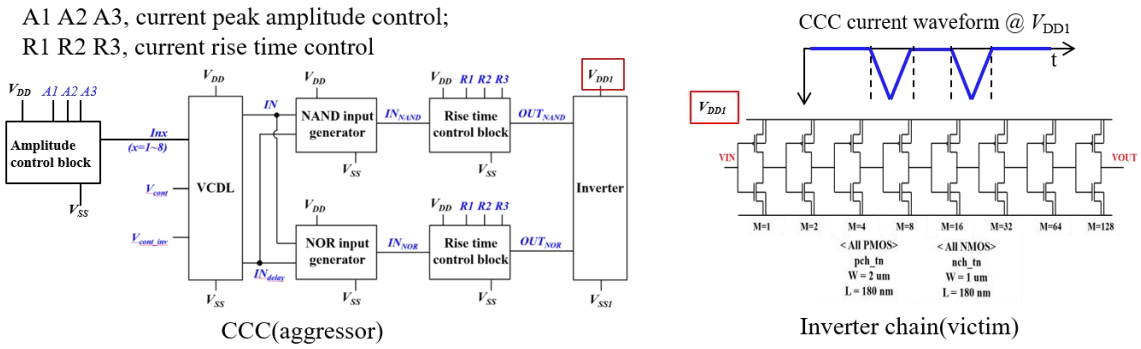


Figure 3.25 Design Block for CCC and Victim Driver.

The measurement setup for the proposed validation procedure is summarized in Figure 3.26.

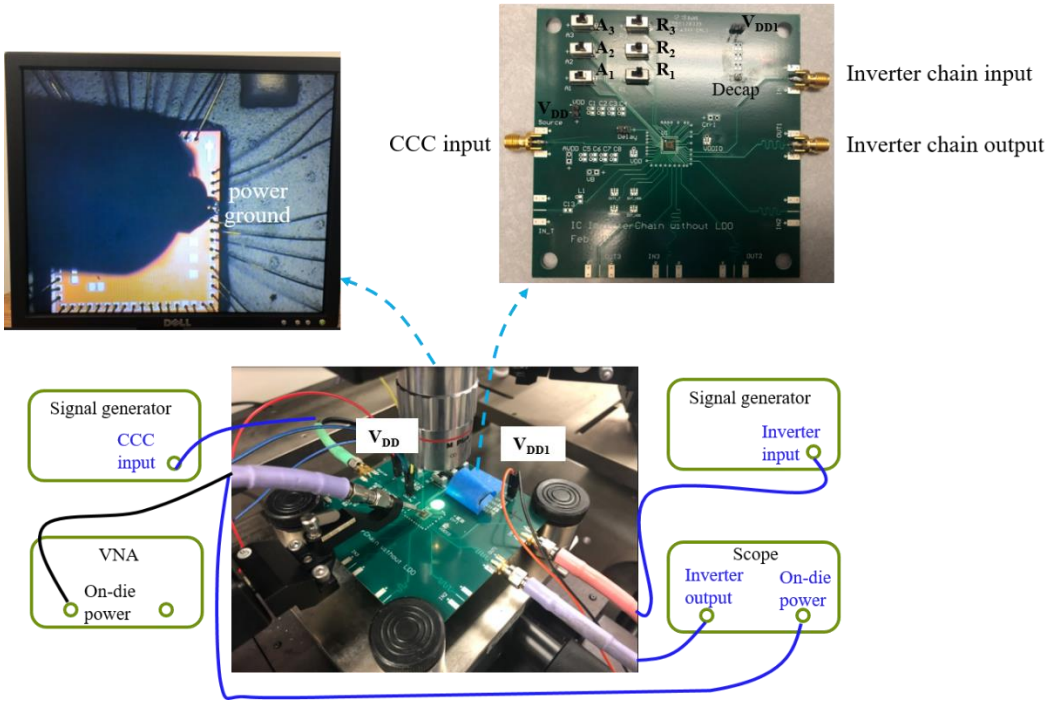
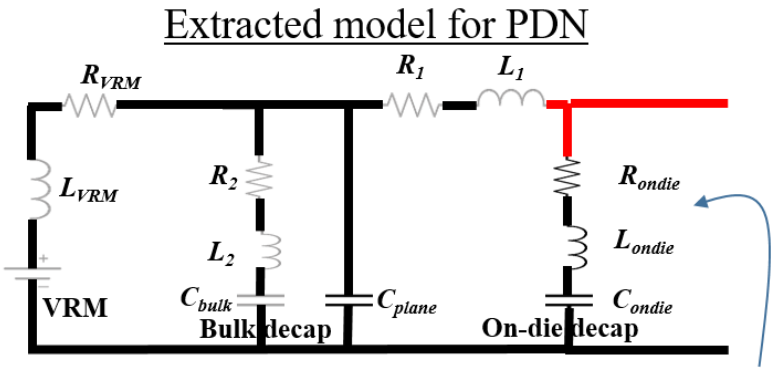


Figure 3.26 Measurement Setup for PSIJ-PDN Correlation Validation.

For the PSIJ characterization, a signal generator will generate the square wave input. The inverter chain output is measured by the scope. Another generator is used for CCC input. The micro SG probe is probing the on-die power net and the voltage waveform is measured by the scope at the same time. For the on-die PDN characterization, the micro probe output is connected to the VNA. The on-die PDN impedance is obtained by transform the one port S parameter [57-61].

3.2.1.1. On-die PDN characterization. The on-die PDN measurement is firstly conducted to extract the R-L-C parameters. The extracted equivalent circuit model is shown in Figure 3.27.



R_{ondie}=1.8Ω, on die resistance L_{ondie}=0, on die inductance
C_{ondie}=200pF, on die capacitance
R_1=1.2Ω, L_1=5nH, wire bond, PCB parasitic resistance, inductance
C_{plane}=440pF, PCB plain capacitance
R_2=0.01Ω, L_2=2nH bulk decap parasitic resistance, inductance
C_{bulk}=800nF, bulk decap capacitance
R_{VRM}=0.2Ω, L_{VRM}=3000nH, VRM parasitic resistance, inductance

Figure 3.27 Extracted Equivalent Circuit for On-Die PDN.

The R_{ondie}, L_{ondie} and C_{ondie} are for on-die portion. R_1 and L_1 are the parasitic resistance and inductance due to the wire bond and PCB board. C_{plane} is the capacitance from the PCB. C_{bulk} is for the bulk decap. R_2 and L_2 are the equivalent series resistance (ESR) and equivalent series inductance (ESL). The bulk decap is 800 nF. For the DC VRM branch, R_{VRM} and L_{VRM} are the parasitic resistance and inductance. The PDN impedance obtained from the R-L-C model is relatively close to the measured result, as shown in Figure 3.28.

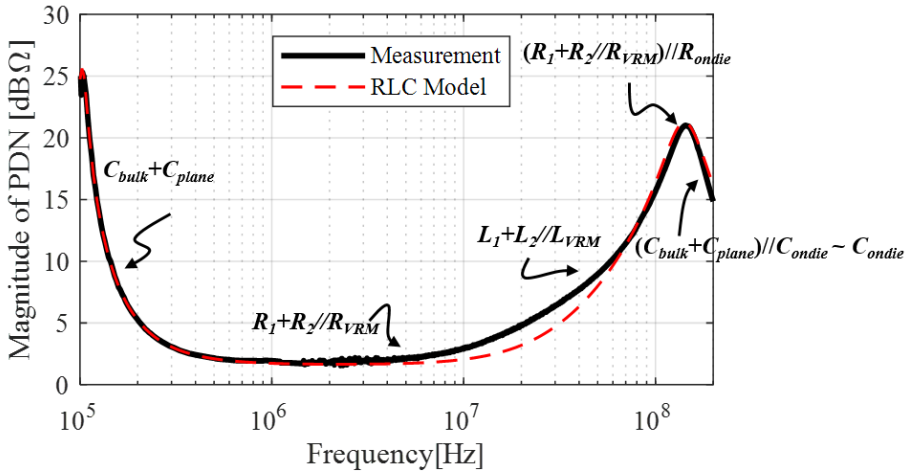


Figure 3.28 Comparison of Measured and Simulated PDN Impedance.

The PDN is firstly dominated by the capacitance portion and is mainly from the C_{bulk} and C_{plane}. Then the PDN is dominated by the resistive portion and is from R_1 in series with the equivalent resistance of the bulk decap branch and VRM branch. With the increase of frequency, the PDN impedance goes up and the inductive portion is from L_1 in series with equivalent inductance of the bulk decap branch and VRM branch. The anti-peak value is determined by the on-die resistance in parallel with the equivalent

resistance for the rest branches. Then the PDN impedance is brought down by the on-die decap. The on-die decap is extracted as 200pF and is very close to the designed value.

3.2.1.2. IC current characterization from on-die power voltage ripple. After the PDN model is established and the related R-L-C parameters are extracted, the next step is to obtain the IC current peak and rise time value. There has been several works related to the measurement of IC switching current [62-64]. In this research, the on-die IC current is not measured directly. With the measured on-die power voltage and PDN model, the rise time and the peak value information of the IC switching current are extracted.

The triangular current can be expressed as in (31). For the triangular IC current pass through this PDN network, the illustration is shown Figure 3.29.

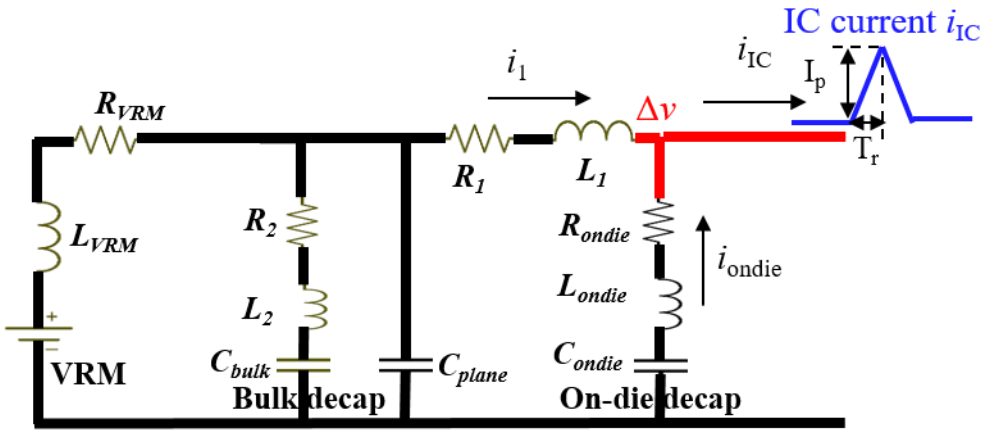


Figure 3.29 Triangular IC Current Passing Through PDN Model.

Since the C_{bulk} and C_{plane} together are much larger than the on-die decap, based on the short circuit approximation [46], the on-die current can be derived as:

$$
\begin{aligned}
&i_{ondie} = \frac{I_p}{T_r}\frac{L_1'}{\left(L_{ondie}+L_1'\right)}\frac{1}{\omega}\begin{pmatrix}\sin\left(\omega t\right)e^{-\alpha t}u(t)-2\sin\left(\omega\left(t-T_r\right)\right)e^{-\alpha\left(t-T_r\right)}u(t-T_r)\\+\sin\left(\omega\left(t-2T_r\right)\right)e^{-\alpha\left(t-2T_r\right)}u(t-2T_r)\end{pmatrix}\\
&L_1' = L_1 + L_2 \,||\, L_{VRM}\\
&R_1' = R_1 + R_2 \,||\, R_{VRM}\\
&\omega = \sqrt{1/\left(L_{ondie}+L_1'\right)C_{ondie}}\\
&\alpha = \left(R_{ondie}+R_1'\right)/2\left(L_{ondie}+L_1'\right)
\end{aligned}
\tag{43}
$$

It can be seen that the on-current is related to the PDN R-L-C parameters and the IC current parameters. Since the on-die inductance is negligible, the on-die voltage ripple can be calculated as the voltage drop on the on-die resistance and on-die capacitance as:

$$
\Delta v = -R_{ondie}i_{ondie} - \frac{1}{C_{ondie}}\int i_{ondie}dt \tag{44}
$$

Inserting (43) into (44), the on-die voltage ripple is expressed as:

$$
\begin{aligned}
\Delta v = &-\frac{I_p}{T_r}\frac{R_{ondie}L_1'}{\left(L_{ondie}+L_1'\right)}\frac{1}{\omega}\begin{pmatrix}\sin\left(\omega t\right)e^{-\alpha t}u(t)-2\sin\left(\omega\left(t-T_r\right)\right)e^{-\alpha\left(t-T_r\right)}u(t-T_r)\\+\sin\left(\omega\left(t-2T_r\right)\right)e^{-\alpha\left(t-2T_r\right)}u(t-2T_r)\end{pmatrix}\\
&-\frac{1}{C_{ondie}}\frac{I_p}{T_r}\frac{L_1'}{\left(L_{ondie}+L_1'\right)}\frac{1}{\omega}\\
&\begin{pmatrix}\dfrac{-e^{-\alpha t}\left(\alpha\sin\left(\omega t\right)+\omega\cos\left(\omega t\right)\right)+\omega}{\omega^2+\alpha^2}u(t)\\-2\dfrac{-e^{-\alpha\left(t-T_r\right)}\left(\alpha\sin\left(\omega\left(t-T_r\right)\right)+\omega\cos\left(\omega\left(t-T_r\right)\right)\right)+\omega}{\omega^2+\alpha^2}u(t-T_r)\\+\dfrac{-e^{-\alpha\left(t-2T_r\right)}\left(\alpha\sin\left(\omega\left(t-2T_r\right)\right)+\omega\cos\left(\omega\left(t-2T_r\right)\right)\right)+\omega}{\omega^2+\alpha^2}u(t-2T_r)\end{pmatrix}
\end{aligned}
\tag{45}
$$

It is analytical and means that the voltage ripple is related to the IC current peak value, rise time, and on-die PDN R-L-C parameters.

The derived PSIJ-PDN formulation is firstly validated with Advanced Design System (ADS) simulation [65], as shown in Figure 3.30. For the extracted model, an ideal triangular current pulse is added. The peak value of the current is set to 80mA and rise time of the current is set to1ns.

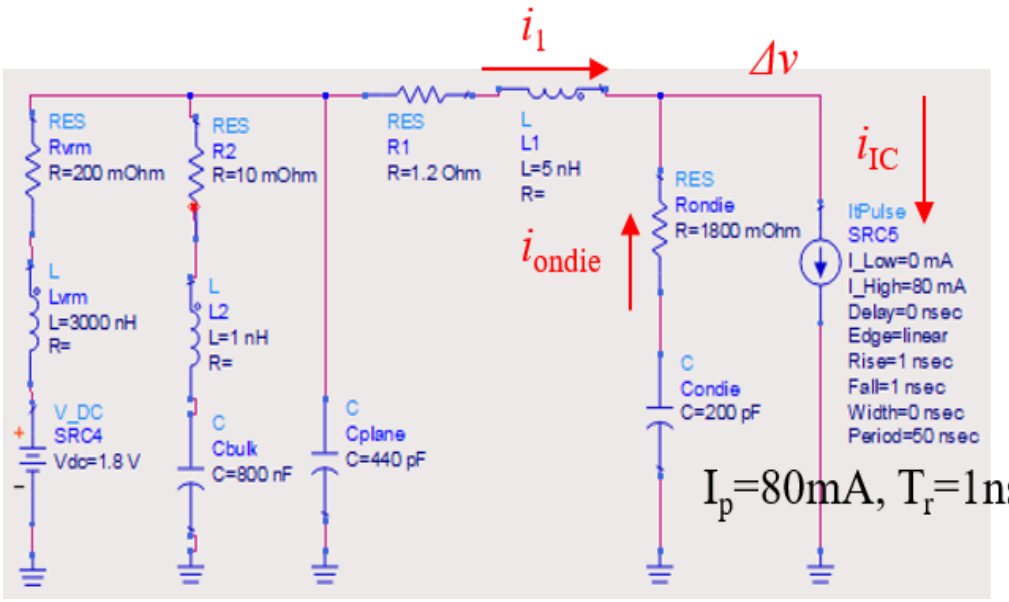


Figure 3.30 ADS Simulation Setup.

The comparison of the formulation calculation and the simulation results for the on-die current, i_1 current and the on-die voltage ripple are shown in Figure 3.31. It can be observed that the formulation can capture the majority of the waveform characteristics. The ringing portion in all three waveforms are related to the anti-peak frequency ω in the PDN network. It can be shown that i_1 and i_{ondie} are comparable. Even though the bulk decap is much larger than the on-die decap, the relatively large R_1 and L_1 will impedance the current to flow all into the bulk decap branch.

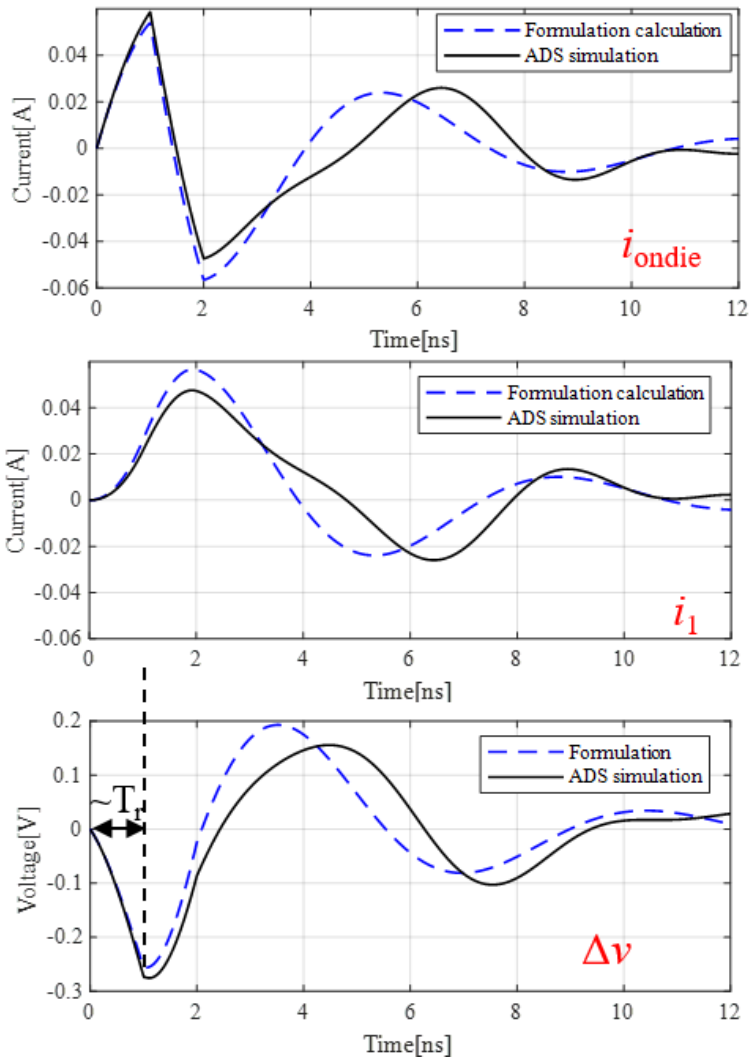


Figure 3.31 Formulation Calculation and ADS Simulation Comparison.

From the on-die voltage ripple, it can be observed that the time when the first voltage dip happens is very close to the rise time of the IC current. In addition, the voltage value at this time point can be calculated using the derived formulation, from which the peak current value can be derived.

The measured on-die power voltage ripple is shown in Figure 3.32. In this case, the 3-bit amplitude control of CCC is used and there will be 8 different cases.

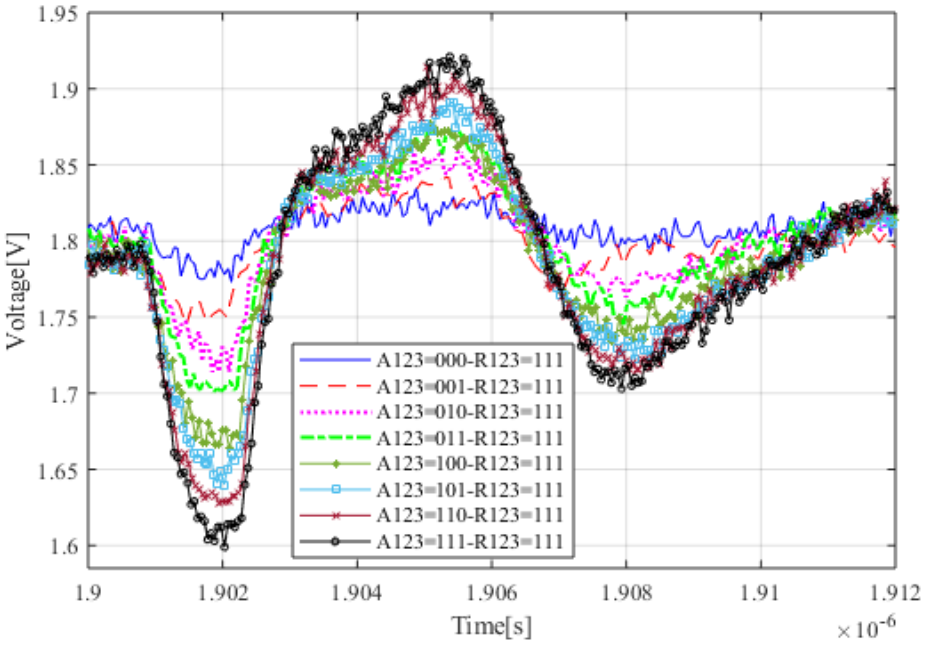


Figure 3.32 Measured On-Die Power Noise under 8 Different Amplitude Control Bits Combinations.

The comparison of the measured maximum voltage ripple and the calculated voltage waveform for the 8 cases are shown in Figure 3.33. The maximum voltage ripple is used since the jitter is the peak-to-peak value of the CTIE sequence. The formulation calculated waveforms are plotted in the orange solid curves. It can be observed that the formulation can correlate with the measurement results with reasonably good accuracy. The formulation calculated curve can capture the majority of the measured waveform characteristics. With the increase of the control bit sequence value, the voltage ripple value is also increased. As mentioned before, from the first dip of the voltage ripple and the time to reach the first voltage dip in the voltage ripple waveform, the IC current rise time and the peak value can be estimated.

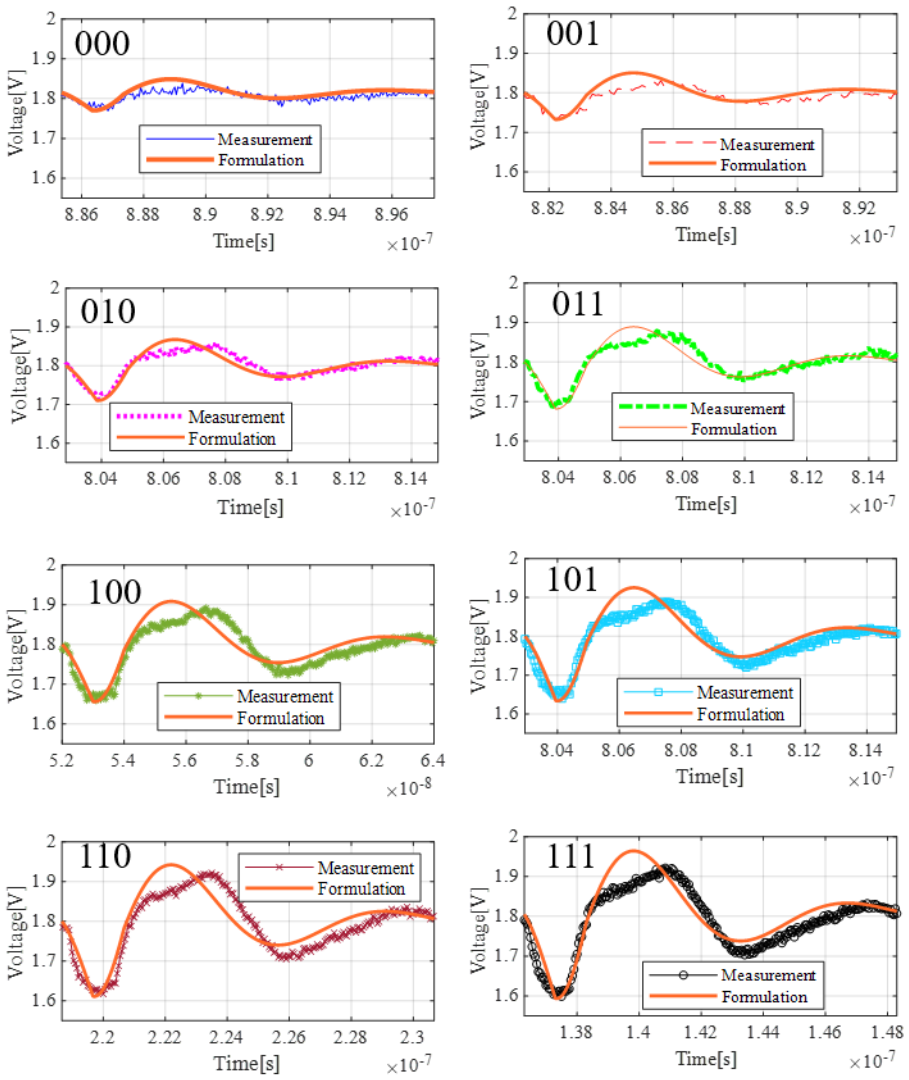


Figure 3.33 Formulation Calculation and Measurement Comparison.

The extracted rise time and peak current value for each case are summarized as follow: for A1A2A3=000, the extracted T_r=1ns, I_p=14mA; for A1A2A3=001, the extracted T_r=1ns, I_p=21mA; for A1A2A3=010, the extracted T_r=1ns, I_p=28mA; for A1A2A3=011, the extracted T_r=1ns, I_p=37mA; for A1A2A3=100, the extracted T_r=1ns, I_p=45mA; for A1A2A3=101, the extracted T_r=1ns, I_p=52mA; for A1A2A3=110, the extracted T_r=1ns, I_p=59mA; for A1A2A3=111, the extracted T_r=1ns, I_p=66mA.

3.2.1.3. Driver PSIJ sensitivity characterization. After the IC current information is obtained, the next step is to derive the victim driver PSIJ sensitivity. To measure the PSIJ sensitivity, it is important to know the on-die power rail voltage [66-70]. However, in many cases, the on-die power net is not accessible. In this part, a measurement procedure is proposed to derive PSIJ sensitivity from the off-chip environment.

The proposed measurement procedure is summarized in Figure 3.34. In the real measurement environment, from the output waveform, the noise voltage and the timing jitter can be extracted. In the simulation environment, the on-die power net is accessible. The PSRR response of the driver can be obtained. With this relationship, the on-die power net noise voltage can be derived from the noise voltage appeared in the output waveform. Using the PSRR response extracted from simulation, the on-die power noise voltage can be calculated back from the measured noise voltage in the output waveform. In the real measurement case, using the measured timing jitter divided by the calculated on-die power noise, the PSIJ sensitivity of the transmitter can be evaluated in the off-chip environment.

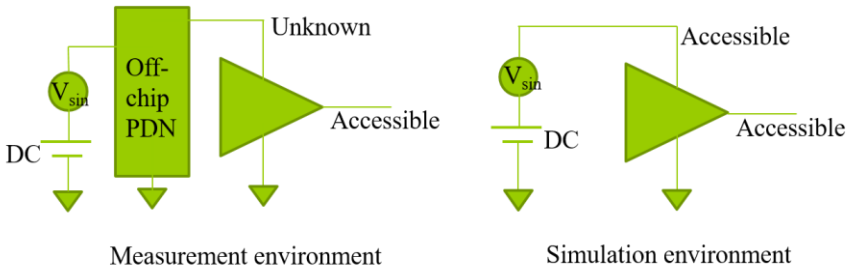


Figure 3.34 Proposed Procedure for Evaluating PSIJ Sensitivity from Off-Chip Environment.

A test board is designed to characterize the driver PSIJ sensitivity as shown in Figure 3.35.

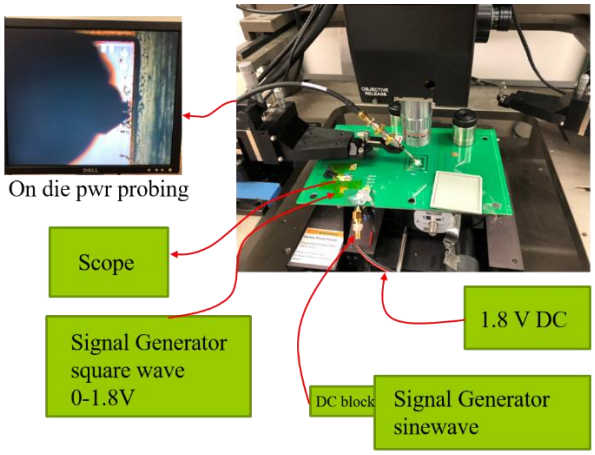
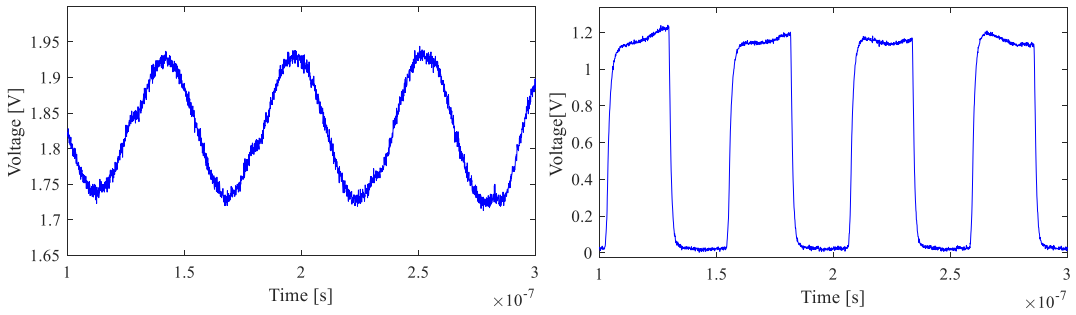


Figure 3.35 Test Board and Measurement Setup.

The die is wire-bonded to the PCB and is exposed for on-die power net measurement. A micro SG probe with 100um pitch is used for probing. All the PCB traces are designed to be 50 Ohm and is connected out through SMA connectors. A semi-rigid cable is soldered on to the PCB power port for sinusoidal power rail noise injection. The DC operation voltage for the driver is 1.8V. The input of the inverter chain is a square wave switching between 0 and 1.8V. The output waveform of the inverter chain is measured through a SMA cable to the oscilloscope. The on-die power net voltage is measured simultaneously using the oscilloscope. The scope is set to 50 Ohm input impedance.

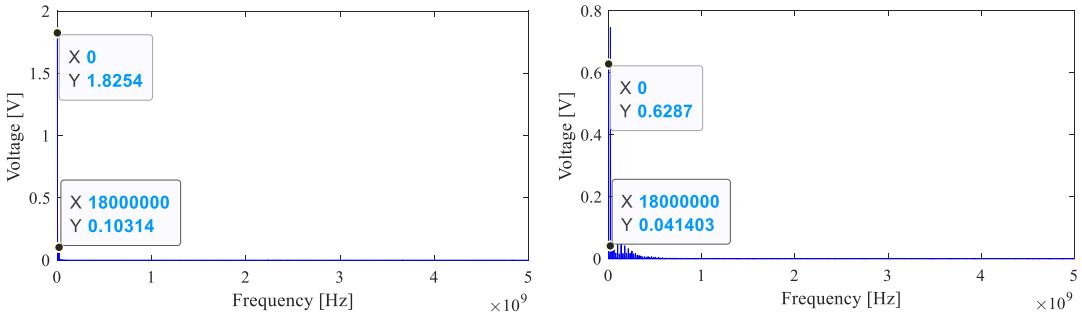
The measured output waveform with 18MHz sinusoidal power noise injection is shown in Figure 3.36(a) as an example. The corresponding measured on-die power noise is plotted in Figure 3.36(b). The fast Fourier transform (FFT) of the two waveforms are

shown in Figure 3.37(a) and (b), respectively. From the FFT of the output waveform, the voltage amplitude of DC component and the component at 18MHz can be extracted. Considering the 50% duty cycle of the output waveform, the DC amplitude and 18MHz noise component amplitude are calculated as 0.6287*2=1.2574V and 0.0414*2=0.0828V, respectively.



a b

Figure 3.36 Measured Time Domain Waveform. a) On-Die Power Net. b) Output Waveform.



a b

Figure 3.37 FFT of Measured Waveforms. a) On-Die Power Net. b) Output Waveform.

The time domain jitter can be read from the peak to peak value of the TIE sequence. In order to extract the TIE sequence, the output waveform measured without any noise voltage is measured as reference. The extracted TIE sequence for 18MHz noise is shown in Figure 3.38. The jitter is read as 230ps. The jitter sensitivity can be calculated as the ratio of the jitter amplitude divided by the on-die power noise amplitude. In the case that the on-die power net is not accessible, the on-die power noise amplitude can be calculated from the noise amplitude in the output waveform using the simulated PSRR response.

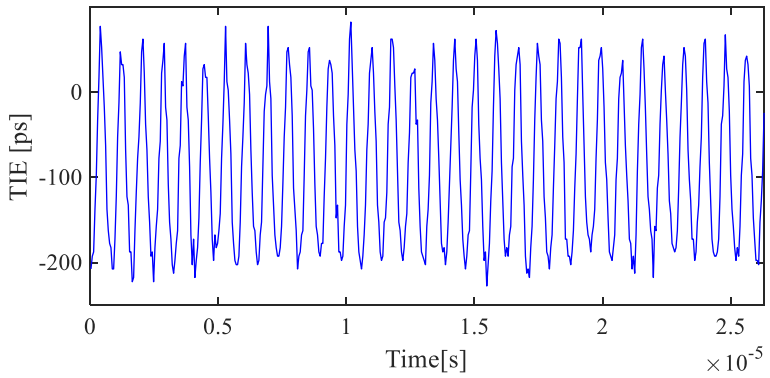


Figure 3.38 Extracted TIE Sequence with 18MHz Noise.

The simulation setup for PSRR response evaluation is shown in Figure 3.39. There will be the ESD protection diodes for the pull-up and pull-down branches. The 9 Ohm resistor and 50 pF are the equivalent parasitic of the wire-bonding and PCB part. The simulated PSRR response, which is the ratio of output noise amplitude to the input noise amplitude, is shown in Figure 3.40(a). Since the on-die power net is accessible in the measurement setup, the measured PSRR response is also shown for comparison in

Figure 3.40(a). The error percentage of the simulated PSRR is within 5% difference compared to the measured PSRR, as shown in Figure 3.40(b).

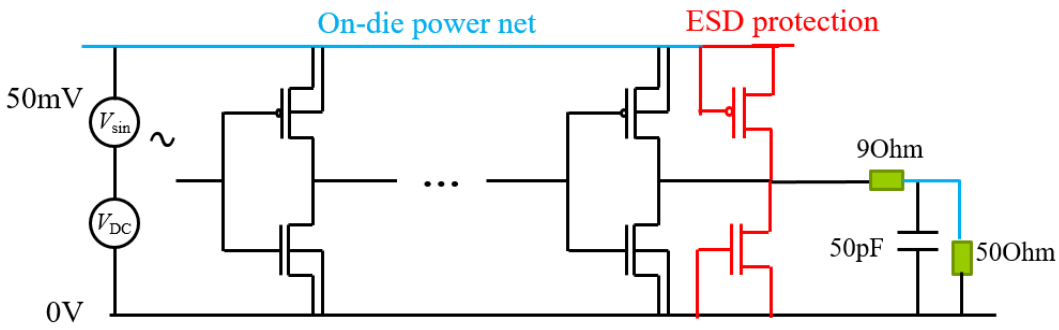
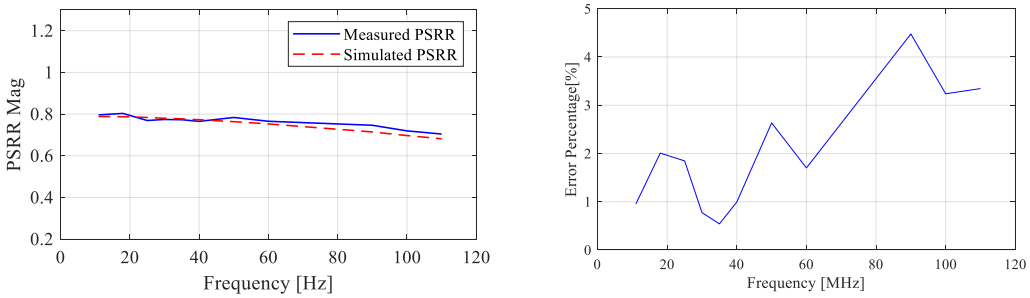


Figure 3.39 Equivalent Simulation Setup for the Real Measurement Case.



a b

Figure 3.40 PSRR Response. a) Measured and Simulated PSRR Comparison. b) Error Percentage.

With the simulated PSRR ratio, the PSIJ sensitivity can be extracted from the off-chip environment. The measured PSIJ sensitivity using directly measured on-die power voltage is shown in Figure 3.41 and is treated as the reference value. It is plotted with the blue solid line. The simulated PSIJ sensitivity is also shown in Figure 3.41. The

simulated PSIJ sensitivity is plotted in the red dashed line. The measured PSIJ sensitivity using the calculated on-die power voltage from simulation is also plotted in Figure 3.41. It is plotted in the black dot-dashed line.

The error percentage of the measured PSIJ sensitivity using the proposed method to the directly measured PSIJ sensitivity is shown in Figure 3.42(a). The proposed method can give a reasonably accurate estimation of PSIJ sensitivity, with the error percentage smaller than 5%. The trend of the error percentage is similar to the trend of the error percentage of the PSRR response. The error percentage of the simulated PSIJ sensitivity to the directly measured PSIJ sensitivity is also shown in Figure 3.42(b). The error percentage is less than 3.5%. With the proposed method, the PSIJ sensitivity can be characterized at the off-chip environment, provided that the PSRR response can be extracted from the simulation.

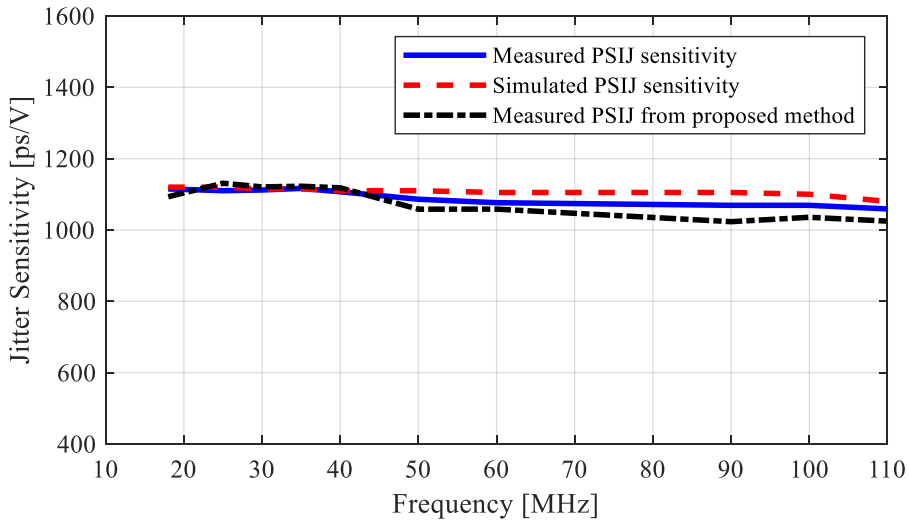
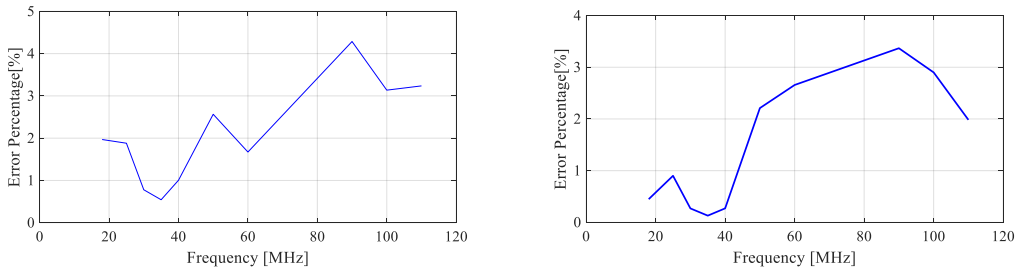


Figure 3.41 PSIJ Sensitivity Comparison between Measured Using On-Die Power Net Noise, Simulation and Proposed Method.



a b

Figure 3.42 Error Percentage. a) Proposed Method Compared to Reference. b) Simulation Compared to Reference.

For the designed PCB as shown in Figure 3.26, the equivalent circuit for the victim inverter chain can also be derived as shown in Figure 3.43. The equivalent series resistance and the equivalent series capacitance are different as shown in Figure 3.39. This is because the PCB designed for CCC test are different from the board in Figure 3.26.

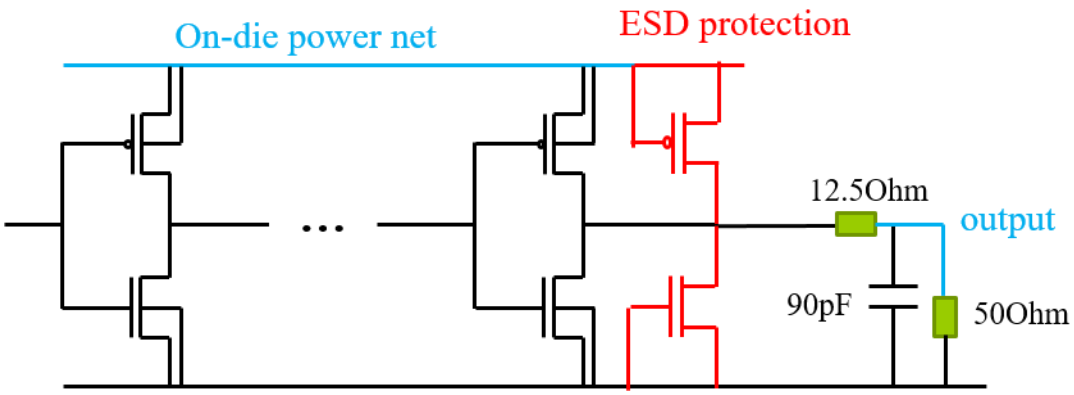


Figure 3.43 Equivalent Simulation Setup.

Based on the derived equivalent simulation circuit, the victim driver PSIJ sensitivity for the CCC test PCB case is shown in Figure 3.44. The result is close to a sinc function and the DC jitter sensitivity is 1720ps/V while the propagation delay is 1.43ns.

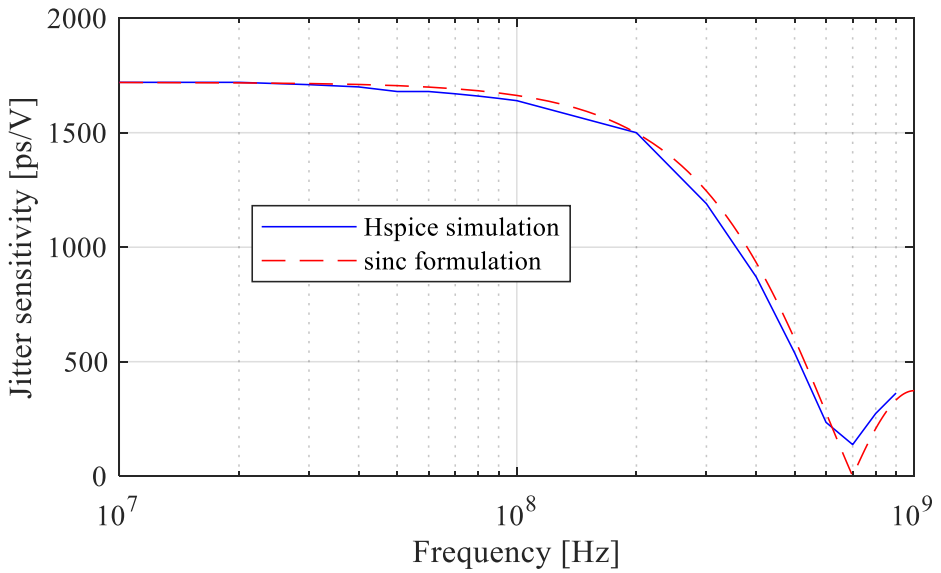


Figure 3.44 Calculated and Simulated PSIJ Sensitivity Comparison.

3.2.2. Validation of PSIJ-PDN Formulation. With the PDN R-L-C information, IC current information and the driver PSIJ sensitivity information, the total PSIJ when an aggressor circuit is operating can be derived. As previously shown, the CTIE is calculated as the convolution of the on-die voltage ripple and the time domain PSIJ transfer relationship [71-73]. The width of this time domain PSIJ transfer relationship is the propagation delay and is denoted as *E*. On the other hand, the height of the rectangular pulse is the ratio of DC jitter sensitivity to the propagation delay and is denoted as *D*.

The convolution process is illustrated in Figure 3.45. Since the jitter is the difference between the maximum and minimum CTIE value, it is only required to find the time point when the minimum and maximum happens. Since *D* is a constant, this process is equivalent to find the minimum and maximum value of the voltage ripple integration in the time range of the propagation delay *E*.

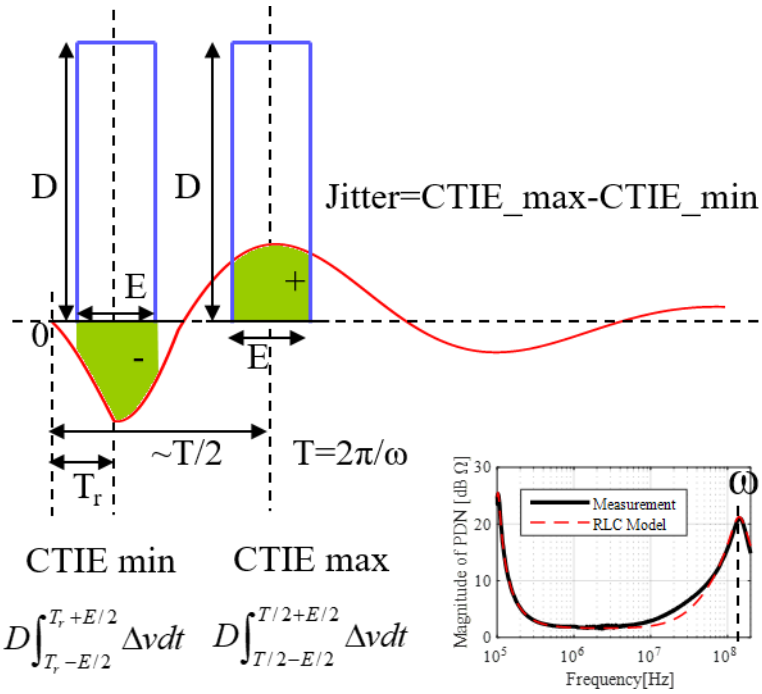


Figure 3.45 Illustration of Convolution Process.

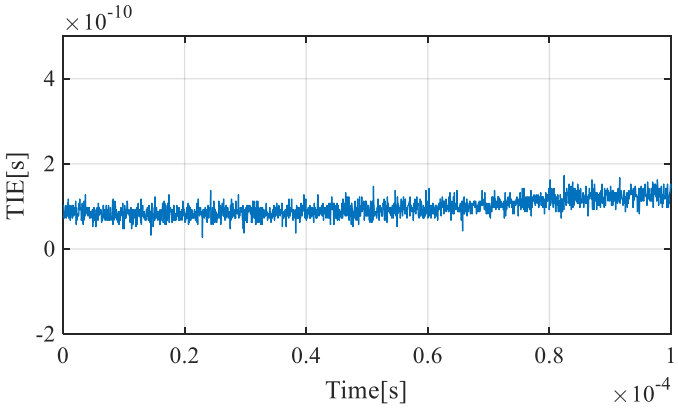
In this case, the minimum will happen when the integration is done between *T*r minus half of *E* to *T*r plus half of E. For the maximum integration value, it can be assumed to happen near the half *T*. In this case, *T* is the period of the ringing corresponds to the anti-peak in PDN. The maximu, will happen when the integration is done between *T*/2 minus half of *E* to *T*/2 plus half of E.

The integration of the on-die voltage ripple is derived as:

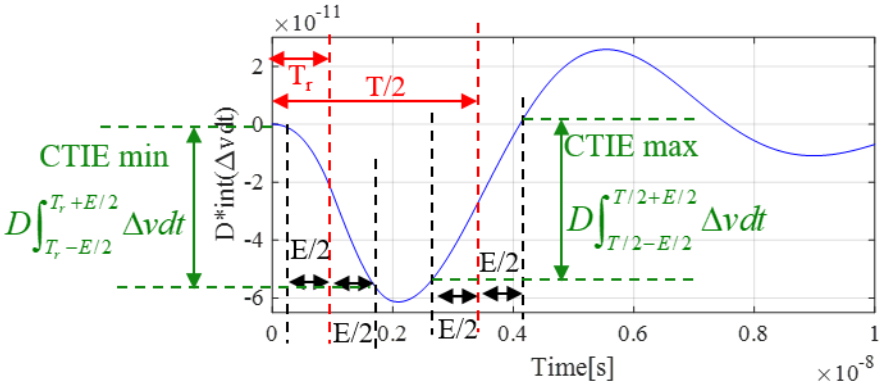
$$\int \Delta v dt = -\frac{I_p}{T_r}\frac{R_{ondie}L_1'}{\left(L_{ondie}+L_1'\right)}\frac{1}{\omega}$$
$$\left(\begin{array}{l}\dfrac{-e^{-\alpha t}\left(\alpha\sin\left(\omega t\right)+\omega\cos\left(\omega t\right)\right)+\omega}{\omega^2+\alpha^2}u(t)\\ -2\dfrac{-e^{-\alpha\left(t-T_r\right)}\left(\alpha\sin\left(\omega\left(t-T_r\right)\right)+\omega\cos\left(\omega\left(t-T_r\right)\right)\right)+\omega}{\omega^2+\alpha^2}u(t-T_r)\\ +\dfrac{-e^{-\alpha\left(t-2T_r\right)}\left(\alpha\sin\left(\omega\left(t-2T_r\right)\right)+\omega\cos\left(\omega\left(t-2T_r\right)\right)\right)+\omega}{\omega^2+\alpha^2}u(t-2T_r)\end{array}\right)$$
$$-\frac{1}{C_{ondie}}\frac{I_p}{T_r}\frac{L_1'}{\left(L_{ondie}+L_1'\right)}\frac{1}{\omega}$$
$$\left(\begin{array}{l}\dfrac{-e^{-\alpha t}\left(\left(\omega^2-\alpha^2\right)\sin\left(\omega t\right)-2\alpha\omega\cos\left(\omega t\right)+\left(-\omega^3-\omega\alpha^2\right)te^{\alpha t}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}u(t)\\ -2\dfrac{-e^{-\alpha\left(t-T_r\right)}\left(\begin{array}{l}\left(\omega^2-\alpha^2\right)\sin\left(\omega\left(t-T_r\right)\right)\\ -2\alpha\omega\cos\left(\omega\left(t-T_r\right)\right)+\left(-\omega^3-\omega\alpha^2\right)\left(t-T_r\right)e^{\alpha\left(t-T_r\right)}\end{array}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}\\ u(t-T_r)\\ +\dfrac{-e^{-\alpha\left(t-2T_r\right)}\left(\begin{array}{l}\left(\omega^2-\alpha^2\right)\sin\left(\omega\left(t-2T_r\right)\right)-2\alpha\omega\cos\left(\omega\left(t-2T_r\right)\right)\\ +\left(-\omega^3-\omega\alpha^2\right)\left(t-2T_r\right)e^{\alpha\left(t-2T_r\right)}\end{array}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}\\ u(t-2T_r)\end{array}\right) \quad (46)$$

The measured TIE for the A1A2A3=000 case is shown in Figure 3.46(a). The calculated *D* multiply with the voltage ripple integration result for this case is shown in Figure 3.46(b). From this curve, the jitter can be read. The minimum CTIE can be read as the value at time *T*r plus half of *E* subtract the value at time *T*r minus half of *E*. The maximum CTIE can be read as the value at time half of *T* plus half of *E* subtract the value

at time half of *T* minus half of *E*. Then the jitter is the difference between the maximum and minimum CTIE. For the amplitude control bits 000 case, the measured jitter is read as 110ps while the calculated jitter is 108.6ps.



a



b

Figure 3.46 Measured and Calculated Jitter for 000 Case. a) Measured TIE. b) Calculated Jitter.

Following the mentioned procedure, the calculated jitter for the other 7 cases can be obtained. The results are summarized in Figure 3.47.

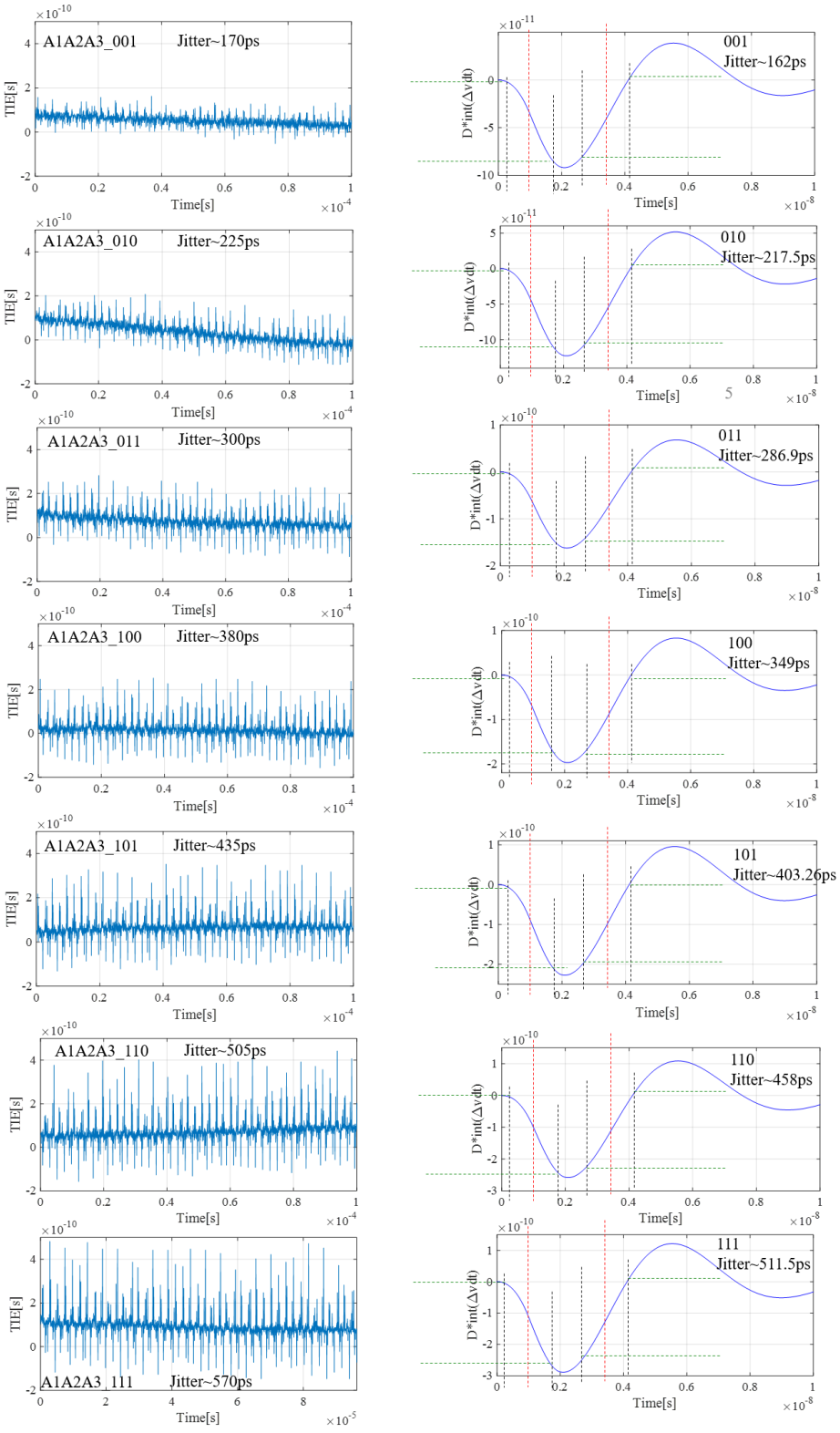


Figure 3.47 Measured and Calculated Jitter for Other Cases.

For the 8 current peak cases, the measurement and calculation results are summarized in Table 3.2.

Table 3.2 Measured and Calculated Jitter

A1A2A3	Measurement[ps]	Calculation[ps]	Error[%]
000	110	108.6	1.27
001	170	162	4.7
010	225	217.5	3.33
011	300	286.9	4.37
100	380	349	8.1
101	435	403.26	7.3
110	505	458	9.3
111	570	511.5	10.26

It can be observed that besides the last two cases. The error percentage is within 8.1%. Since the maximum voltage drop in the last two cases are larger than 0.2V, it is possible that it is too large and will introduce some non-linear effect [74-76]. The proposed derivation is based on the assumption that the PSIJ sensitivity is linear in a small voltage ripple range. So it is reasonable to have relatively large error for these cases.

4. CONCLUSIONS

4.1. SUMMARY

In this research, the PSIJ properties of the high speed buffer and the system with on-die LDO are studied. An improved target impedance concept is also proposed for the PSIJ consideration.

Firstly, the PSIJ sensitivity model based on PSRR response is derived and validated through HSPICE simulation. The obtained PSIJ sensitivity formulations contain both the magnitude and phase information. The proposed PSIJ sensitivity model can be generalized for the PSIJ study of different type of drivers. In general, the PSIJ sensitivity for different type of drivers is related to the PSRR response, transition edge slope and the propagation delay. With the proposed model, the factors influencing the PSIJ sensitivity behavior for different type of drivers can be clearly identified.

Secondly, an analysis method for PSIJ sensitivity evaluation of high speed output buffer with on-die LDO is proposed. The total system PSIJ sensitivity can be derived from the stand-alone analysis of the LDO block PSRR response and the buffer PSIJ sensitivity. This is helpful for reducing the simulation complexity, as the PSRR response of the LDO block can be performed relatively fast. In addition, the PSIJ sensitivity analysis is only required for the buffer part alone. Furthermore, with the proposed modular analysis method, the contribution of different blocks can be clearly identified and could potentially making the design optimization procedure easier.

Thirdly, a method to improve PSIJ simulation accuracy for IBIS model is proposed. The improvement is realized by modifying the switching coefficients as a

function of both time and the time averaged power rail noise. The extraction of the newly introduced correction coefficients only requires the V-t tables measured at additional two different power rail voltages. A plausible algorithm has been provided to implement the proposed new model as spice sub-circuit in the open source Ngspice simulator.

At last, the proposed target impedance concept with jitter specification can help the design of a group of target impedance curves according to the given jitter requirement. The proposed design procedure can reduce over-constrain in the PDN designed based on the original target impedance definition. Most importantly, the PDN design is directly correlated with the jitter of a specific circuit. Depending on the circuit output jitter response to the voltage fluctuation, the PDN can be designed for the needs of a specific circuit. The proposed PSIJ-PDN correlation has been validated through both the simulation and measurement.

4.2. FUTURE DIRECTIONS

The PSIJ study and related PDN design could continuously be the designers concern. Based on this research, the potential future directions could be:

1. Apply the proposed PSIJ sensitivity model for different kinds of drivers for test.
2. Improve the proposed new IBIS model by including the SSN simulation capability.
3. Improve the current characterization method so the PSIJ-PDN correlation method can be applied for a more practical case.

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