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Chaotic Behavior in High-Gain Interleaved Dc-dc Converters

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Abstract

In this paper, chaotic behavior in high gain dc-dc converters with current mode control is explored. The dc-dc converters exhibit some chaotic behavior because they contain switches. Moreover, in power electronics (circuits with more passive elements), the dynamics become rich in nonlinearity and become difficult to capture with linear analytical models. Therefore, studying modeling approaches and analysis methods is required. Most of the high-gain dc-dc boost converters cannot be controlled with only voltage mode control due to the presence of right half plane zero that narrows down the stability region. Therefore, the need of current mode control is necessary to ensure the stability of this type of boost converter. A significant number of the work reported so far has concentrated on explaining the chaos phenomena in the language of the nonlinear dynamics literature. In addition to analyzing and studying chaotic behaviors, this presents some ideas about moving toward gainful utilization of the nonlinear properties of power electronics. Simulation and experimental studies are included to validate the theory, and results will be discussed.

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Keywords: Chaos, bifurcation; nonlinear; Dc-dc; boost; buck; High-gain; interleaved

1. Introduction

Power electronics that are used to convert dc input voltage to dc output voltage can be divided into four categories, as shown in Fig. 1. Linear regulators are usually employed in auxiliary applications, and switched capacitors, which are used as battery charge equalizer and power suppliers to computer servers [1-2]. The switching mode power supply is controlled by pulse width modulation (PWM), and it is the most common type of converter and it used in applications interfacing renewable energy sources to the microgrid [3, 4]. The PWM converters are controlled by devices that take an error signal and convert it to a signal that is suitable for turning on and off the

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active switches. These switches increase the nonlinearity in the dynamic behavior. The PWM signal has a frequency in the range of 10 to 200 kHz, and working with high frequency makes the circuit prone to exhibit some chaotic behavior. Chaos is an unexpected long-term state of disorder. It is happening in nonlinear dynamic systems. To better understand this phenomenon, different tools have been developed [5-7]. Bifurcation figures are an example of an evaluation tool used to study the reaction of the system to change one or more parameters. The bifurcation usually plotted in 2D figures with one variable varying on the x-axis and the other variable on the y-axis. This tool can be helpful if one or more input is highly variable such solar PV voltage, and can improve the design and operation of a system [8-10]. Plotting bifurcation figures in higher dimension requires expensive computations, and hence is not of interest in this paper. In power electronics, one can plot the bifurcation diagram using the discrete models by observing state variables [7]. Other techniques used to test the performance of power electronic converters can be summarized in Fig 2. A phase portrait is a tool that shows if the trajectory is going to converge to a stable point or diverge. The Poincare map is suitable if continuous system discretization is preferred. This method places Poincare section at a selected position on state space and then obtains the discrete time model of the continuous system by finding the intersection of the surface and the trajectory. Time domain waveforms show the transient response and the steady state response. The x-axis is the time, and the y-axis is the dependent variable that changes with time (e.g., inductor current). The Bode plot is a graph to see a behavior of a transfer function against (versus) the frequency. It is widely used to test the stability of a system. The bode plot contains a magnitude plot and an angle plot of the transfer function. The Cobweb plot visualizes sequential iterations of a function. Having to plot the iterations, the long-term stability status can be inferred, and the behavior of the system can be investigated.

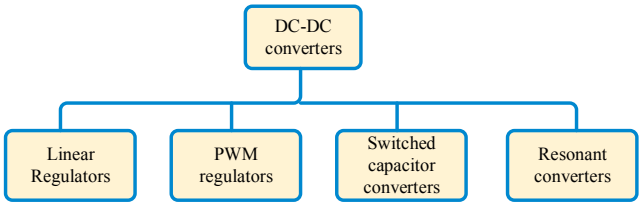

Fig. 1. Types of dc-dc converters

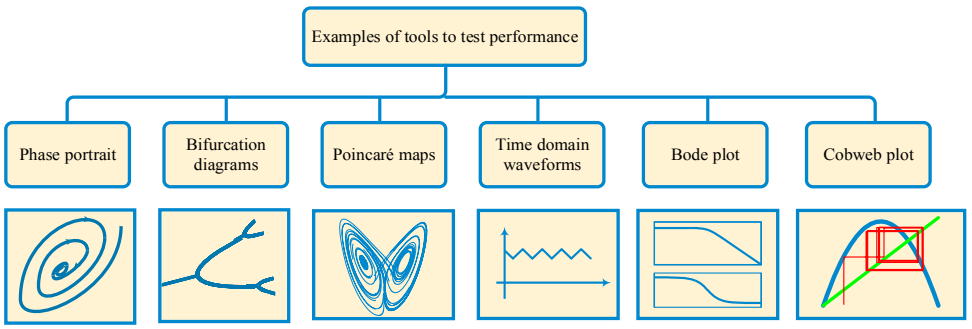

Fig. 2. Examples of tools used to test performance of a system

Figure 3 shows the bifurcation diagram with four different periods and the phase portrait and time-domain waveform associated with each period. In steady state (period 1), the period and the sampling interval are the same. The time domain waveform has one corresponding sample during the interval. The state space trajectory in phase portrait starts from a point and returns to the same point. In other words, the state space trajectory has a single loop. In period 2, the period-doubling bifurcation occurs. During this period, the time-domain waveform has two corresponding samples during the sampling interval. The state-space trajectory is no longer continuous single loop. In period 4, the period-quadrupling bifurcation occurs. The time-domain waveform has four corresponding samples during the sampling interval. The phase portrait has multiple loops. The system is still stable under period 2 and

period 4. The chaos region is where the system becomes unstable. In the chaos period, there is a large number of points during a sampling interval, and the state-space trajectory has many loops. References [11-16] have more details about the performance testing methods.

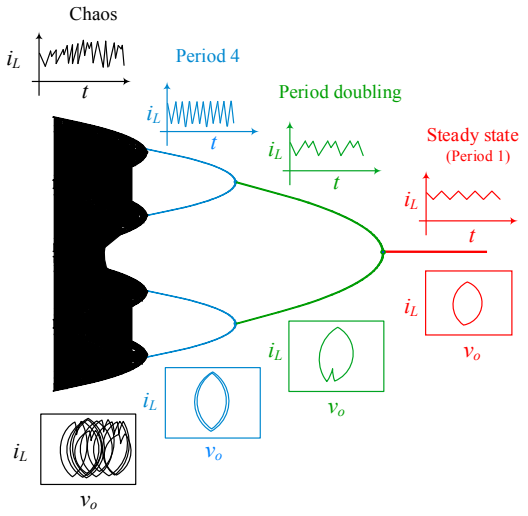

Fig. 3: Bifurcation plot with phase portrait plots and time-domain waveforms

2. Example chaotic behavior in power electronics (buck converter)

This section presents the analysis dynamical behavior of buck converters with valley current mode control in continuous conduction mode (CCM). Figure 4a shows the schematic of a buck converter. The converter has two modes of operation. There are two operating modes of buck converter; mode 1, where the MOSFET is turned on, and mode 2, where the MOSFET is turned off. In this paper, internal components of buck converter are assumed to be ideal.

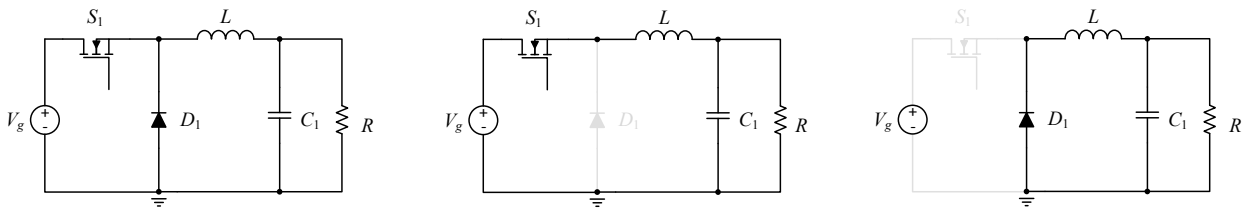

Fig. 4. Buck converter (a) the circuit diagram (b) mode 1: active switch is on (c) mode 2: active switch is off

Figure 4b shows the equivalent circuit of mode 1. During this mode, the inductor starts charging from the input source. The inductor current and output capacitor voltage are given by

$$\frac{di_L}{dt} = -\frac{1}{L}v_c \tag{1}$$

$$\frac{dv_c}{dt} = -\frac{1}{C}i_L - \frac{1}{RC}v_c \tag{2}$$

Figure 4c shows the equivalent circuit of mode 2. During this, the inductor current and capacitor voltage are given by

$$\frac{di_L}{dt} = \frac{1}{L}V_{in} - \frac{1}{L}v_c \tag{3}$$

$$\frac{dv_c}{dt} = -\frac{1}{C}i_L - \frac{1}{RC}v_c \tag{4}$$

By applying voltage second balance on inductors, one can obtain the average of (1) and (3) as well as (2) and (4) , we can get

$$\frac{di_L}{dt} = \frac{D}{L}V_{in} - \frac{1}{L}v_c \tag{5}$$

$$\frac{dv_c}{dt} = -\frac{1}{C}i_L - \frac{1}{RC}v_c \tag{6}$$

The buck converter is usually analysed using state space averaging. However, in this paper, a discrete time iterative map is used. The buck converter is controlled using valley current mode as shown in Fig.6. Discrete maps model the evolution of buck converter's state variables over discrete time steps. In this method, voltages and currents are sampled. That is, the continuous signal is reduced to a sampled signal by taking a measurement of the instantaneous value of the continuous-time signal at the selected time t. Figure 5a shows the waveforms and the process of valley current mode control. The sampled voltage and current are noted as v_n and i_n, respectively, where v_n and i_n are at the beginning of n^{th} sample, and v_{n+1} and i_{n+1} are at the n^{th} end of the n^{th} sample, as illustrated in Fig. 5a. In this paper, the buck converter must work in continuous conduction mode, where the average value of inductor current is always bigger than its peak-peak value. In other words, the inductor current must not hit zero. To ensure operating in CCM mode, the inductor value must be higher than the minimum inductance, which is given by

$$L_{min} = \frac{(1-D_{min})R_{L,max}}{2f_s} \tag{7}$$

where D_{min} is the minimum duty cycle, and $R_{L,max}$ is the lightest output load (maximum output resistance).

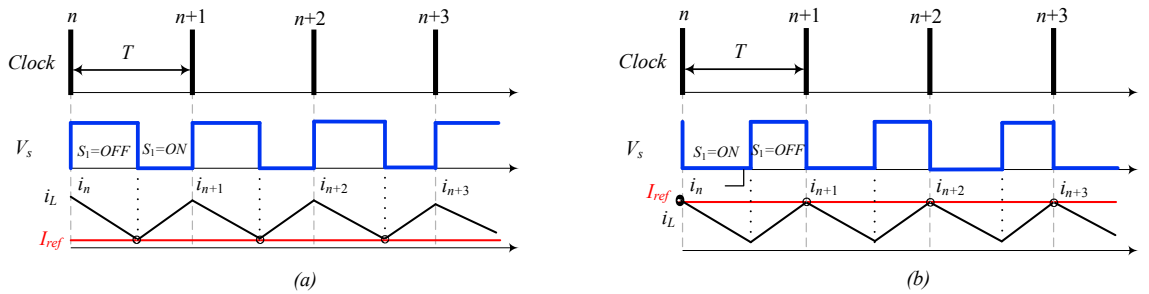

Fig. 5. Current mode control waveform (a) valley (b) peak

During mode 2, the switch is disconnected, and the output inductor will be discharged. Therefore, the inductor current decreases as a result. The duration of mode 2 can be can be calculated using (8).

$$\Delta_n = \frac{L(i_n - I_{ref})}{v_n} \tag{8}$$

The capacitor voltage at $nT+\Delta_n$ is given by

$$v_c(\Delta_n) = e^{-\alpha\Delta_n}\left[v_n\cos(\omega\Delta_n) + \left(\frac{1}{\beta C}i_n - \frac{\alpha}{\beta}v_n\right)\sin(\omega\Delta_n)\right] \tag{9}$$

where $\alpha = \frac{0.5}{RC}$ and $\beta = \sqrt{\frac{1}{LC} - \alpha^2}$. To plot the discrete map of the controlled buck converter, we need to derive the discrete model in two cases: when $\Delta_n > T$ and when $\Delta_n < T$. If $\Delta_n > T$, the active switch will stay off, and the inductor current will start decreasing. The state variables in this case can be given by

$$i_{n+1} = e^{-\alpha\Delta_n}\left[i_n \cos(\beta\Delta_n) + \left(\frac{\alpha}{\beta} i_n - \frac{1}{\beta L} v_n\right)\sin(\beta\Delta_n)\right] \tag{10}$$

$$v_{n+1} = e^{-\alpha\Delta_n}\left[v_n \cos(\beta\Delta_n) + \left(\frac{1}{\beta C} i_n - \frac{\alpha}{\beta} v_n\right)\sin(\beta\Delta_n)\right] \tag{11}$$

If $\Delta_n < T$, then the switch will start conducting and the inductor current will start increasing. The state variable in this case can be given by

$$i_{n+1} = e^{-\alpha(T-\Delta_n)}\left[\left(I_{ref} - \frac{V_{in}}{R}\right)\cos(\beta(T-\Delta_n)) + \left(\frac{\alpha}{\beta}\left(I_{ref} - \frac{V_{in}}{R}\right) + \frac{V_{in} - v_C(\Delta_n)}{\beta L}\right)\sin(\beta(T-\Delta_n))\right] + I_o \tag{12}$$

$$v_{n+1} = e^{-\alpha(T-\Delta_n)}\left[\left(v_C(\Delta_n) - V_{in}\right)\cos(\beta(T-\Delta_n)) + \left(\frac{\alpha}{\beta}\left(v_C(\Delta_n) - V_{in}\right) + \frac{I_{ref}R - v_C(\Delta_n)}{\beta RC}\right)\sin(\beta(T-\Delta_n))\right] + V_{in} \tag{13}$$

where $I_o = \frac{V_o}{R}$.

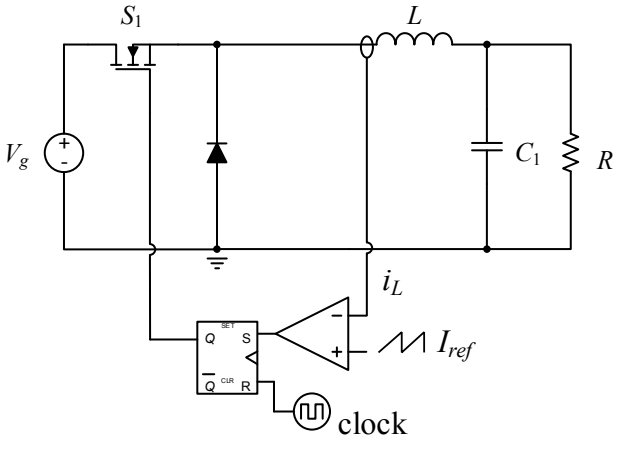

Fig. 6. Valley mode current control

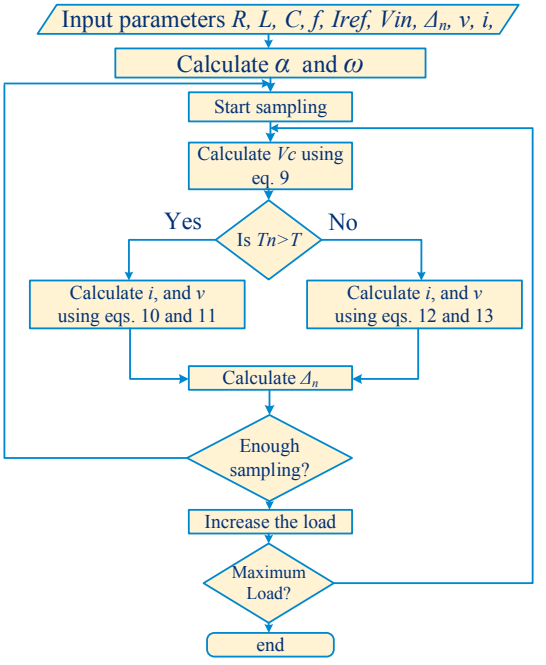

Fig. 7. Flowchart of bifurcation diagram

To obtain the bifurcation plot, one has to follow the procedure explained by the flowchart in Fig 7. Having done simulation, the discrete modeling is completed. Figure 8 shows the bifurcation diagram obtained by varying the output load and reference current. The parameters used in the simulation are given in Table 1. From Fig. 8, one can see that the border collision occurs when R=10. Then, the converter starts exhibiting chaotic behavior when the output resistance decreases. The bifurcation diagram looks different when varying reference current. The period

doubling occurs at I_{ref}= 0.72 A. The chaos occurs at lower reference current. With varying circuit parameters, the buck converter has routes to chaos [6]

Table 1: Simulation parameters of buck converter

V_{in}	12 V
L	600 μF
C	200 μF
Frequency	50 kHz
I_{ref}	6 A

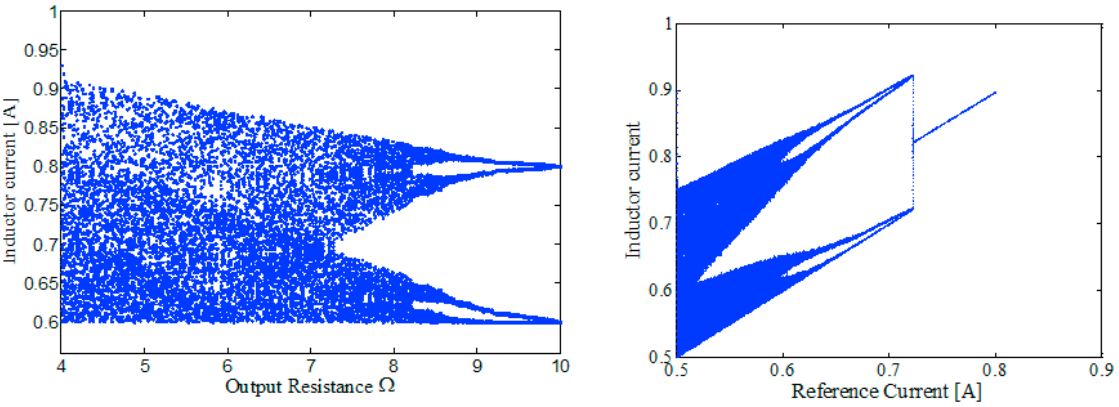

Fig. 8. Bifurcation of the buck converter with varying the output resistance and with varying the reference current

3. Example of an interleaved high-gain dc-dc boost converter

Interleaved high-gain dc-dc converters have smooth input current and high voltage gain. The converter shown in Fig. 9. will be analyzed, and the steady-state voltage gain will be derived for N number of stages. This converter was used in [17] to interface a photovoltaic panel to a distribution bus. The proposed converter has three modes of operations. The switching pattern is given in Fig. 10. The components of this converter were assumed to be ideal, and the duty cycles are equal d_1=d_2=D. Figure 11 shows the converter with two-stage voltage multiplier cell. The converter has three modes of operation. Mode 1 is when both switches are ON. In this mode, all diodes are OFF, they are reversed biased, and the load is supplied by C_5. The equivalent circuit of mode 1 is shown in Fig.11a. The voltage across inductor is given by

$$L_1 \frac{di_{L_1}}{dt} = L_2 \frac{di_{L_2}}{dt} = V_{in} \tag{14}$$

Mode 2 is when S_1 is on and S_2 is off. The equivalent circuit of this mode is shown in Fig. 11b. During this mode, the diodes D_1, D_3, D_4, and D_6 are ON, and diodes D_2 and D_5 are OFF. The load, in this mode, will be fed by capacitors C_3, C_5, and C_6. The voltage across inductors is given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} \tag{15}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{in} - v_{C_1} = V_{in} - v_{C_2} \\ = V_{in} - v_{C_1} - v_{C_2} - v_o + v_{C_3} + v_{C_4} \tag{16}$$

In mode 3, S_1 is OFF and S_2 is ON. The equivalent circuit of this mode is shown in Fig. 11c. In this mode, diodes D_1, D_3, D_4, and D_6 are OFF, and diodes D_2 and D_5 are ON. The output load in this case will be fed by C_5, similar to mode 1. The voltage across inductors is given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} + v_{C_2} - v_{C_4} + v_{C_1} \\ = V_{in} + v_{C_2} - v_{C_3} + v_{C_1} \tag{17}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{in} \tag{18}$$

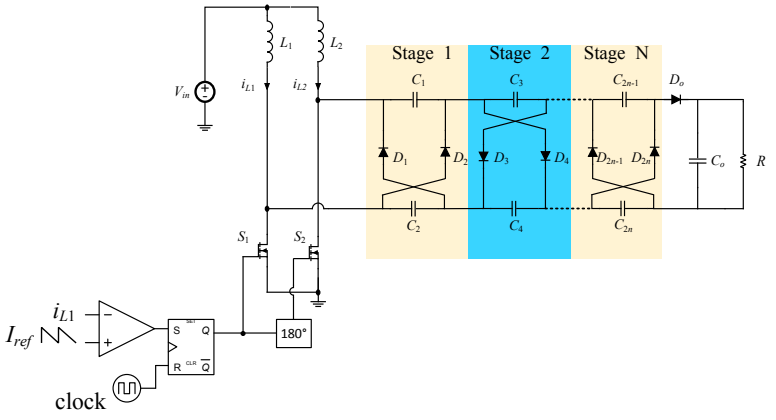

Fig. 9. Interleaved boost converter with N number of voltage multiplier cell

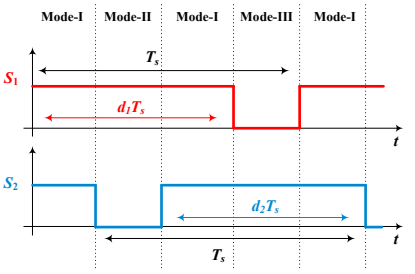

Fig. 10. Switching pattern of the converter

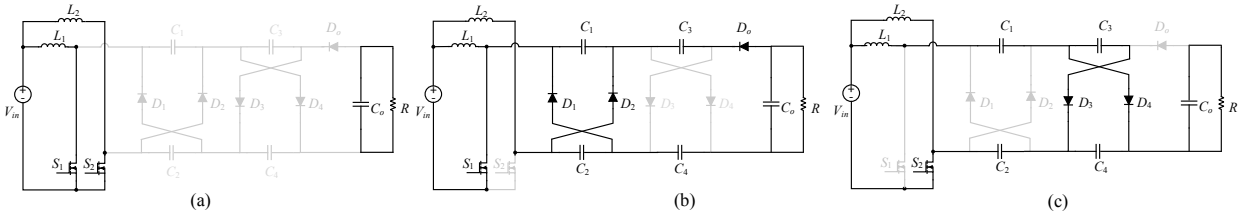

Fig. 11. The proposed converter with its three different modes of operation (a) first mode (b) second mode (c) third mode

The steady state voltage gain of interleaved boost converter with two-stage voltage multiplier is given by

$$\frac{V_o}{V_{in}} = \frac{5}{1-D} \tag{19}$$

For N number of stages, the voltage gain is given by

$$\frac{V_o}{V_{in}} = \frac{2N+1}{1-D} \tag{20}$$

The chaotic behavior of this converter was simulated using PLECS blockset with MATLAB. The trajectory of the open loop interleaved boost converter was plotted at different output loads, as shown in Fig. 12. The trajectory takes a longer time to reach steady state at lower loads. At higher output load, the inductor current increases and reaches the steady state faster. Figure 13 shows the bifurcation diagram of the interleaved boost converter with both one and two stages of voltage multiplier cell. From Fig. 13., one can see that period doubling occurs at 1.95A for interleaved boost converter with one stage, while period doubling occurs at higher reference current. Therefore, adding extra stage moves the chaotic region to the higher reference current.

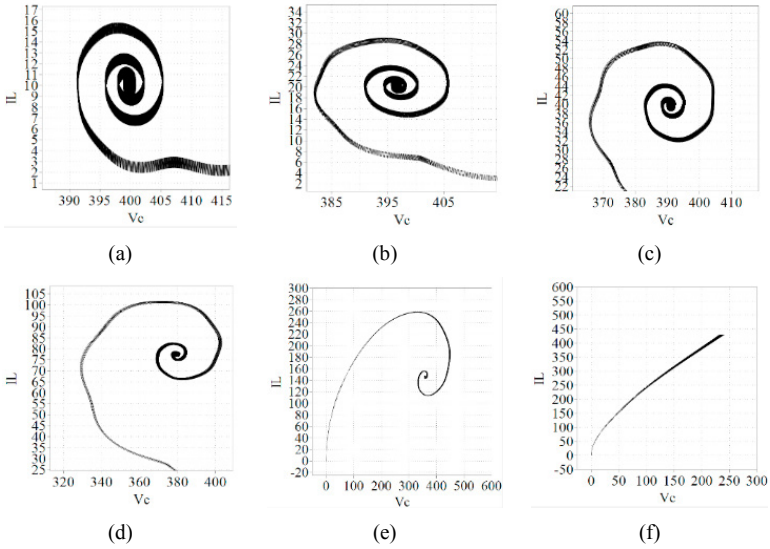

Fig. 12. The phase portrait for different load (a) *P*= 200 *W* (b) *P*= 400 *W* (c) *P*= 800 *W* (d) *P*= 1600 *W* (e) *P*= 3.2 k*W* (f) *P*= 9 k*W*

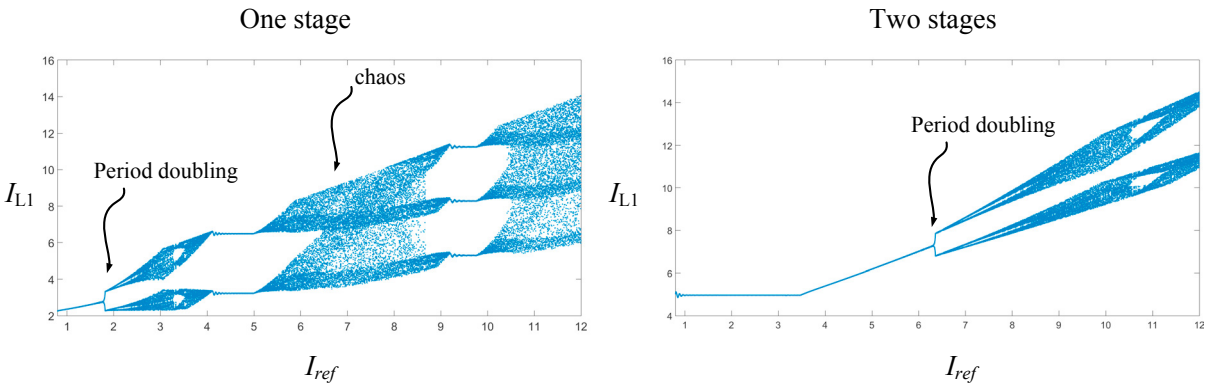

Fig. 13. Bifurcation diagram of high gain dc-dc converter with one-stage voltage multiplier cell (left) and two-stage voltage multiplier cell (right)

4. Conclusion

In this paper, a chaotic behavior in high gain dc-dc converters was explored. The discrete map model for current mode was both derived and simulated. Different parameter variations were studied such as load resistance and reference current. The bifurcation diagram was plotted, and stability was investigated. The interleaved high gain dc-dc converter exhibits chaotic behavior through period-doubling and border collision routes. The stability region of interleaved boost converter is narrower than the one of the conventional boost converter. The advantage of the high gain dc-dc converter over the conventional boost converter is that the input current ripples are lower, and it has lower voltage stress across its switches. Future work includes obtaining the discrete map model for the high gain dc-dc converter and implementing the converter experimentally.

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