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# Electromagnetic compatibility in power inverter design

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# ELECTROMAGNETIC COMPATIBILITY IN POWER INVERTER DESIGN

by

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## PUBLICATION DISSERTATION OPTION

This dissertation has been prepared in the form of four papers for publication.

The first paper, from pages 4 to 30, presents A Measurement-Based Model of the Electromagnetic Emissions from a Power Inverter. This extended work has been accepted for publication with the IEEE Transactions on Power Electronics. The second paper, from pages 31 to 61, presents the Development of Simple Physics-Based Interconnect Models for Power Electronics, and is to be submitted to IEEE Transactions on Electromagnetic Compatibility. The third paper, from pages 61 and 74, presents Prediction of Common-Mode Current Reduction Using Ferrites in Systems with Cable Harnesses, and has been published in the Proceeding of the IEEE EMC Symposium 2012, Pittsburgh, August 2012, pp. 80-84. The fourth paper, from pages 74 to 100, presents a Common-mode Impedance of a Ferrite Choke on a Cable Harness, and has been submitted to IEEE Transactions on Electromagnetic Compatibility.

## ABSTRACT

Power inverter systems generate significant electromagnetic emissions. Methods were studied to model these systems and to reduce their emissions. Three topics are presented in this dissertation.

Methods were developed to obtain simple SPICE models for complex systems which relate circuit components to physical geometry within the system. These models were derived using measurements or using partial element equivalent circuit (PEEC) and model size reduction techniques developed in this dissertation. Methods were proposed for developing a measurement-based model and were applied to a real power inverter/motor system. The model was used to identify system geometries responsible for critical resonances and to guide development of emission reduction strategies. A method was also proposed for developing a simple SPICE circuit by collapsing the many elements in a PEEC model into a reasonable number of elements which can still be related directly to the physical geometry responsible for the parasitics. This method was validated on realistic interconnects used in power electronics based on the frequency-dependent behavior of port impedances.

Methods were also developed to predict the effects of ferrite chokes on the common-mode impedance and common-mode current of an active power systems when the ferrite is placed on the power cables. A high frequency analytical ferrite choke model was developed. Active common-mode loop impedance is found using the dual current clamp technique. The effectiveness of the approach was demonstrated on a real, active power/inverter system.

# ACKNOWLEDGMENTS

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# 1. INTRODUCTION

Electromagnetic Interference (EMI) is one of the major challenges to design of modern high power inverter/motor drive systems. EMI is mainly generated through fast switching of inverter outputs, leading to large dv/dt and di/dt components interacting with inverter parasitics to create conducted and/or radiated emissions. The switching times of the insulated gate bipolar transistors (IGBTs) in power inverters must be fast for efficiency and thermal reasons. The high values of dv/dt and di/dt cannot be easily reduced. The design of the inverter electronics, heatsink, harness and grounding structure, however, can be modified. Adding filtering or modifying the inverter parasitics can decrease the unwanted electromagnetic emissions.

While full wave modeling is accurate, applying full wave models to complex systems like power/inverters is difficult, as it requires substantial time and memory. More importantly, such simulations are often a "black box" that without additional simulations and effort generally do not help improve understanding of which parts of the system are responsible for a particular EMI problem and how to solve it. Many such systems also often contain non-linear elements that cannot be modeled easily with a full-wave solver and should be considered using circuit analysis. Thus development of a SPICE based model of the complex system is a better approach. This model should have straightforward correlation between system geometry and parasitic circuit elements. It can be used to better understand the physics behind the creation of common mode current in an inverter/motor system. Such a model can be obtained based on schematics, harness information, and the overall system layout (e.g. the IGBT, heatsink, and enclosure geometry). Parasitic inductive and capacitive elements inside the inverter are needed for this SPICE model.

One of the well-known methods to extract SPICE elements from complex geometries is the PEEC method, where a problem is transferred from the electromagnetic domain to the circuit domain. Generally with the PEEC approach many (sometimes thousands) of extracted parasitic L and C elements are obtained. This is too many elements for a basic understanding of the system, so some reduction is required. Some known model order reduction (MOR) techniques help to obtain an equivalent circuit representation, but these

circuits are purely functional and do not provide physical insight into the device. Another approach is obtaining an equivalent model based on measurements or combination of measurements and full-wave simulations.

In this dissertation two approaches to obtain such model are presented: a measurement-based method and a method using PEEC followed by developed physics-based model size reduction (PMSR) technique. The first method involves dividing the system into a number of subsystems and obtaining simple equivalent elements from step by step measurements. This method allows one to obtain rather simple equivalent model without 3D modeling. The second approach requires development of PMSR technique to collapse the many elements obtained using PEEC into a reasonable number of elements which can still be related directly to the physical geometry responsible for the parasitics. In both cases the resulting simplified model will have similar basic topology containing only a few circuit elements and the real geometry will be correlated to these elements. Both approaches are validated through experiments and full-wave modeling. Further the obtained SPICE models can be used to better understand the physics behind the creation of common mode current in an inverter/motor system.

Another contribution of the work is the introduction of a methodology to predict the effects of ferrite chokes on the common-mode impedance and common-mode current of active power electronics systems when the ferrite is placed on the cable harness. The method is based on combination of high frequency analytical ferrite choke model and dual current clamp measurement technique for common-mode loop impedance. Effectiveness of the approach is demonstrated on a real active power/inverter system.

The main contributions of the dissertation include:

A methodology is developed to obtain relatively simple measurement-based SPICE models of complete power systems with clear correlation between system geometry and circuit elements (paper 1).

The methodology is validated on a real power inverter system up to 100 MHz (paper 1).

The equivalent model is analyzed to determine possible causes of radiated emissions (paper 1).

Recommendations are made based on the SPICE model to mitigate main resonances of the system (paper 1).

Effectiveness of proposed countermeasure techniques is demonstrated (paper 1).

Prediction of reduction in radiated emissions with presence of mitigation techniques is shown (paper 1).

A methodology is developed to obtain simple physics-based SPICE circuit from large PEEC models, where there is a clear correlation between geometry and parasitic circuit elements (paper 2).

With the method the number of inductors and capacitors is reduced separately, which helps to ensure physicality of the reduced model (paper 2).

An approach to deal with model reduction containing a closed loop is introduced (paper 2).

Methodology is applied to a simple power electronics component (paper 2).

Error estimation of the reduced model is done using port impedance (paper 2).

The approach can potentially allow an easy combination of both the macro- and micro-models (paper 2)

A methodology is developed to predict effect of a ferrite choke on common-mode current and common-mode impedance of power inverter systems (paper 3, paper 4).

A high frequency analytical model of a ferrite choke is derived using transmission line model quasi static approximation (paper 4).

Application of the dual current clamp for predicting impact of a ferrite is considered (paper 3, paper 4)

The method is validated on simple passive structures and active real power inverter/motor system. The prediction agrees with measurements within 3 dB (paper 3, paper 4).

PAPER

# I. A MEASUREMENT-BASED MODEL OF THE ELECTROMAGNETIC EMISSIONS FROM A POWER INVERTER

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***Abstract***—Rapidly switching semiconductors in modern high power inverter/motor-drive systems generate fast changing voltages and currents which may result in unwanted emissions. While models of power inverters have been built in the past to predict emissions, they are typically "black box" models where the cause of and solution to emissions problems is difficult to analyze. To improve inverter system design strategies, a detailed measurement-based SPICE model of a power inverter system was built in which there is a straightforward correlation between system geometry and parasitic circuit elements. This model was validated through measurements. The model was able to predict transfer characteristics between ports of the inverter within 4 dB from 100 kHz to 100 MHz. Once built, this model was used to identify structures responsible for resonances and to determine possible improvements of the power inverter design to reduce emissions. Measurements of S21 and radiated emissions after adding these improvements demonstrated that they were able to reduce emissions by 10-20 dB, thus confirming the accuracy of the model and its ability to improve understanding of emission mechanisms and to guide development of emissions reduction strategies.

***Index Terms***— Electromagnetic interference (EMI), electromagnetic modeling, parameter estimation, variable speed drives, electromagnetic radiation

## I. INTRODUCTION

Electromagnetic Interference (EMI) is a major challenge to design of modern high power inverter/motor drive systems. EMI is mainly generated through fast switching of inverter outputs. Large dv/dt and di/dt components in the output interact with inverter parasitics to create conducted and/or radiated emissions [1]-[3]. The switching times of

the insulated gate bipolar transistors (IGBTs) in power inverters must be fast for efficiency and thermal reasons, so the high values of dv/dt and di/dt cannot be easily reduced. The design of the inverter electronics, heatsink, harness and grounding structure, however, can be modified and filtering can be added to reduce electromagnetic emissions. Ideally, the impact of such mitigation techniques could be evaluated early in the design process through accurate models of the system.

While full wave models are accurate, applying full wave models to complex systems like a power inverter is difficult, as they require substantial computational time and memory [4], [5]. More importantly, such full wave models are often a "black box" that does not directly show which parts of the system are responsible for a particular EMI problem or how to solve the problem without additional simulations and effort. Models of inverters also often require non-linear elements that cannot be modelled easily with a full-wave solver and should be considered using circuit analysis. An equivalent SPICE based model which includes the system parasitics is a better approach, since it can give a straightforward correlation between system geometry and parasitic circuit elements and the resulting common-mode currents.

A SPICE based model can be obtained from schematics, harness information, and system layout (e.g. the IGBT, heatsink, and enclosure geometry). Several methods are available for extracting parasitic SPICE parameters from a complex geometry [6]-[8]. Many of these methods are based on 3D finite-element analysis [4],[5] or the partial element equivalent circuit (PEEC) method [9]-[12]. The output from finite-element analysis is not typically a simple SPICE circuit but a black box measure of circuit characteristics, for example the S parameter values between two ports. The PEEC approach provides a SPICE model of parasitics in terms of RLGC matrices, but may require hundreds or thousands of elements to represent even a simple geometry, which is too many for an intuitive understanding of how the circuit works. Model order reduction (MOR) techniques may help provide an equivalent circuit representation [13], but these circuits are purely functional and, like the S parameters, do not provide significant physical insight into the inner workings of the device. In [14], equivalent SPICE circuit elements are determined from Z-parameters found from 3D full-wave models. While the

resulting circuit is useful, modelling the complete power inverter (whose precise geometry may be unknown) requires substantial time and effort.

Parasitics may also be obtained through measurements or a combination of measurements and full-wave simulations. One approach is to use Time Domain Reflectometry (TDR) and transmission line theory to extract parasitics [15]. This approach is limited by the ability to accurately extract parasitics which may be much larger or smaller than 50 ohms. Impedance measurements were similarly used in [16] to determine equivalent circuits for some inverter modules. In another recent study [17] a measurement-based inverter model was presented, where scattering parameters were converted to equivalent common mode (CM) and differential mode (DM) impedances. Although the model is based on measurement, it is still a "black box" model of the inverter which does not represent specific parasitics. A study is presented in [18] which develops a low-frequency parameter-based model of induction machines using DM and CM impedance measurements. A number of other studies [4], [19]-[20] have demonstrated the usefulness of using a combination of measurements and simulations.

Existing studies lack the development of a simple model for a complete power inverter system and do not demonstrate how to use this model to reduce radiated emissions. A methodology is presented in the following paper to build a rather simple, yet accurate, equivalent model of a real power inverter which has a clear correlation between parasitic circuit elements and system geometry. The method is applicable up to 100 MHz, which is above the frequency where problems are typically seen in power inverter systems, and was the maximum frequency of interest specified by our industry partners. For this application, the power inverter and attached motor (Fig. 1) was divided into subsystems representing the DC cables, DC link capacitance block with DC bus bars, IGBT module, AC bus bars, AC cables, and motor/load. A simple equivalent model was built for each subsystem and validated through measurements. The subsystem models were assembled to create a model of the complete system. This relatively simple model was used to find the system components responsible for the most important resonances and then, based on the understanding of these resonances, to demonstrate how changes could be made to the system to mitigate these resonances. The effectiveness of the

mitigation strategies was demonstrated through measurements of the output voltage and radiated emissions.

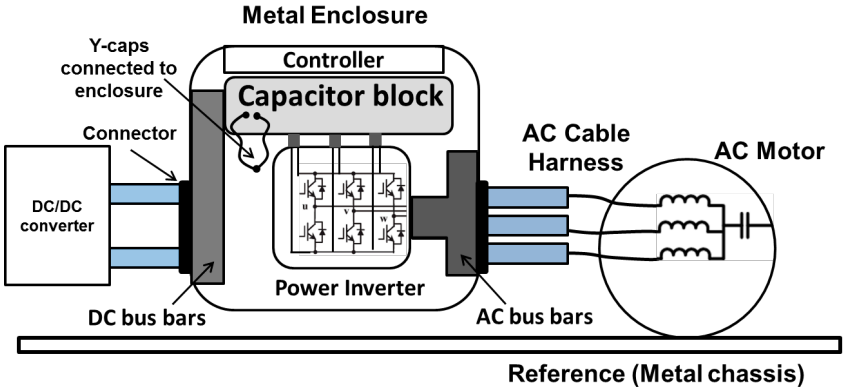



Fig. 1. Power inverter/motor system.

## II. CONSTRUCTION OF THE EQUIVALENT CIRCUIT

An example of the power inverter/motor system is shown in Fig. 1. The equivalent circuit should include information about the cables (both DC and AC), parasitic inductances of the Y capacitors, parasitic inductances due to the DC link capacitor, inductances due to the terminals of the IGBT module, the capacitances between the IGBT and chassis, and the high-frequency impedance of the motor (or dummy load). As the Pulse Width Modulated (PWM) inverter structure is symmetrical, it is only necessary to model the behaviour of one inverter leg.

The inverter under study is housed in a metal enclosure (Fig. 2) and generally well shielded from its environment. All power cables going in or out of the enclosure are shielded, with the shields making a good 360° connection at the enclosure. The one location where there is a good potential to drive parasitic antennas and cause radiated emissions is at the connection between the AC cables and the motor. While a good 360° connection of the shield at this location may be used, in many cases a long pigtail is used to connect the shield to the motor housing. Even with a good connection, the RF shielding within the motor itself is highly variable. Because the cable connection to the motor is the only place where emissions may reasonably be generated by this well-shielded device, the voltage between the inner conductor and shield of the AC cable at

the connection to the motor was used as a reference when proposing schemes to mitigate emissions. Later measurements confirm the suitability of this approach.

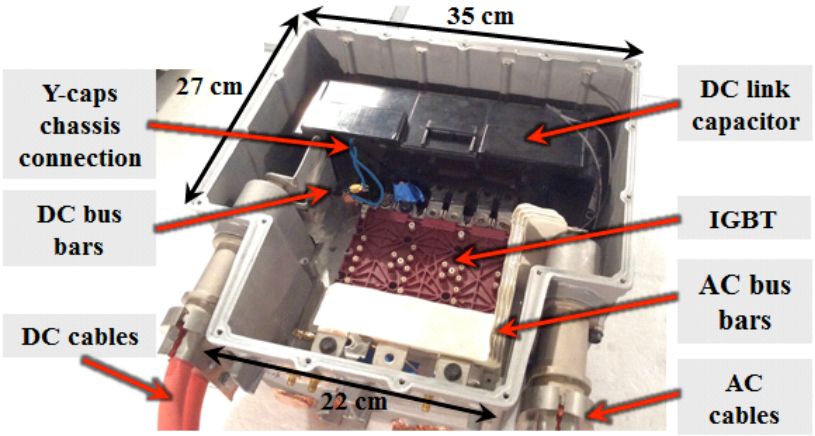



Fig. 2. Power inverter enclosure with DC link capacitor, DC bus bars, IGBT and AC bus bars.

A simple model of the IGBT is illustrated in Fig. 3. For each IGBT phase leg there are parasitic capacitances from the emitter to chassis, from collector to chassis and from phase (the emitter/collector node) to chassis. Most emissions are expected to result from the voltage between the phase node and chassis, since the switching occurs at this node and this common-mode voltage can directly drive a voltage between the center conductor and shield of the AC cable at the motor connection.

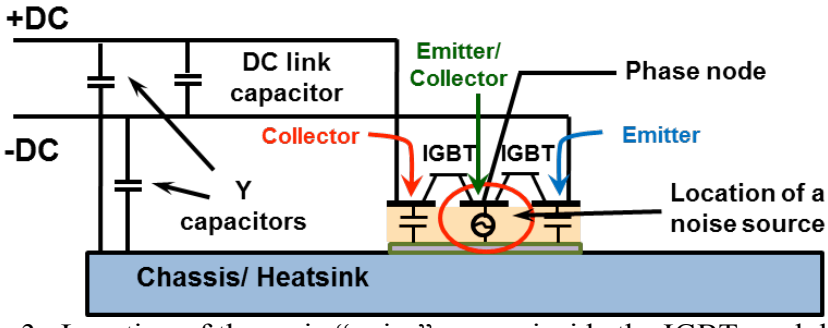



Fig. 3. Location of the main "noise" source inside the IGBT module.

The parasitic antenna that drives emissions is primarily composed of the shields of the cables and the motor and inverter housings. The characteristics of this antenna cannot be changed significantly during testing, since standards specify the placement of these

components. Since this antenna is driven primarily by the voltage at the end of the AC cable, and this voltage results primarily from the voltage between the IGBT phase node and chassis, the value of S21 between the phase-node-to-chassis voltage and the center-conductor-to-shield voltage of the AC cable connection to the motor is critical to understanding and mitigating emissions mechanisms.

### *A. AC and DC cables*

The DC and AC cables were modelled as transmission lines. This model requires information like the characteristic impedance, dielectric constant of the insulation and loss tangent. The datasheet provided only geometrical information, so measurements were made with a Time Domain Reflectometer (TDR) and a Vector Network Analyzer and parameters were determined from the measurements. Fig. 4 shows a comparison of the predicted and measured impedance, where simulations were performed using a transmission line model of a 1.86 m long cable with $Z_0 = 8.56\,\Omega$, $\varepsilon_r = 2.65$, and loss tangent of 0.108. A 4 nH parasitic inductance was placed in series with the cable to model the SMA connector used to make the measurement.

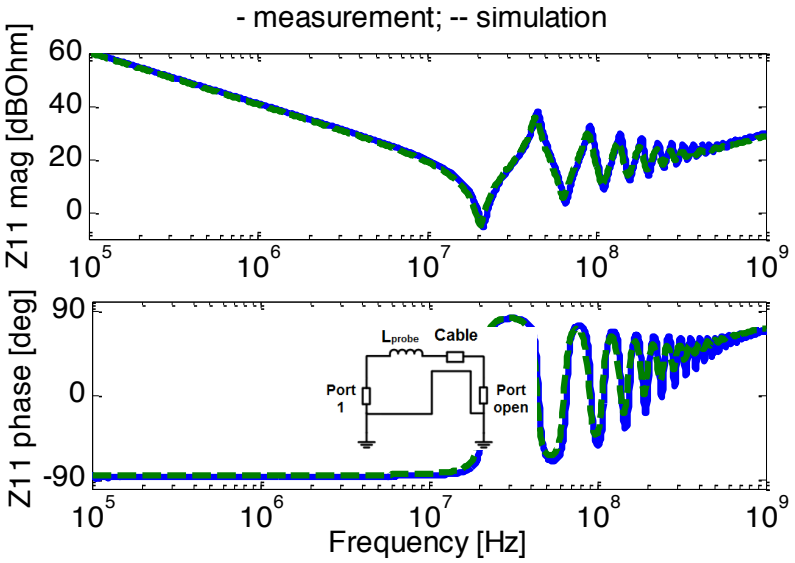



Fig. 4. Validation of the transmission line model for the open ended DC cable. Measured values are shown with a solid line and simulated values with a dashed line.

The DC link capacitor block consists of a DC link capacitance (with nominal C=1028 μF) and two Y-capacitances (with nominal C=0.98 μF), as illustrated in the model shown in Fig. 5. This circuit template was constructed with some information of circuit geometry. Parameter values could then be filled in later through measurements. While inductance is a property of loops, an approximate model was constructed using partial inductances. The inductances $L_{DC\ bus\ bar}$ and $M_{DC\ bus\ bar}$ are due to the bus bars of the capacitor block, L2 and $L_{Link}$ are parasitic inductances associated with the link capacitor, $L_{y\text{-}cap}$ and $M_{y\text{-}cap}$ are associated with the Y-capacitors, and L3 is the inductance due to the output of the capacitor block (where it connects to the IGBT module). The simple model without mutual inductances was used initially, but later it was found useful to split $L_{DC\ bus\ bar}$ between the DC+ and DC- buses, and to include the mutual inductance between the buses. The mutual inductances help to differentiate between the impedance seen by common mode and differential mode currents.

*B. DC Link*

Measurements of the DC link capacitor block were performed with the capacitor block alone and also with the block connected to the DC cable to determine the values of the parasitic inductances due to Y-capacitors and DC bus bars. A number of Z11 and Z22 measurements were performed while other ports were made open or short. The value of Z11 looking into the Y-capacitors was also obtained by measuring impedance between one of the Y-capacitor connections and the chassis. The values of the parasitic inductances could not be determined from a single measurement, but could be determined mathematically from the set of measurements. The measurements and associated equations are illustrated in Table 1, where parameters used in the equations are given in Fig. 5.

Table I

Equations Describing DC link Capacitor Block Inductances

| Measurement | Equation |
|---|---|
| DC cable, DC link block, Y-caps | $L_{@1MHz} \approx L_{DC\ cable} + L_{DC\ bus\ bar} + \frac{L_{Y-cap} + M_{Y-cap}}{2}$ |
| DC cable, DC link block, | $L_{@2MHz} \approx L_{DC\ cable} + L_{DC\ bus\ bar} + L_2 + L_{Link}$ |
| DC link, looking into Y-caps | $L_{@10MHz} \approx 2(L_{Y-cap} - M_{Y-cap}) + L_2 + L_{Link}$ |
| DC link input shorted, Y-caps open | $L_{@14MHz} \approx L_3 + L_{Link} \parallel (L_{DC\ bus\ bar} + L_2)$ |
| DC link, Y-caps open | $L_{@11MHz} \approx L_3 + L_{Link}$ |

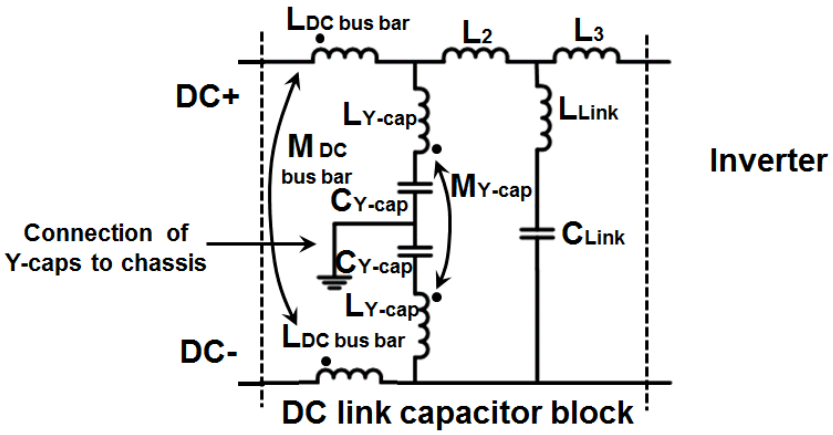



Fig. 5. Schematic of DC link.

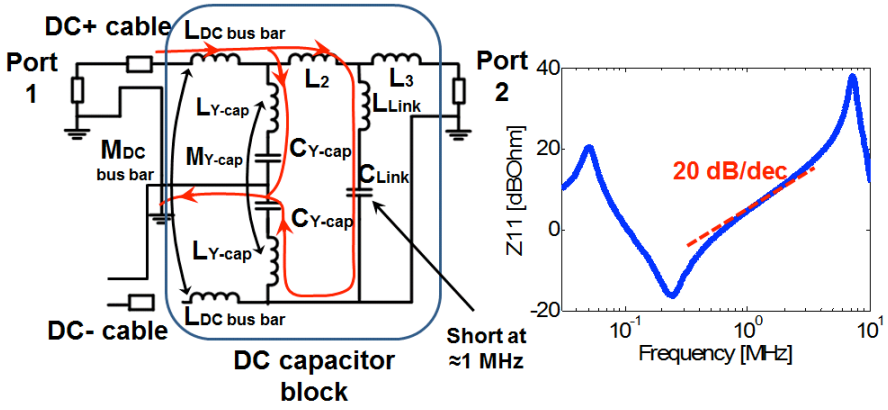
Example measurements are demonstrated in Fig. 6. In the measurement in Fig. 6a, Port 1 is at the beginning of the DC+ cable and Port 2 is at the output of the DC capacitor block. The DC- cable is not connected. The Y-capacitors are connected to the chassis. The shields of both DC cables are connected to the enclosure. At about 1 MHz the capacitance due to the DC block ($C_{Link}$=1028 μF) looks like a short, the current returns to the chassis through both Y-capacitors, and the input impedance is equivalent to a 272 nH inductor. Tracing the currents during the Z11 measurement at this frequency gives:

$$L_{1MHz} \approx L_{DC+cable} + L_{DC\ bus\ bar} + \frac{L_{Y-cap} + M_{Y-cap}}{2} \approx 272\ \text{nH}. \quad (1)$$

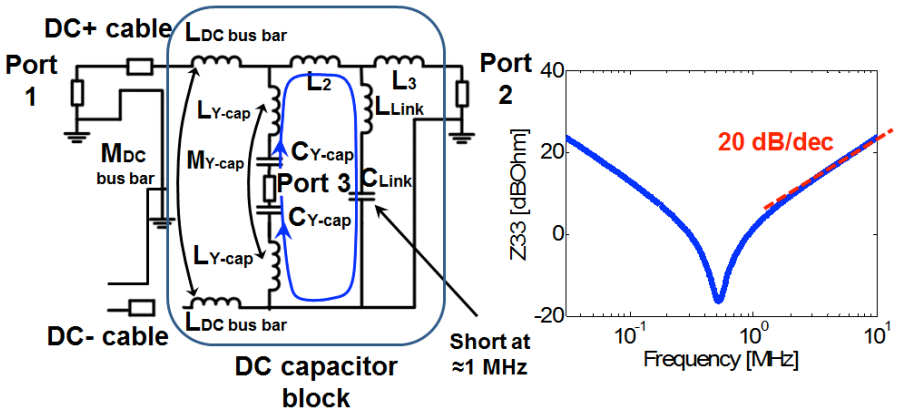
An additional measurement of the $L_{Y\text{-}cap}$ inductance is made by breaking the connection of one Y-capacitor to the chassis, and measuring the impedance looking into the Y-capacitor break, as shown in Fig. 6b. Tracing this impedance at10 MHz gives,

$$L_{10MHz} \approx 2\left(L_{Y-cap} + M_{Y-cap}\right) + L_2 + L_{LINK} \approx 214\ nH\ . \tag{2}$$

Using these equations (along with other measurements), the mutual inductance $M_{Y\text{-}cap}$ was found to be 108 nH, and the self inductance associated with each Y-capacitors to be about 150 nH. As demonstrated by the relative size of $M_{Y\text{-}cap}$ and $L_{Y\text{-}cap}$, the mutual inductance could not be ignored. The importance of mutual inductances between busses was noted on several occasions while developing the model.




(a)




(b)

Fig. 6. Example measurement made to obtain the DC link capacitor block parasitics (a) from connected DC+ cable, DC link and Y-caps connected to chassis, at 1 MHz and (b) from impedance looking into Y-caps at 10 MHz.

*C. IGBT*

To model the IGBT module, two Z11 measurements were made looking into the output of the module while the input was open or short. These measurements were used to determine the IGBT junction capacitance and the loop inductance due to the IGBT bus bars (provided this inductance is not dominated by the inductance of the probe used to make the measurement). The measured junction capacitance across both the pull-up and pull-down IGBTs when the DC- and DC+ terminals were shorted was about 13 nF, as illustrated in Fig. 7. The IGBT bus bar inductance was determined from a Z11 measurement looking into the IGBT when a return was provided using a large metal plate. This measurement gives an estimate of the loop inductance associated with one phase leg of the IGBT module. This inductance was found to be approximately 26 nH. The measured parasitic capacitance from the phase node to chassis (across the direct bonded copper substrate) was measured using an LCR meter. The measured value was about 850 pF. This capacitance is a distributed capacitance (from collector to chassis, from emitter to chassis and from the phased node to chassis) as shown in Fig. 3. From the size of the plates collector, emitter, and phase nodes plates in the IGBT, and the measured total capacitance, the size of each parasitic capacitances was estimated to be 412 pF, 380 pF and 89 pF, as shown in Fig. 7 [16]. As will be demonstrated later, it is the total value of capacitance, 850 pF, which is critical to resonances in the circuit.

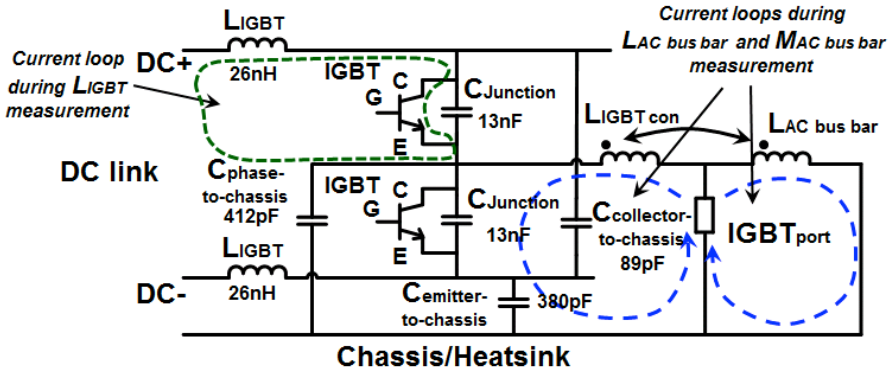



Fig. 7. Equivalent model of one phase of the IGBT module, IGBT connection and AC bus bar.

*D. AC bus bars*

To estimate the loop inductance associated with the AC bus bars, which carry current from the output of the IGBT to the AC cables (Fig. 2), a measurement of Z11 looking into the output of the IGBT module was made while its input was open and the end of AC bus bars was shorted to the enclosure. This setup creates two current loops: one from the input port through the AC bus bars and chassis and another loop from the input port through the IGBT connection, through the parasitic capacitance to the chassis as indicated in Fig. 7. These currents must return to Port 1 through a metal connector approximately 2 cm long (connecting the SMA connector to the chassis). The shared return path through the connector creates a large mutual inductance between the loop associate with the AC bus bar and the loop associated with the IGBT connection. The partial self-inductances were directly extracted from Z11 and are about 130 nH and 25 nH respectively. The mutual term was approximated from a measurement of S21 for a port between the phase node to chassis and a port at the end of the AC cable. As the length of the metal connector is about 2 cm, the mutual inductance should be around 10-20 nH. The mutual inductance was found to be about 12 nH by comparing the simulated and measured values of S21 while tuning the mutual inductance.

*E. Complete system*

The model of the complete circuit was assembled from the models of the individual subsystems, as shown in Fig. 8. This model is for a single phase leg of the IGBT and a single AC cable. The motor is not shown, since measurements determined its impedance was too large to be significant over the frequency band of interest. The values of the circuit parameters are shown in Table II.

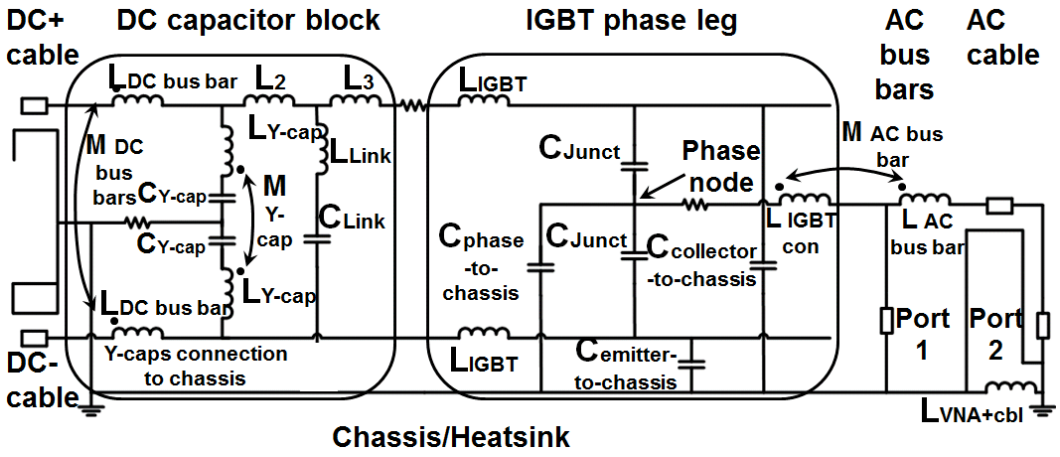



Fig. 8. Complete equivalent circuit model. Port one: between phase node and chassis, Port 2: between inner and outer conductors at the end of the AC cable.

Table II.

Values of Components within Equivalent Circuit

| Component | Value | Component | Value |
|---|---|---|---|
| $L_{DC\ bus\ bar}$ | 50 nH | $M_{DC\ bus\ bar}$ | 40 nH |
| $C_{Y-cap}$ | 700 nF | $L_{Y-cap}$ | 150 nH |
| $M_{Y-cap}$ | 108 nH | $L_2$ | 2 nH |
| $L_3$ | 12 nH | $C_{Link}$ | 1028 uF |
| $L_{Link}$ | 10 nH | $C_{Junction}$ | 13 nF |
| $L_{IGBT}$ | 26 nH | $C_{phase-to-chassis}$ | 412 pF |
| $C_{collector-to-chassis}$ | 89 pF | $C_{emitter-to-chassis}$ | 380 pF |
| $L_{IGBT\ con}$ | 25 nH | $L_{AC\ bus\ bar}$ | 130 nH |
| $M_{AC\ bus\ bar}$ | 12 nH | | |

## III. VALIDATION OF COMPLETE MODEL

Each subsystem was modelled and characterized separately because accurate models of these systems cannot reasonably be obtained using only measurements of the complete system. Characterizing the subsystems separately, however, assumes that the parasitic coupling between subsystems is small. This assumption is reasonable because of the distances between components, but must be verified through measurements of the complete, assembled system.

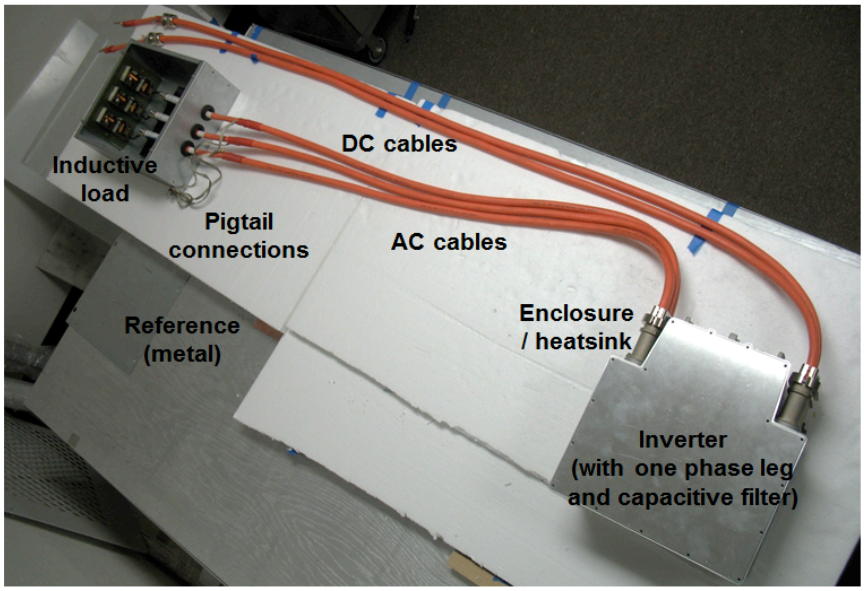



Fig. 9. Measurement setup used to validate overall inverter model.

The model was validated, in part, by comparing the input impedance and/or S-parameters at ports of both the individual subsystems as well as the overall model. The complete circuit model was validated using the experimental setup shown in Fig. 9. Port 1 was placed between the phase node and chassis (at the source of switching) and Port 2 was placed between the inner and outer conductors at the end of the AC cable (where the noise is most likely to drive radiated emissions). Comparisons of the simulated and measured transfer characteristics between these ports are shown in Fig. 10 from 100 kHz to 1 GHz. Measured and simulated values of Z11 and Z22 are presented in Fig. 11. The model describes behavior of the system at these ports within 4 dB from 100 kHz to 100

MHz. It should be noted that there is some difference in the level of S21 for frequencies higher than 100 MHz, which may be caused by parasitic couplings between the subsystems, which were not included in the model, but that become important at those frequencies.

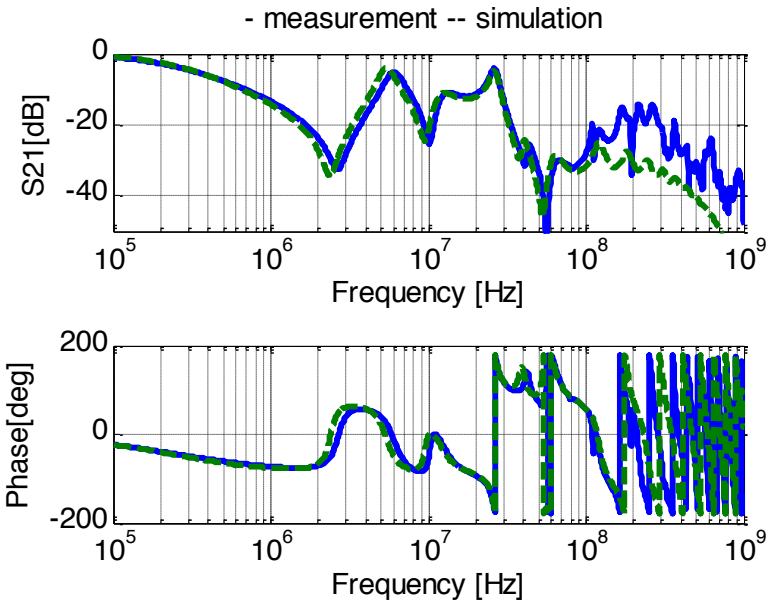



Fig. 10. Magnitude and phase of S21 between the phase node and the output of the AC cable.

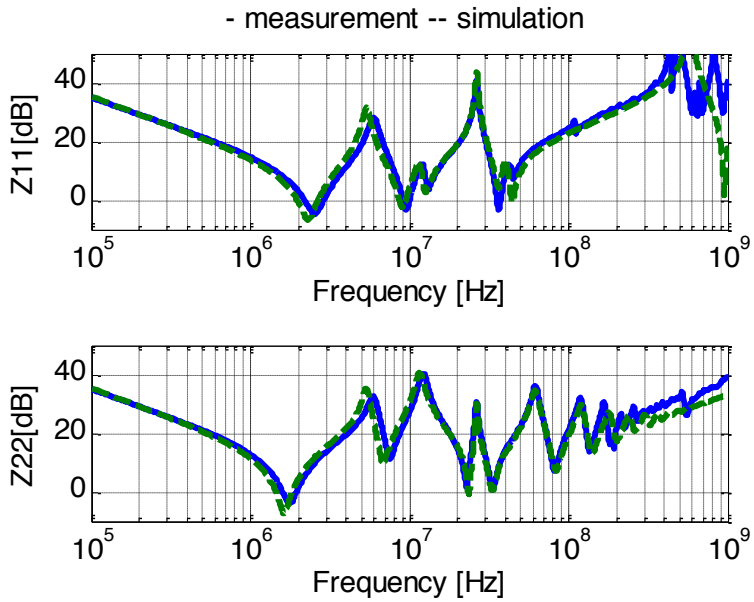



Fig. 11. Magnitude of Z11 looking into the phase node and Z22 looking into the AC cable output.

## IV. CORRELATION OF SYSTEM RESONANCES WITH GEOMETRY

A significant advantage of a simple model is that one can more easily understand the causes of specific behaviors and how to modify the system to improve this behavior. Resonances within the inverter cause peaks in the transfer characteristics from the phase node to the output of the AC cable, which may also cause peaks in the radiated emissions. If one can understand which components or current paths are involved in these resonances, one can better understand how to remove or mitigate their effect.

The most critical resonant frequencies associated with this power inverter system are around 5 MHz, 10 MHz and 30 MHz, as seen in the values of S21 in Fig. 10 and later in measurements of radiated emissions (Fig. 18). When Port 1 is between the phase node and chassis, Z11 and S21 are closely related since both are highly dependent on the impedance looking into the IGBT. Since Z11 is easier to relate to inductance or capacitance, Z11 was studied to identify causes of resonances. Fig. 12 is marked with a value of inductance or capacitance that *might* be associated with each portion of the curve. These approximations were used to help guide the analysis.

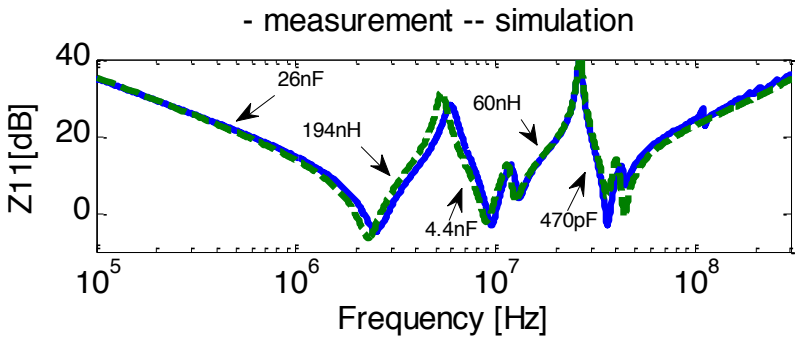



Fig. 12. Magnitude of Z11 and corresponding value of parasitics.

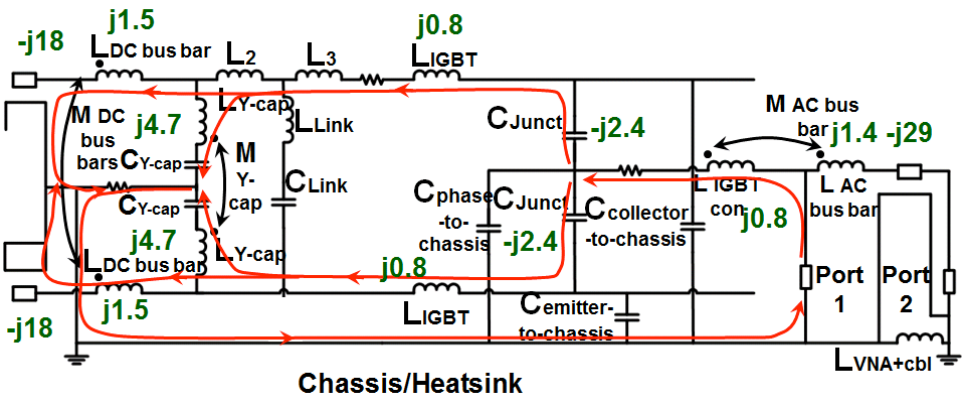



Fig. 13. Analysis of current path for one problematic frequency (5 MHz).

To illustrate the methodology used to determine the current path and elements responsible for each resonance, consider the resonance at 5 MHz. To help find the elements responsible for the resonance, the impedance of each circuit element at 5 MHz was determined as shown in Fig.13. At 5 MHz the impedance of the DC cable is about –j18 Ω:

$$Z_{DCcable} = \frac{1}{j\omega C_{cable}} = \frac{1}{j2\pi f * c_{p.u.l} * l_{cable}} \approx -j18 \text{ ohm} \qquad (3)$$

where $c_{pul}$ is the capacitance per-unit-length of the cable and $l_{cable}$ is its length. The effective impedance of the two DC cables in parallel is about –j9 Ω. If the inductance due to DC bus bars ( $j2\pi f(L+M) \approx j3 \text{ ohm}$ ) is included, the effective impedance for the DC cable and bus bars is about -j6 Ω. At 5 MHz the effective impedance associated with the two Y-capacitors in parallel is about j6 Ω:

$$Z_{Y-caps+} = j\omega(\frac{L_{y-caps}}{2} + M_{Y-caps}) \approx j6 \text{ ohm}. \qquad (4)$$

While other impedances may also play a role, the impedances of the DC cable capacitance and Y-cap inductance are sufficiently close to reliably identify these components as responsible for the resonance around 5 MHz.

A similar analysis was conducted at other resonant frequencies. The elements determined to be responsible for critical resonances are listed in Table 3.

Table III. Elements Responsible for Resonances

| Frequency | Responsible elements |
|---|---|
| Below 2 MHz | IGBT collector to emitter capacitances (26 nF total) |
| 2 MHz resonance | Collector to emitter capacitances of IGBT and inductance of Y-caps |
| 5 MHz resonance | Capacitances of DC cables and inductance of Y-caps |
| 9 MHz resonance | Transmission line resonance of DC cables and additional series inductance |
| 10 MHz resonance | Inductance of the DC bus bars and cable resonating with the capacitance looking toward the AC bus bar and cables |
| 30 MHz resonance | IGBT capacitance between the DC+, DC-, and phase nodes to the chassis (881pF) and the effective inductance of the AC + DC cables + bus bars |

## V. MITIGATION OF SYSTEM RESONANCES

The impact of resonances within the inverter can be reduced by lowering their quality factor, or in some cases by changing the frequency at which they occur (thus moving them to a frequency which is unimportant). Some possibilities for mitigating the impact of resonances at 5 MHz, 10 MHz and 30 MHz were proposed and tested.

In general, to reduce the amount of energy coupled from the noise source between the phase node and chassis to the end of the AC cables, the overall magnitude of S21 between these ports should be reduced. The equivalent model shows that any significant increase in impedance of the AC cable will reduce S21 and thus should reduce emissions.

For example, ferrites around the set of AC cables should decrease S21 since the common-mode impedance from the phase-node to motor will increase (a ferrite cannot be added to an individual cable because the high intended current would saturate the ferrite). Similarly, any significant decrease in the impedance between the AC cable and shield will reduce emissions. For example, adding a filtered connector (possibly with some losses) to the AC cable should decrease S21. While this suggestion was added for completeness, it should be noted that adding capacitance to any switching node is challenging due to the substantial current this capacitor may consume during operation.

Mitigation strategies depend on which components become important at specific frequencies. For example, at 5 MHz, where the resonance includes common-mode current through the Y-capacitors, a ferrite around the capacitor connections can be used to add loss and reduce the quality factor of the resonance. Similarly at 5 MHz, a lossy capacitive filter (connected with low inductance) could be added in front of the DC cables, with a larger capacitance than the DC cables, so the 5 MHz resonance occurs between the Y-capacitor inductance and the lossy capacitive filter, rather than the capacitance of the cables. Placing a lossy capacitor across the DC cables is reasonable since the high-frequency voltage on the DC cables is low. This resonance also involves common-mode current flowing through the DC bus-bars, which implies that a ferrite choke around the bus bars could also add loss to reduce this resonance.

A similar analysis was performed at other resonant frequencies to determine potential mitigation strategies. These strategies were tested as explained in the following section. Strategies included adding ferrite chokes to the Y-capacitors, DC bus bar, AC bus bar, and adding an RC filter to the DC cables and AC bus bar. A combination of these countermeasures (using a model of a real ferrite choke) was also investigated to demonstrate their overall impact. Individual strategies were tested through simulation. The best of the strategies were validated through measurements.

### *A. Adding low frequency ferrite chokes*

Low frequency ferrite chokes were added in simulation to the Y-capacitors, the DC bus bars and the AC bus bars. The ferrites were modeled as a simple parallel RLC circuits, with an associated mutual inductance with the circuit sharing the choke. Values

of R, L, and C were chosen similar to parameters for commercially available ferrites (R=20 Ω, L=12 uH and C=2 pF). The ferrite choke significantly reduced the peak values of S21 as demonstrated in Fig. 14.

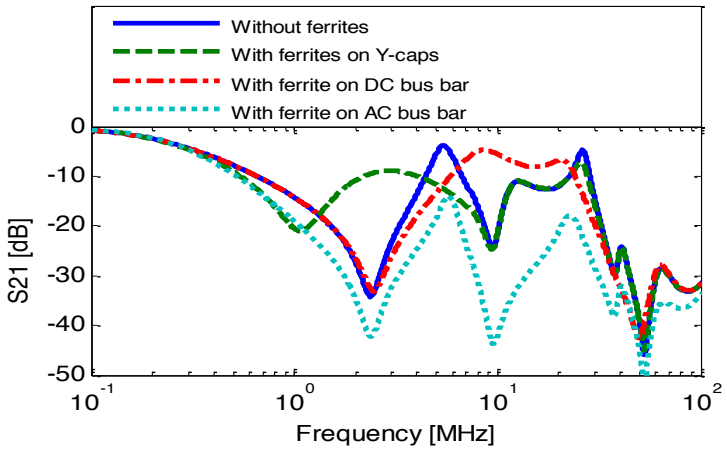



Fig. 14. Change in S21 from added low-frequency ferrites.

*B. Adding RC filters*

An RC filter was added to the DC and the AC bus bars. The capacitance of the filter was set so that the filter would generally have a lower impedance than the DC cable, and thus would impact resonant peaks that would normally be due to the DC cable. In this study it was found that adding an RC filter to the DC cables is more effective at 5 MHz at reducing the resonance peak than adding a low-frequency ferrite choke, especially when the capacitance value is higher than 1 nF. When the capacitance is increased, the peak of S21 is mitigated more effectively. The series resistance of the RC filter should be greater than about 2 Ω.

While the AC cables were not initially identified as part of the resonance at 5 MHz, adding the capacitive filter to the AC cables made them more important at lower frequencies, so the filter also had an impact at 5 MHz. In general, the larger the value of capacitance, the greater the reduction in emissions.

*C. Combined mitigation strategies*

The impact of a combination of the proposed mitigation strategies is shown in Fig. 15. The most effective reduction of emissions was obtained when RC filters (C=50 nF, R=10 Ω) were added between the DC cables and the shield and a low-frequency ferrite choke (C=60 pF, L=12 uH and R=38 Ω) was added to the AC bus bars. This strategy was able to reduce values of S21 by 10-20 dB at critical resonant frequencies.

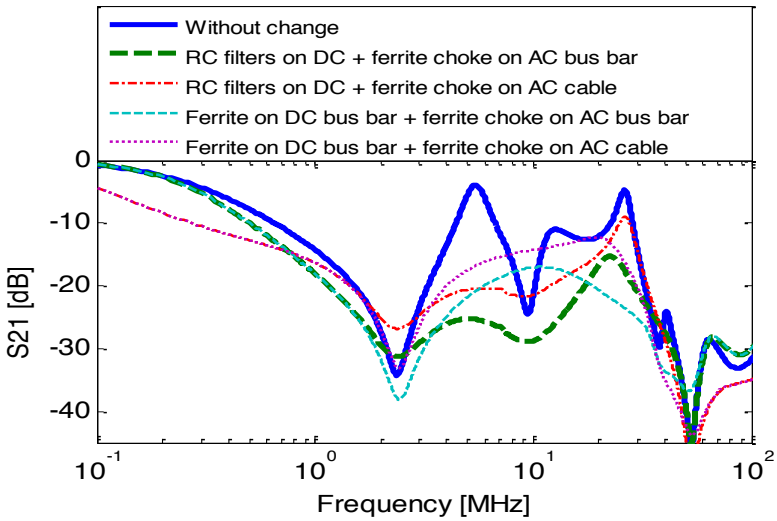



Fig. 15. Predicted effect of combined countermeasures on S21.

*D. Validation of mitigation techniques*

Two of the mitigation techniques discussed above were applied to the real system. Specifically RC filters (C=56 nF, R=13 Ω) were added to the DC bus bars and a ferrite choke (high frequency ferrite by Laird) was added to the AC bus bar. The ferrite was modelled as a parallel RLC circuit (60 Ω, 0.35 uH, 0.1 pF), which was found from datasheet and measurement information. Comparison of measured and predicted values of S21 is shown in Fig. 16. The values match within a few decibels from 100 kHz to 100 MHz. Some disagreement is expected, particularly at high frequencies, because of difficulty in modelling the ferrite.

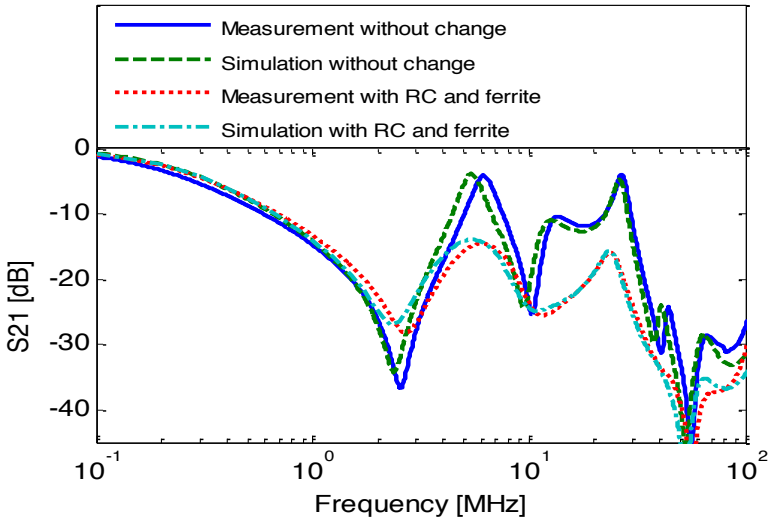



Fig. 16. Measured and simulated values of S21 when RC filters and a ferrite are added to the inverter.

## VI. RADIATED EMISSIONS

To further validate the model and demonstrate its effectiveness, changes in radiated emissions were predicted and measured while using the mitigation strategies. Radiated emissions were measured inside a semi anechoic chamber, as shown in Fig. 17. The IGBT phase node was driven with a rectangular pulse to mimic a switching noise source. The measurement setup is similar to the CISPR 25 standard. During measurement, the ends of the DC cables were shielded with foil, since in the real setup the shields are connected at 360 degree to the chamber wall and the ends are thus well shielded. Fig. 18 shows the predicted impact of the mitigation strategies on S21 and the measured impact on radiated emissions. The predicted changes in S21 correlate well with the changes in the radiated emissions up to about 35 MHz. The correlation is not perfect, as adding circuitry can change the interaction between the circuit and the parasitic radiating antenna (for example, changing the antenna resonance). While the model cannot predict such changes, as it does not include a model of the antenna, it still provides good guidance toward the impact of design changes on radiation.

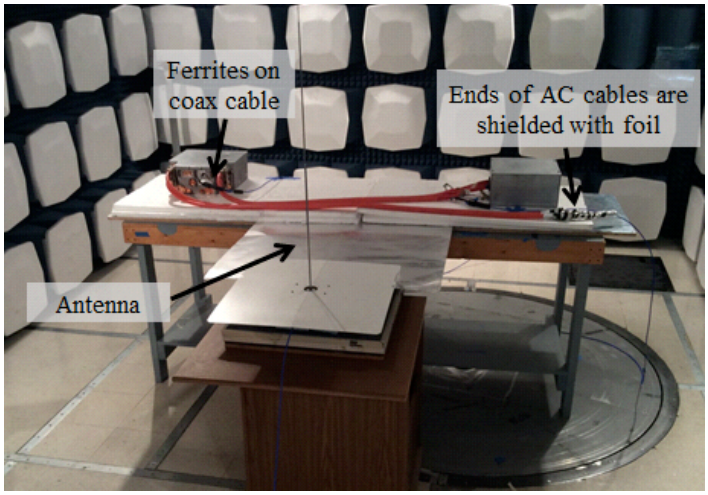



Fig. 17. Setup used for radiated emissions measurements.

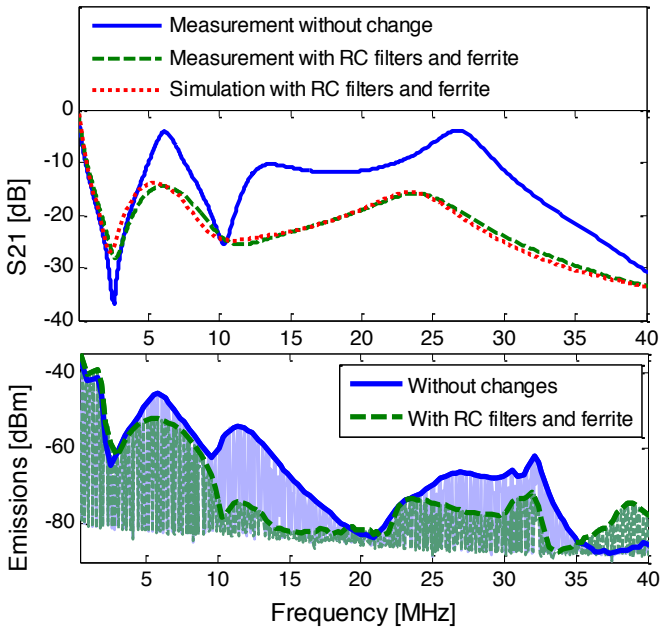



Fig. 18. Correlation between changes in S21 and radiated emissions.

## VII. GENERAL METHODOLOGY

While this paper demonstrates the development of a model for a specific power inverter, the methodology can be applied to more general power systems. The model can be developed in the following steps:

Step 1. Divide main system into subsystems for analysis.

Step 2. Estimate rough equivalent model based on parasitics associated with subsystem geometry (e.g. for cables – a transmission line model, for DC link - a combination of link capacitor, Y capacitors and some related bus bar inductances, etc.).

Step 3. Identify the location of the main noise source (for a power inverter usually between the phase node and chassis) and the most critical point where energy could be coupled to cables or other antenna structures (e.g. at the end of the AC cables). These locations are used as ports.

Step 4. Perform network parameters measurements on each subsystem to identify the values of parasitic R, L and Cs.

Step 5. Assemble complete model from equivalent models of all subsystems. Validate model with measurements and make minor reasonable adjustments as needed. During this step, it may be necessary to adjust for coupling between subsystems that was not accounted for in steps 2-4.

Step 6. Correlate circuit elements (representing real geometry components) of the model with the most important resonances of the system by tracing currents at these resonant frequencies.

Step 7. Use critical circuit elements at (or between) resonances to determine practical countermeasures to mitigate or reduce unwanted emissions.

Critical to this method is dividing the system into simple subcomponents that can be characterized with simple models, and then using the overall (simple) model to understand the root components involved at frequencies where problems occur.

## VIII. CONCLUSIONS

The development and analysis of a model for a complex power system was illustrated in this paper. While the methodology was applied to a power inverter system, it can be applied to other systems as well, where frequencies of interest are below 100 MHz. The equivalent model contains only the most important parasitic elements of the system. Each element can be clearly correlated with real system geometry. The model developed here was able to describe the impedance of a real inverter system well from 100 kHz to 100 MHz. Simulations of S21 for this system showed resonances at

frequencies similar to those at which peak radiation has been observed from the real system.

A substantial advantage of a simple circuit representation is that it allows analytic determination of the possible causes of and mitigations strategies for emissions. This process is possible because the circuit is simple and because circuit elements are directly correlated with physical structures within the system. An analysis of the inverter studied here revealed the parasitics responsible for resonances associated with peak emissions. Recommendations to mitigate emissions were made based on the elements and current paths involved in these resonances. The most effective reduction of emissions was found using a combination of an RC filter added between the DC cable and chassis and a low-frequency ferrite choke added on the AC bus bars, which was validated by measurements.

100 MHz was the highest frequency of interest for the power inverter studied here. Below 100 MHz, there was no significant parasitic coupling between the subsystems, which allowed the subsystems to be characterized separately. At higher frequencies, parasitic coupling between systems might not be ignored. For example enclosure resonances may allow efficient coupling between components that are electrically far apart. Parasitic coupling between subsystems may also be an issue at low frequencies for other inverter systems. Parasitic coupling between subsystems was not explored in this paper. This possibility must be checked through validation measurements of the overall system impedances, and accounted for when needed.

While the proposed model does not directly predict the radiated emissions, since it does not include a model of the parasitic radiating antenna, it can still be used to understand and mitigate radiation problems. The validity of this approach was demonstrated by measurement which showed that it was able to effectively predict changes in radiated emissions as a result of adding filtering strategies to the design.

# IX. APPENDICES

The length of the AC and DC cables may vary in the final application. The effect of different lengths of DC and AC cables was investigated. From a practical application standpoint the AC cables cannot be very long, while the DC cables can be quite long. Comparisons of values of S21 when the AC cable length varied from 1 m to 3 m and DC cables length varied from 1 m to 20 m are shown in Fig. 20. When the DC cables were 2 meter long and the AC cables lengths ranged from 1 to 3 meters, the length of the AC cable had an impact on the 10 MHz resonance, but did not have an effect on resonances at other frequencies. When the AC cables were 2 meters long, and the DC cable length varied from 1 to 20 meters, the length of the DC cables had a large impact on resonant frequencies, particularly at 5 MHz and below. While the resonant frequencies changed above 5 MHz as the DC cable length was changed, peak values of S21 above 5 MHz, however, were not changed much. Influence of DC cable length when the tangent loss value was 0.003, instead of 0.108 was also investigated. Overall, the loss of the cable becomes critical when the DC cable is long. A low loss cable generates many resonances at higher frequencies. If the loss is large, as it is for some commercially available high power cables, these resonances are largely damped by the cable loss. Similar mitigation/analysis strategies explored earlier should also apply to longer cables.

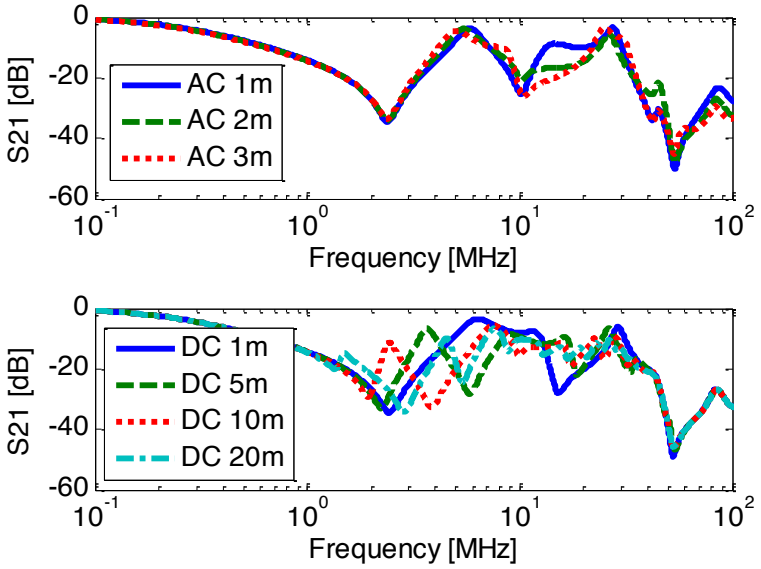



Fig. 19. Effect of AC and DC cable length on S21.

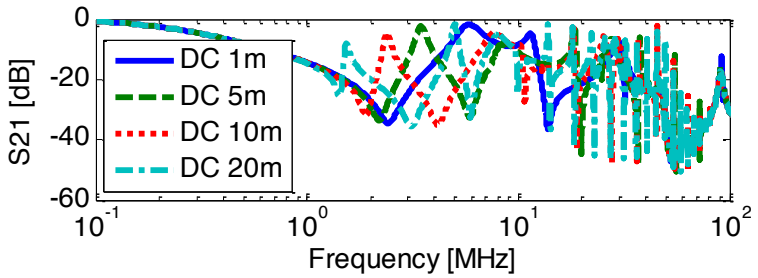



Fig. 20. Effect of DC cable length when the cable is low loss.

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## II. DEVELOPMENT OF SIMPLE PHYSICS-BASED INTERCONNECT MODELS FOR POWER ELECTRONICS

***Abstract***— Interconnect parasitics are important for Electromagnetic Interference (EMI) within power electronics systems. Simple yet accurate physics-based lumped-circuit models of interconnect parasitics can allow fast analysis and better understanding of the system performance. Most known model reduction techniques speed up calculation, but do not preserve physicality. In this paper, a methodology is developed for obtaining a simplified SPICE circuit from a large scale Partial Element Equivalent Circuit (PEEC) model, where there is a clear correlation between geometry and parasitic circuit elements. With this method reduction for inductors and capacitors is done separately, to preserve correlation between obtained equivalent circuits and physical geometry. First reduction is done for L and R based on geometry, then capacitance reduction around nodes from reduced LR model. Obtained reduced model gives better insight of a problem

and can be used for making changes in the design. The method is validated on simple realistic power electronics geometries using frequency-dependent behavior of port impedances.

## I. INTRODUCTION

In problems related to Electromagnetic Compatibility (EMC) analysis of power electronics devices, one of the main concerns is to identify structures that have the most influence on the device behavior and Recently, the range of frequencies of importance in power electronics has increased with the inclusion of higher frequency switching circuits. This demands the modelling of power electronics interconnect structures which are suitable up the maximum frequency of interest which may be between 100 kHz and in some cases up to 1 GHz. While full-wave modeling is powerful, it does not directly show which parts of the system are responsible for particular EMI problem without additional efforts. Moreover some models require including non-linear components that cannot be modeled easily with a full-wave solver and should be considered using circuit analysis. Simple equivalent circuits that can describe physics are very useful tools for such problems [2]. The advantage of a physical or physics-based model is that the circuit elements can be correlated to certain components of the actual geometry, which is very important for the root-cause analysis of EMC problems in the system design [3]. Partial element equivalent circuit (PEEC) is a well-known method where a problem is transferred from the electromagnetic domain to the circuit domain [4]. Using PEEC models to directly represent complex structures often does not lead to an intuitive understanding of the system since the number of circuit elements can be in the tens of thousands and no physical insight is gained [1]. In addition, combined with the non-liner components, the large PEEC circuit becomes even harder to analyse.

In literature, there are various techniques for obtaining rather small and accurate reduced equivalent circuits, however, most of the approaches do not preserve correlation between circuit elements and physical geometry. Certain model order reduction (MOR) techniques are available that replace large PEEC circuit with a small equivalent circuit representation with approximately similar behaviour in the desired frequency range [4]. Some examples of a reduction include a passive reduction order interconnect

macromodelling algorithm (PRIMA), which is a projection method that uses Krylov subspace, and an asymptotic waveform evaluation (AWE) moment matching approximation method [15]. Another quasi-static reluctance-based approach is presented in [19]. Such reduced circuits are very useful and speed up calculation, however, they are purely functional and still do not give physical insight. Model reduction that preserves information about physics of the system is preferable.

A number of recent works have looked into obtaining reduced models preserving some physical information. In [16] an adapted PEEC method is presented to get reduced equivalent circuits in application to variable speed drives. In this work a relatively fine subdivision was used to represent the interconnects, however, the work is not focused on getting physics-based model and no systematic approach to choosing nodes for the reduce model is presented. In [2] and [3], an equivalent SPICE circuit model is obtained from Z-parameters found using 3D full-wave simulation, where model reduction is based on finding equivalent circuits for the dominant eigenvalues of a structure. Another recent work [14] aims to develop physics-based models for active power converters working up to 5 MHz, extracting equivalent models using finite element analysis and analytical IGBT model. Resulting reduced model is simple and is useful for analysis of different modulation techniques, but lacks direct correlation between system geometry and equivalent components.

In this work a methodology is developed for extracting simple physics-based equivalent circuits for the interconnects from a complex PEEC model in application to power systems. The motivation of the reduction is not accelerating computation speed (like for example in [19]), as it can be achieved by many known MOR techniques, and not just about getting a coarse mesh for fast analysis, since coarse mesh cannot sufficiently describe physics, but acquiring better understanding of the model behavior, since with the proposed method clear correlation between simplified circuit elements and real geometry. This is very important for improving the design. To get such a model, complex model solution is needed which is used to derive reduced model. The advantage of this model reduction is that specific parasitic components within the circuit can be associated with specific structures (i.e. geometries) within the system. This approach can be very useful, especially for "lower frequency" power engineering problems, where

frequency range is between 10 kHz and a few hundreds of megahertz (considerably lower than for higher frequency signal integrity problems). The proposed Physics-Based Model Size Reduction (PMSR) technique helps to obtain reduced models while maintaining physical insight. For this reason, with proposed method, the inductive and capacitive sub-models are separated as much as feasible. This separation helps to ensure physicality of the reduced model. This is what is lacking in many other available model reduction techniques. Proposed method starts with complex and detailed PEEC model solution up to highest frequency of interest (a few hundreds of megahertz). The minimum number of nodes for reduced model are chosen based on geometry, presence of lumped elements, and correct behaviour of the model up to desired frequencies. Reduction for inductors and resistors is performed based on these nodes using impedance matrix. Reduction of capacitors is done next based on reduced model for inductors and voltage distribution found from complex PEEC solution at some frequencies. The resulting simplified electrical circuit will have small number of components and thus will make analysis of the model easier. Moreover these circuit elements are easily correlated to geometry, or to physical properties of system components. This correlation can be very important when a change in the design is required.

The structure of the paper is the following. In Section II, the PEEC formulation and analysis are shown. Section III presents proposed model size reduction approach for R, L and C components and some validation results. Application of the method to a simplified power electronics system is presented in Section IV. The conclusions are summarized in Section VI.

## II. PEEC FORMULATION

The partial element equivalent circuit (PEEC) method is based on an integral equation formulation of the geometry that is interpreted in terms of circuit elements [4]. The main difference of PEEC compared to other integral equation based methods is that it provides a circuit interpretation of electric field integral equation (EFIE) in terms of partial elements (e.g. partial inductances, partial capacitances) [5]. And the resulting circuit can be analysed by SPICE-like circuit solvers in both time and frequency domain.

*A. Partial elements*

To develop a PEEC model, first the total electric field is written in terms of magnetic vector potential and electric scalar potential (in frequency domain) as

$$\vec{E}_0(\vec{r},w) = \frac{\vec{J}(\vec{r},\omega)}{\sigma} + jw\vec{A}(\vec{r},\omega) + \nabla V(\vec{r},\omega), \tag{1}$$

where $\vec{E}_0$ is applied electric field, if observation point $\vec{r}$ is on the surface of a conductor then $\vec{J}$ is a current density of that conductor with conductivity $\sigma$, $\vec{A}$ and $V$ magnetic vector and electric scalar potential. The vector potential $\vec{A}$ at observation point $\vec{r}$ is given by

$$\vec{A}(\vec{r},w) = \mu\int_{v'} G(\vec{r},\vec{r}')J(\vec{r}',\omega)dv', \tag{2}$$

where $\vec{r}'$ is the source point. The electric scalar potential is given by

$$V(\vec{r},\omega) = \frac{1}{\varepsilon}\int_{v'} G(\vec{r},\vec{r}')q(\vec{r}',\omega)dv', \tag{3}$$

where $q$ is the charge density at the source point. The free space Green's function in the frequency domain has the from

$$G(\vec{r},\vec{r}') = \frac{e^{-j\omega\tau}}{4\pi|\vec{r}-\vec{r}'|}, \tag{4}$$

where $\tau$ is a time delay of the retarded electric and magnetic coupling

$$\tau = \frac{|\vec{r}-\vec{r}'|}{c}. \tag{5}$$

To apply the PEEC model, first a special discretization of the structure is required (hexahedral in the standard approach). Then the electric current and charge on these elemental cells are expanded into series of basis functions. Usually pulse basis functions are used as expansion and weight functions. These basis functions correspond to assumption that for the discrete model the unknown electrical current and charge densities are set to be constants over each cell. After the standard Galerkin's testing procedure, branches and nodes are generated and electrical lumped elements are identified. Magnetic field couplings are modeled by partial inductances and electric field couplings are modeled by coefficients of potentials. Partial resistances are also introduced to represent power dissipation.

The magnetic field coupling between two conductive cells α and β is described by the following partial inductance:

$$Lp_{\alpha\beta} = \frac{\mu}{4\pi}\frac{1}{a_\alpha a_\beta}\iint_{u_\alpha u_\beta}\frac{1}{R_{\alpha\beta}}du_\alpha du_\beta, \tag{6}$$

where $R_{\alpha\beta}$ is the distance between any two points in volumes $u_\alpha$ and $u_\beta$, with $a_\alpha$ and $a_\beta$ are corresponding cross sections. For α=β case the integral is taken over the same cell and becomes the partial self-inductance.

The electric field coupling between two capacitive surface cells $\delta$ and $\gamma$ is modeled by coefficient of potential

$$P_{\delta\gamma} = \frac{1}{4\pi\varepsilon}\frac{1}{S_\delta S_\gamma}\iint_{S_\delta S_\gamma}\frac{1}{R_{\delta\gamma}}dS_\delta dS_\gamma, \tag{7}$$

where $R_{\delta\gamma}$ is the distance between any two points surfaces $\delta$ and $\gamma$, while $S_\delta$ and $S_\gamma$ corresponding to the area of their respective surface.

The definition for coefficient of potential implies that the charges reside only on the surface of the conductors.

Short circuit capacitance is obtained directly from the coefficients of potential.

An example of PEEC cells is shown in Fig.1. Fig. 2 shows a basic PEEC cells circuit. In this representation $V_m^L$ is a current controlled voltage source (CCVS), to account for the magnetic field couplings and $i_1$and $i_2$ are current controlled current sources (CCCS), to account for the electric field couplings. The procedure of model discretization leads to a very large equivalent electrical circuit which can be solved with standard circuit solvers.

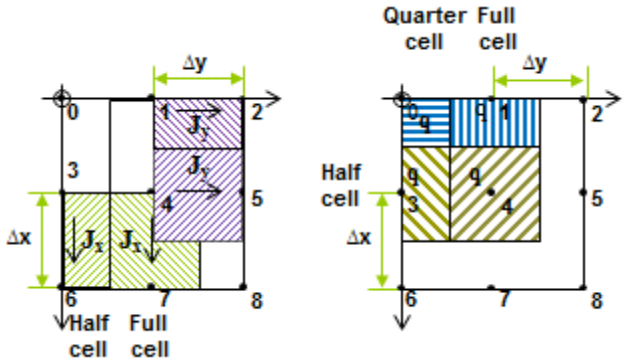



Fig.1. Example of inductive and capacitive cells for a thin metal plane

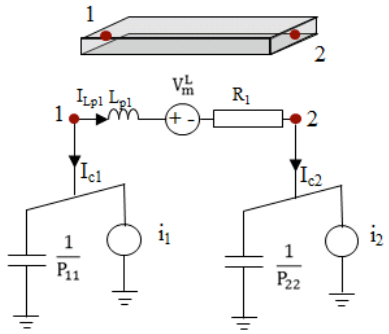



Fig. 2. Example of a classic PEEC cell circuit.

In this work a closed form analytical solution of (6) and (7) )for zero thickness planes are used [11], [17]. Retardation effect is not taken into account, since for power electronics applications frequencies of interest are not very high and lumped components are used.

*B. PEEC analysis*

The modified nodal analysis (MNA) is one of the well-known general formulation methods used in the analysis of electric circuits. This method is usually used to form and

analyse the PEEC models. It is easy to implement for both time and frequency domain analysis and is used in general purpose circuit simulators such as SPICE. MNA combines KVL and KCL equations in a compact form. The connections between nodes and branches in the circuit are described using the connectivity or incidence matrix A. For N+1 nodes and M branches this matrix A has correspondingly N+1 rows and M columns. The element of the connectivity matrix is 1 if the current of the branch flows away from the node, -1 if the current flows into this node and otherwise is zero. In the beginning of getting MNA matrix first one of the nodes has to be assigned a reference node or ground. This A matrix with removed reference node is called a reduced incidence matrix. General form of MNA for impedance formulation (with only current sources) is [15]

$$(\mathbf{G}+s\mathbf{C})\mathbf{X}=\begin{bmatrix} s\mathbf{A}_c\mathbf{C}_c\mathbf{A}_c^{\,T} & \mathbf{A}_l \\ \mathbf{A}_l^{\,T} & -(s\mathbf{L}+\mathbf{R}) \end{bmatrix}\begin{bmatrix} \mathbf{V}_p \\ \mathbf{I}_L \end{bmatrix}=\mathbf{B}\mathbf{I}_{in}, \tag{8}$$

where

$$\mathbf{C}=\begin{bmatrix} s\mathbf{A}_c\mathbf{C}_c\mathbf{A}_c^{\,T} & 0 \\ 0 & -(s\mathbf{L}+\mathbf{R}) \end{bmatrix}, \tag{9}$$

and

$$\mathbf{G}=\begin{bmatrix} 0 & \mathbf{A}_l \\ \mathbf{A}_l^{\,T} & 0 \end{bmatrix}, \tag{10}$$

In these expressions, $\mathbf{C}$ and $\mathbf{G}$ matrices contain conductance and energy storing elements; $\mathbf{A}_l$ and $\mathbf{A}_c$ are connectivity matrices of the inductance and capacitance components. $\mathbf{C_c}$, $\mathbf{L}$, and $\mathbf{R}$ are matrices with capacitive, inductive and resistive elements, $\mathbf{V}_p$ are nodal voltages, $\mathbf{I}_L$ are branch currents, $\mathbf{B}$ is an input selector matrix, $\mathbf{X}$ contains all nodal voltages and branch current or all system unknowns, and $\mathbf{I}_{in}$ is the input current.

## III. PHYSICS-BASED MODEL SUZE REDUCTION

With proposed method, number of inductors and capacitors is reduced separately. This separation helps to ensure physicality of the reduced model. Method starts with complex PEEC model solution up to highest frequency of interest (a few hundreds of

MHz). Based on geometry, location of lumped elements (e.g. capacitors in a power inverter DC link) and how rapidly the current changes it is decided on the initial base nodes (or "boundaries" combining nearby nodes as explained below), that should remain in the reduced model. Minimal number of additional base nodes is found based on acceptable impedance behaviour of the reduced model up to highest desired frequency. Step by step algorithm for the reduction of L and R matrices is summarized in Fig.3.

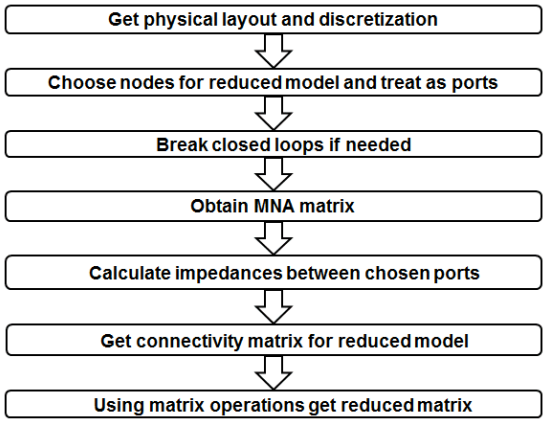



Fig.3. Steps for R and L matrices reduction.

Reduction for capacitors is done next based on reduced model for inductors and voltage distribution found from the complex PEEC solution.

*A. R and L matrices reduction*

For reduction of L and R matrices, first initial detailed PEEC model representation is obtained based on geometry information. This PEEC model contains many mesh cells, enough to have good description of the problem. As it was mentioned in the Introduction, the nodes for reduced model are chosen based on geometry and presence of lumped elements. This requires calculation for the frequency sweep up to highest frequency of interest and looking at rapidly changing currents. If the reduced model contains loops, they should be broken to distinguish between different current paths, as it will be discussed in more detail later in this section. The chosen nodes as then treated as ports and impedance matrix using MNA containing only L and R elements is found. This port impedance can be found from (9) and

$$\mathbf{V}_{out} = \mathbf{B}^T \mathbf{X}, \tag{11}$$

as

$$\mathbf{Z}_{port} = \mathbf{B}^T (\mathbf{G} + s\mathbf{C})^{-1} \mathbf{B}, \tag{12}$$

This impedance should be same in original and reduced problems. This port impedance matrix and knowledge of the simplified model structure is used to get L and R elements of the reduce model.

Derivation of the inductance and resistance matrix for reduced physics-based model is based on the assumption that we know how many nodes will be left in that model. This knowledge provides us with known connectivity matrix A for the reduced model's MNA matrix. It is denoted as $\mathbf{A}_r$. We can write an MNA matrix for reduced model containing L and R elements as

$$\begin{bmatrix} 0 & \mathbf{A}_r \\ \mathbf{A}_r^{\mathrm{T}} & -(\mathbf{R}_r + s\mathbf{L}_{pr}) \end{bmatrix} \begin{bmatrix} \mathbf{V}_p \\ \mathbf{I}_{Lr} \end{bmatrix} = \begin{bmatrix} \mathbf{I}_s \\ \mathbf{0} \end{bmatrix}. \tag{13}$$

For both original complete and reduced models the voltages at the chosen ports to remain in the reduced model are the same Vp. From the first equation of system (13), after multiplying both sides by $\mathbf{A}_r^T$ we get

$$\mathbf{A}_r^T \mathbf{A}_r \mathbf{I}_{Lr} = \mathbf{A}_r^T \mathbf{I}_S. \tag{14}$$

If there exists an inverse of $\mathbf{A}_r^T \mathbf{A}_r$ (this necessary condition is discussed further), we can rewrite the above expression as

$$\mathbf{I}_{Lr} = (\mathbf{A}_r^T \mathbf{A}_r)^{-1} \mathbf{A}_r^T \mathbf{I}_S. \tag{15}$$

Substituting (15) into the second equation of system (13)

$$(\mathbf{R}_r + s\mathbf{L}_{pr})(\mathbf{A}_r{}^T\mathbf{A}_r)^{-1}\mathbf{A}_r{}^T\mathbf{I}_S = \mathbf{A}_r{}^T\mathbf{V}_p. \tag{16}$$

Using previously obtained expression (12) for Y or Z matrix

$$\mathbf{A}_r{}^T\mathbf{V}_p = \mathbf{A}_r{}^T\mathbf{Y}_{port}{}^{-1}\mathbf{I}_S = \mathbf{A}_r{}^T\mathbf{Z}_{port}\mathbf{I}_S. \tag{18}$$

Thus the inductance and resistance matrix for reduced model is found from

$$(\mathbf{R}_r + s\mathbf{L}_{pr}) = \mathbf{A}_r{}^T\mathbf{Z}_{port}\mathbf{A}_r = \mathbf{A}_r{}^T\mathbf{B}^T(\mathbf{G} + s\mathbf{C})^{-1}\mathbf{B}\mathbf{A}_r. \tag{17}$$

*B. Branch Tearing for Loops*

In some models a loop of inductance situation arises [15, pp.161]. A simple example of a loop problem is presented in Fig.4. The two inductances representing upper left corner and lower right corner of the geometry cannon be found uniquely, since there is only one impedance value between +DC contact and –DC contact. This impedance value will provide one inductance value that is a combination of two generally different inductances. The loop has to be broken at +DC contact.

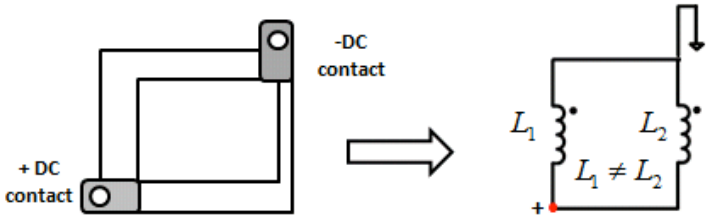



Fig.4. Simplest example of the loop problem for reduction.

Moreover from mathematical standpoint, as it was discussed in the previous subsection, the main requirement for using the proposed model reduction technique is

that there exists an inverse of (where $\mathbf{A}_r$ is the connectivity matrix for the reduced model) $\mathbf{A}_r{}^T\mathbf{A}_r$, which is true only if there is no loop in the reduced model . In some cases, however, the desired reduced model will contain a closed loop. Generally, according to a well-known theorem from linear algebra [10], the Gramian matrix $\mathbf{A}^T\mathbf{A}$ is invertible if and only if the columns of A are linearly independent. When there is a loop, some columns of A are linearly dependant on one another. As more nodes are added to a loop the linear dependence is remained.

To avoid the singularity problem we propose to use a breaking loops, or tearing concept. The main idea behind such breaking inductive branches is to create an intermediate circuit model where loops are broken into independent branches and where any path between nodes in the intermediate model can only go through one set of independent branches. These independent branches can be reconnected (to form loops) in the final reduced model, but must be disconnected during intermediate steps for $\mathbf{A}_r{}^T\mathbf{A}_r$ to be invertible.

Consider the example shown in Fig. 5. In this case nodes n1 and n2 are to remain in the reduced model. The left picture shows the original model and the right picture shows the intermediate model with nodes n1a, n1b and n2. The group containing i1, i4, and i9 will be reconstructed as a single branch (a single inductor) and is independent of the branch containing i2. Notice that any path between the selected nodes (n1 and n2) in the intermediate model contains only one set of independent branches. Nodes n1a and n1b will be reconnected after circuit reduction.

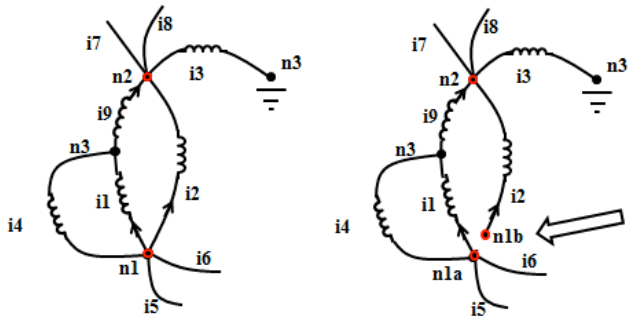



Fig. 5. Loop definition and example of breaking a loop.

It should be noted again that not all the loops have to be broken (which would be a major problem since with the PEEC method loops are created between each 4 neighbouring nodes), but only those that are remained in the reduced model. This is demonstrated on the example in Fig. 6. The loops at the right side of the circuit are not of concern, since they are combined into one element in the reduced model.

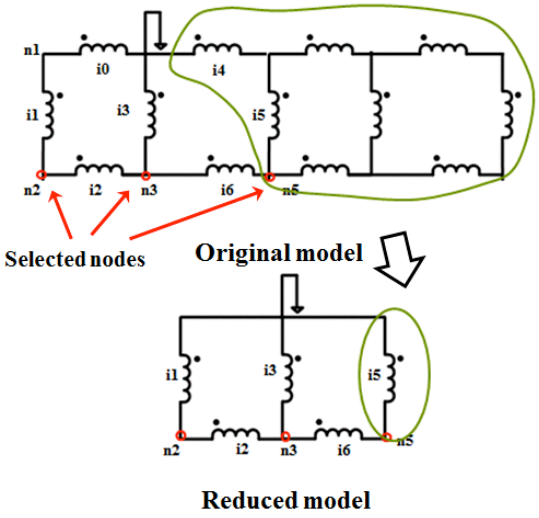



Fig. 6. Example of grouping loops.

Place where a loop should be broken can be specified manually by a user or found automatically. Automatically a loop can be found using algorithm of a loop search in a directional graph or looking for linear dependence in connectivity matrix. Reduced row echelon form can be used. RREF for the connectivity matrix in the example in Fig. 6 is shown in Fig.7. In this example two loops are indicated by reduced row echelon form. In A matrix columns related to i5 and i6 currents have linear dependence, and to get rid of dependence these currents should be disconnected from nodes n3 or n5. Columns related to i2 and i3 currents also have linear dependence, and to get rid of this dependence these currents should be disconnected from nodes n2 or n3. Thus, RREF shows possible nodes where a break can be made to get rid of the linear dependence in connectivity matrix of the reduced model.

$$A_r = \begin{array}{c} \begin{matrix} \mathbf{i1} & \mathbf{i2} & \mathbf{i3} & \mathbf{i5} & \mathbf{i6} \end{matrix} \\ \begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix} \end{array} \begin{matrix} \mathbf{n2} \\ \mathbf{n3} \\ \mathbf{n5} \end{matrix}$$

**Connectivity matrix of reduced model**

$$R = \begin{bmatrix} 1 & 0 & 1 & 0 & -1 \\ 0 & 1 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix}$$

**Reduced row echelon form of A. Indicates two loops**

Fig. 7. Using reduced row echelon form to find possible locations to break loops.

Breaking the loop involves making some changes to original MNA matrix by adding intermediate node and thus increasing MNA matrix. A new connectivity matrix after breaks were made in n2 and n3 from example in Fig. 7 is shown in Fig. 8 The operation required to break the loop is not linear, but is simple to implement numerically.

$$A_r = \begin{array}{c} \begin{matrix} \mathbf{i1} & \mathbf{i2} & \mathbf{i3} & \mathbf{i5} & \mathbf{i6} \end{matrix} \\ \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix} \end{array} \begin{matrix} \mathbf{n2} \\ \mathbf{n3} \\ \mathbf{n5} \\ \mathbf{n2a} \\ \mathbf{n5a} \end{matrix}$$

Fig. 8. Connectivity matrix after breaking two loops

*C. Example with the loop for L reduction*

A simple example containing a loop after reduction is presented in this subsection. The structure consists of a closed loop and of a semi closed loop (Fig.9). In Fig. 10 the original model and desired reduced model are shown with marked nodes, branch currents, partial inductances and ports. Since the bars in this example are narrow, as a first approximation we can model each bar (vertical or horizontal) as one partial self-inductance. This approximation helps to have minimal number of elements, thus making this example as simple as possible. This model has a closed loop and inverse of $\mathbf{A}_r^T \mathbf{A}_r$ does not exist. To solve this problem proposed grouping concept for loops discussed in previous subsection is used.

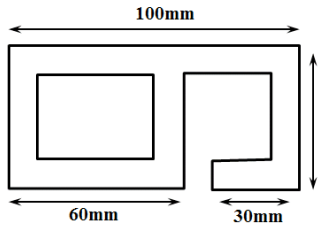



Fig. 9. Simple structure with a closed and a semi closed loop.

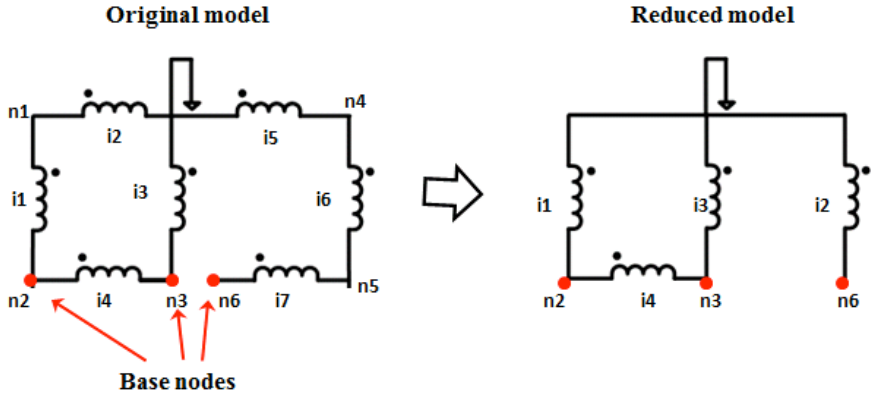



Fig.10. Original model and desired reduced model with ports representing nodes that we want to keep in the reduced model.

For this particular example ports were chosen at nodes 2, 3 and 6. The loop was broken by splitting node 2 into 2 intermediate nodes, 2a and 2b, which could have been made at other locations. So the grouping was made from node 3 to node 2 and from node 1 to node 2. In Fig. 11 the same model after grouping is shown. For this particular configuration now only one path exists between each node.

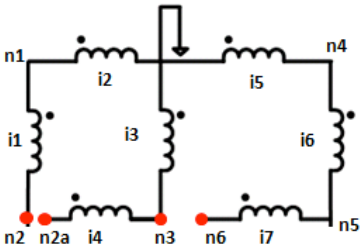



Fig.11. Grouping two parts of a loop

The original inductance matrix for 7 element case is

$$L_p = \begin{bmatrix} 36.5 & 0 & 6.5 & 0 & 3.9 & 0 & 3.8 \\ 0 & 18.3 & 0 & 2.3 & 0 & 0.993 & 0 \\ 6.5 & 0 & 30.4 & 0 & 4.2 & 0 & 2.1 \\ 0 & 2.3 & 0 & 24.3 & 0 & 2.8 & 0 \\ 3.9 & 0 & 4.2 & 0 & 24.3 & 0 & 2.8 \\ 0 & 0.993 & 0 & 2.8 & 0 & 18.3 & 0 \\ 3.8 & 0 & 2.1 & 0 & 2.8 & 0 & 18.3 \end{bmatrix} nH. \quad (19)$$

The matrix of the reduced model after reconnecting n2 and n2a is

$$L_{pr} = \begin{bmatrix} 24.3 & 2.8 & 2.3 & 0 \\ 2.8 & 55.3 & -1.107 & -0.1 \\ 2.3 & -1.107 & 48.7 & 6.5 \\ 0 & -0.1 & 6.5 & 36.5 \end{bmatrix} nH. \quad (20)$$

Validation was performed by comparing obtained reduced model inductances with inductances calculated analytically.

Increasing number of mesh cells leads to necessity to define “boundaries”. By boundaries we mean a group of nodes that is combined together in order to treat it as one node in a reduced model. The nodes that are combined into the boundaries are treated as having same voltage potential, e.g are shorted together. An example is shown in Fig.12.

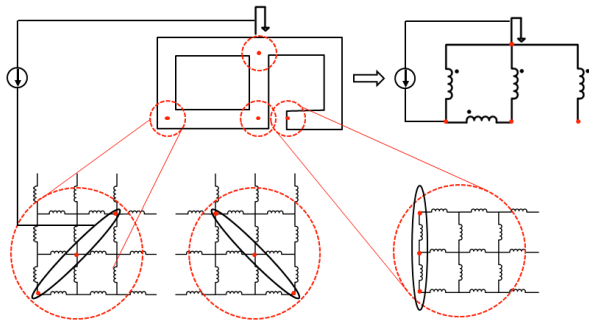


Fig.12. Increasing number of mesh cells and defining “boundaries”.

Validation of the loop inductance for 3.6mm gap case is shown in the Table I. In this table PMSR result is obtained with many mesh cells. Agreement is within a few nH.

Table I.

Validation of simple double loop case

| | *Measurement* | *CST* | *PMSR* |
|---|---|---|---|
| $L_{loop}[nH]$ | 65.4 | 64.7 | 62.5 |

*D. C model reduction*

For capacitance model reduction, capacitive cells are grouped around nodes, or boundaries used for reduced inductance model. Reduction is done by applying the same potential within a group. The groups are formed based on voltage distribution for chosen frequencies. A possible example of capacitive groups is shown in Fig. 13.

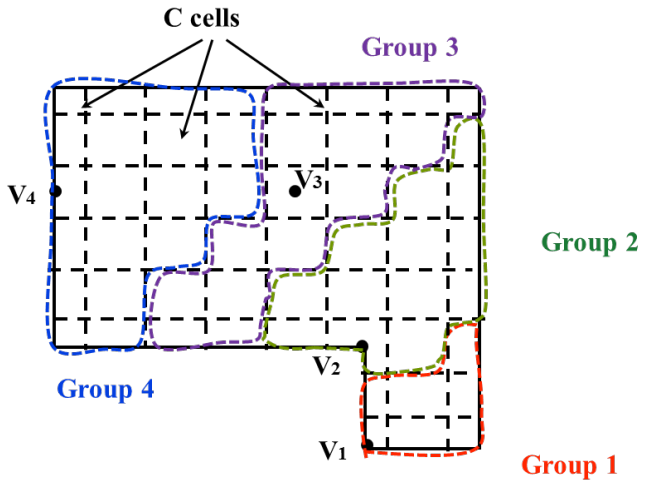



Fig.13. Forming groups for capacitance reduction based on voltage distribution.

Let's consider N conductor cells and divide them into two groups with the same potential each. System of equations for N capacitive cells relating charge, voltage potential and capacitance is

$$\begin{cases} C_{s11}V_1 + C_{s12}V_2 + \ldots + C_{s1n/2}V_{n/2} + \ldots + C_{s1n}V_n = Q_1 \\ C_{s21}V_1 + C_{s22}V_2 + \ldots + C_{s2n/2}V_{n/2} + \ldots + C_{s2n}V_n = Q_2 \\ \vdots \\ C_{sn1}V_1 + C_{sn2}V_2 + \ldots + C_{snn/2}V_{n/2} + \ldots + C_{snn}V_n = Q_n \end{cases}. \quad (21)$$

Setting the same potentials to one half of the cells and to another half of the cells (in order to get two groups)

$$\begin{aligned} V_1 = \ldots = V_{n/2} = V' \\ V_{n/2+1} = \ldots = V_n = V'' \end{aligned}. \tag{22}$$

The system can be rewritten as

$$\begin{cases} \sum_{i=1}^{i=n/2} \sum_{j=1}^{j=n/2} C_{ij} V' + \sum_{i=1}^{i=n/2} \sum_{j=n/2+1}^{j=n} C_{ij} V'' = \sum_{k=1}^{k=n/2} Q_k \\ \sum_{i=n/2+1}^{i=n} \sum_{j=1}^{j=n/2} C_{ij} V' + \sum_{i=n/2+1}^{i=n} \sum_{j=n/2+1}^{j=n} C_{ij} V'' = \sum_{k=n/2+1}^{k=n} Q_k \end{cases}. \tag{23}$$

The resulting reduced capacitance matrix consists of two self and two mutual capacitances and is

$$\begin{bmatrix} \sum_{i=1}^{n/2} \sum_{j=1}^{n/2} C_{ij} & \sum_{i=1}^{n/2} \sum_{j=n/1+1}^{n} C_{ij} \\ \sum_{i=n/2}^{n} \sum_{j=1}^{n/2} C_{ij} & \sum_{i=n/2+1}^{n} \sum_{j=n/2+1}^{n} C_{ij} \end{bmatrix}. \tag{24}$$

Same approach is used further, but for greater number of groups. With such grouping method significant reduction of capacitance model is obtained, while preserving relation between elements in reduced model and geometry parts.

Capacitance grouping algorithm can be summarized into several steps:

- Define base nodes, around which groups will form (these nodes are used for reduction of L and R matrices)
- Find neighbors for each existing node from connectivity A matrix
- Define tolerance as *T* percent of voltage range as

$$\varepsilon_{tot} = \left| \frac{V_{\min} - V_{\max}}{V_{\max}} \right| \cdot T. \tag{25}$$

- Iterate through neighbors.
  - A neighbouring node is considered a part of group if the following is true:

$$\left| \frac{V_{node} - V_{base\ node}}{V_{base\ node}} \right| < \varepsilon_{tot}. \tag{26}$$

  - During one iteration, a cell group is grown around each base node, i.e. the neighbors that satisfy condition (26). All groups spread simultaneously
  - Continue iterating until run out of neighbors.

### *A. Negative capacitance*

Negative capacitance can occur due to non projectional meshing [11]. A technique called projection meshing has to be used to obtain convergent results without using an excessive number of cells. Otherwise short circuit capacitor matrix has positive off diagonal terms [16]. In some cases very dense meshing is required to avoid this problem. Some mutual capacitive terms are very small and can be eliminated if their values are small compared to larger self terms.

The number of cells used for the meshing of the planes is an important issue for the accuracy of the model.

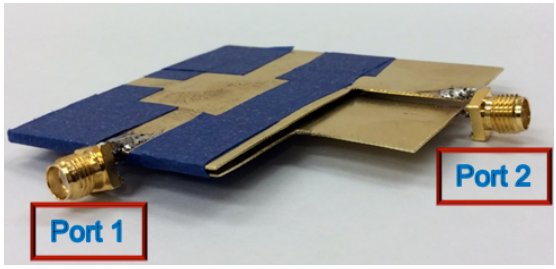
Using grouping method the negative capacitances are avoided. This is one of the advantages of proposed model reduction approach.

## IV. APPROACH VALIDATION

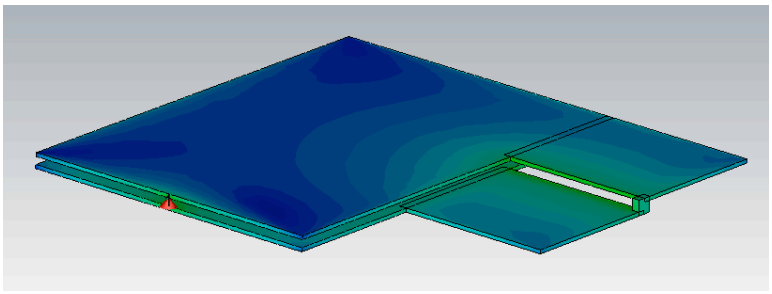
Validation of the proposed method was performed on several geometries.

*A. Simple structure*

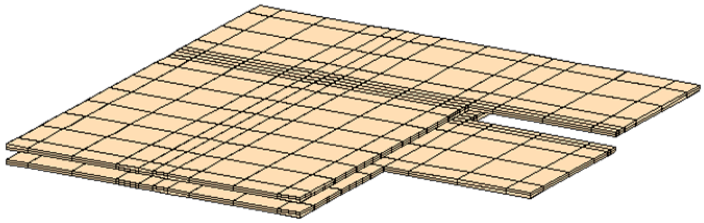
The first geometry is a part of a realistic DC link used in power electronics. The structure consists of two parallel brass plates with two ports. In Fig.14 an actual geometry, a CST model with current distribution at 50 MHz and a Power PEEC model are shown that were used for validation.




(a) Actual geometry



(b) CST model with current distribution at 50 MHz



(c) PowerPEEC model with inductive mesh cells

Fig.14. Simple structure used to validate the method.

In Fig. 15 horizontal inductive mesh cells and chosen base nodes are shown. This model contains 1265 self terms (all self L, self C and all R elements). The base nodes are chosen based on port locations (nodes 1, 5, 4 and 8), current distribution (nodes 4 and 7) and location of potential lumped components (nodes 2 and 6).

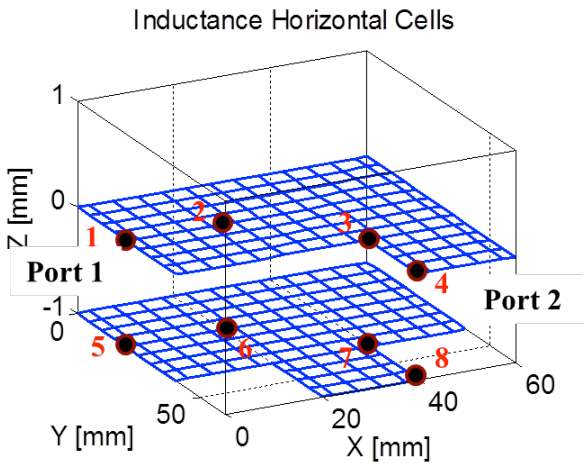
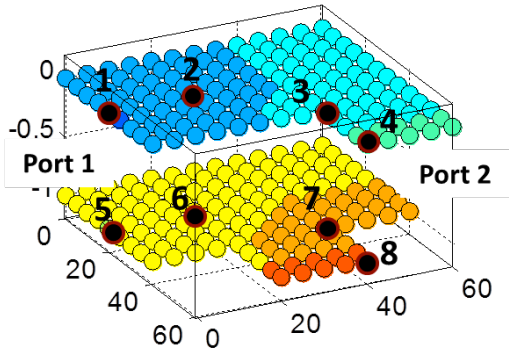
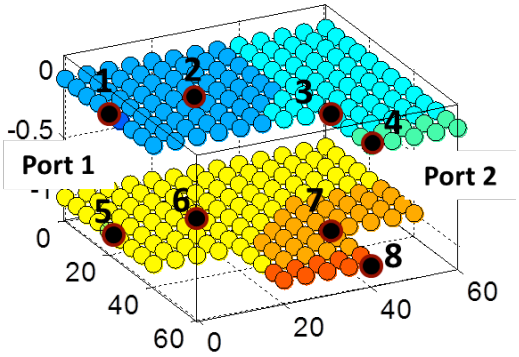



Fig. 15. Inductive cells and base nodes of a simple structure.

Input impedance is considered for two cases: when Port 2 is open and when Port 2 is shorted. Fig.16 shows capacitive groups formed around base nodes based on voltage distribution for 50 MHz. Groups are different for the two considered cases. Capacitive groups around port 1 nodes (1 and 5) contain only one cell due to rapid voltage change.



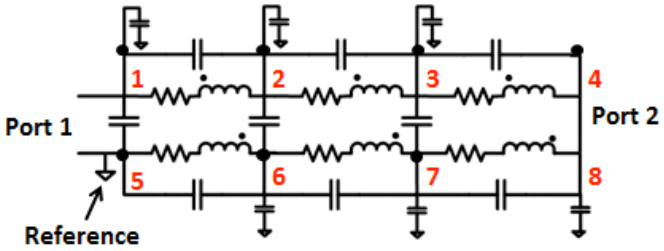

(a) Port 2 is open



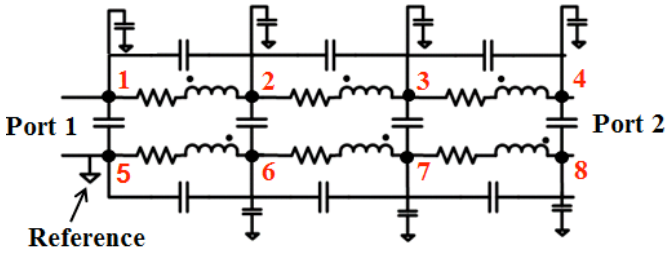

(b) Port2 is shorted

Fig.16. Capacitive groups around base nodes for cases when Port 2 is open and closed at 50 MHz.

Fig. 17 shows reduced circuits for cases when Port 2 is open and shorted. Reduced models contain 18 and 19 self terms compared to 1265 and 1264 terms in the original model.




(a) Port 2 is open




(b) Port 2 is shorted

Fig. 17. Reduced model with 19 self terms when Port 2 is open. Node numbers correspond to nodes marked in Fig. 16.

Comparison of loop inductance and resistance when Port 2 is shorted and capacitance when Port 2 is open is shown in the Table II. It should be noted that during the port impedance measurement (to get inductance and capacitance) an SMA connector is present and is adding some parasitic inductance and some capacitance, thus measured values are larger. Resistance was measured using RLC Meter.

Table II.

Validation of loop inductance and plate capacitance

| *Measurements* | *PowerPEEC* | *CST* | *PMSR* |
|---|---|---|---|
| 12.3 nH | 10.6 nH | 10.5 nH | 10.3 nH |
| 28 pF | 20 pF | 24 pF | 22 pF |
| 0.95 mΩ | - | - | 0.77 mΩ |

Input impedance looking into Port 1 when Port 2 is shorted before and after reduction is compared with a full wave result in Fig.18. The model describes system behavior well up to about 500 MHz. This is even higher frequency than intended frequency bound of the method (about 100 MHz). First resonance is captured correctly.

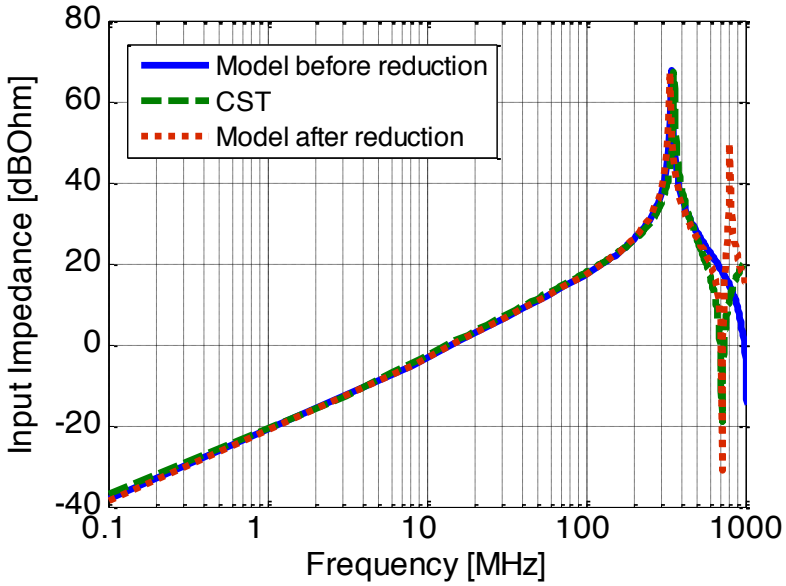



Fig. 18. Magnitude of the input impedance of a simple test structure when Port 2 is shorted.

Input impedance looking into Port 1 before and after reduction is compared with a full wave result in Fig. 19. The model describes system behavior well up to about 300 MHz. The resonance is not captured correctly. This result suggests that the reduced model might be too simplified to describe higher frequencies. This case is one of the examples where simplified model is two rough to correctly describe higher frequencies. If we need to describe behaviour for frequencies above 300 MHz, we need to add more nodes to the simplified model.

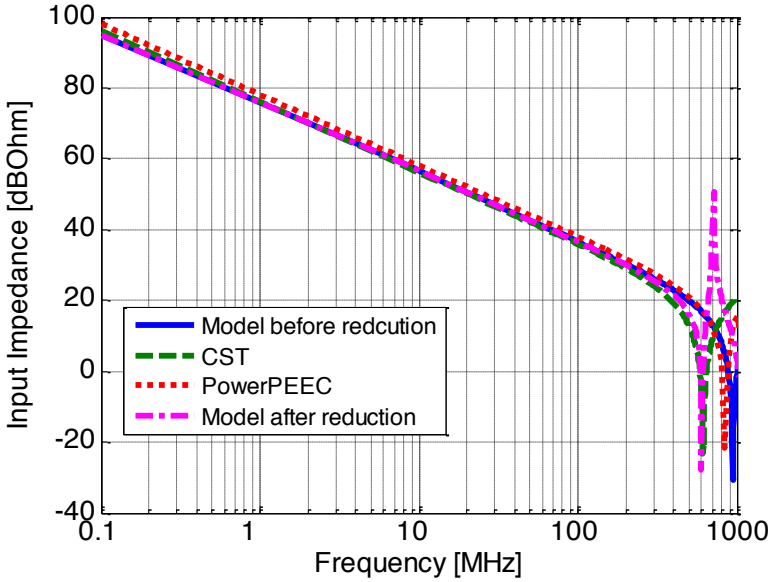
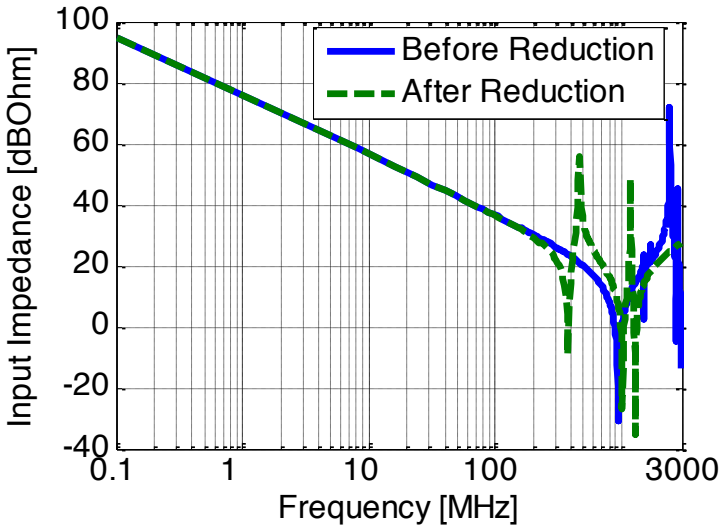
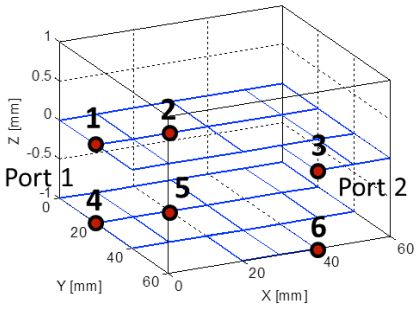


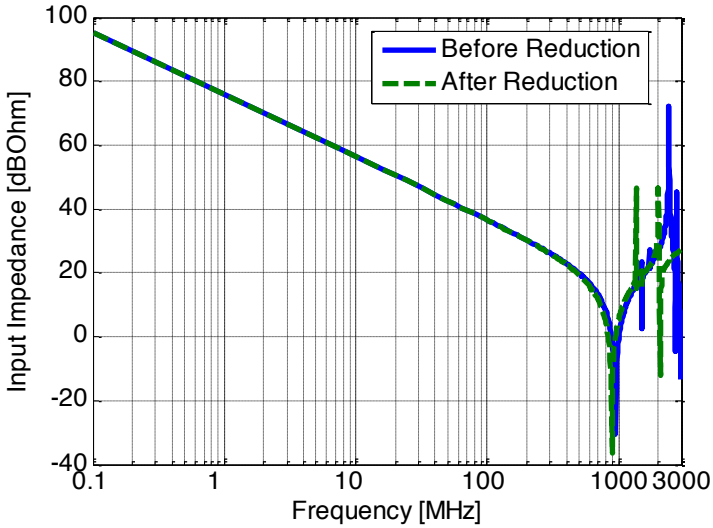

Fig. 19. Magnitude of the input impedance of a simple test structure when Port 2 is open.

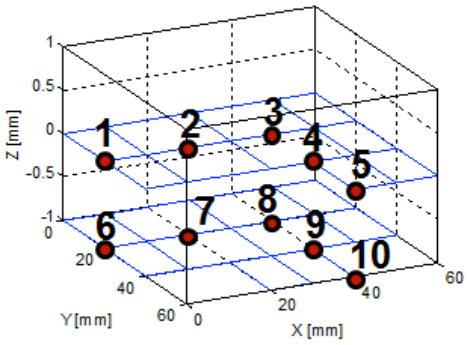
Cases when two and four more base nodes were added to the simplified model are considered. It should be noted that nodes are added in pairs (on upper and lower plates) in order to get more projection based capacitance groups. Comparison of Z11 for different number of base nodes and location of the corresponding nodes is shown in Fig. 20. Resulting simplified model in Fig. 20 (b) contains more elements, but can describe higher frequencies. One of the advantages of the approach is that the number of base nodes can be modified relatively fast and finding simple model that describes system behaviour with accepted accuracy is not complicated.






(a) 6 base nodes




(b) 10 base nodes

Fig. 20. Input impedance for Port 2 open case with different number of base nodes.

*B. Real DC link*

As a next example a real DC link block used in the power electronics system is considered. A picture of a real DC link inside a power inverter enclosure is shown in Fig. 21. Geometry of the DC link capacitor is presented in Fig. 22.

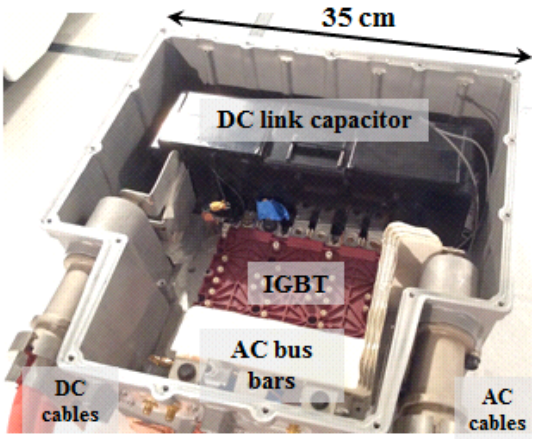



Fig .21. DC link in power inverter system.

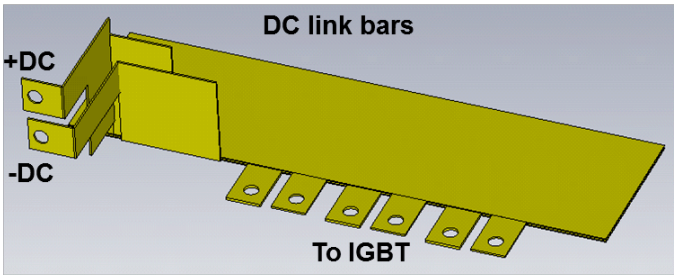



Fig. 22. Geometry of the power inverter DC link capacitor.

Initial unsimplified model consist of more than 2,500 self terms (including both inductive and capacitive elements). Inductive horizontal cells of the plates are shown in Fig. 23. Capacitive groups at 50 MHz for the case when the port 2 is open are shown in Fig. 24.

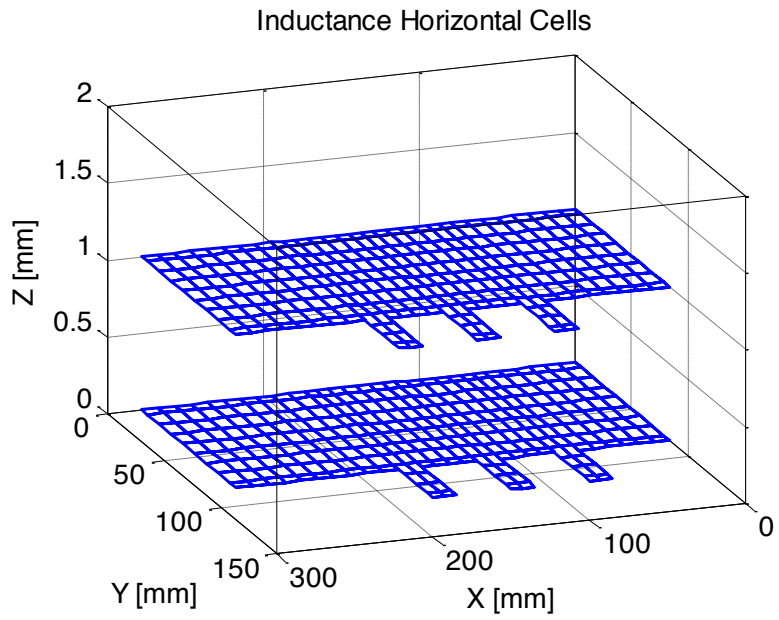



Fig. 23. Inductive cells for upper and lower DC link bus bars.

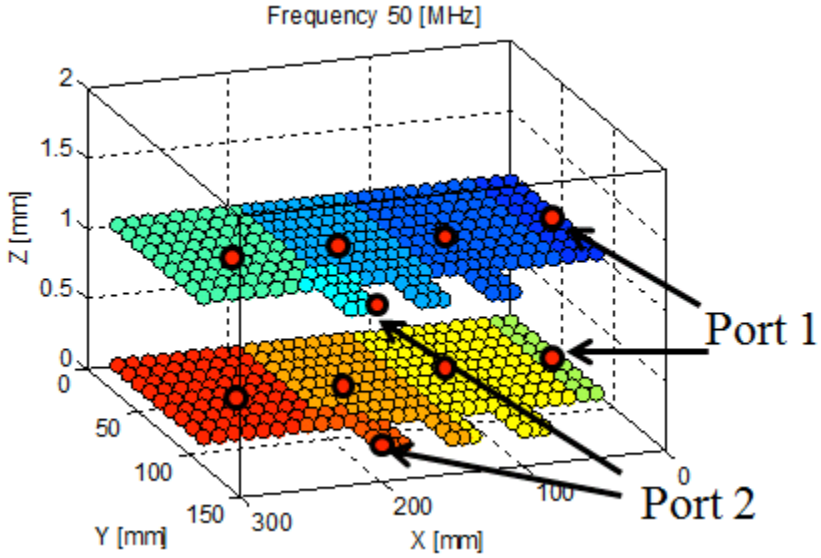



Fig. 24. Capacitive groups for 50 MHz frequency when Port 2 is open.

Comparisons of input impedances for port 2 open and shorted before and after reduction are shown in Fig. 25 and Fig. 26. Reduced model agrees with original model within 1-2 dB up to

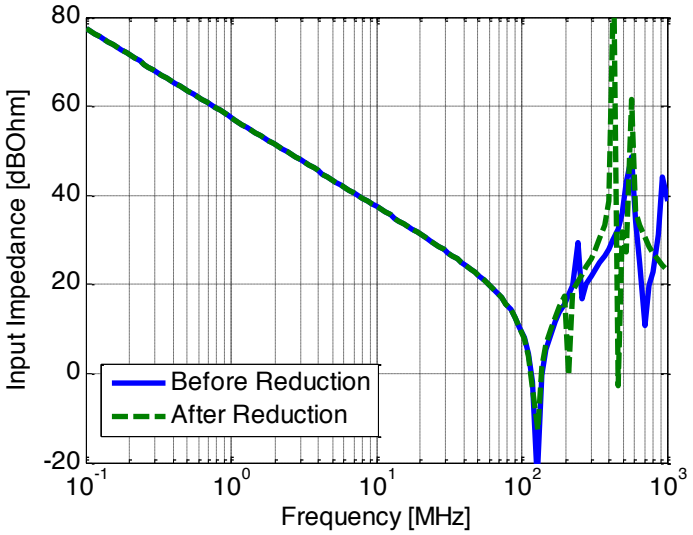



Fig. 25. Magnitude of Z11 before and reduction for open DC link case.

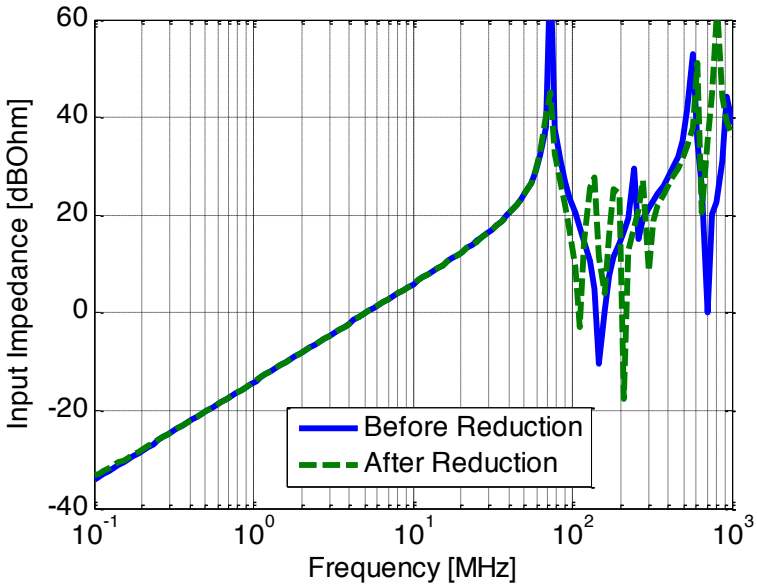



Fig. 26. Magnitude of Z11 before and after reduction for shorted DC link case.

*C. Error estimation*

The proposed reduction method is supposed to work till a few hundreds of megahertz. The error of the proposed approach can be estimated using maximum deviation and a window error function for the resonance frequencies of the impedance. If the error is high, it indicates that the number of nodes/boundaries is not enough to describe model behavior in this frequency range. The error can be found from

$$ME_{\Delta} = \left| \frac{1}{n} \sum_{i=f_i}^{f_i+\Delta} (U_i - Y_i) \right|, \tag{27}$$

where *Ui* correspond to impedance after reduction , and *Yi* is a true value or reference full-wave solution.

The error function is smoothed by moving start frequency for each window. An example of the error for simple structure considered in subsection A is shown in Fig. 27. The result indicates that the accuracy of the reduced mode is good up to about 450 MHz, where the error is below 6 dB

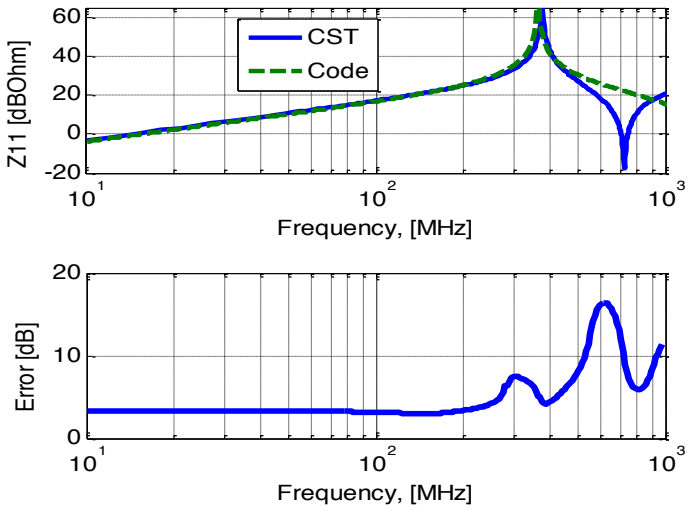



Fig. 27. Error estimation of reduction method.

## V. RULES FOR REDUCTION METHOD

The rules for applying the proposed approach are the following:

- Initial base nodes that remain in reduced model are chosen based on location of ports, location of any lumped components and where the there is a rapid change in current density.
- Tearing inductive branches is necessary if there are loops in the reduced model. This tearing is done in such a way that any path between nodes can only go through one set of independent branches.

- Model reduction for inductive and resistive elements is done separately from capacitive elements.
- Size of elements to be collapsed, and minimum number of base nodes is decided by the bandwidth of the problem. Specifically the size of the reduced elements is made such that error of impedance is less than set threshold.
- Reduction for capacitive elements is done by forming groups of cells around base nodes based on voltage distribution at chosen frequency and applying same potential within each group.

## VI. CONCLUSIONS

In this work a methodology is proposed to obtain a simplified physics-based SPICE circuit from a large scale PEEC model. With this method reduced circuits are obtained based on geometry information and some knowledge of simplified model. The purpose of the reduction is not accelerating computation speed, as it can be achieved by many known MOR techniques, and not just about getting a coarse mesh for fast analysis, but acquiring better understanding of the model behavior, since with the method clear correlation between simplified circuit elements and real geometry. This is very important for improving the design. It takes time to develop such a simple and accurate reduced physics-based mode, since solution and some analysis of the original model is needed, however once it is built it can be easily used to analyze system behavior and combine with any non-linear components.

Methodology was applied to a realistic DC link structure and showed good agreement with reference results for reasonably small number of elements in reduced model.

The approach can be useful for exploring the impact of small geometries (e.g., the current density around a via may require a fine mesh to reconstruct accurately, a simplified model can be constructed with nodes close to the via which could be used to accurately predict the voltages and currents at these nodes, the area around the via could afterward be explored using a fine-mesh PEEC micromodel and simulated along with the rest of the system). The approach allows an easy combination of both the macro- and micro-models. This is a topic for future research. Another future extension of current

work can include automated selection of nodes for reduced model and better definition of "boundaries" for various complex structures.

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## III. PREDICTION OF COMMON-MODE CURRENT REDUCTION USING FERRITES IN SYSTEMS WITH CABLE HARNESSES

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***Abstract***—Bulk ferrite chokes are widely used to reduce common-mode (CM) currents on system harnesses. The impact of the ferrite on the CM currents depends on a variety of factors and is difficult to predict. A simple closed-form analytical model of the CM impedance of the ferrite that allows efficient evaluation of the impact of the ferrite is considered. In order to apply this model to a real active power system with cable harnesses, information about the system's CM loop impedance is measured using the minimally-invasive dual current clamp method. The predicted impact of the ferrite on the CM loop impedance of the system and the CM currents on the harness showed reasonable agreement with measurements in both a simple passive test setup and in a real active system.

# I. INTRODUCTION

Rapidly switching gates in power inverters and switching power supplies may cause unwanted radiated emissions as a result of common-mode (CM) currents on wire bundles connected to the device. To reduce CM currents, bulk ferrite chokes are commonly placed on the cable [1], [2]. The impact of a ferrite is difficult to predict, however, since the impact depends on a variety factors like the CM impedance of the system, the location of the ferrite on the cable, the geometry and material properties of the ferrite, and other parameters. To choose or specially design a choke with acceptable performance, it is important to correlate the series impedance added by the ferrite choke with the CM impedance and current of the system. Trial and error methods, where many chokes are experimentally placed on a system to see which one has a reasonable impact, are not always possible and are not always acceptable. Full-wave numerical simulations of the system may be used, but modelling may require large computer resources, expensive software, expertise of a designer in computational electromagnetics, and accurate knowledge of the ferrite's intrinsic parameters. Even so, numerical simulations may need validation by experiments or other numerical methods. A better method is to use a simple analytical model that allows for efficient evaluation and optimization of the ferrite.

Several previous studies have attempted to develop analytical models of ferrite chokes. In [3]-[6] low-frequency lumped element models are developed for wound ferrite cores. In [7], a low-frequency model of a ferrite choke on a wire was considered. These models all work at relatively low frequency and ignore the impact of the return plane. The authors of [8] develop a high frequency, closed-form analytical model of the common mode impedance of ferrite chokes based on transmission line theory. This model was shown to work well up to 1 GHz when predicting the common-mode impedance of simple passive test structures.

The main objective of the current work is to demonstrate the ability of the model developed in [8] to predict the impact of the ferrite on the CM impedance and the CM current when the model is applied to a real industrial system. The paper begins with a discussion of the ferrite model. In order to apply the analytical model to a real active system, information about the CM loop impedance of the system is needed. This

impedance is not trivial to measure, because the impedance is often associated not with a single conductor, but with a harness consisting of many conductors, and since the “loop” of an active system cannot always be broken to make the CM impedance measurement. A non-invasive measurement method should be used. One way to measure this impedance is using the dual current clamp (DCC) method [9], [10]. In this approach CM energy is injected into the system by one current probe and the amount of resulting CM current is measured by another current probe using a Vector Network Analyser (VNA). The system’s CM loop impedance can be found from the amount of injected current. The measured CM loop impedance of the system without the ferrite is then combined with the analytic model of the ferrite to predict the change in the system’s CM loop impedance and CM current when the ferrite is added. Results are presented when this approach is tested on a simple passive system and on a real active inverter/motor system. The approach is shown to work well.

## II. ANALYTICAL MODEL

The transmission line model of the CM impedance of a ferrite choke proposed in [8] is wideband (working up to at least 1 GHz) and allows for efficient prediction of impedance while modifying ferrite parameters, geometry, and placement with respect to the source. The ferrite is modelled as a transmission line above a return plane, carrying a single propagating TEM wave (Fig.1).The height of the ferrite is assumed to be small compared to a wavelength ($h<<\lambda$) to meet the TEM assumption. This model allows prediction of impedance when the cable or ferrite is electrically long.

The CM impedance associated with the ferrite on the harness can be characterized from the per-unit-length RLGC parameters of a wire over a return plane, accounting for the ferrite material between the wire and the return plane. These parameters can be derived analytically from the geometry and constitutive electromagnetic parameters of the ferrite material.

Consider the ferrite choke shown in Fig. 1. By calculating the flux penetrating the area between the conductor and the return plane, the equivalent inductance per-unit-length can be found as [8],

$$L = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{R_{in}}{R_{cond}}\right) + \ln\left(\frac{h}{R_{out}}\right) + \mu_r' \times \ln\left(\frac{R_{out}}{R_{in}}\right)\right], \quad (1)$$

where $R_{in}$, $R_{out}$, $R_{cond}$, and $h$ are shown in Fig. 1 and $\mu_r$ is the complex relative permeability of the ferrite.

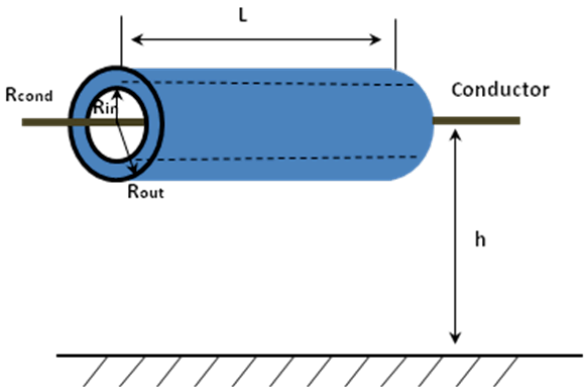


Fig. 1. Geometry associated with the ferrite over the return plane.

The per-unit-length resistance associated with the transmission line including the ferrite choke is due primarily to losses in the ferrite, given approximately by

$$R = \frac{\omega}{2\pi} \cdot \mu_0 \cdot \mu_r'' \cdot \ln\left(\frac{R_{out}}{R_{in}}\right) \quad (2)$$

To approximate the capacitance, the electric field between the conductor and the ferrite, and the electric field within the ferrite are assumed to be radially symmetric. The per-unit-length capacitance between the conductor and the ferrite, $C_1$, per-unit-length capacitance between the inner and outer wall of the ferrite, $C_2$, and per-unit-length capacitance between the ferrite and return plane, $C_3$,can thus be calculated using the coaxial capacitance formula. The total per-unit-length capacitance is then

$$C = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}} = \frac{1}{\frac{\ln(\frac{R_{in}}{R_{cond}})}{2\pi\varepsilon_0}+\frac{\ln(\frac{R_{out}}{R_{in}})}{2\pi\varepsilon_0\varepsilon_r'}+\frac{\cosh^{-1}(\frac{h}{R_{out}})}{2\pi\varepsilon_0}}, \quad (3)$$

where $\varepsilon_r$ is the complex relative permittivity of the ferrite.

Conductive losses are primarily due to dielectric losses in the ferrite, which can be found from the capacitance associated with the ferrite as

$$G = \omega \cdot C_2 \frac{\varepsilon_r''}{\varepsilon_r'}, \quad (4)$$

where $C_2$ can be found from

$$C_2 = \frac{2\pi\varepsilon_0\varepsilon_r'}{\ln(\frac{R_{out}}{R_{in}})}. \quad (5)$$

These RLGC parameters can be used to find the characteristic impedance and propagation constant of the transmission line model. Tests of this analytic model on a simple passive test structure in [8] showed good agreement with measurements up to 1 GHz.

## III. MEASUREMENT OF COMMON-MODE LOOP IMPEDANCE

While the CM loop impedance of the system is difficult to estimate since it depends largely on parasitics that are unknown and change when the system is active, a number of measurement techniques can be used to obtain this information. One possible technique is using the dual current clamp method [9, 10]. In this method, CM energy is injected into the system by one current probe and the resulting CM current is measured by another current probe using a VNA as shown in Fig. 2. The two current probes are placed

adjacent to each other, so the distance between the measurement and injection location is electrically short.

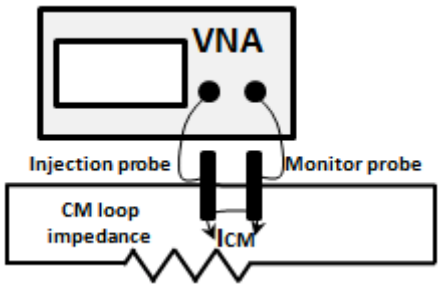


Fig. 2. Common-mode loop impedance measurement setup for the dual current clamp method.

The frequency response of the current probes are de-embedded through a calibration procedure using a calibration ring [9], similar to the calibration fixture shown in Fig. 3. This fixture generates a better calibration than using a simple ring. S-parameter measurements are made while the ring is terminated with known loads, typically a short and a 50-ohm load. The loop impedance of the calibration ring is assumed to be negligible. Once these calibration measurements are made, the loop impedance of the system of interest can be determined as

$$Z_{loop} = Z_{load} \frac{S_{load}}{S_{short} - S_{load}} \left(\frac{S_{short}}{S_{loop}} - 1\right), \quad (6)$$

where $S_{load}$ and $S_{short}$ are calculated from S parameters measured when the calibration ring is terminated with a known load impedance and a short circuit, $S_{loop}$ is the value of S measured when the two current probes are clamped on to the system under test, and $Z_{load}$ is the value of the load impedance used during calibration. The value of S is given by

$$S = \frac{S_{21}}{1 - S_{11}}, \quad (7)$$

where $S_{21}$ and $S_{11}$ are the S-parameters measured in each case.

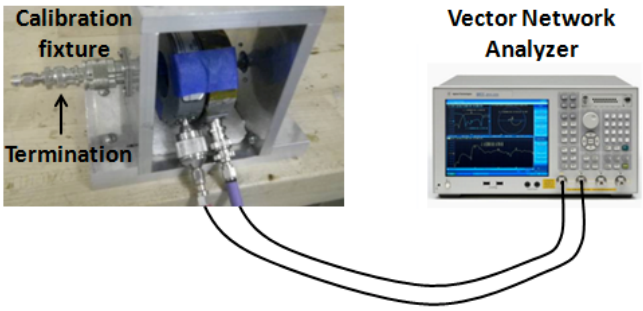


Fig. 3. Setup for calibration using a calibration fixture.

The current probes and calibration fixture used in the measurements shown here produced good results up to 100 MHz. Different probes/calibration methods might be used to generate results to higher frequencies. Our experience with the dual current clamp approach suggests that application of the probes and the calibration procedures must be performed very carefully for accurate results. Maintaining the same relative position and orientation of the clamps during calibration and measurement by using tape or some other method is particularly important, as is choosing the right sized probes for the measurement. Just because a probe is rated for a given frequency range does not mean it will be effective over that entire range for the dual current clamp measurement.

## IV. APPLICATION OF ANALYTICAL MODEL TO A SIMPLE SYSTEM

Tests were first performed on a simple passive test structure consisting of a single conductor above a current return plane as shown in Fig.4. This structure has the advantage that the CM impedance measurements can be verified by direct connection of a network analyser to the system. The conductor is a brass tube located 8 cm above a metallic return plane. A low frequency LFB259128 ferrite by Liard Technologies was chosen for this test.

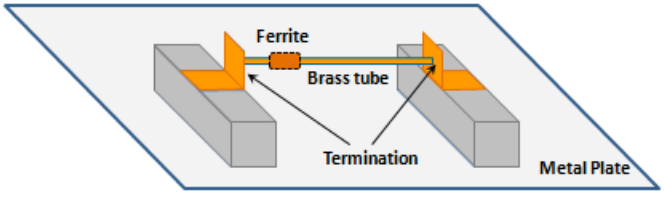


Fig. 4. Simple passive system with a ferrite core.

The influence of the ferrite on the system impedance can be predicted relatively easily if the ferrite is electrically small and is placed at the point of CM impedance and CM current measurement, and if the presence of the ferrite does not change the source of the CM emissions – only the CM impedance of the system. In this case, the impedance seen looking out from the ferrite may be modelled as a lumped element, even if the rest of the system is electrically large. To predict the impact of the ferrite, the CM system is modelled as a CM voltage source in series with the CM loop impedance, which results in the CM current. If the ferrite is electrically small, the CM impedance at the point of placement of the ferrite is given by the summation of the ferrite impedance and the original system impedance. The CM currents after adding the ferrite to the system is similarly given by:

$$I_{CM,estimated} = I_{CM,measured} \frac{Z_{loop,measured}}{Z_{loop,measured} + Z_{ferrite,analytical}}. \quad (8)$$

The CM loop impedance of the simple passive test structure with the ferrite added is shown in Fig. 5 as measured using the dual current clamp method, as measured using a network analyser, and as predicted from the impedance of the ferrite, using (1)-(4). The DCC method did a good job of determining the CM impedance of the system found through direct measurement. The analytical prediction is within about 2 dB of both the direct and DCC measurement results. The small glitch in the DCC result around 10.3 MHz is associated with a current probe resonance.

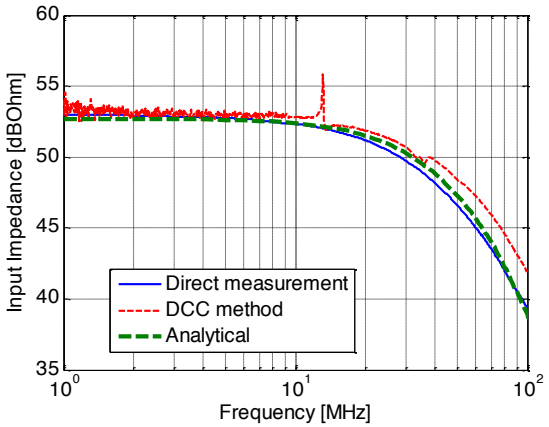


Fig. 5. Prediction of ferrite influence on CM loop impedance for simple passive structure.

# V. APPLICATION OF ANALYTICAL MODEL TO A REAL POWER SYSTEM

The analytical model for the ferrite was also applied to a real, active power inverter/motor system. The CM loop impedance and the CM current were measured when a broad band 28B2000 ferrite by Liard Technologies was placed on the system and when no ferrite was present. The measurement setup for CM loop impedance measurement using the DCC method is shown in Fig. 6 and Fig. 7.

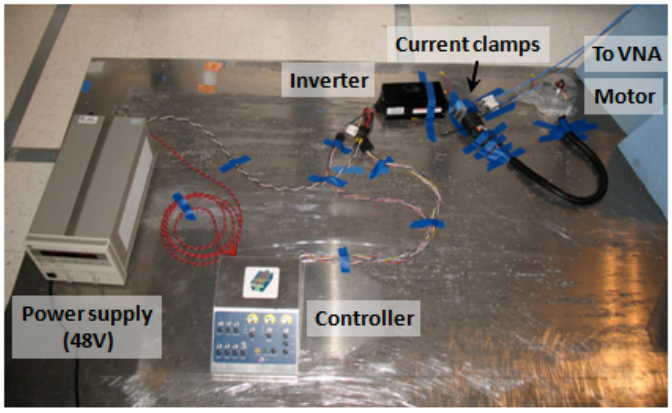


Fig. 6. Measurement setup for real active power inverter system.

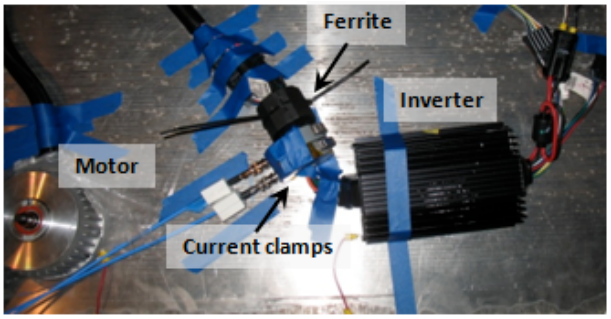


Fig. 7. Placement of DCC current clamps and the broad band ferrite.

While some CM current may occur when the motor is off and the control system is turned on, the currents are not large. The CM currents when the motor is on and off are shown in Fig. 8. As expected, there is significant increase in CM current when the motor is on.

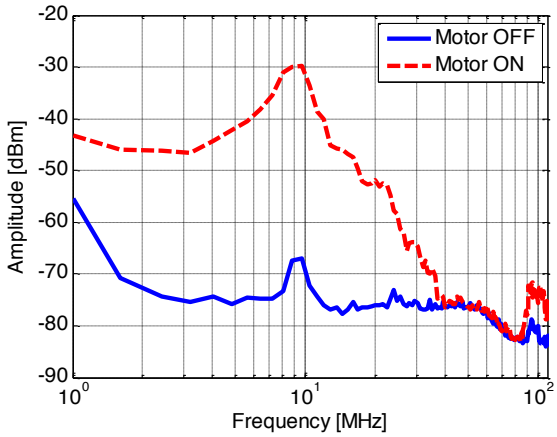


Fig. 8. CM current when the motor is on and off.

The impact of the broad band ferrite on the magnitude of the CM loop impedance is shown in Fig. 9. All loop impedance curves were obtained while using averaging by the VNA. Averaging was found to significantly reduce errors in the DCC method caused by the CM currents of the active system.

The presence of the ferrite on this particular system not only influences the level of CM current or impedance, but also affects the frequency of system resonances. As a result, a ferrite can lower CM currents at some frequencies by increasing the CM loop impedance but can also increase the CM currents at other frequencies by reducing the loop impedance as shown by the impedance changes in Fig. 9. Simply placing a large ferrite on a system cable may not solve an emissions problem at all frequencies.

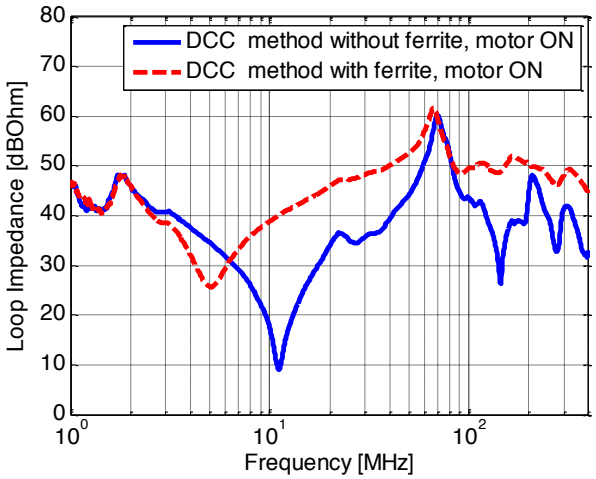


Fig. 9. Influence of the broad band ferrite on the CM loop impedance of the system.

The predicted impact of the ferrite on the CM loop impedance and the CM current of the active system is shown in Fig. 10 and Fig. 11. The curves show the value of CM current or impedance both before and after the ferrite was added to the system, and show the values predicted using the ferrite model shown earlier. The analytic methods presented here do a reasonably good job of predicting the measurement at most frequencies, which indicates that the underlying physics is modelled basically correctly. Some errors in the agreement are likely due to errors in the predicted value of the system impedance at resonances within the measurement system. These resonances may be difficult to account for properly in the DCC measurement. Nonetheless, the measurement provides useful insight into which ferrite will best solve a CM problem.

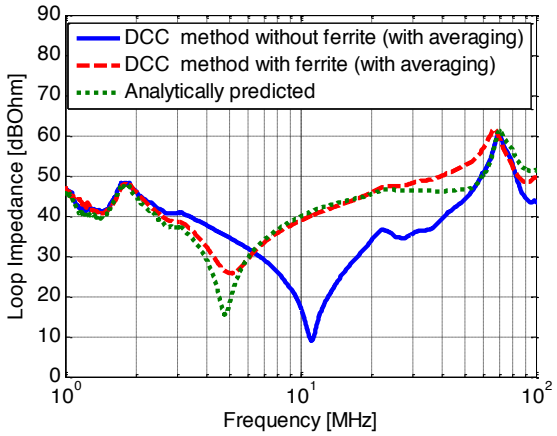


Fig. 10. Measured and predicted common mode impedance with an added ferrite.

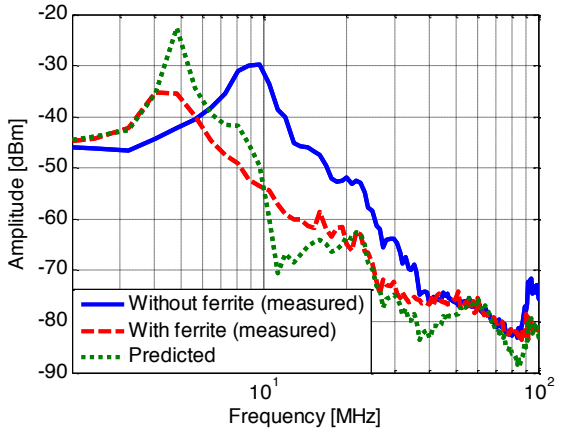


Fig. 11. Measured and predicted common mode current with an added ferrite.

## VI. CONCLUSIONS

The closed-form analytic model of the ferrite choke did a good job of predicting the impedance of a simple test setup and the change of impedance of a real system. This model allows relatively rapid calculation of the ferrite impedance and provides the framework for optimizing the characteristics of the ferrite (the ferrite material type and geometry) to solve specific emissions problems. Comparisons were made up to 100 MHz. While the analytic model of the ferrite would work to higher frequencies, experimental verification would require the use of different current clamps and possibly a different calibration technique.

The DCC method, when properly calibrated, performed well both when the system was fully passive, and when it was active and contained large CM currents generated by the system. Errors in the CM measurements were significantly reduced by measuring S-parameters for the DCC method while using averaging on the VNA. The largest errors in the predicted CM current/impedance were near resonances in the system impedance, suggesting an error in the DCC measurement. Good results with the DCC method generally required very careful application of the probes and calibration techniques.

## VII. AKNOWLEDGMENT

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# IV. COMMON-MODE IMPEDANCE OF A FERRITE CHOKE ON A CABLE HARNESS

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*Abstract*— Ferrite chokes are widely used to reduce common-mode (CM) currents in power systems. The CM impedance of the ferrite depends on the frequency–dispersive permeability and permittivity of the ferrite, the geometry of the system, and the location of the ferrite in it. An analytical model was developed to predict the CM impedance of a wire harness above a return plane with a ferrite on it. The model is based on transmission line theory for a cable, a ferrite, and a return plane. The parameters of the model are calculated using a frequency-dependent quasistatic model for a ferrite choke. This model accurately predicts the CM impedance of a mock harness within 3 dB up to 1 GHz. The proposed model is also applied to a real power system consisting of an inverter and motor. Knowledge of the CM impedance of the system in the operating regime is critical to determining the impact of the ferrite on CM currents. The CM impedance is determined using the dual current clamp technique. The impact of the ferrite on the CM impedance and currents of the power inverter system was predicted within 3 dB, demonstrating the usefulness of the modelling approach for analysis of power systems.

## I. INTRODUCTION

Ferrite chokes are used to reduce common-mode (CM) currents on cables and wire bundles in power systems by increasing their CM impedance and providing loss over a certain frequency range. A typical power system is shown in Fig. 1. It consists of a source (a power inverter), a three-phase power cable over a return plane (a metal chassis), and a load (a motor). The power inverter produces CM current on the power cable, which can generate unwanted radiation. A ferrite choke can be placed on the power cable to reduce CM current.

The best choice for a ferrite choke depends on many factors, including the CM impedance of the system and the choke. The impedance of a choke, typically a toroidal structure made of non-conducting magneto-dielectric ferrite material, depends on its permittivity and permeability, as well as geometrical factors like the size and shape of the choke, the geometry of the system the ferrite is used in, and the position of the ferrite choke within this system [1]-[13]. Determining the best choke through experimental "trial and error", where multiple ferrite chokes are placed in a system to observe the change in emissions, may be expensive and time-consuming, and often does not yield an optimal solution, particularly when size and weight are a concern.

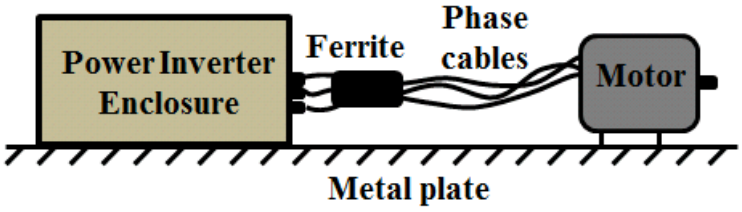



Fig. 1. A power system with a power cable bundle using a ferrite choke.

The objective of this work is to predict the effects of ferrite chokes on the CM impedance and CM current of a power system when the ferrite is placed on the cable harness. Predicting these effects requires a simple analytical or semi-analytical model of a ferrite choke. Of particular interest is the case where the harness runs above a return plane. A model for the ferrite and harness was built using transmission line theory, to account for wave propagation effects through the ferrite, and using a frequency-dependent quasistatic model of the ferrite choke. Since power systems typically generate problematic emission at frequencies less than 1 GHz, a working bandwidth up to 1 GHz was targeted for the model. Methods were also developed to apply the model within "real" power systems, where the harness CM impedance must be found when the system is turned on and running.

Although there are several publications describing models of ferrite cores [1]-[5], the simple models are applicable only at relatively low frequencies (less than a hundred

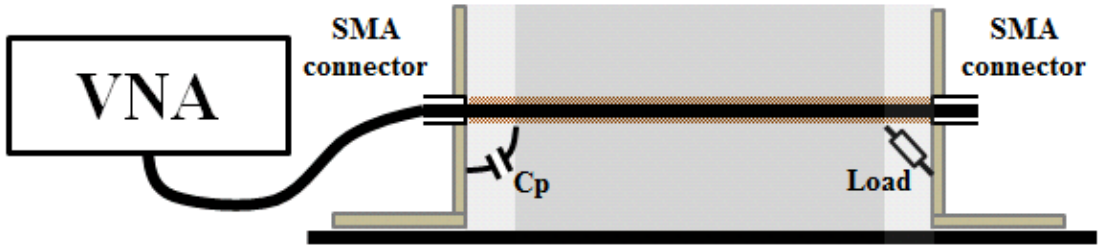
MHz). More complex lumped element models for ferrite cores may extend the frequency range [6]-[8]. In these published works, however, no propagation effects in the extended structures are considered. The radiated electric field from a system of a wire and ferrite choke suspended over the return plane is considered in [9] at frequencies up to 1 GHz, but these results are not sufficient to retrieve the CM impedance of power systems of interest. The frequency-dependent RLC parameters of toroidal and axial inductors with wire windings were considered in [10]. This model was applied to the surface-mounted components on printed circuit boards in [11], [12]. The approach in [10]-[12] for torroids may be modified and applied to a ferrite choke on a wire, but only at low frequencies. This was done in [13], where the frequency range was limited to about 200 MHz. No traveling-wave effects were taken into account, however, which limited the applicable frequency range of the published models. In addition, no connectors or supporting planes were considered either. None of the models in the literature fully account for the CM current in the return structure, and there are no simple analytical models to quantify the CM impedance of a power system with a ferrite choke. Information about the CM impedance is required to understand the impact of the ferrite.

In this paper transmission line theory is used with a frequency-dependent quasistatic model of the ferrite choke to predict the effects of the chokes on the CM loop impedance and CM current of a power system. The CM loop impedance is not trivial to measure, since a 'loop' of an active system cannot always be broken to make this measurement. The dual current probe method [14] is one possible approach to non-invasively measure the CM impedance of the system. This method was initially tested to predict the impact of ferrites on a system in [15]. This present paper extends the work in [15] through development of a simple approximate analytical broadband model of the ferrite choke and through application of the model to analyze a real power inverter/motor system.

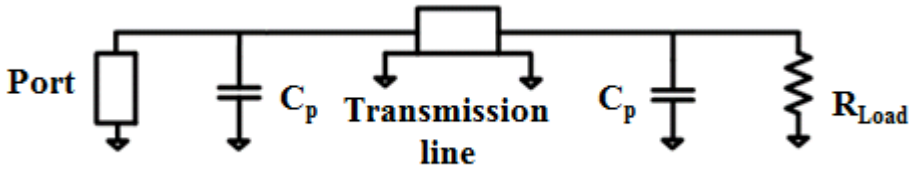
The structure of the paper is as follows. The analytic model of a harness with a ferrite choke over a metal chassis is developed in Section II, and per-unit-length parameters for the choke are derived. Section III contains an experimental validation of the model in a simple laboratory setup. In Section IV, methods are presented and tested for using the model within a real, active, power inverter system. The conclusions are summarized in Section V.

## II. ANALYTICAL MODEL

The electrical behavior of a ferrite choke depends not only on the constitutive parameters of the ferrite material, but also on the geometry of the structure where it is employed. The geometry used here is shown in Fig. 1. The multi-phase power cable is represented by a single wire, since CM currents see this harness as a single conductor. The current return path is represented as a solid perfectly-conducting plane, located underneath the cable. The test structure can thus be treated as a two-conductor distributed transmission line system carrying a single propagating TEM wave. This approximation is most appropriate when the cable or ferrite become electrically long. High-order modes may appear at high frequencies, but they are not considered in this model. A simple test structure and corresponding equivalent model used for initial experiments are shown in Fig. 2.




(a)




(b)

Fig. 2. Simplified structure of the system under test: (a) representation of the system as a conductor over a return plane connecting a source and load, and (b) an equivalent circuit for the structure.

The input impedance seen by the source looking into the cable is needed to characterize the system behavior. The characteristic impedance of a portion of a transmission line with a single propagating TEM wave, $Z = \sqrt{(R + j\omega L)/(G + j\omega C)}$, and the

propagation constant, $\gamma = \sqrt{(R + j\omega L) \cdot (G + j\omega C)}$, depend on the per-unit-length RLGC (resistance, inductance, conductance, and capacitance) parameters for the line. For a lossless transmission line running through the air above a return plane, RLGC parameters [16] are

$$R = \frac{1}{2\pi r_{wire} \delta \sigma_c}; \tag{1}$$

$$L = \frac{\mu_0}{2\pi} \ln\left(\frac{2h}{r_{wire}}\right); \tag{2}$$

$$C = \frac{2\pi\varepsilon_0}{ln(\frac{2h}{r_{wire}})}; \tag{3}$$

$$G = 0, \tag{4}$$

where $\sigma_c$ is the conductivity, $\delta$ is skin depth of the conductor, $r_{wire}$ is the radius of the conductor, and $h$ is the height of the conductor over the return plane.

The formulas to calculate the RLGC parameters of a cable suspended over a return plane with and without a ferrite choke are derived below. The ferrite structure is assumed to be concentric, which is the most common practical case, since the ferrite choke typically tightly embraces the cable for better elimination of the possible surface currents by the magnetic properties of the ferrite. During measurements, supporting styrofoam washers were used to assure the concentric position of the cable and the chokes.

*A. Calculation of per-unit-length inductance (L)*

The per-unit-length inductance of an infinitely long transmission line is defined as

$$L = \frac{\psi}{I \cdot l} = \frac{\int \mathbf{B} \cdot d\mathbf{S}}{I \cdot l}, \tag{5}$$

where $\psi$ is the total flux through the loop created by the CM current along the wire of unit length; $\boldsymbol{B}$ is the magnetic flux density over the loop, $d\boldsymbol{S}$; $l$ is the wire length; and $I$ is the CM current. Since the loop consists of a conductor over a return plane, the electrical parameters can be found using image theory (Fig. 3). The return plane can be removed and replaced with a mirror image of the conductor. The flux penetrating the area between the conductor and return plane is calculated to obtain the equivalent inductance per-unit-length. The flux is generated by both the CM current and its image. The magnetic flux density is higher in the ferrite material than in air.

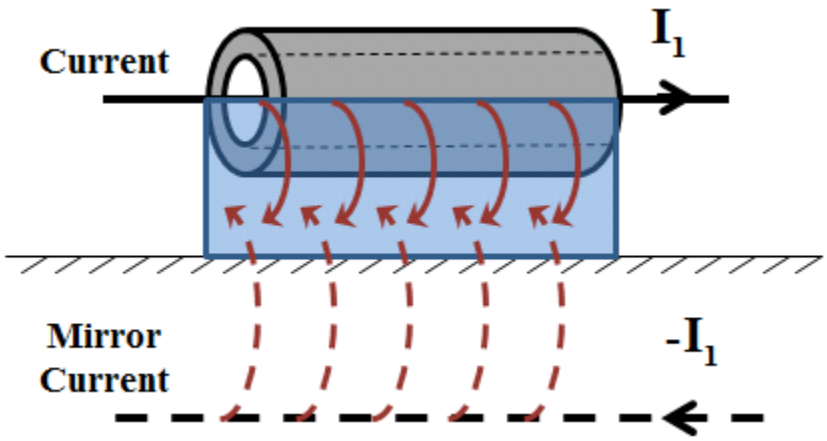



Fig. 3. Calculation of the inductance per unit length of the transmission line through the ferrite choke.

The flux generated in the ferrite by the mirror currents can be neglected. It is reasonable to assume that the inner radius of the choke is much less than the height of the cable above the return plane ($r_{in}$<<$h$), as is shown in Fig. 4. The maximum magnetic flux density in the ferrite generated by the mirror current is given by

$$B_{mirror} = \frac{I\mu}{2\pi(h+h-r_{fer})}, \tag{6}$$

where $r_{fer}$ is the outer radius of the ferrite. The maximum flux density in the ferrite generated by the current on the cable is given by

$$B_c = \frac{I\mu}{2\pi r_{in}}, \tag{7}$$

where $r_{in}$ is the inner radius of the ferrite. Since

$$\frac{I\mu}{2\pi(h+h-r_{fer})} < \frac{I\mu}{2\pi h} = \frac{I\mu}{2\pi r_{in}}, \tag{8}$$

the flux generated by the mirror current is negligible and can be ignored.

The magnetic flux between the wire and the return plane was calculated over three regions as shown in Fig. 4: *S1* is the area between the cable and the ferrite ($\mu=\mu_0$); *S2* is the area inside the ferrite ($\mu=\mu_0\mu_{r\_fer}$), and *S3* is the area between the ferrite and the return plane ($\mu=\mu_0$). The magnetic flux per-unit-length within each region is

$$\psi_1 = \int_{S1} \boldsymbol{B} d\boldsymbol{S} \approx \int_{r_{wire}}^{r_{in}} \frac{I\mu_0}{2\pi r} dr, \tag{9}$$

$$\psi_2 \approx \int_{r_{in}}^{r_{fer}} \frac{I\mu_0\mu_r'}{2\pi r} dr, \tag{10}$$

and

$$\psi_3 \approx \int_{r_{fer}}^{h} \frac{I\mu_0}{2\pi r} dr, \tag{11}$$

where $\psi_1$, $\psi_2$, and $\psi_3$ are the per-unit-length magnetic flux in regions *S1*, *S2*, and *S3*, respectively, and $\mu_r'$ is the relative permeability of the ferrite. The total flux between the wire and the return plane is

$$\psi \approx \frac{\mu_0 Il}{2\pi}[\ln\left(\frac{r_{in}}{r_{wire}}\right)+\ln\left(\frac{h}{r_{fer}}\right)+\mu_{r\_fer}{}'\ln(\frac{r_{fer}}{r_{in}})], \tag{12}$$

and the per-unit-length inductance is

$$L_{fer} = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{r_{in}}{r_{wire}}\right)+\ln\left(\frac{h}{r_{fer}}\right)+\mu_{r\_fer}{}'\ln\left(\frac{r_{fer}}{r_{in}}\right)\right]. \tag{13}$$

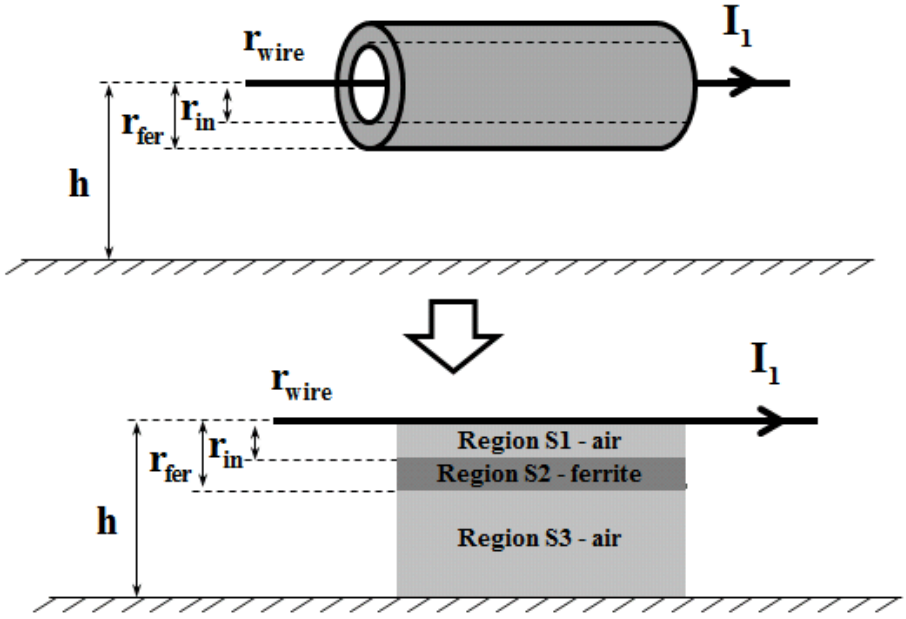



Fig. 4. Geometry associated with the ferrite over the return plane.

*B. Calculation of per-unit-length resistance (R)*

The per-unit-length resistance of the transmission line with the ferrite choke is due to the skin-effect in the conductor, and due to the ohmic loss in the ferrite. The magnetic loss in the ferrite choke is associated with the imaginary part of permeability. By replacing $\mu_{r\_fer}{}'$ in (13) with $\omega\mu_{r\_fer}{}''$, and $\omega\mu_{r_{air}}{}''$ for air, where $\omega=2\pi f$ is angular frequency, one can find the per-unit-length resistance associated with the ferrite choke as

$$R_{fer} \approx \frac{\omega\mu_0}{2\pi}\left[\mu_{r\_air}'' \ln\left(\frac{r_{in}}{r_{wire}}\right) + \mu_{r\_air}'' \ln\left(\frac{h}{r_{fer}}\right) + \mu_{r\_fer}'' \ln\left(\frac{r_{fer}}{r_{in}}\right)\right]. \quad (14)$$

Since there is practically no magnetic loss in the air, the per-unit-length resistance due to the ferrite choke is then

$$R_{fer} = \frac{\omega}{2\pi}\mu_0\mu_{r\_fer}'' \ln\left(\frac{r_{fer}}{r_{in}}\right), \quad (15)$$

These losses will dominate conductive losses over the frequency range where ferrite is used.

*C. Calculation of per-unit-length capacitance (C)*

The electric field distribution between the wire and return plane is affected by the presence of the ferrite choke. Analytical calculation of the capacitance requires simplifying assumptions. For this purpose, the electric field between the conductor and the ferrite, and the electric field within the ferrite are assumed to be radially symmetric.

The cross-section of the cable and ferrite over the ground plane with the corresponding parts of the capacitance are shown in Fig. 5.

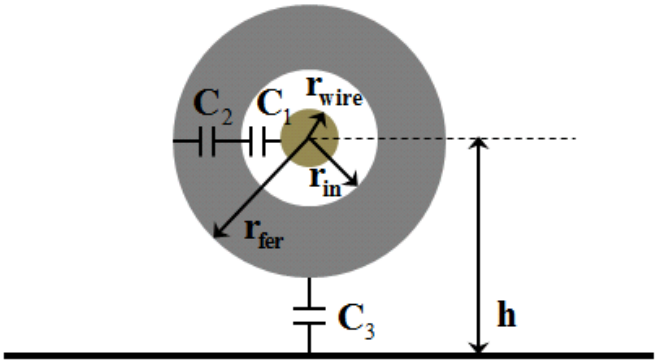



Fig. 5. Cross- section of the cable and ferrite over the return plane.

The per-unit-length capacitance between the conductor and the ferrite, $C_1$, and the per-unit-length capacitance between the inner and outer wall of the ferrite, $C_2$, can be calculated from the capacitance of the coaxial structure as

$$C_1 \approx \frac{2\pi\varepsilon_0}{ln(\frac{r_{in}}{r_{wire}})}, \tag{16}$$

and

$$C_2 \approx \frac{2\pi\varepsilon_0\varepsilon_r^{'}}{ln(\frac{r_{fer}}{r_{in}})}, \tag{17}$$

where $\varepsilon_r'$ is the real part of permittivity of the ferrite. The per-unit-length capacitance between the ferrite and the return plane, $C_3$, can be found from the formula for capacitance of a conductor over a return plane

$$C_3 = \frac{2\pi\varepsilon_0}{cosh^{-1}(\frac{h}{r_{fer}})}, \tag{18}$$

The total per-unit-length capacitance of the ferrite part is found from the three capacitors in series,

$$C_{fer} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}. \tag{19}$$

*D. Calculation of per-unit-length conductance (G)*

The per-unit-length conductance can be found from the capacitance associated with the ferrite and the dielectric loss in the ferrite as [17]

$$G_{fer} = \omega C_2 \frac{\varepsilon_r''}{\varepsilon_r'}. \tag{20}$$

The RLGC parameters in (13), (15), (19), and (20) can be used to find the characteristic impedance and propagation constant for the transmission line including the ferrite. In the next section, this model of the ferrite choke is validated along with a model of the larger system.

## III. EXPERIMENTAL VALIDATION OF THE SYSTEM

To validate the approximate analytical model of the ferrite choke, tests were performed on a simple setup consisting of a brass tube over a return plane. This simple test setup shown in Fig. 6 is analogous to the system shown in Fig. 2. Since the details of the test setup are known, the system impedance can be calculated analytically. In the experiment, a Vector Network Analyzer (VNA) was used to measure $Z_{11}$ from the source side of the system, as indicated in Fig. 6. Measurements of the input impedance were made both with and without a ferrite placed on the brass tube. In many power systems, the inverter and motor are covered by metal enclosures. In the test setup used here, the enclosure was simulated using L-shaped brass stands, which support the brass tube at a chosen height above the return plane, as is shown in Fig. 6. The interface between the

brass stand and brass tube creates parasitic capacitances similar to the capacitances that would be seen in a real system with an enclosure. The L-shaped stands are built to have a good electric contact with the return plane. In a real system, the ferrite choke will be placed around the whole bundle of cables. In the test setup, the ferrite is placed on the brass tube simulating the CM component of current on the cables. The input impedance of the setup calculated analytically will be compared to the measured result.

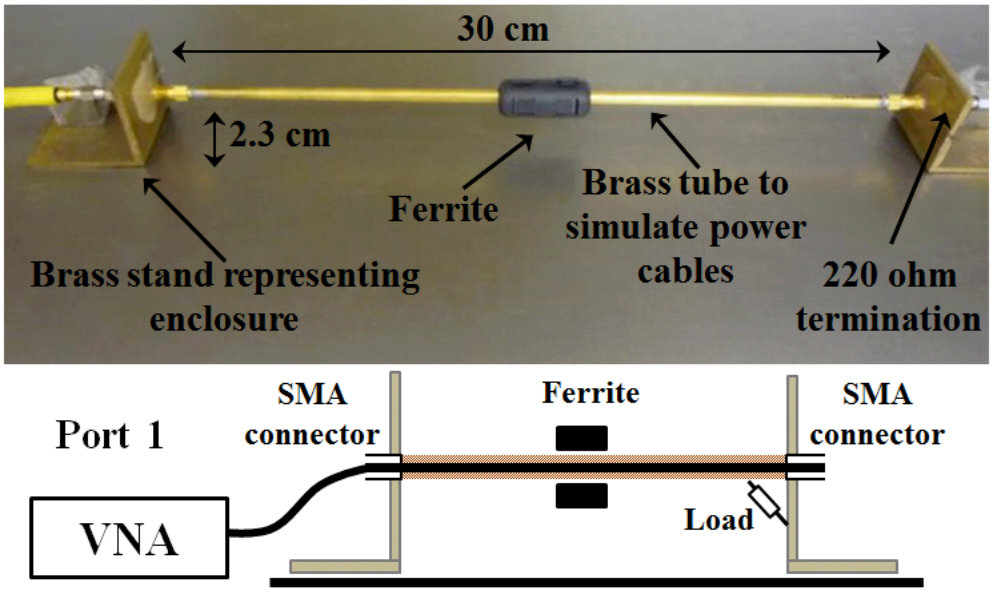



Fig. 6. Simplified test structure based on the real power system.

*A. Modeling the test structure*

The test structure shown in Fig. 2 and Fig. 6 includes an impedance related to the source, an impedance of the load, a transmission line, and a set of parasitic capacitances between the transmission line and the "enclosure" (the L-shaped brass stands). The source impedance is 50 Ω and is associated with the VNA. The brass tube over the return plane represents the transmission line. The brass tube was terminated with the brass stand on the right using a 220 Ω resistor. This termination impedance (220 Ω) was chosen to approximately match the characteristic impedance of the transmission line when no ferrite was placed on the brass tube.

Lumped element parasitic capacitors, $C_p$, between the brass tube and brass stands were added to each end of the transmission line to model the parasitic capacitance between the enclosure and brass tube. These capacitors are crucial to an accurate modeling of the high-frequency impedance of the system. They are present at both the source and the load ends of the transmission line. Their values are approximately the same due to the structure symmetry. The value of these capacitors can be found from the geometry decomposition of the structure around the brass stands, as is shown in Fig. 7. The parallel capacitors C', C", and C"' determine the value of $C_p$ in Fig. 2b,

$$C_p = C' + C'' + C'''. \tag{21}$$

where $C'$ is the capacitance between the brass tube and the brass stand. $C''$ is the capacitance between the outer shield of the connector and the brass stand, and $C'''$ is the capacitance between the inner conductor of the connector and the brass stand. The capacitances at the two ends of the transmission line, $C_p$, are assumed to be equal for this study.

The capacitance $C'$ between the brass tube and the brass stand placed at the $90^0$ angle can be calculated as follows. While the entire brass tube and brass stand contribute to this capacitance, the most important contributors are the portions of the two structures which are closest to each other. The capacitance $C'$ was calculated between a metal plate the size of the brass stand and a cylindrical conductor with the same length as the height of the brass stand. This capacitance can be approximately estimated by unfolding the cylindrical brass tube into a sheet and then calculating the capacitance between the two perpendicular sheets as [18]

$$C' = \varepsilon_0 \left( \frac{K'(k_{in})}{K(k_{in})} + \frac{K'(k_{out})}{K(k_{out})} \right) \tag{22}$$

where $\varepsilon_0$ is the permittivity of free space, and $k_{in}$, $k_{out}$, $K'(\cdot)$, and $K(\cdot)$ are given in [18].

The capacitance $C''$ is the capacitance between the end of the brass tube and the brass stand. This capacitance can be calculated from the capacitance of two parallel plates of different size, as is shown in Fig. 9. This capacitance is approximately

$$C'' \approx \frac{\varepsilon_0 A}{d} \tag{23}$$

where $A$ is the area of the end-plate and $d$ is the distance between the connector and the brass stand.

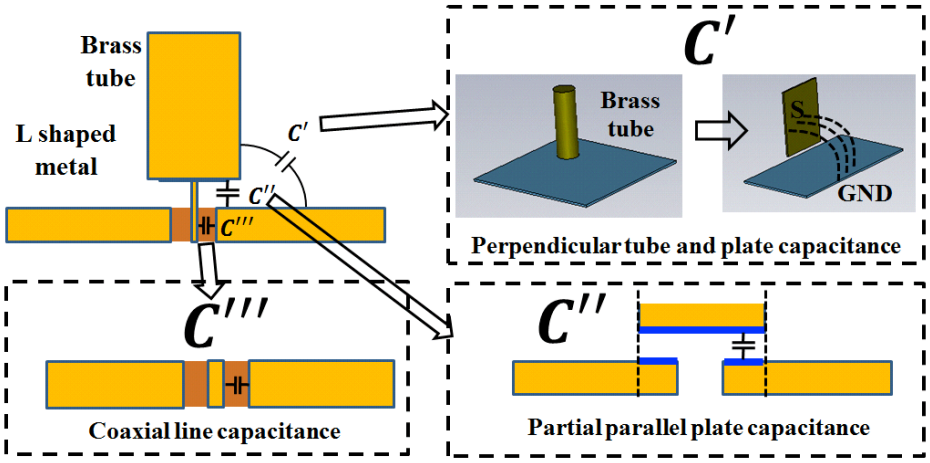



Fig. 7. Calculation of capacitance between the brass tube (common-mode carrying conductor) and the brass stand ("enclosure").

The capacitance $C'''$ is between the inner conductor and the brass stand over the area where the conductor penetrates the stand, as shown in Fig. 9. If fringing fields are neglected, this capacitance can be found from the equation for capacitance of a coaxial structure:

$$C''' \approx \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_{inner}}{r_{stand}}\right)} \tag{24}$$

where $r_{inner}$ is the radius of the inner conductor of the connector, $r_{stand}$ is the inner radius of the hole in the brass stand, and, in this case, $\varepsilon_r$ is the dielectric constant for the standard SMA connector dielectric material (PTFE).

*B. Test-structure impedance without ferrite*

The characteristic impedance of the transmission line without ferrite is calculated using the per-unit-length RLGC parameters. The input impedance at the source end can be calculated step by step starting from the termination (220 Ω load) as illustrated in Fig. 8. The impedance looking into the load is given by

$$Z_{input\_load} = \frac{R_{load}}{R_{load} j\omega C_p + 1} \tag{25}$$

where $R_{load}$ is 220 Ω for this setup and $C_p$ is the capacitance between the brass tube and the brass stand as calculated in the previous section. The input impedance looking into the transmission line after the parasitic capacitance is

$$Z_{input\_after\_Cp} = Z_0 \frac{Z_{input\_load} + Z_0 \tanh(\gamma l)}{Z_0 + Z_{input\_load} \tanh(\gamma l)} \tag{26}$$

where $Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}}$ is the characteristic impedance of region 1, $R_0$, $L_0$, $G_0$ and $C_0$ can be found as in (1)-(4), and $l$ is the length of region 1. The impedance looking into the transmission line from the source $Z_{input}$, is

$$Z_{input} = \frac{Z_{input\_after\_Cp}}{Z_{input\_after\_Cp} j\omega C_p + 1} \tag{27}$$

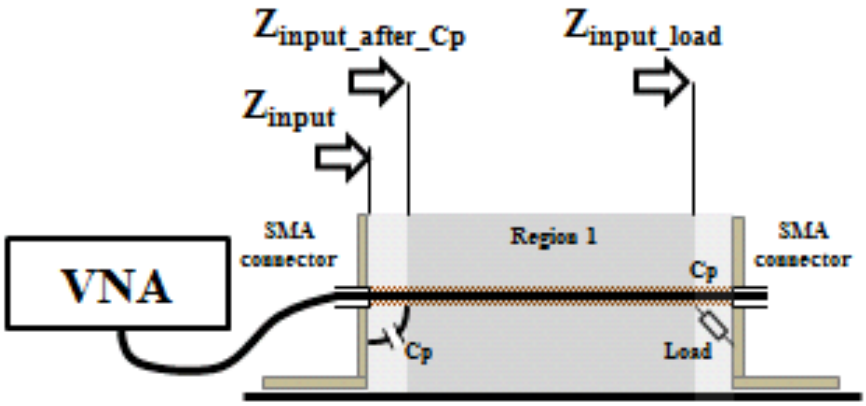
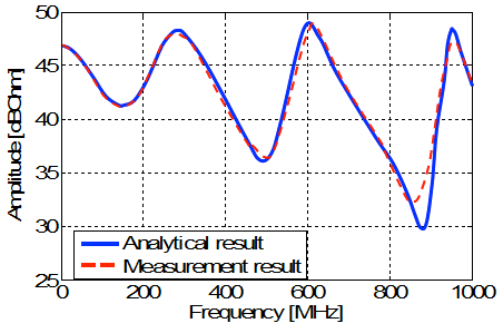
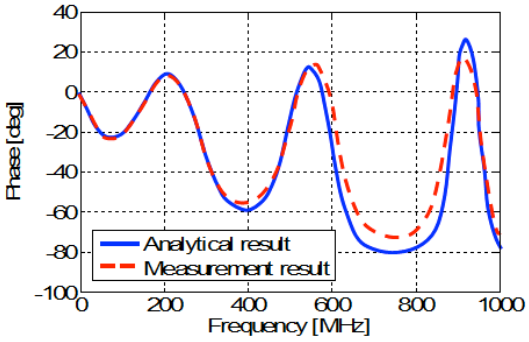



Fig. 8. Distinguishing input impedances of the structure.

The input impedance, $Z_{11} = Z_{input}$, corresponding to the experimental setup shown in Fig. 8, was calculated analytically and was measured using a VNA. The radius of the brass tube used in the experiment was 2.16 mm, its total length was 30 cm, and the distance between the lower points on the brass tube and the return plane was 2.3 cm. The calculated and measured amplitude and phase of $Z_{11}$ are shown in Fig. 9. The measured input impedance and the analytical results agree well up to 1 GHz (within less than about 2 dB and 10 degrees).




(a)




(b)

Fig. 9. Magnitude (a) and phase (b) of the measured and estimated input impedance of the test structure without a ferrite.

*B. Test structure impedance including the ferrite choke*

The next step was to develop and verify a model of the system including a ferrite choke. The input impedance was calculated using the model shown in Fig. 10. The characteristic impedance of the portion of the transmission line containing the ferrite choke (region 2 in Fig. 10) was found using its RLGC parameters as in Section II.

The impedance looking from the ferrite toward the load is

$$Z_{input\_after\_ferrite} = Z_0 \frac{Z_{input\_load} + Z_0 \tanh(\gamma l_1)}{Z_0 + Z_{input\_load} \tanh(\gamma l_1)} \tag{28}$$

where $Z_0$, is the characteristic impedance of region 1, $\gamma$ is the complex propagation constant in region1, $R_0$, $L_0$, $G_0$and $C_0$ are obtained from (1)-(4), and $l_1$ is the length of region 1. The impedance looking into the ferrite toward the load is

$$Z_{input\_before\_ferrite} = Z_{ferrite} \frac{Z_{input\_after\_ferrite} + Z_{ferrite} \tanh(\gamma_{fer} l_2)}{Z_{ferrite} + Z_{input\_after\_ferrite} \tanh(\gamma_{fer} l_2)} \tag{29}$$

where $Z_{ferrite}$ is the characteristic impedance of Region 2, $l_2$ is the length of the ferrite, and $\gamma_{fer}$ is the complex propagation constant in ferrite. $Z_{ferrite}$ is given by

$$Z_{ferrite} = \sqrt{\frac{R_{fer} + j\omega L_{fer}}{G_{fer} + j\omega C_{fer}}} \tag{30}$$

where $L_{fer}$, $R_{fer}$, $C_{fer}$, $G_{fer}$, can be calculated from (13), (15), (19), and (20). The impedance looking into the transmission line from the source end is given by

$$Z_{input\_after\_Cp} = Z_0 \frac{Z_{input\_before\_ferrite} + Z_0 \tanh(\gamma l_3)}{Z_0 + Z_{input\_before\_ferrite} \tanh(\gamma l_3)} \tag{31}$$

where $l_3$ is the length of Region 3. The overall input impedance, $Z_{input}$, is then

$$Z_{input} = \frac{Z_{input\_after\_Cp\_f}}{Z_{input\_after\_Cp\_f} j\omega C_p + 1}, \tag{32}$$

where $Z_{input\_after\_Cp\_f}$ is the input impedance looking into the transmission line after capacitance with presence of a ferrite.

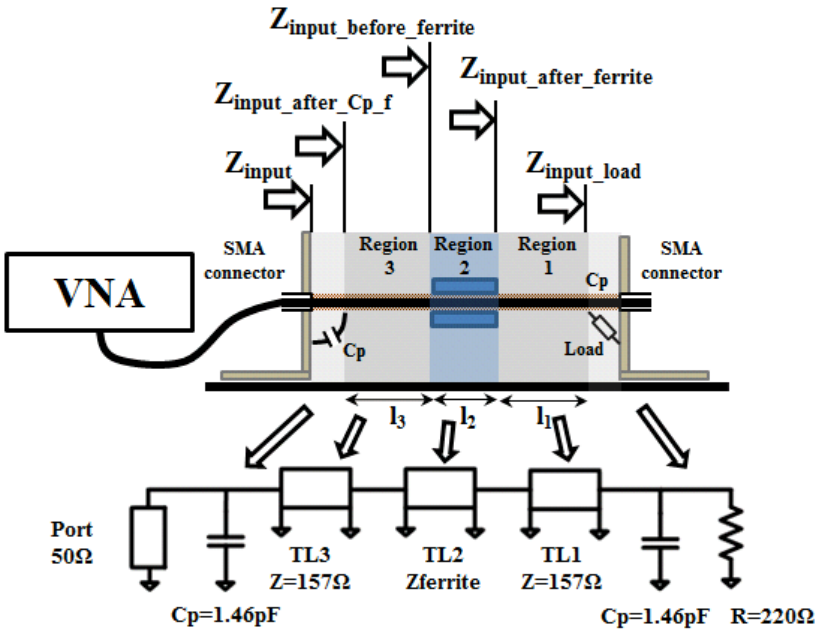



Fig. 10. Calculation of input impedance with ferrite on transmission line.

The model was tested while placing a ferrite choke at different locations on the brass tube. The inner radius of the ferrite choke was 1.2 cm, its outer radius was 1.8 cm, and its length was 1.3 cm. The permeability and permittivity of the ferrite material of the choke are shown in Fig. 11. The height of the brass tube above the return plane was 2.3 cm in initial tests. The input impedance was measured and calculated analytically, and the results compared.

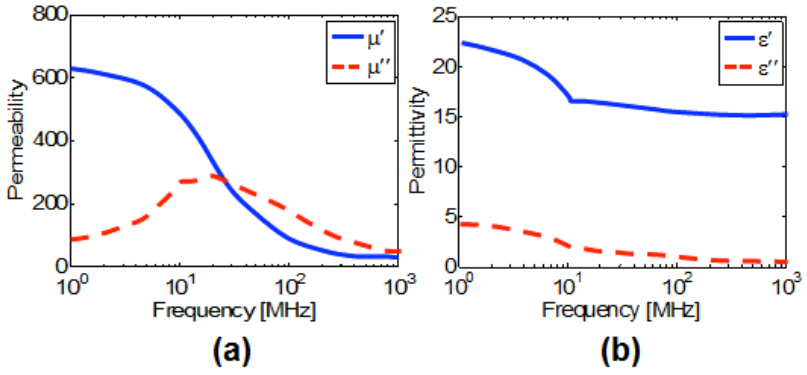



Fig. 11. Permeability (a) and permittivity (b) of the ferrite choke.

The model was tested while placing a ferrite choke at different locations on the brass tube. The inner radius of the ferrite choke was 1.2 cm, its outer radius was 1.8 cm, and its

length was 1.3 cm. The permeability and permittivity of the ferrite material of the choke are shown in Fig. 11. The height of the brass tube above the return plane was 2.3 cm in initial tests. The input impedance was measured and calculated analytically, and the results compared.

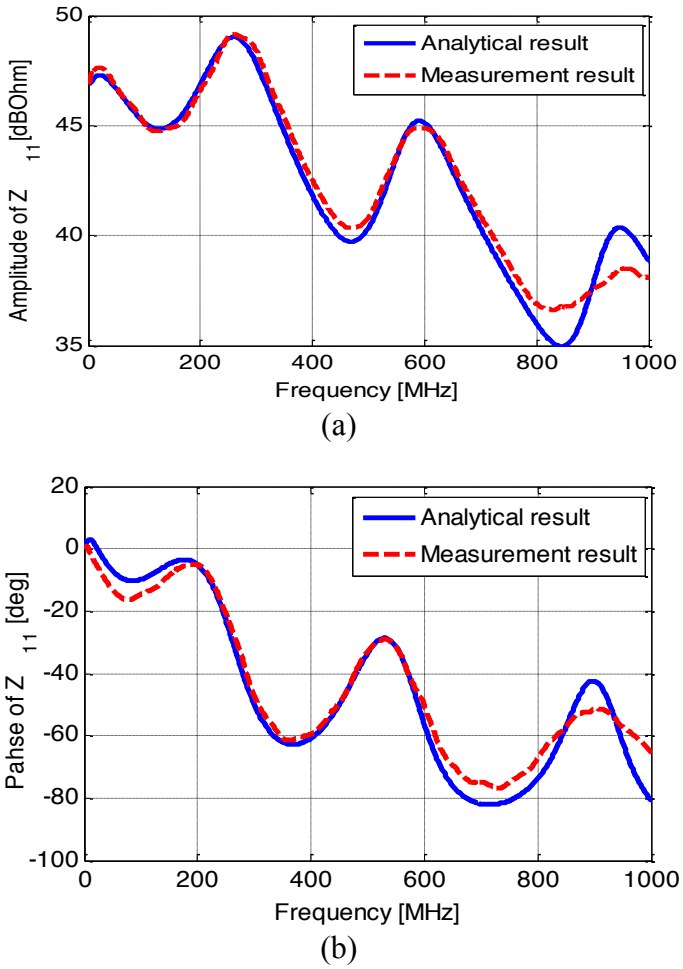



Fig.12. Magnitude (a) and phase (b) of the measured and estimated input impedance of the test structure when the ferrite is placed close to the source.

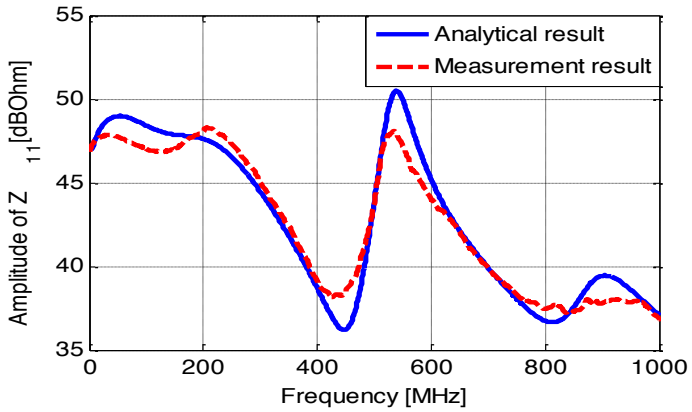



Fig. 13. Magnitude of the measured and estimated input impedance of the test structure when the ferrite is placed at the center of the brass tube. .

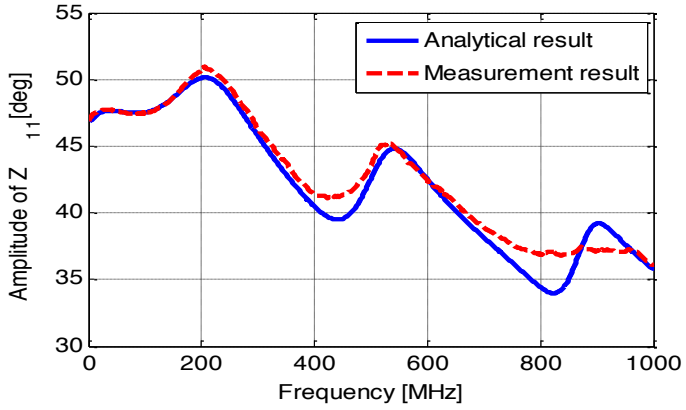



Fig. 14. Magnitude of the measured and estimated input impedance of the test structure when the ferrite is placed at a height of 7.7 cm and close to the source.

Ferrite chokes of different sizes and of different composition were also tested. The tested sizes are indicated in Table I. Previous tests were performed using ferrite choke "d", whose material characteristics are given in Fig. 11. Ferrite choke "e", was made from a different material than ferrites a-d. This ferrite had a center frequency of approximately 80 MHz. Measured and simulated impedances matched within 2-3-dB. Analysis of the results using Frequency Selective Validation (FSV) [19], [20], showed that all of the simulated impedances were "good" (max Global Difference Measure = 0.37) to "excellent" (min Global Difference Measure = 0.09).

Table I.

Different Ferrites Under Test

| | | | | |
|---|---|---|---|---|
|  |  |  |  |  |
| Ferrite a | Ferrite b | Ferrite c | Ferrite d | Ferrite e |
| $r_{in} = 13.5$ | $r_{in} = 8.6$ | $r_{in} = 10.3$ | $r_{in} = 12$ | $r_{in} = 12.7$ |
| $r_{out} = 25.4$ | $r_{oiut} = 19.5$ | $r_{oiut} = 15.9$ | $r_{oiut} = 18$ | $r_{oiut} = 25.6$ |
| $l = 29$ | $l = 21.9$ | $l = 21.9$ | $l = 13$ | $l = 39.7$ |

## IV. APPLICATION TO A REAL POWER SYSTEM

To apply the ferrite model to a real system requires knowledge of the CM loop impedance of the system. This CM loop impedance is not trivial to measure as it is often associated with a harness consisting of many conductors, and also because for an active system a "loop" cannot be broken to make the CM impedance measurement. In this work the CM loop impedance was measured using the Dual Current Clamp (DCC) techniques described in [14] and [15]. In this technique, CM energy is injected into the system by one current probe and the resulting CM current is measured by another current probe using a VNA. The CM loop impedance can be found from the amount of injected current. The frequency response of the current probes is de-embedded through a rather simple calibration procedure using a special calibration fixture as described in [14], [15].

The ferrite model was tested with a real, active power inverter/motor system with emissions up to about 100 MHz. To predict the influence of a ferrite, the CM circuit of the system was simplified as a CM voltage source in series with a CM loop impedance. Assuming that the ferrite is electrically small below 100 MHz the CM impedance at the ferrite location can be found as a sum of the original system loop impedance and the analytically calculated ferrite impedance. The CM currents after adding a ferrite is then

$$I_{CM,estimated} = I_{CM,measured} \frac{Z_{loop,measured}}{Z_{loop,measured} + Z_{ferrite,analytical}}, \quad (35)$$

where $I_{CM,measured}$ and $Z_{CM,measured}$ are the measured CM current and CM impedance of the ferrite, respectively, and $Z_{ferrite,analytical}$ is the analytically estimated impedance of the ferrite.

The tested power system consists of a motor drive generating 230 V RMS signals, a harness, and a 20 hp motor as shown in Fig. 15. A broadband ferrite was placed on the harness as shown in the figure. The CM loop impedance and CM current was measured with and without the ferrite using a VNA. For emissions measurements, the VNA was replaced with a spectrum analyzer. The current clamps were places around all three phase cables.

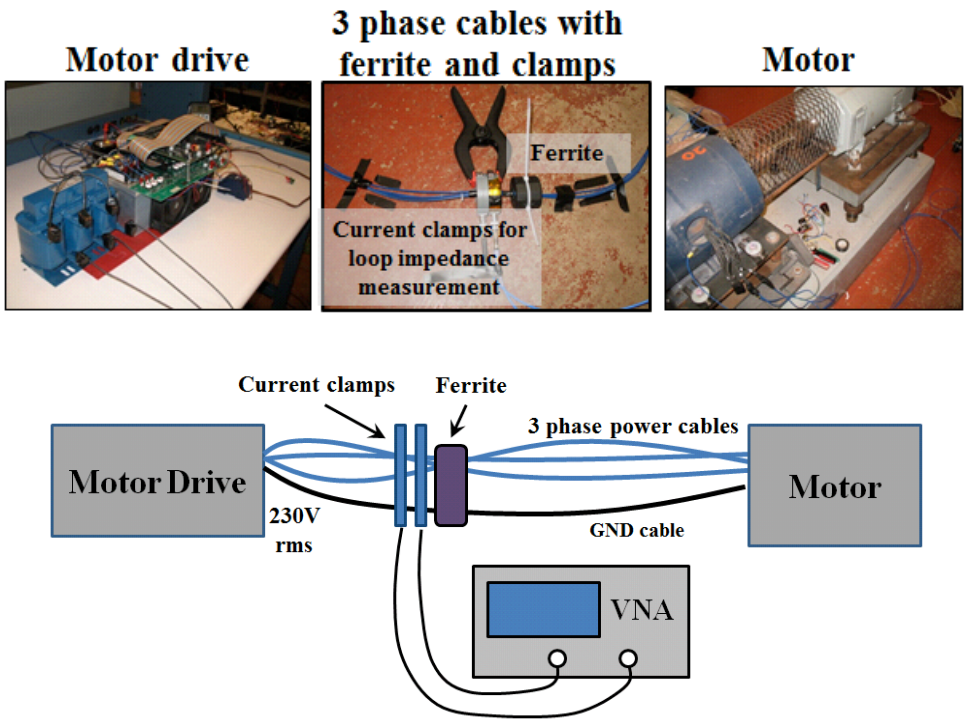



Fig. 15. Power system measurement setup.

The measured and predicted CM loop impedance and CM current with and without a ferrite are shown in Fig. 16 and Fig. 17. The CM loop impedance and CM current with the ferrite was predicted based on measurements without the ferrite. The proposed model was able to predict the CM impedance or CM current with the ferrite within 3 dB up to

100 MHz, validating the usefulness of both the ferrite model and the system characterization technique for predicting the impact of ferrites in real power systems.

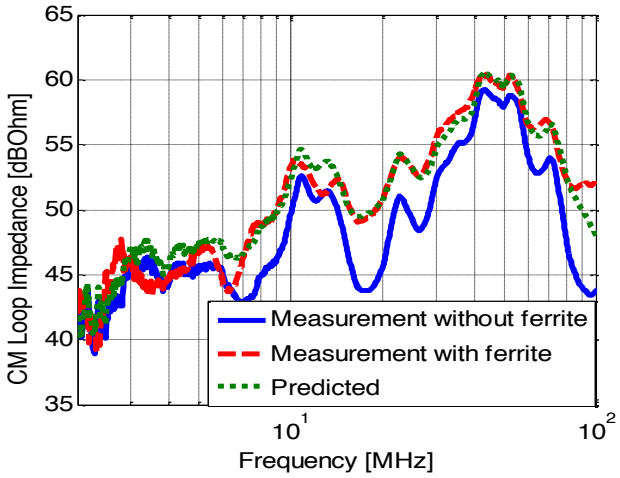



Fig. 16. Measured and predicted CM impedance with an added ferrite.

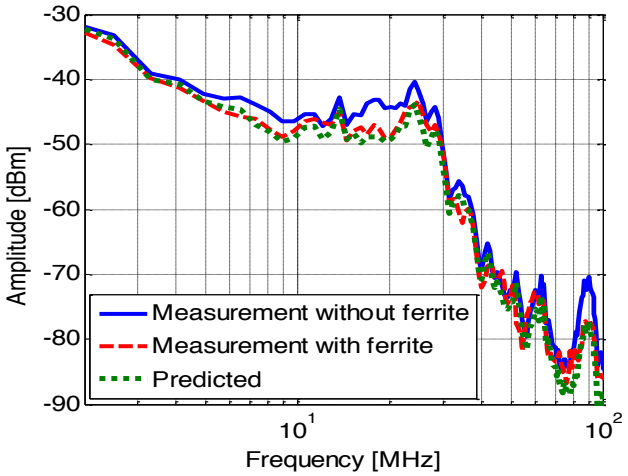



Fig. 17. Measured and predicted CM current with an added ferrite.

## V. CONCLUSIONS

A comparatively simple analytical model was proposed for a ferrite choke on a cable above a return plane. This model uses a transmission line approximation of the cable, ferrite, and return plane, and uses a frequency-dependent, quasistatic approximation of the ferrite to determine transmission line parameters. The proposed model allows prediction of the CM input impedance of a cable with a ferrite choke on it. Because the model is relatively simple, it provides the possibility of analytically optimizing ferrite characteristics to mitigate unwanted emissions. Efficient variation of ferrite material

parameters, choke and cable geometry, and their placement with respect to the source and to the return plane can be done. Experimental validation of the model showed the CM impedance of a transmission line with the ferrite could be approximated within 3 dB up to 1 GHz.

The proposed model was further applied to predict the impact of a ferrite on the CM impedance and CM currents of a power system consisting of a power inverter and motor. Measurement of the CM impedance of the system without the ferrite was critical for predicting the impact of the ferrite on the CM current in the active inverter system. This CM impedance was determined using the dual current probe approach. Using this impedance as a starting point, the impact of the ferrite on the CM impedance and current was predicted within 3 dB up to 100 MHz (the practical limit of the current clamps and calibration technique). This result demonstrates the proposed techniques can be useful for applications to power systems.

One possible limitation of the model is that it assumes TEM propagation through the ferrite above a return plane. If there are not many structures around the power cable, the CM current return path is typically a return plane and, if the return plane is close and frequencies sufficiently low, the TEM approximation should be valid. If the CM current does not return through a plane, however, the RLGC approximations calculated here may not apply. At sufficiently high frequencies, the TEM approximation also breaks down. For the geometry under consideration, the TEM approximation is valid up to 1 GHz. The limiting frequency, however, depends on the geometry of the structure.

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# SECTION

# 2. CONCLUSIONS

In this dissertation different methods were studied to model power inverter systems to reduce their radiated emissions. These methods are presented as four separate papers.

In the first paper, a methodology is presented to develop a relatively simple measurement-based equivalent circuit of a complex system. The methodology was applied to a real power inverter/motor system. The equivalent model was built for each subsystem and validated through measurements. The subsystem models were assembled to create a model of the complete system. The model agreed with measurements within 3-4 dB. Elements of the model were correlated to the system geometry, and analysis of possible causes of resonances was discussed. Possible mitigation strategies were evaluated and their effect on radiated emissions was predicted and validated. While the methodology was applied to a power inverter system, it can be applied to other systems, where frequencies of interest are below 100 MHz.

In the second paper, development of simple physics-based models from partial element equivalent circuit is considered. With this method reduced circuits are obtained based on geometry information and some knowledge of simplified model. The purpose of the reduction is not accelerating computation speed, as it can be achieved by many known model order reduction techniques, and not getting a coarse mesh for fast analysis, but acquiring better understanding of the model behavior. With the method clear correlation between simplified circuit elements and real geometry is obtained. This is very important for root-cause analysis of EMC issues and improving the design. To ensure physicality, model reduction for inductive and capacitive elements is done separately. The proposed reduction method is supposed to work up to a few hundreds of megahertz. It was applied to simple power electronics systems and showed agreement within a few dB with reference results for reasonably small number of elements in the reduced model.

In the third and fourth papers, transmission line theory is used with a frequency-dependent quasistatic model of the ferrite choke to predict the effects of the chokes on the

common-mode loop impedance and common-mode current of active power systems. Developed model is relatively simple and provides the possibility of analytically optimizing ferrite characteristics to mitigate unwanted emissions. Experimental validation of the model showed the common-mode impedance of a transmission line with the ferrite could be approximated within 3 dB up to 1 GHz. The common-mode loop impedance of an active system is measured using noninvasive dual current clamp measurement technique. Using this impedance as a starting point, the impact of the ferrite on the common-mode impedance and current was predicted within 3 dB up to 100 MHz (the practical limit of the current clamps and calibration technique). This demonstrated that the proposed techniques can be successfully used for applications to power systems.

# VITA

Natalia Bondarenko was born in Tbilisi, Georgia, Europe. She received her Bachelor of Science degree in Applied Mathematics and Computer Science (2006) and Master of Science degree in Electrical and Electronics Engineering (2009) from Ivane Javakhishvii Tbilisi State University. From 2005 to 2009, she was with EMCoS, Ltd., working on consulting projects for automotive Electromagnetic Compatibility. In 2010 she was a summer intern at Robert Bosch GmBH in Applied Research Electronics Group. Her research interests include EMC of power inverter systems, system level EMC/EMI modeling and measurement methods. In May 2015 she received her Doctor of Philosophy degree in Electrical Engineering from Missouri University of Science and Technology.