01 Aug 2007

Redundancy Optimization for Clock-Free Nanowire Crossbar Architecture

Yadunandana Yellambalase

Ravi Bonam

Minsu Choi
Missouri University of Science and Technology, choim@mst.edu

Recommended Citation

Y. Yellambalase et al., "Redundancy Optimization for Clock-Free Nanowire Crossbar Architecture," *Proceedings of the 7th IEEE International Conference on Nanotechnology (2007, Hong Kong, China)*, pp. 621-623, Institute of Electrical and Electronics Engineers (IEEE), Aug 2007.
The definitive version is available at https://doi.org/10.1109/NANO.2007.4601267

Proceedings of the 7th IEEE
International Conference on Nanotechnology
August 2 - 5, 2007, Hong Kong

Redundancy Optimization for Clock-Free Nanowire Crossbar Architecture

Yadunandana Yellambalase, Ravi Bonam, Minsu Choi

***Abstract*—In this paper a method is being proposed to find the optimal dimension of Programmable Gate Macro Block (PGMB) in clock-free nanowire crossbar architecture. A PGMB is a nanowire crossbar matrix with discrete number of rows and columns on which the NCL (Null Convention Logic) gates can be programmed. This method uses inherent redundancy to route through defective crosspoints. A 6 X 10 defect-free crossbar can be used to program any of the 27 threshold gates. Due to imperfections and variations in nanoscale manufacturing process, high defect densities are anticipated. Thus, such defects should be located when tested and the logic has to be rerouted around them to maintain proper functionality. This paper discusses this problem and tried to find an optimal solution through simulations. In the final submission, more effective logic mapping techniques will be proposed and validated.**

***Index Terms*—Clock-free Nanowire Crossbar Architecture, Null Conventional Logic (NCL), Defect-Avoidance mapping,**

I. Introduction

Researchers have proposed many nanowire crossbar architectures and many have developed methods for programming the crosspoints and routing of signals through the crossbar network. Nanowire crossbar is a two dimensional network of horizontal and vertical wires overlapping each other and crosspoints are used as programmable junctions. A clock-free architecture has been proposed by the authors' research group. A delay-insensitive encoding called NCL (Null Convention Logic) [1,2] is used to remove the clock distribution network from the conventional clocked counterparts. The proposed architecture has various advantages such as improved manufacturability, scalability, robustness and defect & fault-tolerance. In this paper, we will propose a method to find the optimal dimension of the programmable logic blocks used in the clock-free nanowire crossbar architecture. In the final submission, more effective logic mapping techniques will be proposed and validated.

The Authors are with the Electrical and Computer Engineering Dept. University of Missouri Rolla, Rolla, MO 65409 USA ({ypymy9, rkbcdf, choim} @umr.edu).

A. Null conventional logic

NCL uses two signals, the NULL wave front and DATA wave front so that data and control can be integrated into a single signal which eliminates the need of clock to synchronize operation of a circuit. We will introduce combined nanowire crossbar with asynchronous logic called Null Conventional Logic (NCL) [1] to produce asynchronous crossbar architecture. There are 27 gate macros in NCL using which any complex delay-insensitive circuit can be implemented [2][3].

B. Programmable Gate Macro Block (PGMB)

A crossbar architecture consisting of 6 rows and 10 columns with feedback logic can be used to implement any of 27 NCL threshold gates. This logic block consists of pull up and pull down

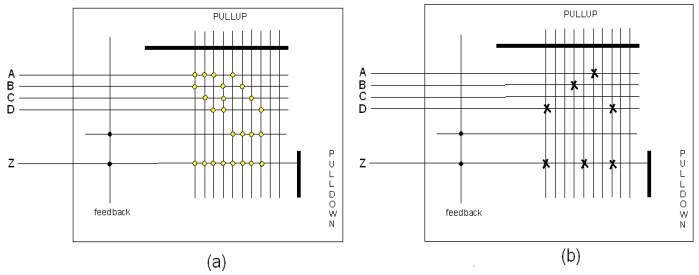

Figure 1: PGMB with a)TH34w2 b) Defects

resistors forming OR and AND planes. This basic unit is referred as PGMB (Programmable Gate Macro Block) and a new architecture based on this consists of 2-dimensional grid structure of PGMBs.

Figure 1[a] shows a threshold gate TH34w2 implemented on PGMB. Even though the minimum required rows and columns of PGMB gives flexibility to implement any of the 27 gate macros, the defects present at the PGMB cross points will prevent implementation of some of them as shown in Figure 1[b] where the same gate can not be programmed. These defects will lead to several nonprogrammable PGMBs resulting in lower yield of the grid structure.

II. SIMULATION AND RESULTS

We can overcome this problem by simply increasing the number of rows and columns of the PGMBs. This will increase the probability of programming a PGMB by working around the defective cross points. The following sections describe the Matlab simulations performed to find an optimum size of PGMB .

A. Defect map of a 2D- grid structure of PGMB

A defect map of a PGMB was generated in the form of a matrix. To indicate a non-programmable crosspoint at a certain location, 1 was allocated and a programmable cross-point was marked with 0. In fabricating PGMB structures, physical imperfections may result in defective crosspoints in clusters. Thus, cluster defect model was considered in this paper rather than the random defect model. The defect maps were randomly generated in the form of clusters with negative binomial distribution as described by Stapper [4]. The probability of introducing a fault into a given cross-point during a time interval Δ t of the manufacturing process is given by:

$$p(\Delta t \mid k, l_1, l_2, \cdots, l_n) = c(x, y) + b_k + \sum_{l=0}^{n} b_i l_i \quad \psi$$

where c(x, y) is the susceptibility function, k is the number of defects already present in the PGMB, the index i pertains to the adjacent and other neighboring crosspoints, n indicates the number of neighboring crosspoints considered, b is the global cluster actor, bi is the local cluster factor and li is the number of faults that occur on neighboring circuit area. In Figure 2 a grid of PGMBs with 9 rows and 14 columns with 10% defect rate is shown. White dots represent non-programmable crosspoints (i.e., stuck-open defects) while black dots represent programmable crosspoints.

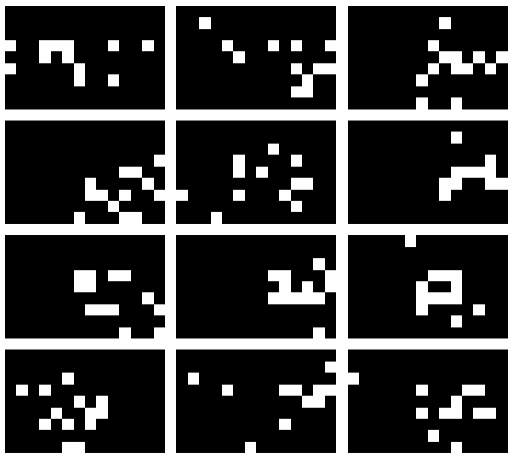

Figure 2: 2D-grid of 9x 14 PGMBs with 10% defect rate

B. Programming of PGMBs and logic rerouting

A PGMB will have m–rows and n-columns forming AND and OR planes. An NCL macro gate can be programmed on a PGMB in many different ways. Shuffling of columns in the NCL gate will not alter the logic in anyway, that is the order of columns will not change the final output from the PGMB. Here, the order of NCL gate columns is rearranged first so that the possibility of successful mapping could be improved. The idea is to arrange columns in such a fashion that ON-inputs in the gate logic maps to a programmable crosspoint of the physical column. But the same method can not be used to shuffle rows. The output row (OR plane) is connected to a pull down resistor and the AND plane will be driven by inputs. The row shuffling has to be restricted to their respective planes. Figure 3 shows TH24, TH23 and TH54w322 randomly programmed on 2D grid of PGMBs by shuffling. The gray color dots represent the crosspoints which are programmed by avoiding defective white color points. The input switching block has to be reconfigured according to newly generated layout and it is assumed to be defect free in this paper.

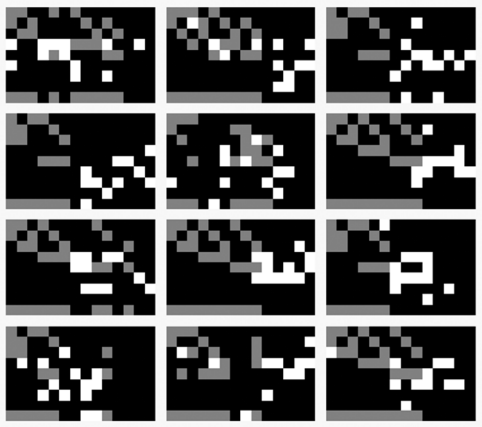

Figure 3: Programmed PGMB grid

C. Optimum dimension of a PGMB

A 10 x 20 2D-Grid architecture of PGMBs with different defect rates were constructed using the algorithm mentioned above. A set of NCL gates were chosen to represent normal distribution of ON cross points and they were randomly programmed on the grid. The dimensions were fine tuned to achieve maximum programmability for the given defect rate. For the simulation purpose the number of rows with pull down resistors is assumed to be 20% of the total number of rows. The number of rows (m) was varied from 6 to 11 and corresponding number of columns were maintained at (m+4). Many simulations were carried out and average percentage of the successful programming of gates was plotted for different defect rates. The Figure 4 shows that with 10% defect rate the grid can be completely programmed by having the dimensions 8x12. We can see that as redundancy increases it significantly increases the yield and we can easily

tolerate up to 30% defect in 10 x 14 PGMB.

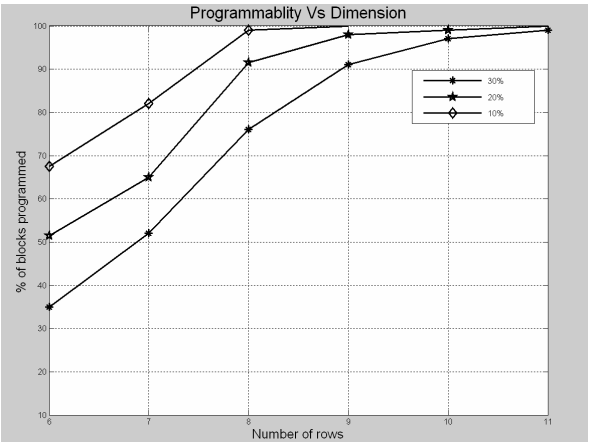

Figure 4: Effect of defect rate on programming

III. CONCLUSIONS

The clock distribution network is one of the major technical difficulties in manufacturing nanoscale systems such as the nanowire crossbar architecture, since it is hard to assemble and may incurs numerous timing failure modes. In order to resolve this issue, we recently proposed a novel clock-free architecture for the nanowire crossbar systems based on a self-timed logic encoding scheme known as Null Convention Logic (NCL). The proposed architecture has two major building blocks – programmable gate macro blocks (PGMB) and reconfigurable switch blocks. A PGMB can be programmed as any NCL gate and programmed PGMBs can be interconnected by configuring switch blocks. Both DATA wavefront and NULL wavefront are alternatively initiated and propagated through the circuit to time itself without the clock distribution network.

Even though the proposed clock-free nanowire crossbar architecture provides numerous benefits including improved manufacturability and robustness, it is still not free from defects. So, we have analyzed the relationship between the defect rate and the programmability of PGMB. The simulation results shown in this paper suggest that the dimension of PGMB can be optimized to provide inherited redundancy to cope with specific defect rate and clustering.

REFERENCES

[1] Karl M. Fant, Scott A. Brandt, "NULL Convention Logic : A Complete and Consistent Logic for Asynchronous Digital Circuit Synthesis", IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP'96) , pp 261-273, 1996.

[2] S. C. Smith, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, "Optimization of NULL Convention Self-Timed Circuits" Elsevier's Integration, The VLSI Journal, Vol. 37/3, pp. 135-165, August 2004.

[3] S. Smith, R. DeMara, J. Yuan, M. Hagedom and D. Ferguson, "Delay Insensitive gate-level pipelining", Integration, the VLSI journal, Vol. 30, pp. 103 – 131, 2000.

[4] Stapper. C.H., "Simulation of spatial fault distributions for integrated circuit yield estimations," IEEE Transaction on Computer-Aided Design, Vol. 8, No. 12, pp. 1314-1318, 1989.

.