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# Over-Distention Operation of Cascaded Multilevel Inverters

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***Abstract*** **– Established research has shown that cascaded multilevel inverters can provide more voltage vectors per number of active semiconductors compared to typical multilevel converters. This feature is significant for increasing the drive performance as well as reducing the drive complexity and losses. When two inverters are cascaded, the maximum number of effective levels (or maximal distention operation) is the product of the number of levels of the individual inverters. It is possible to operate the cascaded inverter beyond maximum distention. The over-distention operation is desirable since it effectively increases the number of voltage levels in spite of some missing switching levels. This paper studies over-distention operation based on an inverter system where two three-level inverters are cascaded, which can generate eleven equivalent converting levels instead of nine levels under maximal distention condition. An advanced modulation technique is introduced to handle both the missing line-to-ground voltage levels and the balance of dc link capacitor voltages in over-distention operation. Computer simulation and experimental validation are presented to verify the proposed methods.**

***Keywords***: **multilevel inverter, multilevel converter, capacitor balancing, Pulse Width Modulation, voltage vector, space vector.**

## I. INTRODUCTION

Modern medium-voltage dc/ac inverter design usually involves the multilevel concept, which improves power quality by inserting a certain number of small voltage steps to the ac side in between the line-to-ground voltages. Diode-clamped multilevel inverters [1], flying capacitor multilevel inverters [2] and series connected H-bridge multilevel inverters [3,4] are the three most well known multilevel inverter topologies. The cascaded multilevel inverter [5,6] as shown in Fig. 1 is constructed by splitting the ac electrical machine neutral and connecting each end of each phase coil to a multilevel inverter which could be made from the above three topologies. The main advantage of the cascaded multilevel inverter over other multi-level inverters is that it offers more voltage vectors per number of power semiconductor devices. This feature is significant since the drive performance increases with the number of voltage vectors while the drive cost, complexity, and conduction losses increase with increasing power semiconductors. Cascaded inverters also feature unevenly distributed semiconductor voltages and switching frequencies between the two inverters. High-voltage low-frequency devices like GTOs and Low-voltage high-frequency devices such as IGBTs can be used in the two cascaded inverters accordingly. By varying the level of the two cascaded inverters as well as the dc voltages, an infinite number of voltage vector diagrams can be obtained. In order to gauge the ability of cascaded multilevel inverter and make it comparable to the conventional multilevel inverters, the maximal distention case has been discussed in [5]. This paper will discuss the over-distention case, which is the operation mode beyond maximal distention. The over-distention operation is desirable since it effectively increases the entire voltage converting levels in spite of some missing levels. However, in the voltage space vector plot, those missing switching levels will result in a certain number of missing space vectors, which will tend to bring in negative influences to inverter performance. Although the duty-cycle modulation method introduced in [7] works perfect for the maximal distention case, it dose not consider the missing phase levels thus needs to be amended. This paper will present an advanced modulation technique for the over-distention operation mode based on a cascaded-3/3 multilevel inverter, which commonly provides nine equivalent line-to-ground converting levels under maximal distention [5,7]. The proposed technique can configure the inverter to work as an equivalent eleven-level inverter. When the modulation index is higher than 91.7% of the physical modulation limitations, the control can bypass the missing vectors with no redundant states. This will slightly degrade the performance compared to conventional eleven-level inverter. When the modulation index is lower than 91.7%, the control can configure the inverter to utilize the redundant space vector of the missing

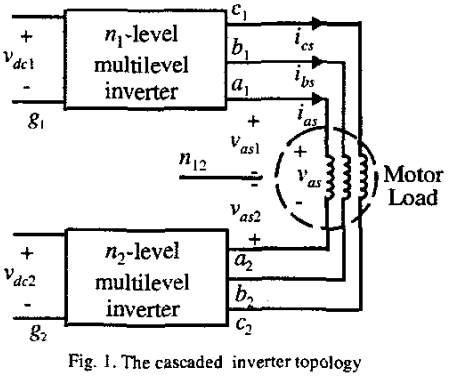


Fig. 1. The cascaded inverter topology

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switching levels. Although the line-to-ground voltages still contain missing levels, the phase voltage obtain a performance as good as the conventional eleven-level inverter. In addition, the proposed modulation technique can also be used to balance the capacitor voltages. For clarity, this paper will first review the general topology of the cascaded multilevel inverters in section II, followed by the discussion of the space vector patterns. Then in section III, the advanced modulation technique for over-distention mode is depicted. Section IV will take a future step on discussing the capacitor balancing issue under the over-distention operation mode. Simulation and experimental results are presented in the consecutive sections, which verify the proposed method.

## II. The Cascaded Multilevel Inverter

### A. General Topology

In Fig. 1, $n_{12}$ indicates the fictitious system neutral common to inverter 1 and 2. As mentioned before, all of the three most common multilevel inverter topologies can be used to construct the cascaded multilevel inverter. In this paper, however, the diode-clamped multilevel inverter topology is adopted. Figure 2 shows a cascade-3/3 multilevel inverter constructed by two diode-clamped inverters. The phase-to-ground voltage of an $n$-level multilevel inverter can be expressed as

$$v_{xg} = \frac{s_x}{(n-1)} v_{dc}, \quad s_x = 0,1,...(n-1) \tag{1}$$

where $x$ represents the phase which can be $a$, $b$ or $c$, and $s_x$ represents the phase switching states selected by the transistor gating signals. The line-to-neutral voltages are given by [8]

$$v_{as} = \tfrac{2}{3} v_{ag} - \tfrac{1}{3} v_{bg} - \tfrac{1}{3} v_{cg} \tag{2}$$

$$v_{bs} = \tfrac{2}{3} v_{bg} - \tfrac{1}{3} v_{ag} - \tfrac{1}{3} v_{cg} \tag{3}$$

$$v_{cs} = \tfrac{2}{3} v_{cg} - \tfrac{1}{3} v_{ag} - \tfrac{1}{3} v_{bg} . \tag{4}$$

When two inverters are cascaded together by splitting the machine neutral as shown in Fig. 1, the machine phase voltage can then be represented by following the Kirchoff's voltage law.

$$v_{as} = v_{as1} - v_{as2} \tag{5}$$

$$v_{bs} = v_{bs1} - v_{bs2} \tag{6}$$

$$v_{cs} = v_{cs1} - v_{cs2} \tag{7}$$

In terms of the phase-to-ground voltages of the two cascaded inverters, the machine voltages are given by [4]

$$v_{as} = \tfrac{2}{3}(v_{a1g} - v_{a2g}) - \tfrac{1}{3}(v_{b1g} - v_{b2g}) - \tfrac{1}{3}(v_{c1g} - v_{c2g}) \tag{8}$$

$$v_{bs} = \tfrac{2}{3}(v_{b1g} - v_{b2g}) - \tfrac{1}{3}(v_{a1g} - v_{a2g}) - \tfrac{1}{3}(v_{c1g} - v_{c2g}) \tag{9}$$

$$v_{cs} = \tfrac{2}{3}(v_{c1g} - v_{c2g}) - \tfrac{1}{3}(v_{a1g} - v_{a2g}) - \tfrac{1}{3}(v_{b1g} - v_{b2g}) \tag{10}$$

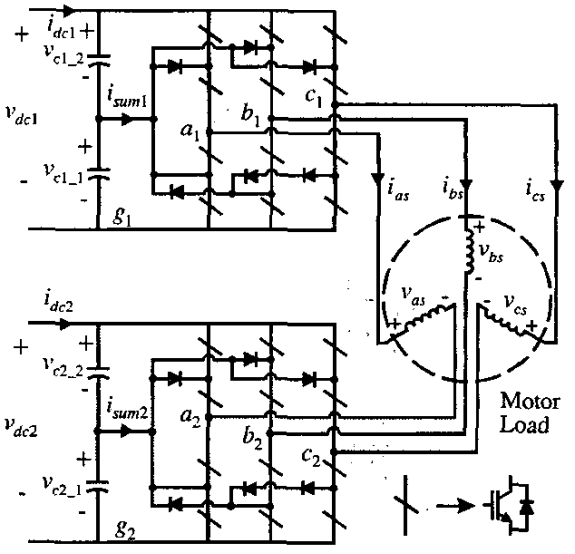



Fig. 2. The cascade-3/3 diode-clamped multilevel inverter topology

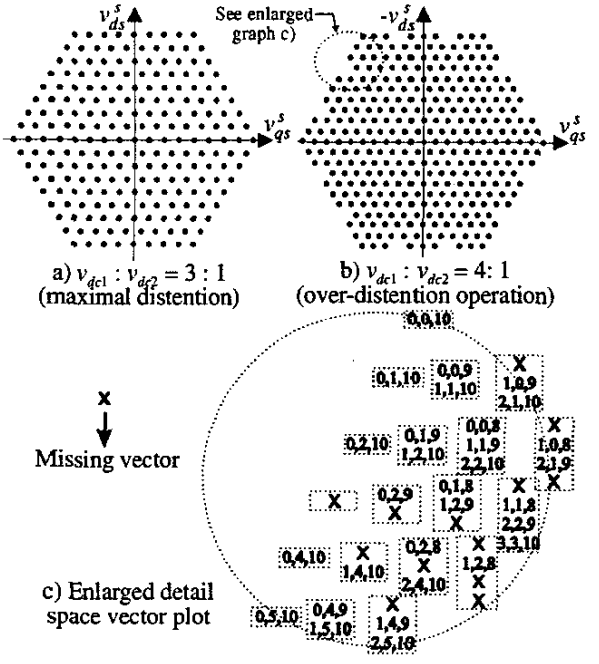



Fig. 3. Voltage vector plot for the cascade-3/3 inverter

In order to make the cascaded inverters comparable to the conventional multilevel inverters, it is helpful to define the fictitious line-to-ground voltages as follows:

$$v_{agf} = v_{a1g} - v_{a2g} \tag{11}$$

$$v_{bgf} = v_{b1g} - v_{b2g} \tag{12}$$

$$v_{cgf} = v_{b1g} - v_{b2g} \tag{13}$$

*B. Voltage Vector Diagram*

The stator voltage vectors achievable from the switching states of the cascaded multilevel inverters can be plotted by transforming the *a*- *b*- and *c*-phase stator voltages to the *q*- and *d*-axis stationary reference frame. The transformation to the arbitrary reference frame is given by [8]

$$v_{qs}^{s} = \frac{2}{3}\left(v_{as}\cos(\theta) + v_{bs}\cos\left(\theta - \tfrac{2\pi}{3}\right) + v_{cs}\cos\left(\theta + \tfrac{2\pi}{3}\right)\right) \quad (14)$$

$$v_{ds}^{s} = \frac{2}{3}\left(v_{as}\sin(\theta) + v_{bs}\sin\left(\theta - \tfrac{2\pi}{3}\right) + v_{cs}\sin\left(\theta + \tfrac{2\pi}{3}\right)\right) \quad (15)$$

In the stationary reference frame, $\theta$ is set to zero. By varying the level of the two cascaded inverters as well as the dc voltage, an infinite number of voltage vector diagrams can be obtained. In order to gauge the ability of cascade-$n_1/n_2$ multilevel inverter as shown in Fig. 1, and make it comparable to the conventional *n*-level multilevel inverter with $v_{dc}$ as the dc input voltage, it is necessary to define the maximal distention [5] operation of the cascade-$n_1/n_2$ inverter. The cascade-$n_1/n_2$ inverter is maximally distended to be equivalent to a *n*-level conventional inverter when

$$v_{dc} = v_{dc1} + v_{dc2} \quad (16)$$

$$\frac{v_{dc2}}{v_{dc1}} = \frac{n_2 - 1}{n_1 \cdot n_2 - n_2}. \quad (17)$$

The resulting number of voltage levels is

$$n = n_1 \cdot n_2. \quad (18)$$

Consider the cascade-3/3 inverter shown in Fig. 2. If the dc voltage ratio is set to $v_{dc2}$:$v_{dc1}$ = 1:3, it can provide nine effective line-to-ground voltage levels and is maximally distended as an equivalent nine-level conventional inverter. Figure 3a shows the space vector plot of the cascade-3/3 inverter under maximal distention. Table I lists the equivalent switching states. Here, $s_x$ is the equivalent switching state of the cascaded inverter, $s_{x1}$ is the switching state of the top inverter, and $s_{x2}$ is the switching state of the bottom inverter. This cascaded-3/3 inverter is of particular interest since it can be constructed out of conventional three-level inverters, which have been studied thoroughly in the literature and are commercially available from a number of drives manufactures. More important, inverter operation beyond maximal distention is possible for any cascaded inverter where $n_1$ and $n_2$ both are greater than or equal to 3. This operation is desirable since it effectively increases the number of levels by $n_1$–1 compared to the maximal distention operation. The dc voltage ratio for a cascaded inverter in over-dissension operation is represented by [4]

$$\frac{v_{dc2}}{v_{dc1}} = \frac{n_2 - 1}{n_1 \cdot n_2 + n_1 - n_2 - 1}. \quad (19)$$

Particularly, a cascaded-3/3 inverter may result in a pseudo eleven-level inverter by setting the dc voltage ratio to $v_{dc2}$:$v_{dc1}$ = 1:4. Figure 3b shows the voltage vector plot of the over-distended cascade-3/3 inverter. Table II lists the equivalent switching states for the over-distended cascade-3/3 inverter. From Fig. 3b, it can be seen that the cascaded-3/3 inverter has an equivalent eleven-level space vector plot except for some missing vectors. As it turns out, there are missing switching state combinations for inner vectors as well, which are not seen in Fig. 3b. Since redundant state combinations produce the same vector, these missing vectors can be classified into non-redundant missing vectors (NRMV) and redundant missing vectors (RMV). To be clear, it is helpful to define $s_{max}$, $s_{min}$ and *rd* (redundant degree) as

$$s_{\max} = \mathrm{MAX}(s_a, s_b, s_c) \quad (20)$$

$$s_{\min} = \mathrm{MIN}(s_a, s_b, s_c) \quad (21)$$

$$rd = nl - (s_{\max} - s_{\min}) \quad (22)$$

where the MAX function returns the maximum switching state among the three-phase joint switching states $s_a$ $s_b$ $s_c$ and MIN function returns the minimum. *nl* represents the number of the equivalent switching levels or fictitious line-to-ground levels. For NRMVs, the *rd* is always equal to 1 and one of the switching state among $s_a$ $s_b$ $s_c$ includes the missing level 3 or 7. For RMVs, *rd* is greater than 1 and some switching states among $s_a$ $s_b$ $s_c$ are 3 or 7. The twelve NRMVs are located around the outer loop of Fig. 3b For example, there should be a vector determined by the joint switching states (0,3,10) in the space vector plot of the conventional 11-level inverter. However, due to the missing level 3 caused by the over-distention operation, this vector is missing. Since the redundant degree of NRMVs is 1, there is no remedy for these missing vectors, and this leads to the empty vector spots in the outer loop as shown in Fig. 3b. For RMVs, it is easy to see from Fig 3c that there are always some redundancies available. For example there should be a vector determined by the joint switching states (0,3,9) in the space vector plot of the conventional eleven-level inverter. However, due to the missing switching level 3 caused by the over-distention operation, (0,3,9) is missing. Since the *rd* of this joint switching state is 2, there is a group of joint redundant switching state (1,4,10) available to generate the same space vector, and this state can be regarded as the remedy for the missing vector when performing the space vector modulation. The over-distention operation of the cascade-3/3 inverter generates two more fictitious line-to-ground converting levels compared to the nine converting levels under the maximal distention operation. However, from Table II and Fig 3b, 3c, it can be seen that the two missing switching levels $s_x$ = 3 and $s_x$ =7 show negative influences to the space vector plot. First, twelve outer voltage vectors are missing and the cascaded inverter cannot work equivalently as a conventional eleven-level inverter when the commanded voltage is higher than 91.7% of the maximum voltage and the performance will be degraded slightly in this scenario. However, the power quality will still be better than that of maximal distention (nine-level) operation. Second, the missing switching levels

decrease the number of joint switching state redundancies thus bringing in difficulties on balancing the dc capacitor voltages. To minimize the negative influences, special care needs to be taken when performing the modulation techniques.

## III. Modulation Techniques For Over-Distention Mode

### A. General Description

The final purpose of the modulation technique is to control the gating signals so that power semiconductor may switch on/off as desired. The gating signals are directly related to the switching states (or levels) $s_x$. As shown in (1), these switching states may be computed by normalizing the commanded line-to-ground $v_{xg}$ to $v_{dc}$. PWM switching is typically accomplished by defining duty-cycles based on the normalized commanded line-to-ground voltages which may be expressed as

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \tfrac{m}{6}\cos(3\theta_c)\right] \quad (23)$$

$$d_b = \frac{1}{2}\left[1 + m\cos(\theta_c - \tfrac{2\pi}{3}) - \tfrac{m}{6}\cos(3\theta_c)\right] \quad (24)$$

$$d_c = \frac{1}{2}\left[1 + m\cos(\theta_c + \tfrac{2\pi}{3}) - \tfrac{m}{6}\cos(3\theta_c)\right] \quad (25)$$

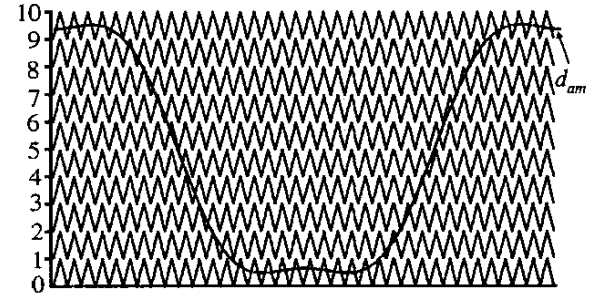
TABLE I
Equivalent Switching States for the Maximally Distended Cascaded-3/3 Inverter ($v_{dc1} = 6E$, $v_{dc2} = 2E$)

| $s_x$ | $s_{x1}$ | $s_{x2}$ | $v_{fxg}$ | $v_{x1g}$ | $v_{x2g}$ |
|---|---|---|---|---|---|
| 0 | 0 | 2 | -2E | 0 | 2E |
| 1 | 0 | 1 | -E | 0 | E |
| 2 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 2 | E | 3E | 2E |
| 4 | 1 | 1 | 2E | 3E | E |
| 5 | 1 | 0 | 3E | 3E | 0 |
| 6 | 2 | 2 | 4E | 6E | 2E |
| 7 | 2 | 1 | 5E | 6E | E |
| 8 | 2 | 0 | 6E | 6E | 0 |

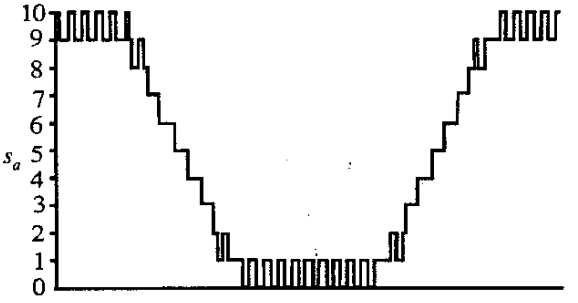
TABLE II
Equivalent Switching States for the Over-Distention Operation of Cascaded-3/3 Inverter
($v_{dc1} = 8E$, $v_{dc2} = 2E$)

| $s_x$ | $s_{x1}$ | $s_{x2}$ | $v_{fxg}$ | $v_{x1g}$ | $v_{x2g}$ |
|---|---|---|---|---|---|
| 0 | 0 | 2 | -2E | 0 | 2E |
| 1 | 0 | 1 | -E | 0 | E |
| 2 | 0 | 0 | 0 | 0 | 0 |
| Missing | | | | | |
| 4 | 1 | 2 | 2E | 3E | 2E |
| 5 | 1 | 1 | 3E | 3E | E |
| 6 | 1 | 0 | 4E | 3E | 0 |
| Missing | | | | | |
| 8 | 2 | 2 | 6E | 6E | 2E |
| 9 | 2 | 1 | 7E | 6E | E |
| 10 | 2 | 0 | 8E | 6E | 0 |

The inverter switching states $s_x$ may be determined by

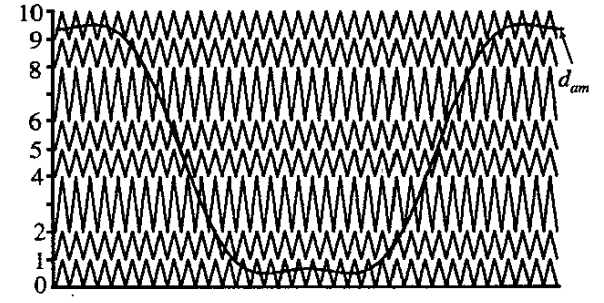



a) modified duty cycle and triangle waveforms

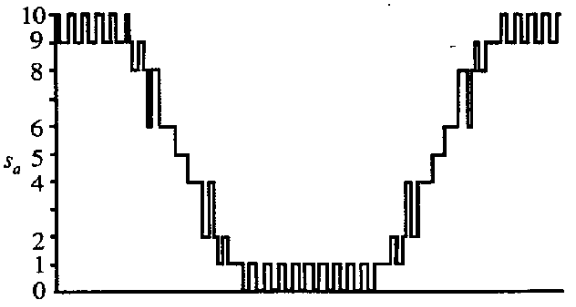



b) switching state

Fig. 4. 11-level sine-triangle modulation technique for the over-distention operation of cascaded-3/3 inverter(m<1.05)




a) modified duty cycle and triangle waveforms




b) switching state

Fig. 5. 11-level sine-triangle modulation technique for the over-distention operation of cascaded-3/3 inverter(m>=1.05)

comparing the duty-cycles to multiple triangle waveforms [9,10]. Alternatively, some drive systems utilize a digital signal processor (DSP) implementation in which definition of the triangle waveforms is not necessary [7]. These methods can also be applied to the over-distended cascade-3/3 inverter. However, when cascaded inverters are working in over-distention mode, some missing switching levels may occur as being discussed before. Special care needs to be taken due to the specialty. For simplicity, the multilevel sine-triangular modulation technique will be used in the following discussion.

### B. *Modulation When m<1.05*

When the modulation index is lower than 91.7% ($m < 1.05$) of the physical modulation limitation, the over-distended cascade-3/3 inverter is equivalent to an eleven-level inverter. Even though the fictitious line-to-ground level 3 and 7 do not exist, from space vector point of view, those missing levels result in RMVs as shown in Fig 3b and 3c. Therefore, the eleven-level sine-triangle modulation technique can be applied directly except that a redundant states selection (RSS) procedure for RMVs needs to be followed. The discussion for the RSS of RMVs can be found in section D. Figure 4 demonstrates the eleven-level sine-triangular modulation technique.

### C. *Modulation when m>1.05*

When the modulation index is higher than 91.7% (m > 1.05) of the physical modulation limitations, NRMVs will be encountered. In this scenario, a suitable modulation technique needs to be able to bypass the NRMVs by jumping to joint switching states close to the missing ones. However, the modulation techniques adopted in section B aim in providing evenly distributed switching levels and thus cannot handle the jumping requirements from NRMVs. To solve this problem, a fictitious eleven-level sine-triangle modulation technique is introduced as shown in Fig 5. It can be noticed that the switching level ranges from 0 to 10, but level 3 and 7 are avoided by using triangle carriers with double magnitude.

### D. *Space Vector Control Patterns*

It has been discussed in the above sections that two groups of missing vectors bring in negative influences to the vector plot as shown in Fig. 3.b and 3.c. The purpose of studying the voltage space vector patterns of the cascaded-3/3 inverter under over-distention operation is to minimize the negative influence of the missing switching levels. Transferring the generated $s_a$ $s_b$ $s_c$ into stationary reference frame may equivalently evaluate the space vectors patterns.

$$s_q = \frac{2}{3}\left[s_a\cos(\theta) + s_b\cos\left(\theta - \tfrac{2\pi}{3}\right) + s_c\cos\left(\theta + \tfrac{2\pi}{3}\right)\right] \quad (26)$$

$$s_d = \frac{2}{3}\left[s_a\sin(\theta) + s_b\sin\left(\theta - \tfrac{2\pi}{3}\right) + s_c\sin\left(\theta + \tfrac{2\pi}{3}\right)\right] \quad (27)$$

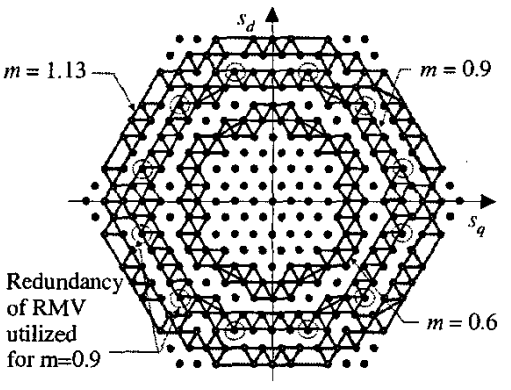



Fig. 6. desired space vector patterns for the cascade-3/3 converter in over-distention operation

The space vector modulation techniques [6,7] tend to utilize the three closest space vectors to provide the best performance. Section *B* and *C* have discussed the methods of generating the switching states by avoiding the missing levels. Reference [7] shows that when the modulation index is higher than 91.7% of its physical limits, the space vectors will be operated around the outer loop, nine actual switching levels ($s_x$ ranges from 0~10 but not equals to 3 and 7) will be generated as described in Section *C* and the joint switching states ($s_a$ $s_b$ $s_c$) will be used directly to generate space vector control pattern. When the modulation index is less than 1.05, all eleven switching levels will all be generate first as described in Section *B*. and the redundant switching state to RMVs are expected to be utilized to obtain a vector pattern as good as the conventional 11-level inverter. Therefore, a redundant switching state selector (RSS) needs to be added so as to utilize those redundancies to RMVs. The RSS evaluates the joint switching states ($s_a$ $s_b$ $s_c$) and finds a redundant joint switching state without 3 and 7 involved. For instance, if a fictitious joint switching state (1,3,9) is generated from the modulator, the RMV redundancy selector will then use its redundant state (0,2,8) or (2,4,10) to provide the same space vector as shown in Fig. 3.c. Figure 6 shows the desired vector patterns acquired by plugging the generated switching states into (26-27) with $\theta = 0$. It can be seen that the space vector pattern can always bypass the NRMVs and utilize the redundancies of RMVS.

### E. *The Method of Finding Redundant States*

In general, a redundant state may be found for a given switching state by incrementing or decrementing the states for all three phases since this results in changing the zero-sequence line-to-ground voltage, which does not affect the load voltages. The boundary states are the joint states with the highest switching level or the lowest switching level involved in some certain phases. For instance, if the converting levels range from 0 to 10, the redundancies of the joint switching states (2,6,7) can be found by continuously adding 1 to or subtracting 1 from each states so as to find

(0,4,5), (1,5,6), (3,7,8), (4,8,9), and (5,9,10), all of which refer to the same space vector. The boundary states are (0,4,5) and (5,9,10) in this example.

## IV. Capacitor Voltage Balancing

It is often necessary to utilize the redundant switching states for balancing the voltages on input capacitor banks [1]. As mentioned before, the over-distention operation of the cascaded inverter yields $nl$ equivalent levels with some jumping transmissions, which eventually decreases the number of redundant states compared to the conventional $n$-level inverter. Therefore, the capacitor balancing method for over-distention operation needs to be studied and it is instructive to use the cascaded-3/3 inverter as an example. For each three-level inverter, the dc capacitor bus might be charged or discharged depending on capacitor voltages and the direction of the summarized phase currents wherein the switching state $s_x$=1 will tend to bring current influence into the capacitor junction. Using the top inverter as example, when $v_{c1\text{-}1}$ is greater than $v_{c1\text{-}2}$, the desired case is to choose a joint switching state ($s_{a1}$ $s_{b1}$ $s_{c1}$) which may yield a positive $i_{sum1}$ represented as

$$i_{sum1} = \delta(s_a - 1)i_{as} + \delta(s_b - 1)i_{bs} + \delta(s_c - 1)i_{cs} \tag{28}$$

where $\delta(x)$ is the Kronecker delta function which has a value of 1 when the argument is zero and a value of 0 for other augments. Similarly, when $v_{c1\text{-}1}$ is less than $v_{c1\text{-}2}$, the desired case is to choose a joint switching state ($s_{a1}$ $s_{b1}$ $s_{c1}$) that may yield a negative $i_{sum1}$. When no redundancy is available to match the desired case, one may try to find a joint redundant state that has less current contribution to $i_{sum1}$. This can alternatively be explained as to find joint switching states which have the least "1" switching state involved. The idea here is that two inverters are cascaded together, so the capacitor-balancing situation needs to be evaluated simultaneously. As can be seen from Table II, the switching states of the cascaded-3/3 inverter $s_x$ need to be first mapped into the switching states of the two 3-level inverter $s_{x1}$ and $s_{x2}$. In practical implementation, sensors measure the phase currents and capacitor voltages. An analog-to-digital conversion is performed to determine the current direction flags and capacitor imbalance [1]. Let $F_{ix}$ denote the current direction flag, $F_{v1}$ and $F_{v2}$ denote the capacitor imbalance of the two cascaded inverters defined by,

$$F_{ix} = \begin{cases} 0 & i_{xs} < 0 \\ 1 & i_{xs} \geq 0 \end{cases}. \tag{29}$$

$$F_{v1} = \begin{cases} 0 & v_{c1\_1} < v_{c1\_2} \\ 1 & v_{c1\_1} \geq v_{c1\_2} \end{cases}. \tag{30}$$

$$F_{v2} = \begin{cases} 0 & v_{c2\_1} < v_{c2\_2} \\ 1 & v_{c2\_1} \geq v_{c2\_2} \end{cases}. \tag{31}$$

Let $DirI_{x1}$ and $DirI_{x2}$ denote the current contribution of phase $x$ to $i_{sum1}$ and $i_{sum2}$ respectively,

$$DirI_{x1} = \begin{cases} (2F_{ix} - 1) & s_{x1} = 1 \\ 0 & s_{x1} = 0,2 \end{cases} \tag{32}$$

$$DirI_{x2} = \begin{cases} (1 - 2F_{ix}) & s_{x2} = 1 \\ 0 & s_{x2} = 0,2 \end{cases}. \tag{33}$$

The summarized current direction contributions are then defined by

$$DirI_{sum1} = DirI_{a1} + DirI_{b1} + DirI_{c1} \tag{34}$$

$$DirI_{sum2} = DirI_{a2} + DirI_{b2} + DirI_{c2}. \tag{35}$$

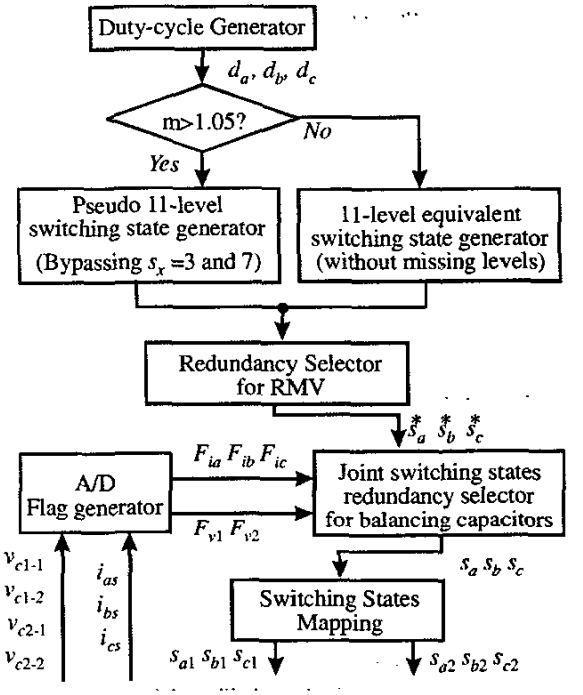



Fig. 7. Modulation block diagram

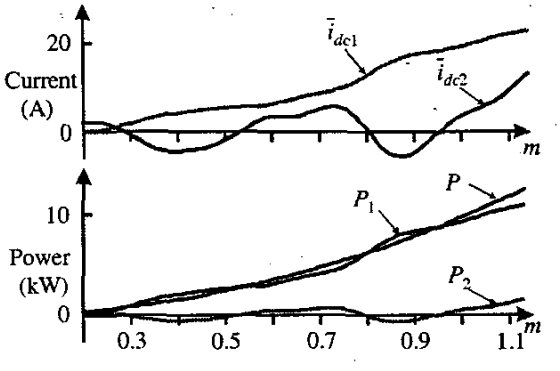



Fig. 8. Average steady-state dc current and power versus modulation index (over-distention operation)

When $Dirl_{sum1}$ equals 2 means that two phases have positive currents and one phase has no contribution to $i_{sum1}$ and this can be the second desired case for $F_{v1}$ =1. Similar analysis shows that the joint switching states which leads to $Dirl_{sum1}$ = -3 is the last choice for $F_{v1}$ =1 case but the first choice for the $F_{v1}$ =0 case. A term goodness degree ($gd$) can then be defined to evaluate the capacitor voltage-balancing situation.

$$gd_1 = (2 \cdot F_{v1} - 1) \cdot Dirl_{sum1} . \quad (36)$$

$$gd_2 = (2 \cdot F_{v2} - 1) \cdot Dirl_{sum2} . \quad (37)$$

When jointly considering the two cascaded inverter,

$$gd = gd_1 + gd_2 . \quad (38)$$

For capacitor balancing purposes, the final selection of the joint redundant switching states ends up with the determination of the joint switching state that has the highest goodness degree.

## V. Simulation and Experimental Validation

A computer simulation and a laboratory prototype have been developed for verifying the cascade-3/3 eleven-level inverter, where $v_{dc1}$ = 625V, $v_{dc2}$ = 156V, and the frequency is 60Hz. Load is an $R$-$L$ load with $R$ = 15.0Ω and $L$ = 24.2mH per-phase. Figure 7 shows the control block diagram for generating the desired switching state of the over-distended cascade-3/3 inverter. It addresses both the missing space

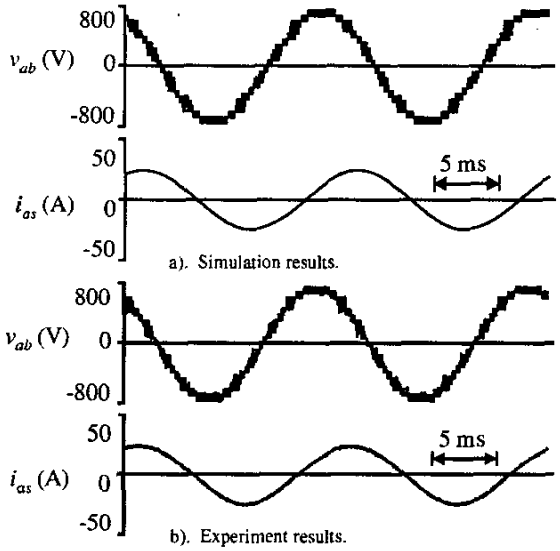



Fig. 9. Eleven-level cascade-3/3 inverter waveform ($m$=1.13)

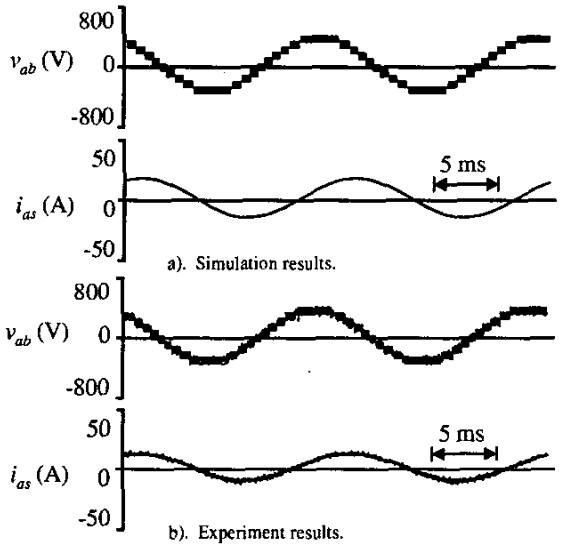



Fig. 10. Eleven-level cascade-3/3 inverter waveform ($m$=0.55)

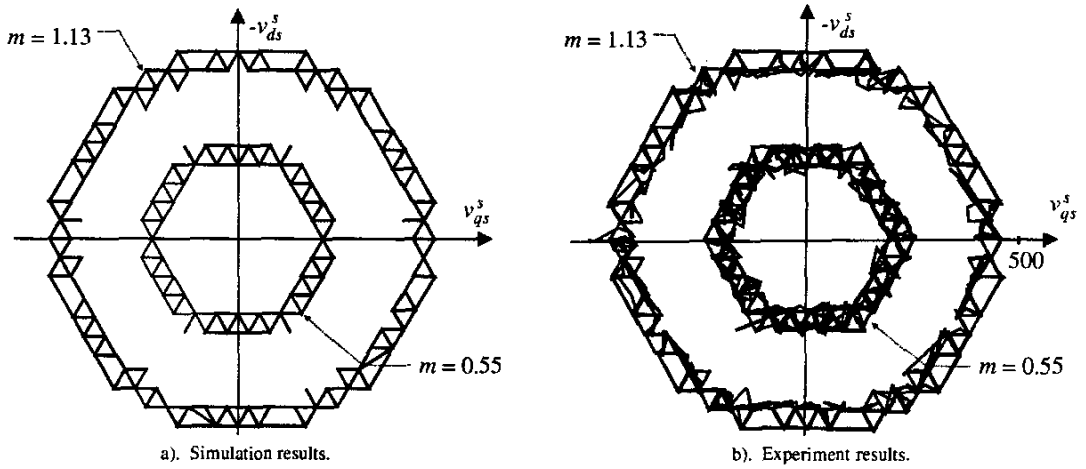



Fig. 11. Eleven-level cascade-3/3 inverter measured space vectors

vector problem and the capacitor-balancing problem.

One thing that needs to be pointed out is that the value of modulation index influences the dc current provided by the two cascaded inverters. Figure 8 shows the dc current and power versus modulation index waveforms, where $\bar{i}_{dc1}$ and $\bar{i}_{dc2}$ denote the average steady state current of the upper and lower inverter respectively. The powers are defined as

$$P_1 = \bar{i}_{dc1} \cdot (v_{c1\_1} + v_{c1\_2}) \quad (39)$$

$$P_2 = \bar{i}_{dc2} \cdot (v_{c2\_1} + v_{c2\_2}) \quad (40)$$

$$P = P_1 + P_2 \quad (41)$$

From Fig. 8 it can be seen that the total power is increased with the increasing of the modulation index for a fixed load and fixed frequency. However, the lower converter may either provide or absorb power. This will not be a problem if the dc source allows power absorption. However, if the dc source does not allow power absorption, one may need to carefully choose the modulation index to avoid negative average current. When $m$ = 1.13 and 0.55, from Fig. 8 it can be seen that both of the upper and lower dc sources provide positive power to the two cascaded converters. Figures 9 and 10 show the related simulation and experimental performance. When the modulation index is 1.13, the phase voltage has some jumping levels, however it is not shown when $m$ is 0.55. This is the expected result contributed by the redundancy selection for RMVs. Figure 13 shows the simulation and experimental space vector plots. As can be seen, desired space vector patterns are achieved, which verifies the proposed modulation technique for the over-distention operation mode of the cascade-3/3 inverter.

## VIII. Conclusion

This paper has studied the over-distention operation of cascaded multilevel inverters. Over-distention operation of cascaded inverters is desired since it effectively increases the entire voltage converting levels in spite of some missing levels. For the over-distention operation of a cascade-3/3 inverter, a pseudo 11-level inverter can be realized. An advanced modulation technique for over-distention operation has been introduced based on the cascade-3/3 inverter. Three of the most important features about this modulation technique are: 1). When the modulation index is lower than 91.7%, it can generate an equivalent space vector pattern as the conventional 11-level inverter. 2) When the modulation index is higher than 91.7% of the upper physical limit, it can generate a slightly degraded 11-level space vector pattern, which still has exceptional power quality. 3). Joint redundant switching state selection rules based on the goodness degree principle introduced herein can successfully solve the capacitor voltage balancing problem. Computer simulation and lab experiments verify the proposed methods.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