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Modeling of Substrate Noise Effects in Dynamic CMOS Circuits

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***Abstract* — The decrease in the feature size has led to the integration of both digital and analog circuits on the same silicon die which has led to many crosstalk issues. The crosstalk due to the substrate interactions also plagiarizes complete digital systems. This paper lays emphasis on this fact and because of the vulnerability of Dynamic CMOS circuits to noise; a brief study of the effects of substrate variations on the performance of the Dynamic CMOS circuits is carried out in this paper. The effects of substrate noise at very high frequencies (above 10 GHz) are also depicted in this paper. In order to accurately estimate the effects of substrate noise a substrate model is proposed and verified for functionality in the last section of this paper.**

***Keywords*— Monte Carlo simulation, Substrate Noise, Substrate Modeling, Dynamic CMOS, Capacitive coupling**

I. Introduction

The decrease in the feature size of the silicon die has curved a way to the integration of the digital and the analog circuits on the same die. Digital devices due their switching activity while making a state transition from one state to another injects noise into the substrate which gets capacitive coupled with the sensitive analog circuits causing a deviation in the output and hence degrades the overall performance of the system. Also with the increase in the need for high speed VLSI circuits, digital Dynamic CMOS circuits are preferred over their static counterparts. But due to the vulnerability of dynamic CMOS circuits to noise, noise is plagiarizing the complete digital systems as well. Substrate Noise contributes to the degradation of performance of dynamic CMOS circuits and hence the entire digital systems as well. Due to the dependence of noise margin of Dynamic Logic circuits on the threshold voltage of the NMOS transistors this family of circuits is more vulnerable to noise [1]. This fact contributes to the dependence of noise margin of Domino Logic circuits on threshold voltage of pull down logic and hence there is a limitation in employing the Domino CMOS circuits. Moreover, with the decrease in feature size, many circuits are being embedded on the same die, which causes the noise to propagate through the common substrate. The substrate coupling problem, though significant in mixed signal circuits, also plagiarizes entirely digital circuits [1-3]. With the Domino logic circuits being more vulnerable to noise, the effects of substrate noise are much more prominent. In order to accurately analyze the functioning of the digital circuits embedded on the same die, it is very important to perform accurate simulations of substrate voltage [4]. Thus, there is a need to perform substrate noise analysis in Domino CMOS circuits to estimate accurate circuit performance. This paper therefore emphasizes analysis of substrate noise effects in the Domino CMOS logic family.

Also, with the increase in operating frequency, the substrate effects become much more prominent. These effects need to be analyzed before manufacturing the product to ensure better performance. Section 4 of this paper focuses on the analysis of the substrate noise effects at high frequency range (the frequencies above 10GHz). The second part of the paper describes the application of the substrate model in the Domino CMOS circuit to accurately analyze the effects of substrate coupling.

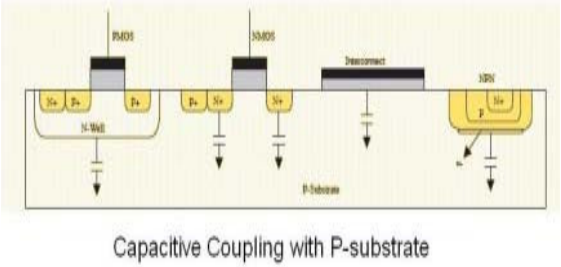

Fig. 1: Noise coupling through substrate

Fig.1 depicts the mechanism of substrate coupling of unwanted signals with other circuit nodes that are generated due to transistor's switching activity coupled via capacitive coupling. The Fig. here considers a system which has both the NMOS and the PMOS to correctly depict the coupling caused by the switching activity of each on one other.

II. Significance & Sources of Substrate Noise

When injected into the substrate, the transient currents become coupled to other circuit nodes via substrate. These currents cause a drift in the substrate potential, which leads to the change in the threshold voltage of the MOSFETs. Since the noise margin of the DOMINO logic depends on the threshold voltage of the NMOS logic, a change in the threshold voltage causes a direct change in the noise margin of the circuit, adversely affecting the performance of the circuit and the system as a whole. The dependence of the threshold voltage on the substrate potential can be seen from the body bias equation as shown in the following equation (1). [5]

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$$V_T = V_{T0} + \gamma(\sqrt{(2|\phi_f| + V_{sb})} - \sqrt{2|\phi_f|}) \quad (1)$$

where,

V_{sb} corresponds to the source to body substrate bias.

$2\phi_f$ is the surface potential.

V_{TO} is the threshold voltage for zero substrate bias and

γ is the body effect parameter.

The various sources that contribute to the generation of substrate noise are as follows:

1. The di/dt noise, the resistive voltage drops at the clock and the power grids which occur due to the combined effect of the inductance at the power supply and the on chip capacitance between the power and the ground rails result in the ground bounce [6-7].

2. Impact ionization, the phenomenon which occurs due to the high electric fields in MOSFETs, results in the transfer of electron's energy to other stationary carriers causing a charge to propagate in the substrate [8].

3. The capacitive coupling of the MOSFET's switching nodes with the substrate causes the unwanted signals to be injected into the substrate. This coupling is caused due to the junction capacitance, which takes up the value as depicted in equation (2).

$$C_{js} = \sqrt{\frac{q\varepsilon}{2(\phi_0 + V_{CS})}\left(\frac{N_C * N_S}{N_C + N_S}\right)} \quad (2)$$

Where, N_C and N_S are the collector and the substrate doping levels, ϕ_0 is the built in junction potential, V_{CS} the collector-to-substrate bias voltage, q the electron charge and ε is the substrate dielectric permittivity. Since the Noise margin of the circuit depends upon the threshold voltage of the NMOS logic [9], a change in the substrate potential is capacitive coupled with the threshold voltage of NMOS via the junction capacitance, thus affecting the Noise Margin of the Domino Logic under consideration and hence the overall performance of the system.

III. Previous Work

Many techniques have been proposed to simulate, model and estimate the substrate noise. The work described in [10] relates to a numerical technique used to model the substrate. A circuit simulator is then defined which takes into account the admittance and the impedance matrix to determine the effects of coupling through the substrate. On the other hand the work described in [11] emphasizes on the Boundary element method for extraction of substrate to generate the circuit model. It uses the Greens function for the numerical analysis. While in some of the techniques as presented in [12] and [13], the authors focus on the modeling of the substrate parasitic. Here substrate optimization techniques based on the semi-analytical techniques is used in physical optimization.

The work as proposed in the literature mentioned above concerns with the representation of the substrate noise and modeling of substrate in the circuits that consist of both the analog and the digital parts and emphasizing on the effect of substrate noise on the analog sections. But with the use of Dynamic Logic, the effect of substrate noise is prominent in complete digital systems as well. Moreover with the increase in the operating frequency of the devices, factors that dominate the cause the substrate noise also involves the frequency dependent parameters which cannot be ignored. It then becomes important to include these factors in the statistical model which is being covered in this paper.

IV. Simulation and Results

A. Monte Carlo Analysis

The Monte Carlo method is a technique of statistical sampling which is employed to approximate solutions to quantitative problems. It helps statistical information to be derived from estimates of the random variability of circuit parameters. Multiple simulation runs are carried out with different sets of parameters. The Monte Carlo method involves a series of consecutive design simulation runs where, for each run, selected circuit parameters vary according to a statistical distribution, such as "uniform", "Gaussian", or "user defined" for each run. Now that the effects of the noise on the system will not be linear, but random, random patterns generated by the Monte Carlo Simulations help to analyze the behavior of circuit designed using the domino logic CMOS based on the various parameters. Since substrate noise is statistical in nature, Monte Carlo analysis is performed to analyze the effect of various parameters on the substrate noise, which affects the overall performance of the circuit.

B. Domino CMOS Circuit Simulations

Much of the work presented in [14] and [15] emphasizes the effects of coupling via interconnects in dynamic CMOS families, but the effects of substrate noise are not often considered. This paper places much emphasis on the parameters contributing to the substrate noise and affecting the output in terms of the system delays and noise margins. The logic circuits of the dynamic circuit family which was considered to analyze the effects of substrate noise were the basic dynamic gates and the circuits described by the Domino CMOS circuit topology. The results and analysis shown here are those of a Domino AND gate.

C. Results

Many techniques have been proposed in order to analyze the effects of substrate noise. For example, voltage comparators can be used as noise sensors as depicted in [16], while a continuous time direct measurement technique which employs the use of analog differential amplifier has been described in [17]. This paper focuses on modulating various parameters that contribute to the generation of the substrate noise. Like the threshold voltage of NMOS, which directly affects the noise immunity of the dynamic logic circuits, the junction capacitance as has been described in equation (2) is also

considered as a parameter which contributes to the substrate coupling. The MOSFET model in this study is the Berkley Spice BSIM3v3 Model and Mayer capacitance model is used. The substrate junction capacitances that are taken into account are those that vary along the bottom and the periphery. Fig. 2 shows the output of the Domino AND gate.

Case1. Varying the junction capacitance

The waveforms shown in Fig. 3 depict the Monte Carlo Simulations by varying the NMOS width. The Rise times and Fall times are noted for the 13th Monte Carlo Run for the two complementary outputs.

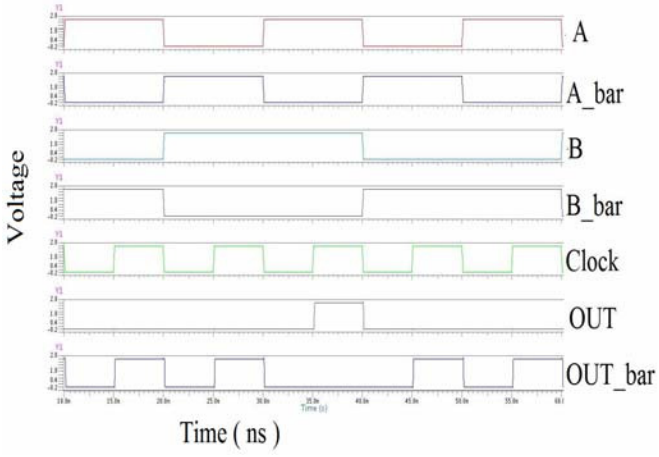

Fig. 2: Output of a Domino AND gate

"OUT": Rise time = 29.979 ps while the expected was 43.340 ps, Fall Time = 32.258ps while expected was 32.253ps. And "OUTBAR": Rise time = 36.016 ps, Fall time = 25.936 ps. Here, the junction capacitance is varied according to the Gaussian distribution with the nominal value being 9.51e-04 and the standard deviation being = .0019.

Case2: Varying the threshold voltage

The waveforms shown in Fig. 4 depict the Monte Carlo Simulations by varying the threshold voltage of NMOS. The Rise times and the Fall times for the 13th Monte Carlo Run for the two complementary outputs are "OUT": Rise time = 56.411ps, Fall time = 31.780ps and "OUTBAR": Rise time = 35.249ps, Fall time = 25.411ps.

The threshold voltage is varied according to the Gaussian distribution with the **nominal value** being **0.37** volts and the standard variation being 0.074. The corresponding random values for the 13h Monte Carlo run is Vth_0= .633971e-01 volts. The different plots correspond to the various Monte Carlo runs.

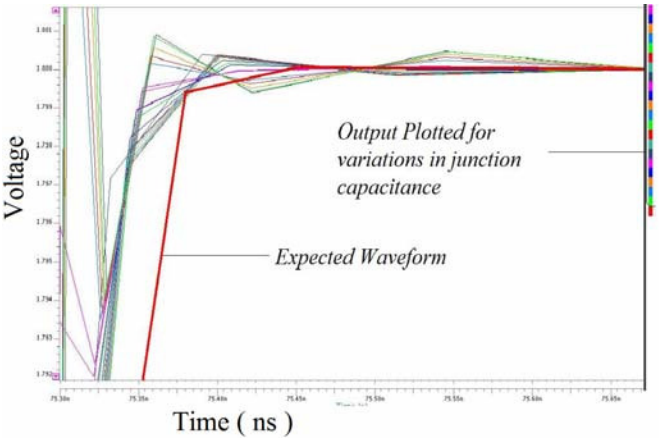

Fig. 3: "OUT" by varying junction capacitance

Case3: Varying the gate to bulk capacitance

The waveform in Fig. 5 shows the Monte Carlo simulation by varying the gate-to-bulk capacitance. The Rise and the Fall times for the 13th Monte Carlo Run for the two complementary outputs are "OUT": Rise time = 52.140ps, Fall Time = 32.312ps and "OUTBAR": Rise time = 32.369ps, Fall time = 26.275ps. The gate-to-bulk capacitance cgbo is varied according to the Gaussian distribution with the nominal value being 1e-12 and the standard deviation being =1.22x10^{-07}. The random value generated for the 13th Monte Carlo Run is 1.025242e-12 f. The different plots correspond to the various Monte Carlo runs.

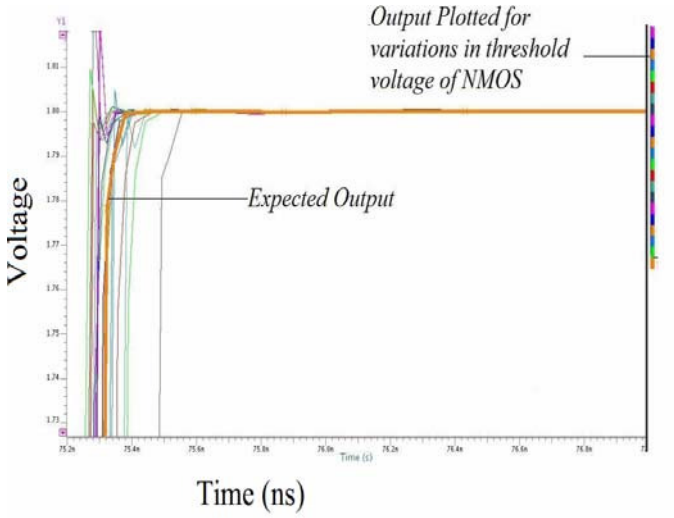

Fig. 4: Output at node "OUT" by varying the threshold voltage of NMOS

Case4. Injecting the transient noise

A noise source is injected between the Ground port (one of the power rails) and the Output ("OUT") port and a transient noise analysis is performed. A noise source had been injected at the power rails because the leakage of voltage bounce on the power supply rails into a substrate is the most dominant source of substrate noises in large scale digital circuits. The different plots correspond to the various Monte Carlo runs.

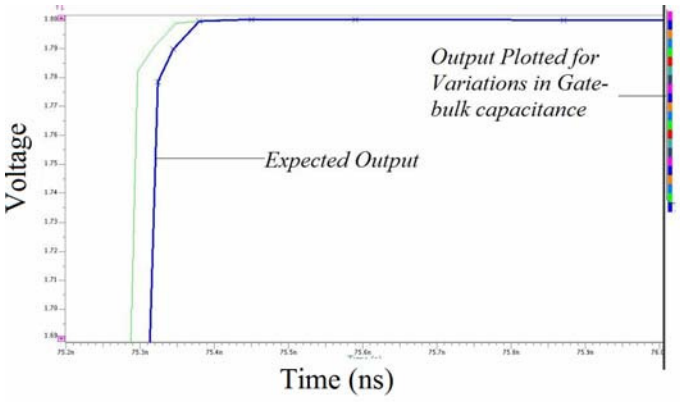

Fig. 5: output by varying the gate to bulk capacitance

The waveform in Fig. 6 shows the current variations in current at the output nodes. The graph plotted reveals the corresponding RMS values of the current at the output nodes.

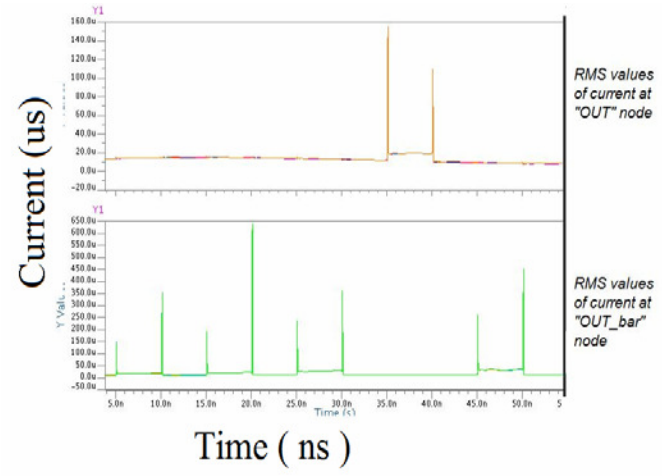

Fig. 6: Current at the output nodes. The outputs after injecting noise

It can be interpreted that, when the parameters that lead to the substrate perturbations are subjected to a change, they lead to a change in the delay of the circuit and, hence, affect the circuit performance.

V. Proposed Substrate Model

There are three possible ways to ensure that the substrate crosstalk does not result in circuit malfunction: fabrication techniques, design techniques, and analysis by modeling.

However the fabrication and design techniques do not result in the complete blocking of noise generation and noise propagation. Hence, to accurately determine the effects of substrate noise prior to manufacturing so that the output can be speculated for deviations from the expected value, a model must be developed that encompasses these effects.

Much of the work done in modeling the substrate emphasizes the resistive nature of the substrate [18]. These models are accurate for frequencies that are below 10GHz [19], but as the range of operating frequencies increases these models no longer prove to be accurate and it is important to consider the capacitive effect at the frequencies above 10GHz. The waveform in Fig. 7 depicts the variations in current at the output node of a dual rail Domino CMOS circuit at frequencies above 10GHz, showing that the variations at output are greater at these frequencies than at lower frequencies.

This paper proposes a substrate model that takes capacitance into account. These capacitances are actually the coupling capacitances of the substrate with the drain, source, and the gate as depicted in Fig. 8.

The equivalent circuit model derived from the circuit configuration in the Fig. 8 is depicted in Fig. 9. The Rsubstrate shown in Fig. 9 can be interpreted as a two plate resistive model [20].

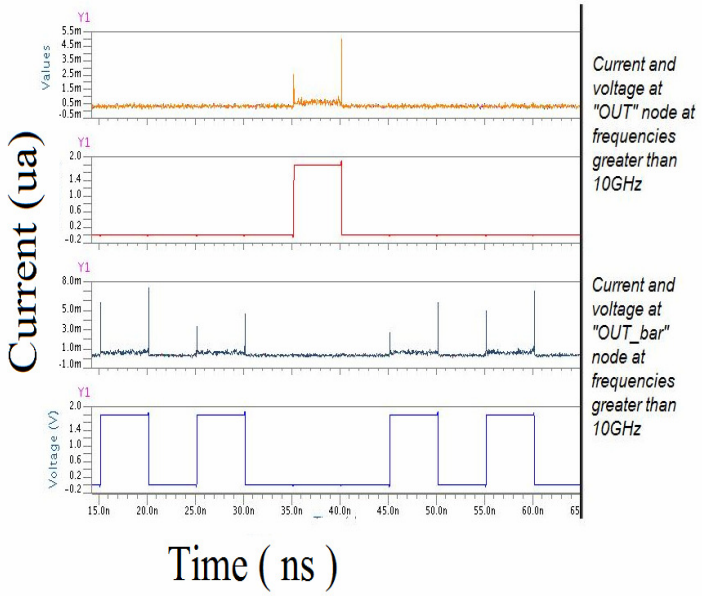

Fig. 7: Spike presentation in Current at output nodes for frequencies above 10GHz.

This model was verified by application to the various subcircuits of the dual rail Domino CMOS circuit. Then the values obtained from the netlist of these subcircuits were plugged in. The variations in the output voltage, as predicted by this model, were similar to those plotted and shown by the ELDO simulations for any of the three cases as shown in Fig.s [3-5].

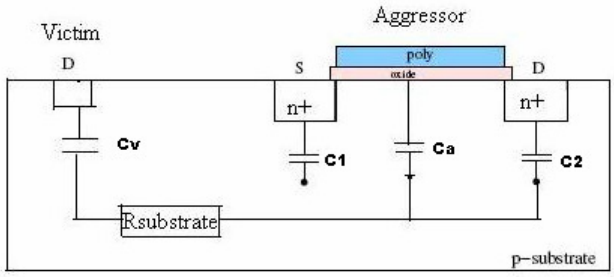

Fig. 8: Aggressor and victim coupling through substrate

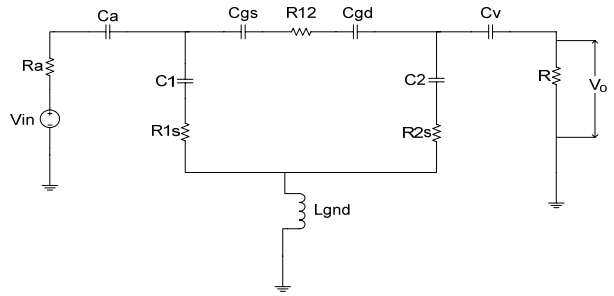

Fig. 9: Proposed substrate model

The equivalent RC model equations that can be derived from the substrate model described in Fig. 9 are listed below.

The output voltage variations can be estimated based on the equation derived from the above RC model.

$$Vo = \frac{Vin}{Za}\left(\frac{ZaZoR1(Zb+R1)}{(Zb+2R1)(Zb+R1)(Za+Zo)}\right) \quad (2)$$

where,

Za = (R1+Xa+Ra), Zb = (Rb+Xv), Zc=(Rc+Xgnd)

$$Ra = \frac{(R1+Xcbd)Zd}{(R1s+Xbs+Rs+Rds+Xbd)}$$

$$Rb = \frac{Zd(Rds+Xcbd)}{(R1s+Xbs+Zd+Rds+Xbd)}$$

$$Rc = \frac{(R1s+Xcbd)(Rds+Xcbs)}{(R1s+Xbs+Zd+Rds+Xbd)}$$

Zd = R12 + Xcgs,cgd)

c1 = combined capacitance of gate to source and source to substrate, c2 = combined capacitance of gate to drain and drain to substrate, and Ca and Cv are the capacitances of the aggressor and the victim nodes respectively. Fig. 10 shows the validation of the model which, when applied to the output node of the circuit, gave similar results to the Rise and Fall times deduced from the waveforms obtained for output by varying threshold voltage.

V. Conclusion

As revealed by the results, the Domino CMOS circuits are affected by substrate crosstalk, causing a change in the propagation delay of the circuit and, hence, affecting performance. Thus, it is important to estimate the effects of the substrate crosstalk prior to fabrication. Also, due to the statistical nature of the noise, statistical modeling is required to capture the effects of noise. Therefore, Monte Carlo simulations were carried out by varying the parameters affecting the substrate. The results obtained from these simulations supported our hypothesis. The simulations were carried out at a frequency both greater than and less than 10GHz. The results reveal that at frequencies above 10GHz the circuit becomes more vulnerable to noise perturbations. Hence, a purely resistive model of a substrate does not seem to accurately analyze substrate noise at frequencies above 10GHz. Therefore, the proposed model, which takes into account the capacitance accurately, correlates to the substrate effects. The effects of substrate were accurately predicted by the model proposed, confirming that, at higher frequencies of operation, capacitance should be considered. The model also gives the dependence of the circuit performance on the frequency.

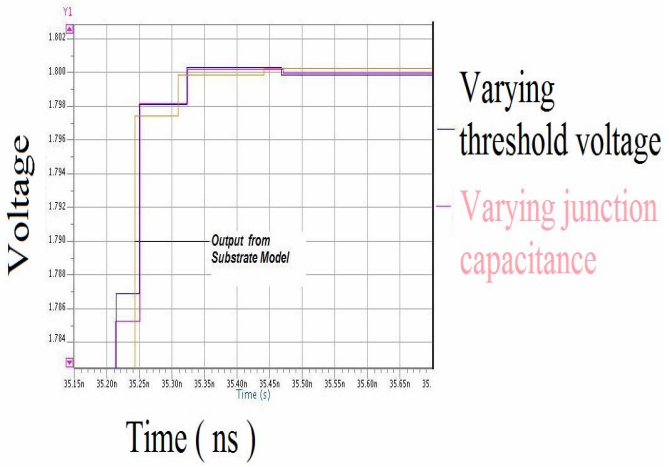

Fig. 10: verification of substrate model

References

[1]. Li Ding, Pinaki Mazumder, "*A Novel technique to improve the noise immunity of CMOS Dynamic logic circuits*", Design automation conference 2004.

[2] Larson Patrik, Svensson Christer," *Noise in digital dynamic CMOS circuits*", IEEE journal of solid state circuits vol29.

[3] Edoardo Charbon,"*Substrate Noise. Analysis and Optimization for IC design", 2003, pp.1-6.*

[4] T. J. Schmerbeck, "*Low-power HF microelectronics: A unified approach"*,G. A. S. Machado, Ed. London, U.K.: Institution of Electrical Engineers,(IEE), 1996, ch. 10.

[5] John P. Uyemura, "Fundamentals of MOS Digital Integrated Circuits", 1988, pp 22-35.

[6] P. Larsson, "di/dt noise in cmos integrated circuits," *Analog Integrated Circuits and Signal Processing*, vol. 14, pp. 113–129, 1997.

[7] T. Gabara, "Reduced ground bounce and improved latch-up suppression through substrate conduction," *IEEE J. Solid-State Circuits*, vol. 23, pp.1224–1232, Oct. 1988.

[8] Bhavna Jharia,S.Sarkar and R.P. Agarwal "Analystical Study of Impact Ionization and sub threshold current in Sub Micron n-MOSFET" , Sixth international Symposium on Quality Electronic Design (ISQED'05).

[9] Marc Van Heijiningen, John Compiet, Piet Wambacq, Stephane Donnay, Marc G.E. Engels and Ivo Bolsens, "*Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-type substrates*", IEEE 2000.

[10] R. Gharpurey and R.G. Meyer, \Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 344-353, March 1996.

[11] T. Smedes,"Extraction of Circuit Models for Substrate Cross-talk," *Proc. of the International Conference. on Computer Aided Design*, pp. 199-206, November 1995.

[12] E. Charbon, "Substrate Optimization Based on Semi-Analytical Techniques,"*IEEE Transaction on Computer-aided design of Integrated Circuits and Systems*,Vol. 18, pp. 172-190, February 1999.
[13] E. Charbon, "Substrate Noise: Analysis and Optimization for IC design,"*Kluwer Academic Publishers*, 2001.
[14] Kundu, R and Blanton, R.D," *Identification of the Crosstalk switch failures in Domino CMOS circuits*", Test Conference, 2000. Proceedings.International, 2000 Page(s):502 – 509
[15] Waleed K. Al- Assadi, Vipin Sharma, Pavankumar Chandrashekhar,"*Crosstalk at the dynamic node of the domino CMOS circuits", part of UMR research.*
[16] Makie-Fukuda, K.; Anbo, T.; Tsukada, T.; Matsuura, T.; Hotta, M., " *Voltage comparator based measurements of equivalently sampled substrate noise waveforms in mixed signal integrated circuits*" Solid-State Circuits, IEEE Journal of Volume 31, Issue 5, May 1996 Page(s):726 – 731.
[17] Makoto Nagata and Atsushi Iwata, " *Substrate noise simulation techniques for analog digital mixed lsi design*", IEICE Trans. Fundamentals, vol. E82-A
[18] A. Samavedam, A. Sadate, K. Mayaram, T. Fiez, A scalable substrate noise coupling model for design of mixed-signal IC's. *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 895-904, June 2000.
[19] R. Singh, A review of substrate coupling issues and modeling strategies. *IEEE 1998Custom Integrated Circuits Conference*, pp. 491, May 1998.
[20] Vijay Raghavan, Ravi Commandur*, "Substrate Noise Analysis in RF integrated circuits"* MS Dissertation, North Carolina State University, 2003