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Modeling Multilayered PCB Power-Bus Designs Using an MPIE Based Circuit Extraction Technique

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I. Abstract

A circuit extraction tool (CEMPIE) has been developed based on the mixed-potential integral equation (MPIE) [1], [2] using a quasi-static approximation [3]. A power-bus in a multi-layered PCB consisting of a pair of dedicated ground and power planes is studied using this tool. The distributed behavior of a power-bus is represented by a collection of passive circuit elements, which is valid up to several gigahertz. The decoupling performance of a power-bus due to its layer spacing and the dielectric constant is evaluated for simple test geometries. The impact of the relative distance between the noise source and the potential receiver is also studied. Novel structures such as a power island were studied in both thin and thick boards, and the decoupling performance due to the locations and values of the decoupling capacitors were also investigated.

II. Formulation

Let S be a perfect electric conductor (PEC) surface. The boundary condition requires

$$\hat{n} \times (\vec{E}^{inc} + \vec{E}^{s})|_S = 0, \tag{1}$$

or,

$$\hat{n} \times \vec{E}^{inc} = \hat{n} \times \left(j\omega\vec{A} + \nabla\phi\right) \tag{2}$$

on S using scalar and vector potential functions. The PEC surface is discretized by a triangular mesh with N cells, the surface current density $\vec{J}$ can be expanded in terms of a set of vector basis functions $\vec{f}_\alpha$ [4], $\vec{J} = \sum_{\alpha=1}^{M} I_\alpha \vec{f}_\alpha(\vec{r})$, where M is the total number of interior edges in the discretized domain of S. If the scalar potential is further assumed to be constant within each mesh cell, then a node based admittance system function for the mixed-potential integral equation (MPIE) results, specifically,

$$\mathbf{Y} = \frac{1}{j\omega}\mathbf{\Lambda}^T\mathbf{L}^{-1}\mathbf{\Lambda} + j\omega\mathbf{K}^{-1}, \tag{3}$$

where the branch-wise inductive matrix elements are

$$L_{\alpha\gamma} = \frac{\mu}{l_\alpha l_\gamma}\int_S ds\vec{f}_\alpha \cdot \int_S \mathbf{G}^A(\vec{r},\vec{r}')\cdot\vec{f}_\gamma ds', \tag{4}$$

and the node-wise inverse capacitive matrix elements are

$$K_{mn} = \frac{1}{\epsilon A_m A_n}\int_{T_m}\int_{T_n} G^\phi(\vec{r},\vec{r}')ds'ds. \tag{5}$$

$\mathbf{\Lambda}$ is the connectivity matrix whose elements are determined by

$$\Lambda_{\alpha n} = \begin{cases} 1, & \textit{if } Cell_n \textit{ is Edge } \alpha\textit{'s positive side} \\ -1, & \textit{if } Cell_n \textit{ is Edge } \alpha\textit{'s negative side} \\ 0, & \textit{otherwise.} \end{cases}$$

$\mathbf{G}^A(\vec{r},\vec{r}')$ is the dyadic Green's function for the vector potential $\vec{A}$, and $G^\phi(\vec{r},\vec{r}')$ is the Green's function for the scalar potential ϕ.

Circuit component values can be extracted by comparing Eqn. (3) with the admittance function of an N-node LC circuit network. This "Circuit Extraction / MPIE" technique is denoted CEMPIE.

III. PCB power-bus analysis using CEMPIE

Two types of board materials were used in this study: (1) a thin board with $d = 10$ *mil* and $\epsilon_r = 2.99$, and, (2) a thick board with $d = 43$ *mil* and $\epsilon_r = 4.7$. CEPIE modeling was compared with two-port measurements using an HP8753D network analyzer for several configurations.

The ground planes used in the power-buses under study are all free of discontinuities with area larger than that of the power plane. The ground plane is treated analytically as if it has infinite extent in the xy-plane, hence, the Green's functions were computed with a PEC plane. Then, only the power plane is meshed. Two power plane geometries were used: A 50 $mm \times 50$ mm power-bus denoted *Power-bus*, and a power-bus with gaps resembling an island denoted *Power-island*. To be efficient, the same mesh was used for *Power-buses* or *Power-islands* with different material properties. The meshes for the *Power-bus* and *Power-island* structure is shown in Fig. 1. The *Power-bus* is has 386 cells with an average edge length of 4.081 mm. The *Power-island* has 416 cell with an average edge length of 3.686 mm. Assuming the upper frequency under consideration is $f_c = 5\ GHz$, a developed meshing constraint in terms of the maximum average edge length are 5.387 mm and 5.505 mm for the thin and thick boards, respectively [3]. Thus, the two meshes are likely to provide reliable extracted equivalent circuit models.

Several cells (or circuit nodes) need to be specially labeled for the following discussions. Since both meshes can be covered by a 50 $mm \times 50$ mm area, a common index

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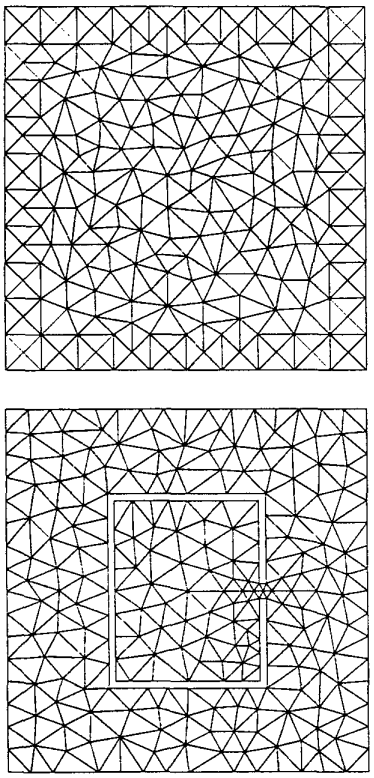

Fig. 1. Meshes for the *Power-bus* (top) and the *Power-island* (bottom) geometry.

map is used as shown in Fig. 2, with further details listed in Table I. Modeled and measured data are presented in Fig. 3 for the *Power-bus* structure when the two ports are selected at Locs. 1, 3. Modeled and measured data for the *Power-island* structure are presented in Fig. 4 when the two ports are selected at Locs. 1, 2. The results are presented in terms of $|S_{21}|$ in order for easily comparing with the swept frequency measurements. The tests show that the MPIE extracted circuit model can predict the responses well up to 3 GHz in most cases and the trends are consistent with the experiments up to 5 GHz. Good agreement has been obtained recently to 5 GHz with more careful measurements.

The behavior of a typical interconnect for a decoupling capacitor was modeled by a capacitor, inductor, and resistor connected in series [5], [6], [7]. A previously developed measurement technique [8] was used to characterize the interconnects for the thin and thick boards, the following parameters are used in the remainder of this study unless specified otherwise:

Board	C (μF)	L (nH)	R ($m\Omega$)
thin	0.01	2	20
thick	0.01	7	50

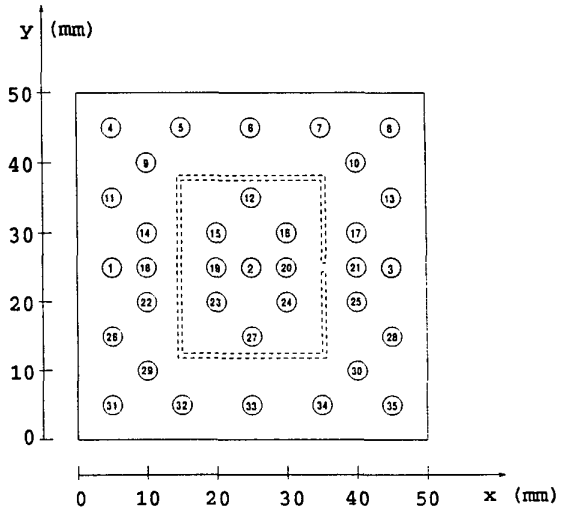

Fig. 2. Indexed locations in both *Power-bus* and *Power-island* geometries.

TABLE I
SELECTED LOCATION INDICES AND THEIR COORDINATES (IN MM).

Index	(x, y)	Index	(x, y)
1	(5, 25)	19	(20, 25)
2	(25, 25)	20	(30, 25)
3	(45, 25)	22	(10, 20)
5	(15, 45)	25	(40, 20)
6	(25, 45)	27	(25, 15)
7	(35, 45)	29	(10, 10)
9	(10, 40)	30	(40, 10)
10	(40, 40	32	(15, 5)
12	(25, 35)	33	(25, 5)
14	(10, 30)	34	(35, 5)
17	(40, 30)		

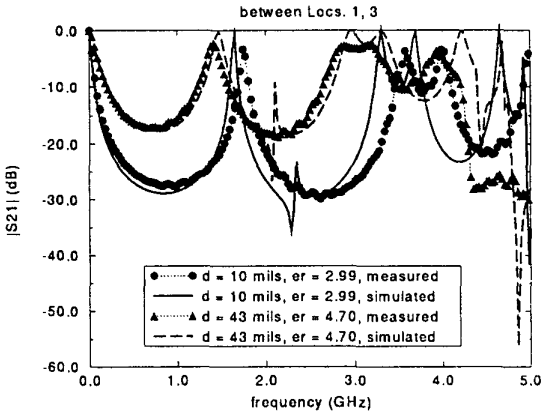

Fig. 3. Comparison of simulations and measurement for the *Power-bus* structures.

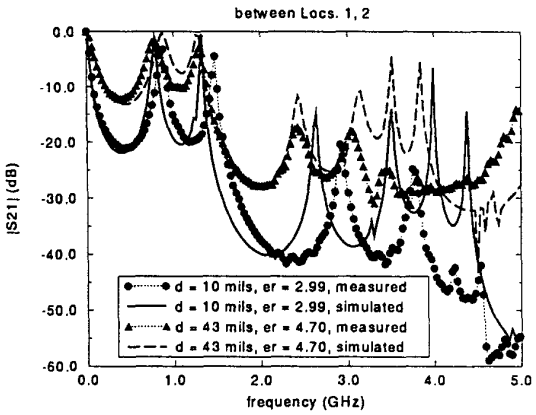

Fig. 4. Comparison of simulations and measurement for the *Power-island* structures.

TABLE II
GRID DIMENSIONS OF THE BARE BOARD *Power-bus*ES.

d in mil	ϵ_r	ρ_c in mm	grid dimension in mm
10	2.99	5.387	5.0
10	4.7	3.17	3.125
10	35.0	–	1.515
43	2.99	8.41	6.25
43	4.7	5.505	5.0

IV. POWER-BUS DESIGN APPLICATIONS

The two-plane power-bus structure has an intrinsic decoupling capability even without any added decoupling capacitors. In the simplistic parallel-plate capacitance model, the intrinsic capacitance is $C_0 = \frac{\epsilon_0 \epsilon_r A}{d}$, which is 260 pF, and 95.2 pF for the thin and thick board, respectively. In addition to the experimental power-bus fixtures, three additional boards with identical geometry but varying thickness and dielectric constant of (d in mil, ϵ_r, C_0 in pF) = (43, 2.99, 60.6), (10, 4.7, 409), and (10, 35.0, 3049) were considered.

The variation in the board response as a function of the interplane capacitance was considered for different plane spacings and dielectric constants. Five meshes were generated for the cases using grid dimensions shown in Table II. The S_{21} modeling results are shown in Fig. 5. Many of the peaks shown in Fig. 5 corresponding to the distributed board resonances have high Q's. Similar results are shown in the modeling and measurement comparisons in Figs. 3 and 4. However, $|S_{21}|$ measurements on populated boards show that there is sufficient loss associated with devices and decoupling capacitors to considerably lower the Q value. Taking account into this loss mechanism, the results in Fig. 5 support the common perception that maximizing interplane power-bus capacitance can be beneficial.

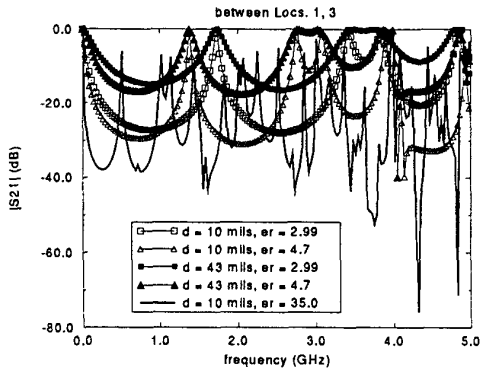

Fig. 5. $|S_{21}|$ responses of the bare board *Power-bus* structures.

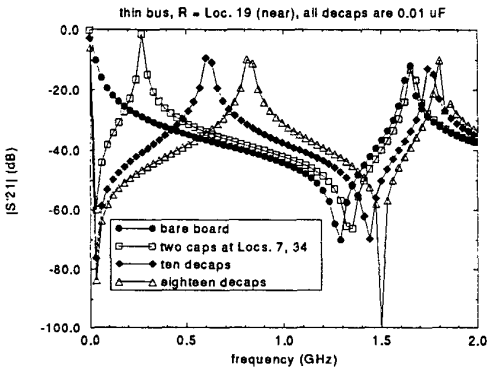

Fig. 6. Simulated $|S_{21}|$ results in the thin board with different numbers of capacitors for a near receiver.

The addition of lumped decoupling capacitors was also modeled. Four cases were studied. A bare board; a board with two capacitors attached at Locs. 7 and 34; a board with ten capacitors attached at Locs. 6, 9, 10, 14, 17, 22, 25, 29, 30, and 33; and, a board with eighteen capacitors attached at Locs. 5, 6, 7, 9, 10, 12, 14, 17, 19, 20, 22, 25, 27, 29, 30, 32, 33, and 34. With the source fixed at Loc. 1, the effect of the number of capacitors is shown in Fig. 6 for the near receiver (Rn at Loc. 19) in the thin board, and Fig. 7 for the far receiver (Rf at Loc. 3) in the thin board. In the above cases an increase in the number of capacitors has little influence on the first zero as expected since it is a lumped element resonance [8], but moves the first distributed resonance peak toward higher frequencies. This effect has been seen experimentally on production PCB's as well.

Another significant design consideration is the value of individual decoupling capacitors. Decoupling capacitors were added at ten sites (Locs. 6, 9, 10, 14, 17, 22, 25, 29, 30, and 33) Identical capacitance values were used for

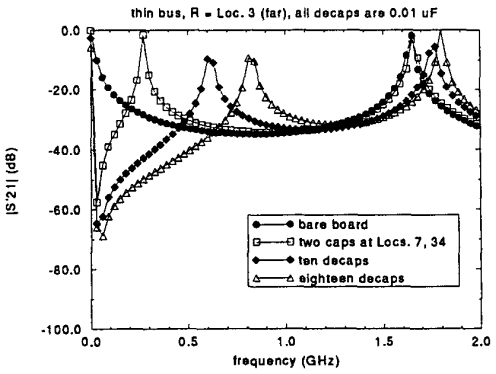

Fig. 7. Simulated $|S_{21}|$ results in the thin board with different numbers of capacitors for a far receiver.

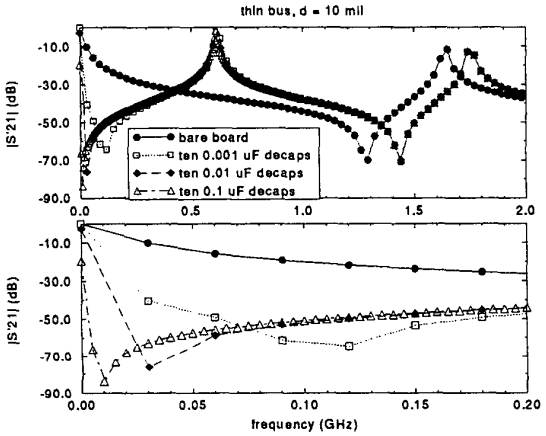

Fig. 8. Effect of capacitance values in the thin board for the near receiver.

three cases considered with $0.001\mu F$, $0.01\mu F$, or $0.1\ \mu F$. In all three cases, each capacitor was greater than the interplane capacitance of the PCB ($C_0 = 409\ pF$). The source was at Loc. 1. The effect of the different capacitance values is shown in Fig. 8 for the near receiver at Loc. 19, and Fig. 9 for the far receiver at Loc. 3. The frequency responses beyond 500 MHz are virtually the same even though the individual capacitance values vary from $0.001\mu F$ to $0.1\mu F$. These results suggest that for identical capacitor package sizes and mounting configurations (interconnects) the largest value of capacitor is of most benefit. Modeling the power-bus as a simpler lumped capacitor, the first minimum in the response occurs at the series LC resonance frequency of the interconnect inductance (2 nH for the thin board) resonating with the decoupling capacitor. For the values of capacitors 0.001, 0.01, and $0.1\mu F$, this occurs at 112, 36, and

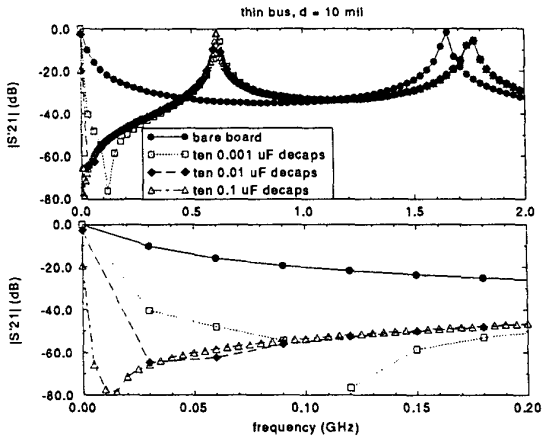

Fig. 9. Effect of capacitance values in the thin board for the far receiver.

11 MHz, respectively. The CEMPIE results in Figs. 8 and 9 support the single-capacitance model in the low frequency range ($f < 200\ MHz$). On the other hand, in the simple lumped capacitance model, the first maximum results from the parallel resonance of the interconnect inductances (ten in parallel) with the PCB interplane capacitance C_0, which would be 556 MHz for the thin board. But the CEMPIE results in Figs. 8 and 9 show the first maximum to be around 600 MHz, which indicates the inadequacies of the lumped capacitance model at higher frequencies.

A gap discontinuity created in the power plane may intuitively suggest an isolation of the noise source from the other devices on the PCB, and is considered here. The gapped structure is suggestive of a π-filter, with the interplane capacitance of the two areas on either side of the gap providing the shunt C, and a thin neck of the gap connecting the two segmented area providing the series L. The measured and modeled results in Figs. 3 and 4 show some isolation between the segmented power-bus portions above 2 GHz. However, below $2GHz$, the segmentation introduces additional resonances with increased coupling between the two areas.

The effect of an additional lumped decoupling capacitor near and remote from the conductor neck joining the two regions. The source and receiver sites were designated: S for the source, Rn for the near receiver, and Rf for the remote receiver. A single decoupling capacitor was added at one of the two locations shown in Fig. 10 for a bare board, the decoupling capacitor near the neck at Loc. 20, and the decoupling capacitor at Loc. 7, remote from the neck. Modeled results are displayed in Figs. 11 and 12 in the thin board for the near and remote receiver, respectively. The location of the decoupling capacitor has little impact on isolation between the two power segments.

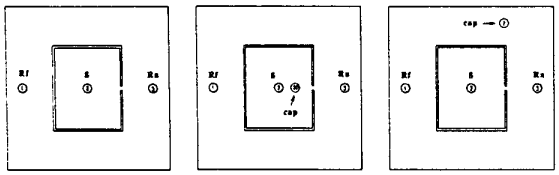

Fig. 10. Configurations for the three decoupling cases.

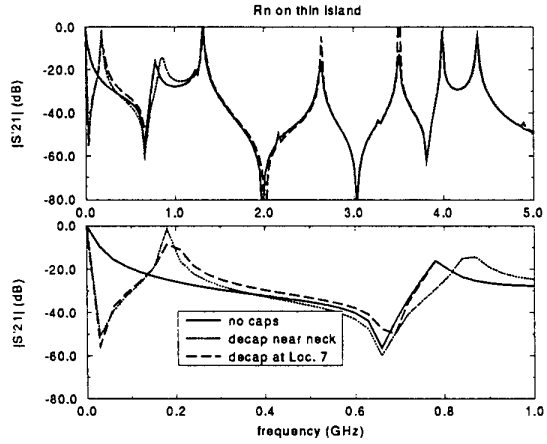

Fig. 11. Simulated $|S_{21}|$ results for the near receiver in the thin *Power-island.*

V. Conclusion

A power-bus modeling tool has been developed based beginning with a mixed-potential integral equation formulation and extracting an equivalent circuit for the power-bus. The advantage of this approach is that the formulation starts from first principles and incorporates the distributed behavior of the planes, yet does not solve the discretized integral equations, rather, extracts an equivalent circuit model. The equivalent circuit model can then be implemented in SPICE, and IC device models and PCB trace models incorporated into the overall modeling for signal integrity. This approach is easily implemented. Further, for known or anticipated EMI coupling paths and antennas, approximate lumped models can be used with the power-bus model to estimate radiated EMI processes.

Modeled and measured results agree well for current work to several Gigahertz. Typical concerns in power-bus design including the benefits of increasing interplane capacitance, the value and location for decoupling capacitors, effects of power plane segmentation, and the impact on EMI are being addressed with this modeling approach. Further, performance differences, and potential differences in designs for thin (10 *mils* or less) and thick (40 *mils* and greater) power buses, e.g., decoupling capacitor locations are being investigated.

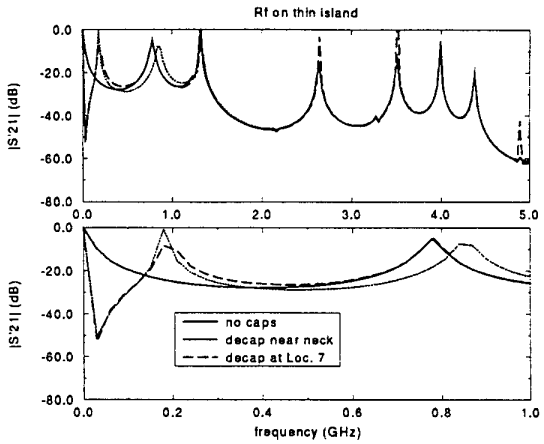

Fig. 12. Simulated $|S_{21}|$ results for the remote receiver in the thin *Power-island.*

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