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Mitigating Power Bus Noise with Embedded Capacitance in PCB Designs

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Abstract: This paper investigates the power bus noise and power bus impedance of printed circuit boards with four different kinds of embedded capacitance. These boards have power-ground plane pairs separated by a very thin layer of material with high dielectric permittivity. It is shown that embedded capacitance effectively reduces power bus noise over the entire frequency range evaluated (up to 5 GHz).

INTRODUCTION

Power bus noise in high-speed printed circuit boards (PCBs) and multi-chip modules (MCMs) can cause serious radiated EMI and signal integrity problems. In current printed circuit board designs, decoupling capacitors are commonly employed to mitigate power bus noise. Typical high-speed digital boards may utilize dozens or even hundreds of decoupling capacitors. These capacitors take up space on the board and can reduce the reliability of the product. In addition, the effective range of discrete decoupling capacitors is generally limited to a few hundred megahertz due to the interconnection inductance [1].

The intrinsic capacitance between adjacent power and ground planes in a multi-layer printed circuit board also provides decoupling [2]. However, this embedded capacitance (or buried capacitance) is too small in most current designs to be of significant benefit over a wide frequency range. By locating the power and the ground planes very close to each other and by filling the space between these two planes with a material that has a high relative permittivity, the board capacitance can be greatly enhanced. As a result, it may be possible to eliminate the local decoupling capacitors (e.g. capacitors with a value of 0.01 microfarads or smaller) in boards with embedded capacitance. Normally, bulk decoupling capacitors (e.g. capacitors with a value of 1 microfarad or greater) are still used in boards with embedded capacitance to reduce low-frequency power bus noise.

As part of the research for the Embedded Decoupling Capacitance (EDC) project led by the National Center for Manufacturing Sciences (NCMS), printed circuit boards utilizing four embedded capacitance materials were evaluated. These materials are described in Table 1. The relative permittivity and the loss tangent of each material were measured by the National Institute of Standards and Technology (NIST) at different frequencies. Additional information on these materials can be obtained from [3].

Table 1. Embedded capacitance materials evaluated in the study

Materials	Dielectric Composition	Thickness	ε_r	$\tan\delta$	C_B (pF/cm^2)
EC#1	FR-4 epoxy/glass	2.1 mils	3.8~4.2	0.015~0.02	~70
EC#2	Unsupported epoxy; ceramic powder filled	4.0 mils	36~37	0.01~0.02	~ 300
EC#3	Unsupported polyimide; ceramic powder filled	1.4 mils	11.6~12	0.008~0.012	~ 300
EC#4	Unsupported epoxy; ceramic powder filled	0.2 mils	20~22	0.01~0.1	~ 4000

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Power bus noise measurements for test boards with these embedded capacitance materials were reported in [4]. Simple models for printed circuit boards with embedded capacitance were presented in [5]. This paper further examines the properties of boards with embedded capacitance and demonstrates the correlation between power bus impedance and power bus noise.

DESCRIPTION OF THE TEST BOARDS

The basic layout of the test vehicle is illustrated in Figure 1. The board contains an oscillator, a 22-μF bulk decoupling capacitor, eight octal clock drivers, and a number of load capacitors in a 7.6-cm by 5.1-cm area. The oscillator supplies a 50-MHz signal to the first clock driver (U5), which in turn supplies 50-MHz clock signals to each of six other clock drivers. The clock driver U4 was used for noise current measurements and was not active for the tests described in this paper. On the boards designated as having discrete decoupling, there are 33 local 0.01-μF decoupling capacitors spread all over the board. In addition, all test boards discussed in this paper have 6 layers. The ground and power planes are located on layers 3 and 4 respectively. In boards with embedded capacitance, the spacing between the power and ground planes was equal to the thickness of the dielectric material as listed in Table 1. The power bus structure was accessed through an SMA coaxial connector (J1) and a 2-pin connector (P1). These connectors are mounted on the surface of the board adjacent to Layer 6, while the rest of the components are mounted on the opposite surface adjacent to Layer 1.

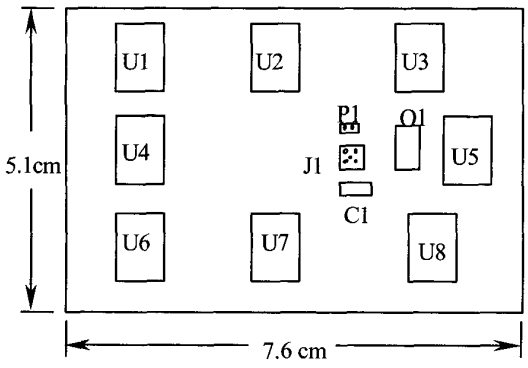

Figure 1. Basic layout of the test vehicle.

EXPERIMENTAL RESULTS

Test boards with embedded capacitance as well as standard FR4 boards were measured in the lab. The power bus input impedance was measured using an HP8753D network analyzer between 30 kHz and 5 GHz. Figure 2 shows the measured power bus impedance at the location of the J1 connector for two standard FR4 boards with and without the discrete decoupling capacitor. The spacing between the power and the ground planes is about 4.5 mils for both test boards. The apparent ~1 ohm-per-GHz slope is mainly due to the small (~120 pH) inductance of the SMA connector's attachment to the power-ground plane pair. Power bus resonances dominate both impedance curves above 900 MHz.

The board without decoupling capacitors has a sharp resonance peak below 100 MHz. This is not a power bus resonance, but a resonance between the board's inter-plane capacitance and the connection inductance of components mounted on the surface. At low frequencies, the decoupling capacitors did a good job of eliminating this resonance. However, above 500 MHz, all the discrete decoupling capacitors have too much connection inductance to be effective. There is no significant difference between these two curves above 500 MHz other than minor shifts in the power bus resonance frequencies.

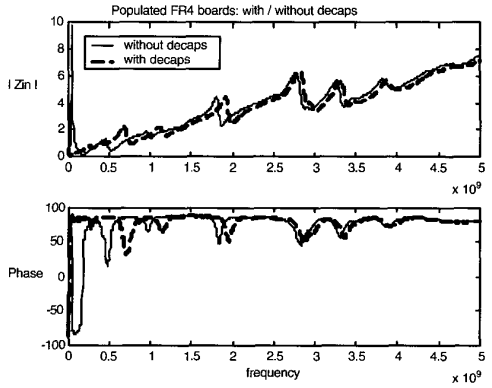

Figure 2. Power bus input impedance of populated FR4 board: with / without discrete decoupling capacitors.

The power bus input impedance of five populated boards employing different dielectric materials is plotted in Figure 3. None of these boards uses local decoupling capacitors. The 4.5-mil FR4 board exhibits significant peaks at power bus resonant frequencies. Several resonant peaks and nulls are also evident in the EC #1 curve. Ripples in the EC #2 and EC #3 curves are less pronounced. The EC #4 curve is nearly a straight line.

Again, this slope is mainly due to the SMA probe's connection inductance.

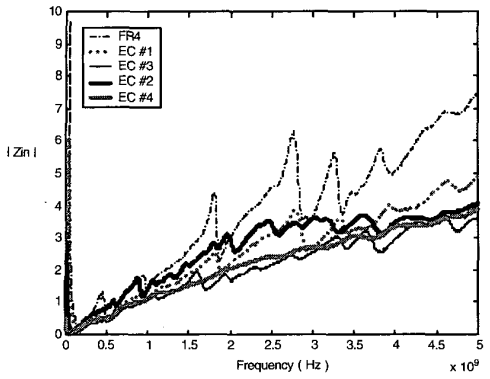

Figure 3. Power bus input impedance of populated boards with different dielectric materials.

To evaluate the power bus noise performance, an HPE3630A DC power supply set to 3.3 volts was connected to the 2-pin connector (P1) on the test board using a 0.6-m unshielded twisted wire pair. A Rohde & Schwarz FSEB30 spectrum analyzer was used to measure the power bus noise with the board operational. In order to achieve a low noise floor and to keep the sweep time reasonable, The measurement was broken into three frequency bands: from 1 MHz to 1 GHz, from 1 GHz to 3 GHz, and from 3 GHz to 5 GHz.

The measured data for two 4.5-mil spacing FR4 boards with and without the discrete decoupling capacitors is plotted in Figure 4, Figure 5, and Figure 6 for each of the three frequency ranges. The spikes in these plots represent power received at the 50-ohm input of the spectrum analyzer at a specific harmonic frequency. The dotted curves for the board with decoupling capacitors are deliberately shifted by +10 MHz in order to make a comparison of the levels easier. As indicated in Figure 4, adding discrete decoupling capacitors significantly reduces the power bus noise at the fundamental 50-MHz signal and its first two harmonics. Between 250 MHz and 400 MHz, the power bus noise of the test board with the decoupling capacitors is about 10 dB lower than the board without decoupling capacitors. However, above 450 MHz, the effectiveness of the discrete decoupling capacitors is questionable. At some harmonics, the board without decoupling capacitors produces more noise, while at other harmonics the board with decoupling capacitors is noisier.

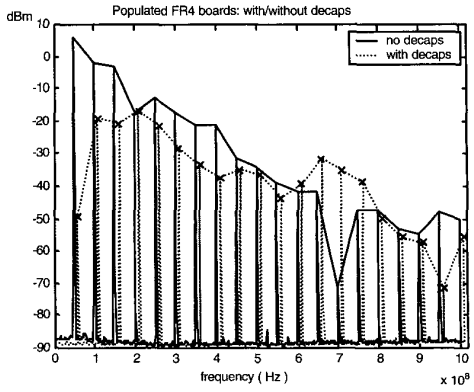

Figure 4. Power bus noise of FR4 boards with/without discrete decoupling capacitors: 1 MHz – 1 GHz.

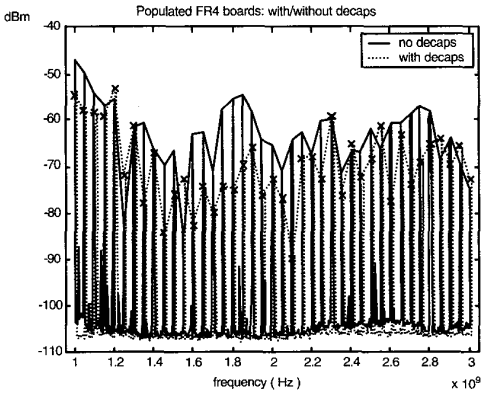

Figure 5. Power bus noise of FR4 boards with/without discrete decoupling capacitors: 1 GHz – 3 GHz.

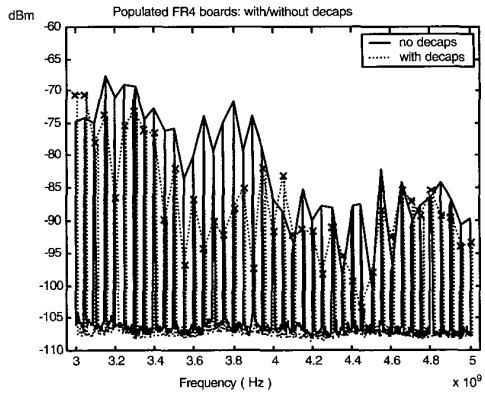

Figure 6. Power bus noise of FR4 boards with/without discrete decoupling capacitors: 3 GHz – 5 GHz.

Peaks in both the power bus impedance and the power bus noise occur at resonant frequencies of the test

board. In Figure 2, the FR4 board without discrete decoupling capacitors exhibits apparent resonant peaks at 47 MHz, 410 MHz, 953 MHz, 1.806 GHz, 2.769 GHz, 3.254 GHz, and 3.81 GHz. The first two resonances are due to the board capacitance and the interconnection inductance of the 22-μF bulk decoupling capacitor. Others are power bus resonances. The power bus noise spectrum of the same board plotted in Figures 4-6, exhibits strong power bus noise components near these resonant frequencies. Adding discrete decoupling capacitors eliminates the resonances at 47 MHz and 410 MHz, and results in a significant decrease in power bus noise below 450 MHz. With 33 0.01-μF discrete decoupling capacitors on the FR4 board, the first resonance occurs at 687 MHz. Correspondingly, the board with discrete decoupling exhibits considerable power bus noise around 650 MHz. Other power bus resonances for the board with discrete decoupling capacitors are shifted to 1.2 GHz, 1.92 GHz, 2.84 GHz, and 3.3 GHz. The power bus noise data also exhibits relatively strong components around 1.2 GHz, 1.9 GHz, 2.85 GHz, and 3.3 GHz

It is inconvenient to evaluate the performance of different test boards by comparing the amplitudes of all 20-40 harmonics in each plot. So, in order to develop a criterion for comparison, the amplitude of the power at all harmonics in a specific frequency range is summed. For example, the total power in the twenty harmonics between 1 MHz and 1 GHz is calculated as,

$$P_{total}(dBm) = 10log_{10}\left(\sum_{n=1}^{20} 10^{P_n/10}\right)$$

where P_n is the power in the nth harmonic in dBm. The total power, P_{total}, is then used to evaluate the relative performance of different test boards.

The power bus noise measurement results for 6 test samples with different materials are summarized in Figure 7. In these figures, each bar is labeled to indicate the material between the power and ground planes. "FR4" in the label indicates the board is made with FR4 material. "FR4 w/d" indicates FR4 material is used and the 33 local decoupling capacitors were mounted. The height of each bar indicates the total noise power in all harmonics within a specific measurement frequency range.

In the 1MHz – 1 GHz range, the power bus noise from the FR4 board with 33 local decoupling capacitors is more than 20 dB lower than its counterpart without discrete decoupling capacitors. However, in the medium and high frequency ranges, the difference between FR4 boards with and without decoupling capacitors is negligible. In all three frequency ranges, embedded capacitance boards exhibit less power bus noise than the FR4 board without discrete decoupling capacitors. Above 1GHz, the boards with embedded capacitance exhibit less power bus noise than boards employing discrete decoupling capacitors. Between 3 GHz and 5 GHz, the total noise power for 3 out of the 4 embedded capacitance boards is more than 10 dB lower than the corresponding FR4 board with discrete decoupling capacitors.

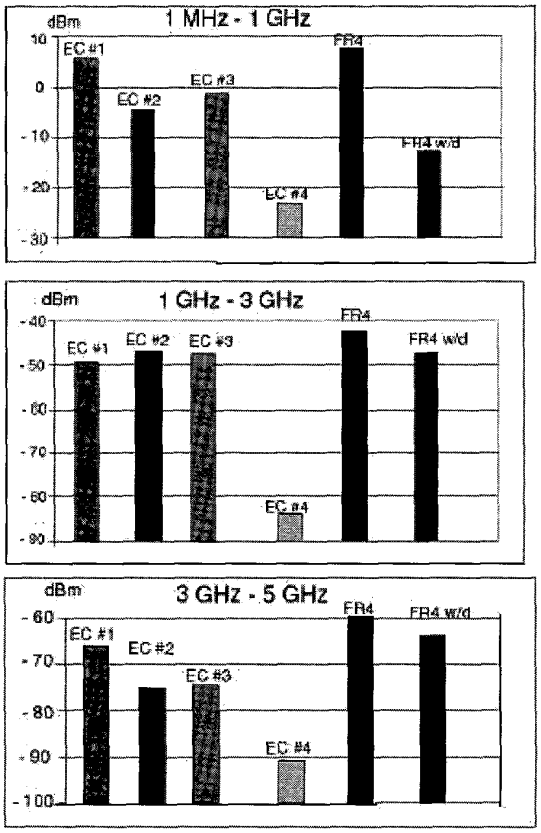

Figure 7. Power bus noise in different frequency ranges.

It is also useful to note that the power bus noise performance of a test board is correlated with its power bus input impedance. The FR4 board has the most significant resonance peaks in the power bus input impedance curve and exhibits the highest power bus noise. The EC #1 board also exhibits apparent power bus resonance peaks and generates more power bus noise than the other 3 embedded capacitance boards. Both the EC #2 and the EC # 3 boards have moderate power bus resonance peaks in the power bus impedance curves and exhibit moderate power bus noise levels. All power bus resonances are essentially eliminated in the EC #4 board

and the EC #4 board consistently exhibited the least power bus noise in the test group.

CONCLUSIONS

Printed circuit boards with 4 types of embedded capacitance were evaluated in this study and compared to boards made with standard FR4 material employing discrete decoupling capacitors. At frequencies above a few hundred megahertz, the embedded capacitance boards exhibited lower power bus impedance and lower power bus noise levels.

The power bus noise tended to peak at frequencies corresponding to power bus resonances. Embedded capacitance boards employing materials with high dielectric constants have more power bus resonances within a given frequency range. However, these resonances were considerably more damped in the embedded capacitance boards evaluated than in the standard FR4 boards evaluated. The EC#4 boards, with a plane spacing of 0.2 mils, had the lowest power bus impedance and exhibited no power bus resonances. These boards were the most effective for reducing power bus noise.

While the discrete decoupling capacitors on the FR4 boards did a good job of reducing power bus impedance and power bus noise at low frequencies, they were ineffective above a few hundred megahertz. On the other hand, the embedded capacitance was effective over the entire frequency range evaluated (up to 5 GHz).

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