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Jingkun Mao

Chen Wang

Giuseppe Selli

Bruce Archambeault

Missouri University of Science and Technology, archamb@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1715

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Memory DIMM DC Power Distribution Analysis and Design

Jingkun Mao, Chen Wang, Giuseppe Selli,
Bruce Archambeault * and James L. Drewniak

EMC Lab.
University of Missouri-Rolla
Rolla, MO, 65409
jingkun@umr.edu

*IBM Co.
Research Triangle Park
NC, 27709
barch@us.ibm.com

Abstract

DC power bus design is critical in meeting signal integrity (SI) and electromagnetic compatibility (EMC) requirements. A suitable modeling tool is beneficial to evaluate power bus design and develop design guidelines. This paper discusses difficulties met in evaluating the power distribution design on a dual inline memory module (DIMM) board, such as a power bus with arbitrary shape, parasitic inductance associated with vias, and so on. Moreover, some solutions are given in this paper. A simple cavity model with a segmentation method was employed to model a power bus with irregular shapes. The partial element equivalent circuit (PEEC) technique was applied to model the electrical properties of a high-speed via interconnect. For each proposed approach, the difference between the estimates and measurements demonstrates the application of these approaches in the DIMM DC power distribution analysis and design.

Keywords

Cavity model, DC power, simultaneous switching noise, segmentation method, PEEC.

INTRODUCTION

Simultaneous switching of digital logic within the core, as well as simultaneous switching of device I/O, results in high-frequency noise in printed circuit boards (PCBs). This high-frequency noise (ΔI noise) on the DC power bus is a common problem in high-speed printed circuit board (PCB) and multi-chip module (MCM) designs [1], [2]. ΔI noise can lead to signal integrity (SI) problems and is a potential source of radiated electromagnetic interference (EMI) [3]. A DC power structure in a multilayer printed circuit board (PCB) that employs two or more planes as dc power and ground is common in high-speed digital design. The parallel plate structure is designed to have a low impedance, however, noise on the power bus is easily propagated throughout this low impedance structure.

The power bus noise can be minimized by using a proper stackup, dielectric constant, and layer thickness. In addition, decoupling as a mitigation method is commonly used. Typical high-speed digital designs require dozens or even

hundreds of discrete decoupling capacitors. These capacitors take up space and can reduce the reliability of the product. In addition, the effective frequency range of discrete decoupling capacitors on printed circuit boards is generally limited to several hundred megahertz due to the interconnection inductance [4]. Many efforts have been made to optimize decoupling designs, such as the number of decoupling capacitors, decoupling locations, and the interconnect designs [5]. Embedded capacitance is an alternative to discrete decoupling capacitors for reducing power bus noise. This method takes advantage of the natural capacitance between solid power and return planes. In most PCB designs, this natural capacitance is too small to be effective. However, by minimizing the distance between the two solid planes and filling this space with a material that has high relative permittivity, the board capacitance can be highly enhanced [6].

With closely spaced power-return plane pairs for power distribution, embedded capacitance boards can achieve very low power bus impedance over a wide frequency range. The impedance associated with active devices mounted on the board surface tends to be much higher than the power bus impedance. Therefore, most active devices can be modeled as current sources. Regardless of the technique used to determine the source current, the key to reducing the power bus noise voltage is minimizing the power bus impedance at all frequencies of interest. A suitable power bus design is desirable for SI and EMC purposes.

To evaluate the power bus design and develop design guidelines, a suitable modeling tool is beneficial. Many studies have focused on modeling the power and ground metal layers of the PCB in order to determine the power bus impedance at a specific location. Herein, some modeling methods were studied and tried to develop a suitable tool for the DIMM DC power distribution analysis and design in this paper.

Some difficulties met in evaluating power distribution design on the DIMM board are discussed in Section II. Based on the difficulties discussed, several solution methods were studied and given in the following sections. A cavity

model with segmentation method to model a power bus with an irregular shape is given in Section III. The PEEC method to evaluate the parasitic inductance parameters of vias is presented in Section IV. The validity of both approaches is demonstrated experimentally, as well as comparing modeling with the measurements. Finally, the proposed modeling methods for DIMM power bus design are summarized in Section V.

ISSUES FOR DC POWER BUS EVALUATION

For DC power bus design, several critical issues should be considered. They include stack-up of the power and ground planes, locations of SMT decoupling capacitors, numbers of SMT decoupling capacitors, and values of SMT decoupling capacitors, and so on. Maintaining closely spaced power and ground layers can minimize power bus noise and is commonly accepted in power bus design. Using the largest value of decoupling capacitor in a given package size is becoming a common design practice as well. But the critical design issues of locations and numbers of SMT decoupling capacitors are unresolved questions.

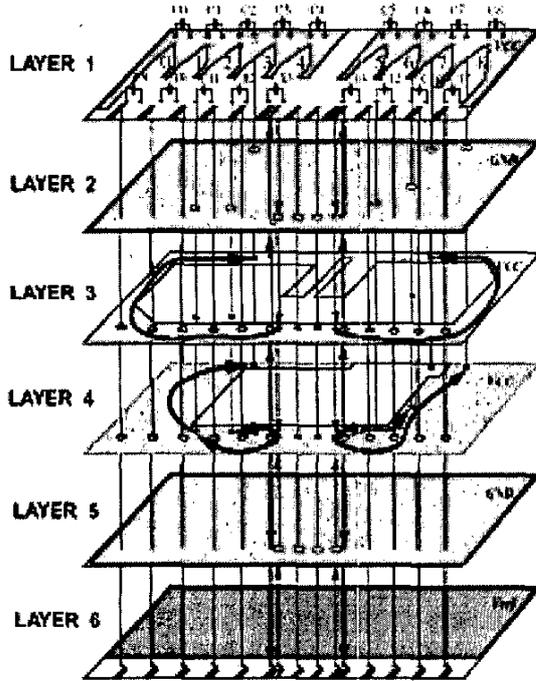


Figure 1. Memory DIMM power distribution diagram.

A power distribution design for a DIMM board is shown in Figure 1. From the figure, it is seen that two critical issues for the power bus modeling should be considered. One is the arbitrary shape of power bus, and the other is the SMT decoupling capacitors. Full-wave methods can be used to model the power/ground layer pair, including FEM, partial element equivalent circuit (PEEC), and finite difference time domain (FDTD). Full-wave modeling that includes

the vias and planes is necessary to adequately detail the effects that are necessary for quantifying the effect of an SMT decoupling capacitor. If all the details are included in the modeling, the time and memory consumption for computing are huge. Moreover, it is difficult to include SMT decoupling capacitors in the model for FDTD or FEM. In addition, an analytical method based on the cavity-mode theory has been applied for determining the impedance for the dc power bus parallel planes. Although SMT decoupling capacitors can be included as lumped circuit elements when extracting a network using the cavity theory, the effect of vias for SMT decoupling capacitors are not included in the modeling. To evaluate the DIMM power bus design, a suitable modeling method is necessary.

CAVITY MODEL WITH SEGMENTATION

Consider a plane structure, which consists of a rectangular power-return plane pair of dimensions $a \times b$, separated by a dielectric substrate of thickness d and permittivity ϵ . Since embedded capacitance boards are electrically thin, they can be modeled as a 2-D TM_z cavity with two perfect electric conductor (PEC) walls representing the power and return planes. The sides of the rectangular board can be modeled with four perfect magnetic conductor (PMC) sidewalls. The feed port is modeled using a z-directed current source located at (x_i, y_i) with an electrically small rectangular cross section of size (dx_i, dy_i) . Thus, a rectangular DC power bus is actually a multi-port planar circuit and it can be modeled with an equivalent circuit, as shown in Figure 2 [7]. The circuit parameters can be derived as [8]

$$Z_{ij}(\omega) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/(j\omega L_{mn}) + j\omega C_0 + G_{mn}} \quad (1)$$

$$\omega_{mn} = \frac{1}{\sqrt{\epsilon\mu}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$$

$$L_{mn} = \frac{d}{\epsilon ab \omega_{mn}^2}$$

$$C_0 = \frac{ab\epsilon}{d}$$

$$G_{mn} = C_0 \omega_{mn} \left(\tan \delta + \frac{r}{d} \right)$$

$$r = \sqrt{\frac{2}{\omega\mu\sigma}}, \text{ (skin depth)}$$

$$N_{mni} = c_m c_n \cos\left(\frac{m\pi x_i}{a}\right) \cos\left(\frac{n\pi y_i}{b}\right) \sin c\left(\frac{m\pi W_{xi}}{2a}\right) \sin c\left(\frac{n\pi W_{yi}}{2b}\right),$$

where $c_m = 1$ if $m = 0$ and $c_m = \sqrt{2}$ if $m \neq 0$, and $c_n = 1$ if $n = 0$ and $c_n = \sqrt{2}$ if $n \neq 0$, and (x_i, y_i) is the location of the port; and W_{x_i} and W_{y_i} are the width of the port in x and y direction, respectively. Note that both the skin effect and the dielectric loss are taken into account.

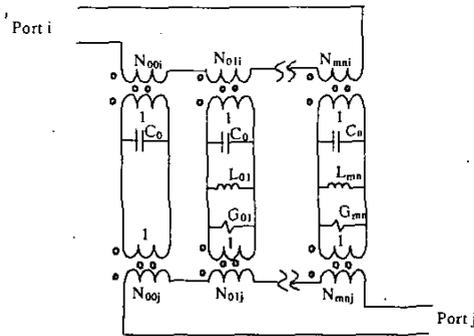


Figure 2. An equivalent circuit of a rectangular DC power bus.

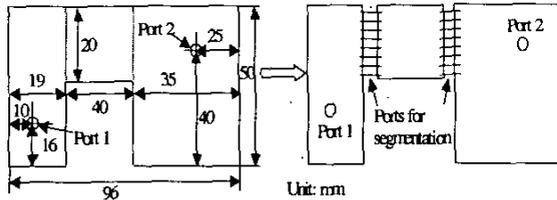


Figure 3. An irregular shaped DC power bus.

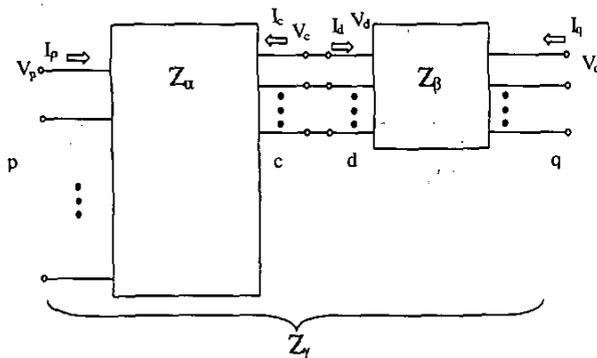


Figure 4. Planar circuits analyzed using the segmentation method.

The planar circuit model is also applicable to a power-bus with irregular shape, which can be divided into regular shapes (segmentation method) [9], [10], or can be converted to regular shapes by adding one or more regular shaped segments to them [11]. Figure 3 shows an example of a DC power-bus of irregular shape. The shape of the power bus is a rectangular power bus with a rectangular cutout. For the planar circuit model, it was divided into

three small pieces of rectangular shape. The impedance of each section was modeled using the planar circuit model separately. Then the impedance for the complete board was calculated using the segmentation method.

The theoretical formulations for the segmentation method are given below. A circuit is shown in Figure 4. As in the segmentation method, the continuous interconnection between α - and β -segments is replaced by a discrete number of interconnected ports, named c -ports on the α -segment and d -ports on the β -segment. Ports p and q are the external (unconnected) ports of the α - and β -segments, respectively.

The Z -matrices for α -, β -, and γ -segments, namely \tilde{Z}_α , \tilde{Z}_β , and \tilde{Z}_γ , respectively, can be partitioned into submatrices corresponding to the external (unconnected) and connected ports as follows:

$$\tilde{Z}_\alpha = \begin{bmatrix} \tilde{Z}_{pp\alpha} & \tilde{Z}_{pc} \\ \tilde{Z}_{cp} & \tilde{Z}_{cc} \end{bmatrix} \quad (2)$$

$$\tilde{Z}_\beta = \begin{bmatrix} \tilde{Z}_{dd} & \tilde{Z}_{dq} \\ \tilde{Z}_{qd} & \tilde{Z}_{qq\beta} \end{bmatrix} \quad (3)$$

$$\tilde{Z}_\gamma = \begin{bmatrix} \tilde{Z}_{pp\gamma} & \tilde{Z}_{pq} \\ \tilde{Z}_{qp} & \tilde{Z}_{qq\gamma} \end{bmatrix} \quad (4)$$

Since the c -ports are connected to the respective d -ports

$$V_c = V_d \quad I_c = -I_d \quad (6)$$

If \tilde{Z}_α and \tilde{Z}_β are known, \tilde{Z}_γ can be computed using the segmentation method. The impedance matrix \tilde{Z}_γ can thus be obtained, by using (2), (3), and (6), is given by

$$\tilde{Z}_\gamma = \begin{bmatrix} \tilde{Z}_{pp\alpha} - \tilde{Z}_{pc} \tilde{Z}_{dq}^{-1} \tilde{Z}_{cp} & \tilde{Z}_{pc} \tilde{Z}_{dq}^{-1} \tilde{Z}_{dq} \\ \tilde{Z}_{qd} \tilde{Z}_{dq}^{-1} \tilde{Z}_{cp} & \tilde{Z}_{qq\beta} - \tilde{Z}_{qd} \tilde{Z}_{dq}^{-1} \tilde{Z}_{dq} \end{bmatrix} \quad (7)$$

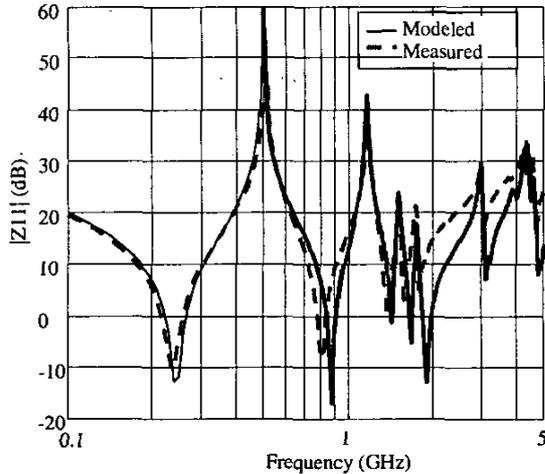
where

$$\tilde{Z}_{dp} = [\tilde{Z}_{cc} + \tilde{Z}_{dd}]^{-1} \tilde{Z}_{cp}$$

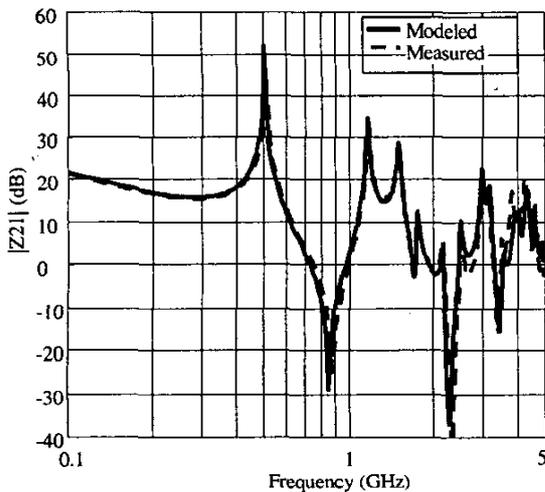
$$\tilde{Z}_{dq} = [\tilde{Z}_{cc} + \tilde{Z}_{dd}]^{-1} \tilde{Z}_{dq}$$

To verify the modeled results, a double-sided PCB was built, as shown in Figure 3. The thickness of the dielectric was 40 mm, $\epsilon_r = 4.3$, and the loss tangent was 0.02. Two SMA jacks were soldered on the board to measure the S-

parameters, which were converted to Z-parameters. The modeled results and the measured results were shown in Figure 5. Comparing them to the results from the measurements, the modeled results agree well with the measured results at lower frequencies, however, there are some discrepancies at higher frequencies. The discrepancies are due to an insufficient of modes calculated in the cavity model. It should be noted that the simulation time of the planar circuit model is much faster than other modeling methods.



(a)



(b)

Figure 5. Z-parameters of the DC power bus with irregular shape. (a). $|Z_{11}|$ and (b). $|Z_{21}|$.

PARASITIC INDUCTANCE OF VIA BETWEEN PLANES

An important component of the power distribution is decoupling capacitors, whose presence alters the impedance. If the location of a decoupling capacitor is assumed as a port, then decoupling capacitors can be incorporated into the plane solution. The impedance of the capacitor includes its parasitic inductance and resistance, and the parasitic inductance of the capacitor connection to the plane. The parasitic inductance and resistance of a decoupling capacitor can be derived from measurement. To estimate the parasitic inductance of the capacitor connection to the plane, a suitable modeling method is necessary.

Ruehli developed a concept called *self partial inductance* [12]. It is defined for a given segment of a loop independent of the location or orientation of any other loop segment. Given a thin straight conductor segment as shown in Figure 6, the segment on one side and infinity on the other side can bound a nominal rectangular loop. Two lines perpendicular to the segment and extending from the ends of the segment to infinity form the other two sides of the loop. Based on Stokes' theorem, it can be shown that the integration over the loop reduces to integration over the conductor segment. The self partial inductance is the ratio of the net flux passing through this loop to the current on the conductor segment, and can be evaluated as,

$$L_{p_i} = \frac{\mu}{4\pi} \frac{1}{a_i a_i} \int_{a_i} \int_{a_i} \int_0^{l_i} \frac{d\vec{l}_i \cdot d\vec{l}_i}{r_{ii}} da_i da_i \quad (8)$$

where the area a_i is the conductor cross section perpendicular to the current flow, and the length l_i is the length of the conductor segment.

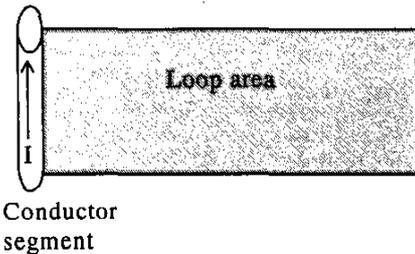


Figure 6. Loop area to define self partial inductance.

Based on the concept of self partial inductance, the parasitic inductance associated with the via between the power and ground planes can be evaluated. Then it can be incorporated into the cavity model solutions.

To validate this approach, a rectangular test board was built, as shown in Figure 7. The test board was a 2-layer board, with dimensions of 152 mm X 90 mm. The dielectric constant of substrate was 2.94, and the loss tangent of material was 0.00119. The thickness of the dielectric is 1.5

mm (60 mils). One test port and one shorted via were mounted on the board. The location of the test port was (122, 60) (unit:mm), and the location of the shorting via was (30, 30) (unit:mm). The width of the port was 1.2 mm, and the width of the via was 1 mm. The modeling procedure is shown in Figure 7 also. Firstly, the parasitic inductances associated with the shorting via and the test port were estimated using the PEEC method. The evaluated parasitic inductance associated with the shorting via was 0.36 nH, and the evaluated parasitic inductance associated with the shorting via was 0.33 nH. These inductances were then incorporated into the cavity model to simulate the solutions.

The simulated results with the estimated inductance of via are shown in Figure 8, and compared with the measured results. To illustrate the necessity of including the parasitic inductance of the via clearly, the simulated results without the estimated inductance of the via are plotted as well. For the simulated results with the estimated inductance, the agreement is good in the entire frequency range of interest (from 100 MHz to 5 GHz). By contrast, for the simulated results without the estimated inductance, the resonance frequencies are shifted to the right. The results demonstrate the utility of the approach.

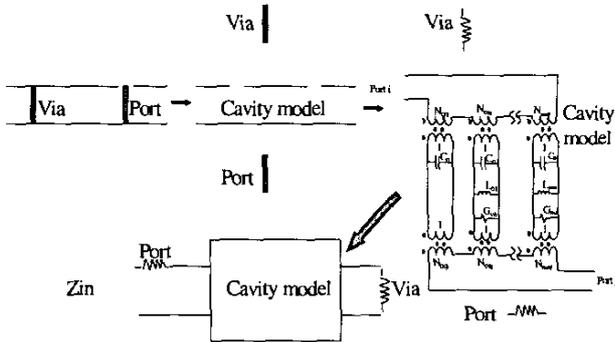


Figure 7. Modeling approach for the test board.

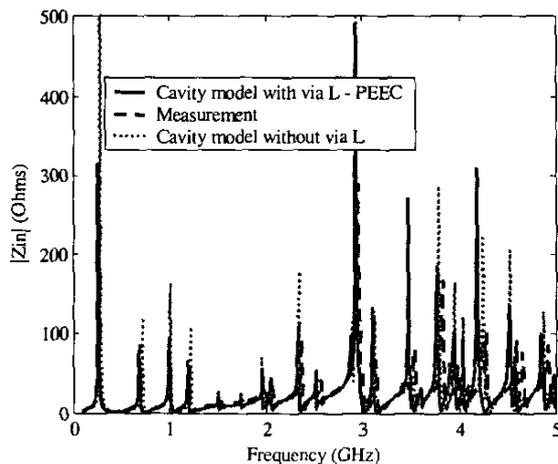


Figure 8. Modeled results with parasitic inductance of via.

CONCLUSIONS

A methodology for plane modeling suitable for DIMM boards has been discussed in this paper. The method described includes modeling for a power bus with irregular shape, and parasitic inductance of the vias between a plane pair. Since the impedance matrix is computed based on analytical equations, ports can be placed at arbitrary locations on a plane and the computation of the frequency response is efficient. The segmentation method allows modeling of the power bus with an irregular shape using the cavity model. A method was demonstrated for evaluating parasitic inductance of a via between planes. Equivalent circuits for ports on plane pairs enable decoupling capacitors and parasitic elements to be incorporated into cavity modeling solutions.

The methods discussed were verified using measured data and simulated data. All simulations showed good agreement with measured data.

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