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Minsu Choi

Missouri University of Science and Technology, choim@mst.edu

Nohpill Park

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# Locally Synchronous, Globally Asynchronous Design for Quantum-Dot Cellular Automata (LSGA QCA)

Minsu Choi<sup>1</sup> and Nohpill Park<sup>2</sup>

<sup>1</sup> Dept of ECE, University of Missouri-Rolla, Rolla, MO 65409-0040, USA  
choim@umr.edu

<sup>2</sup> Dept of CS, Oklahoma State University, Stillwater, OK 74078, USA  
npark@cs.okstate.edu

**Abstract**— The concept of clocking for QCA, referred to as the four-phase clocking, is widely used. However, inherited characteristics of QCA, such as the way to hold state, the way to synchronize data flows, and the way to power QCA cells, make the design of QCA circuits quite different from VLSI and introduce a variety of new design challenges and the most severe challenges are due to the fact that the overall timing of a QCA circuit is mainly dependent upon its layout. This fact is commonly referred to as the "layout=timing" problem. To circumvent the problem, a novel self-timed circuit design technique referred to as the Locally Synchronous, Globally Asynchronous Design for QCA is proposed in this paper. The proposed technique can significantly reduce the layout-timing dependency from the global network of QCA devices in a circuit; therefore, considerably flexible QCA circuit design will be possible.

## I. INTRODUCTION

QCA (Quantum-Dot Cellular Automata) is one of the six promising technologies for nano-scale computing listed in the International Technology Roadmap for Semiconductors (ITRS) 2004 [1]. In the QCA paradigm, a regular array of cells, each interacting with its neighboring cells, is employed in a locally interconnected architecture [2], [3], [4]. The coupling between the cells is given by their electrostatic interactions. Such arrays are in principle capable of encoding digital information. The fundamental unit of QCA is the QCA cell created with four quantum-dots positioned at the vertices of a square. The cell is loaded with two extra electrons which tend to occupy the diagonals due to electrostatic repulsion. Binary information is encoded in the two possible polarizations (i.e., +1 or -1). The cell will switch from one polarization to the other when the electrons quantum-mechanically tunnel from one set of dots to the other [5]. Implementing QCA cells with single molecules is a new area with considerable promise. It is anticipated that molecular QCA architectures could operate at densities over  $10^{12}$  devices/cm<sup>2</sup> and THz frequency domain [6], [7].

It is possible to strategically allocate the number of

QCA cells to build logic devices. The most popular QCA devices include MV (i.e., Majority Voter,  $F(A, B, C) = AB + AC + BC$ ), INV (i.e., Inverter,  $F(A) = \bar{A}$ ) and binary wire. Clocking is important in most computational technologies and a requirement for the synchronization of information flow in QCA. Presently, all QCA circuit proposals require a clock not only to synchronize and control information flow but the clock actually provides the power to run the circuit [6], [8]. The cells are not powered from any other external source apart from the clock. Therefore it is difficult to imagine a QCA circuit that can avoid using a clock.

The concept of clocking for QCA is referred to as the four-phase clocking [9], [10], [11], [12], [13]. Four-phase clocking signal applied to four adjacent buried wires. Each wire has a voltage that raises and lowers linearly in order to adiabatically switch the QCA cells placed above it. Adjacent wires have a  $\pi/2$  phase shift so that every fourth wire has an identical signal. This method will induce a roughly sinusoidal clocking field that propagates along the QCA surface.

When the clock signal is high the potential barriers between the dots are low and the electrons effectively spread out in the cell and no net polarization exists; i.e.  $P=0$ . As the clock signal is switched low, the potential barriers between the dots are raised high and the electrons are localized such that a polarization is developed based on the interaction of their neighbors; i.e. they take on the polarization of their neighbors. Basically clock high means cell is unlatched, clock low means cell is latched. So, the four-phase clocking scheme emulates classical shift register behavior since a binary digit of information can be stored in each cell's latched polarization [10], [11], [14].

## II. "LAYOUT=TIMING" PROBLEM

With the four-phase clocking scheme, it is possible to design QCA circuits while ensuring each QCA cell is powered and the information is processed and forwarded in

timely manner. However, inherited characteristics of QCA, such as the way to hold state, the way to synchronize data flows, and the way to power QCA cells, make the design of QCA circuits quite different from VLSI and introduce a variety of new design challenges and the most severe challenges are due to the fact that the overall timing of a QCA circuit is mainly dependent upon its layout. This fact is commonly referred to as the **"layout=timing" problem** [13], [15]. According to the four-phase clocking scheme, QCA cells placed in one clocking zone require one complete clock cycle to receive data from the previous clocking zone and forward data to the following clocking zone. So, the overall time delay required to forward data through a QCA wire spanning over a number of clocking zones can be calculated by  $t_d = n_z/f$ , where  $t_d$  is the time delay,  $n_z$  is the number of clocking zones and  $f$  is the clock frequency. For example, let us consider a QCA gate with two input wires. If these two inputs do not come through the same number of clocking zones, one of the inputs could be arrived at the gate before the other one arrives. As a result, erroneous output will result due to the race condition. Figure 1 depicts the circuit  $F = (A + B)C$ . The inputs appear in clocking zone 0. The OR must be computed in clocking zone 1 or later, and, as both the result of the OR and the primary input C are required before the AND can be computed, a buffer (indicated by the gray dot) must be inserted into clocking zone 1 for signal C. Although this example is trivial, it depicts the fundamental layout and timing problem for QCA circuits. Also, it is tricky to feedback data in QCA, since another chain of clocking zones that are arranged in opposite direction (i.e., descending order) is needed. To address the various layout-induced design challenges, considerable research efforts have been done in the field of architecture and design automation of QCA [15], [16]. The QCA physical design procedure consists of the following three steps [15]:

- **Partitioning:** The first design step is to partition the given QCA circuit so that they can be placed in to corresponding clocking zones to fulfill the timing constraints. Certain level of Regularity of the clocking zones should be maintained so that the buried clocking wire can be uniformly distributed with ease.
- **Placement:** In QCA circuit, wire crossings should be minimized, since either a large circuit to exchange the position of two signals, or a 45 degree change in the cell orientation should be done and these are expensive in terms of manufacturing.
- **Routing:** The step is to design the optimal wire routing to realize the given QCA circuit with minimal design overhead.

These three steps are not independent each other; rather they trade off each other. If more clocking zones are

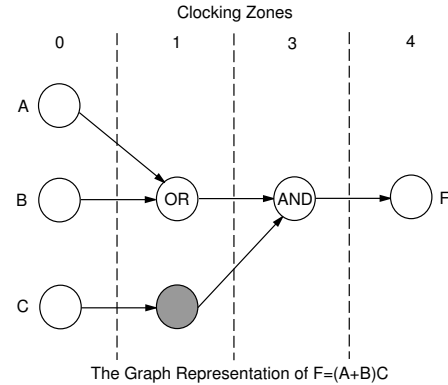


Fig. 1. Example Circuit with Clocking Zones (adopted from [15]).

provided, it will be much easier to make all the signals arrive their destinations in timely manner. Meanwhile, considering the pipeline nature of a QCA circuit, the latency of the circuit will increase [13], [15], [17]. If we try to make a good placement which means to minimize the number of crossing, we will have more difficult routing job to do and may need larger space to route the wires. In addition, if we try to make the clocking zones to have uniform width and height, we will lose some flexibility for the placement, too.

Kogge et al., have identified numerous challenges with designing QCA circuits due to the "layout=timing" problem as follows [13]:

- **Wire Length:** As wire length grows, the probability that a QCA cell will switch successfully decreases in proportion to the distance. Also, wire length determines the clock rate because every cell within the clocking zone must make appropriate polarization changes before a given zone can change phase. Thus, the length of a wire within a given clocking zone should be minimized.
- **Clocking Zone Width:** Clocking zone widths should be also minimized so that wire lengths can be minimized and uniformed to increase the manufacturability of the circuit.
- **Number of QCA cells per Clocking Zone:** If too many cells are included in a single clocking zone, the clock rate could deteriorate, simply because the time for all cells make required transitions will most likely increase.
- **Lack of Feedback:** 4-phase clocking scheme flows data in one direction. Physical feedback is essential in designing sequential circuits. Inclusion of feedback loops in QCA designs may result in complex clocking zone structure and floorplanning.
- **Wasted Area:** QCA circuits with 4-phase clocking are not very space efficient. There are simply too many

design constraints due to the "layout=timing" problem to pack everything within the given area. Also, inclusion of buffer cells in the design to synchronize data flow increases wasted area.

They also proposed various design methods to cope with the problems. QCA inherently lends itself to such a "trapezoidal clocking" structure in which there are an initial  $n$  inputs and after a certain number of  $m$  clocking zones, only an output remains. It is possible to stack another trapezoid with opposite data flow to make feedback possible. By allowing data to flow in two directions and by carefully fitting trapezoids together, denser and compact QCA circuits could be generated. Also, clocking zones can be arranged or tiled so that there are multiple wire loops and wire crossings to allow feedback and routing. The universal clocking floorplan is a standardized clocking zone structure in which various functions can be implemented to allow feedback and routing.

### III. LOCALLY SYNCHRONOUS, GLOBALLY ASYNCHRONOUS DESIGN

Unlike the previous approaches, the proposed methodology is to completely eliminate such "layout=timing" constraints from the global network of QCA gates in a circuit. The key idea is to introduce delay-insensitive data encoding scheme such as NCL (Null Convention Logic) [18] to the circuit-level to eliminate the global layout=timing problem, while preserving the 4-phase clocking scheme for individual gates. Since each gate is locally synchronized by corresponding clocking zone(s), appropriate data forwarding and synchronization are guaranteed at the gate-level and the QCA cells within the gate can be properly powered, as well. As a result, the fundamental "layout=timing" problem for QCA circuits can be completely removed, since the overall layout of the circuit is no more the determinant factor of the global timing.

Among various delay-insensitive data encoding schemes, NCL is suitable for clockless circuit design [18]. So, NCL-based circuit design methodology for delay-insensitive QCA will be extensively researched in the proposed project. NCL circuits switch between a logic based data representation of DATA and a control representation of NULL. This separation between control and data representations provides a self-synchronization throughout the design. Therefore, no global synchronization is needed. Threshold gates provide the basic building block of NCL designs. Threshold gate inputs and outputs can be in one of two states, DATA or NULL. A threshold gate starting with its output in a NULL state will remain in the NULL state until the specified number of inputs are placed in the DATA state. Once the gate reaches the DATA state, it remains in this state until all of the inputs return to the NULL state. The hysteresis in the threshold gate provides the threshold

needed to keep from switching during the intermediate state when the number of inputs in the DATA state is greater than zero, but less than the threshold limit. In addition, hysteresis provides the storage to remain at DATA until all of the inputs have returned to NULL. Since these gates use two values, as traditional Boolean logic does, they can be constructed with traditional digital logic design processes.

In order to demonstrate the feasibility to design a NCL gate with QCA cells, while preserving 4-phase clocking for the gate itself, a TH23 gate (2 out of 3 threshold gate with hysteresis behavior) has been designed using QCADesigner V1.4.1<sup>1</sup> and shown in Figure 2. Note that TH23 gate is equivalent to a sequential Boolean function  $F_{t+1} = (A + B + C)F_t + AB + BC + AC$  and the shown QCA gate design is direct implementation of it (without any logic, cell-count or space optimization), in which five MV gates and one feedback loop are used. Notably, the local network of QCA cells within the gate is fully synchronized and powered by 4-phase clocking scheme, but the gate itself is delay-insensitive, since it has hysteresis behavior. It would be possible to design delay-insensitive QCA circuits using NCL gates.

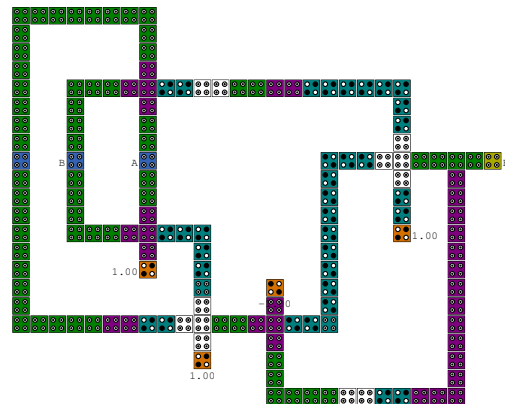


Fig. 2. TH23 QCA Gate (i.e., 2 out of 3 threshold gate with hysteresis). Designed by Hand.

The proposed novel QCA-specific delay-insensitive design approach is referred to as the "Locally Synchronous, Globally Asynchronous QCA (LSGA QCA)". The following advantages are expected from the proposed LSGA QCA architecture over the previously proposed methods:

- *Easier global floorplanning:* The proposed LSGA QCA completely remove the delay-sensitivity from the global QCA circuit. Much easier global floorplanning can be possible.
- *Increased density:* It can be used to minimize unused and wasted spaces from QCA circuit layout. So, much

<sup>1</sup>QCADesigner is a QCA design tool developed by the University of Calgary ATIPS Laboratory.

- more dense and compact floor planning is possible.
- *Reduced number of clocking zones and increased circuit speed:* The total number of clocking zones can be significantly reduced, since there is no need to synchronize dataflows by inserting additional clocking zones. So, much faster circuit operation is possible.
- *Decreased cell count:* There is no need to include additional cells for synchronization purposes, too. So, much less overall cell count can be achieved.
- *Reduced circuit complexity:* The overall circuit design complexity can be also significantly relaxed, since the overall timing is not dependent upon the layout, anymore. So, efficient design automation will be much easier.
- *Defect and fault-tolerance:* All failure modes due to layout=timing problem are eliminated. Also, testing complexity is reduced in that stuck-at-1 faults simply halt the circuit, since threshold gates cannot change their outputs back to NULL. Only stuck-at-0 faults and transient faults need to be exercised with applied patterns. Design time and risk as well as circuit testing requirements are expected to be decreased because of the elimination of the complexity of the clock with its critical timing issues.

For example, a full adder circuit, where  $X$  and  $Y$  denote the input addends and  $C_i$  denotes the carry input,  $S$  and  $C_o$  denote the sum and carry output, respectively, can be designed and optimized by NCL [19]. The optimized full adder design is shown in Figure 3. When implemented in QCA, two TH23 gates and two TH34W2 gates can be located anywhere in the given area and the corresponding interconnects and fan-ins and fan-outs can be also freely placed since the global timing dependency is fully removed. This delay-insensitivity of the proposed LSGA QCA is the primary advantage over the conventional synchronous QCA.

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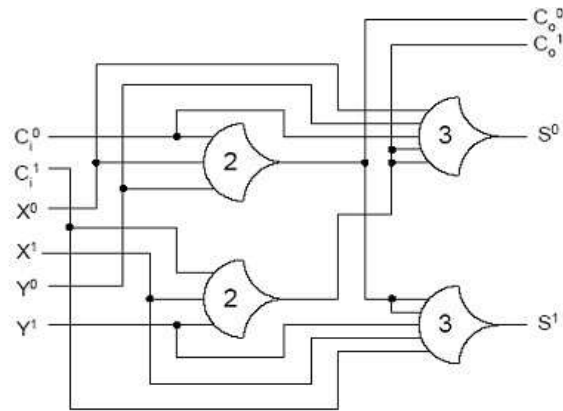


Fig. 3. Dual-rail full adder design [19]. Two TH23 and two TH34W2 gates are used. Since the design is delay-insensitive - in other words, placement-insensitive when implemented in QCA - these gates, fanins and fanouts can be located anywhere in the give area.

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