

01 Aug 1997

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### Recommended Citation

S. Radu et al., "Identifying an EMI Source and Coupling Path in a Computer System with Sub-Module Testing," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (1997, Austin, TX)*, pp. 165-170, Institute of Electrical and Electronics Engineers (IEEE), Aug 1997.

The definitive version is available at <https://doi.org/10.1109/ISEMC.1997.667562>

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# Identifying an EMI Source and Coupling Path in a Computer System with Sub-Module Testing

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**Abstract:** EMI in a workstation server resulting from CPU clock harmonics was investigated. Mechanisms by which noise is coupled off the CPU PCB module were diagnosed from studies and measurements on the CPU PCB alone. A model was then developed. Modifications were made and tested in the fully functional system to support the model.

## I. INTRODUCTION

EMI investigations in a fully functional and operating computer system are often approached in an *ad hoc* fashion relying upon trial-and-error, previous experience, and intuition. However, as clock frequencies and edge rates increase, and low order harmonics exceed 1 GHz, new noise mechanisms and coupling paths can exceed previous experience. EMI in a Sun S-1000<sup>1</sup> server was investigated in this study. The primary contributor to radiated EMI above 1 GHz is CPU harmonics. The CPU is located on a separate daughter card that plugs into the motherboard. Introducing modifications and testing the fully functional system can be time-consuming, and often result in EMI retrofits based on a partial understanding of the problem. Testing at the submodule level by contrast can be done more quickly, modifications that may not be possible in the fully functional system can be made, and more complete models upon which to gain an understanding of the noise process and base design changes can be developed. This paper details a procedure for ascertaining the mechanism and coupling path through which energy at CPU harmonics gets off the PCB sub-module and couples to EMI antennas. The EMI antennas were determined, and models for the noise process developed.

<sup>1</sup>Sun and S-1000 are registered trademarks of Sun Microsystems Computer Company.

## II. NOISE COUPLING PATHS OFF THE CPU PCB

The geometric aspects of the S-1000 system most relevant to the EMI process are shown in Figure 1. The S-1000

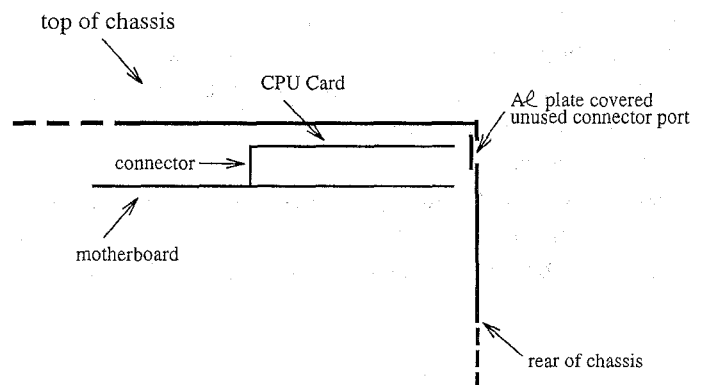


Figure 1. S-1000 geometry relevant to the radiated EMI problem.

accommodates up to four motherboards, and testing was done with an active motherboard in the upper slot with a single CPU PCB. The processor and cache controller on the CPU PCB are both covered by a single large heatsink that spans nearly the dimensions of the CPU board. The CPU PCB on the motherboard is located in proximity to the conducting chassis (shielding enclosure). In addition, the CPU PCB sits directly in front of a conducting, plate-covered unused connector aperture (connector not mounted). Through a process of selective shielding, with no cables other than the power cord attached, the plate covered aperture was identified as a significant EMI slot antenna. The contact of the plate to the chassis was inadequate at high frequencies to effectively "seal" the un-

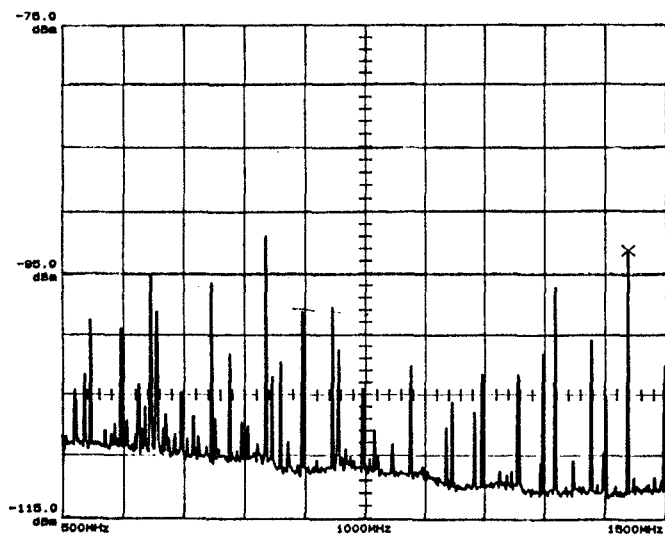


Figure 2. Radiated EMI measurements for the S-1000 system in the original configuration (500 – 1500 MHz, -75 → -115 dBm).

used aperture.

The radiated EMI measured in a shielded room for the S-1000 in the described original configuration is shown in Figure 2. Above 1 GHz the EMI is dominated by 60 MHz harmonics from the CPU. The narrowband nature of the spectrum indicates that the source and coupling path are related to either clock lines or power bus switching noise. A coupling path that included data lines might be expected to result in broadband “filling” in the spectrum between the distinct 60 MHz harmonic spikes. Consequently, only power and ground leads were used throughout the sub-module testing.

The CPU PCB is a 12-layer board with a processor and a cache controller, eight cache memory ICs, an oscillator, and a buffer for driving the clock lines to the processors and memory. Since no intentional 60 MHz comes off the CPU board, and the EMI is not expected to be related to data lines, the CPU PCB alone was tested only with 1 m power and ground leads attached, and powered with 5 V power from a laboratory bench supply. Radiated EMI measurements were made for this configuration (CPU PCB alone) and several different modifications to the CPU PCB geometry. This configuration differs cosmetically from the module in the chassis, and functionally in that the software was not running. The extended ground that provides the “other half of the EMI antenna” or coupling path in the system is the chassis, and in the test configuration is the ground in the power wires. While the lack of software running, and the difference in the other portion of the EMI antenna lead to different measured EMI results, the coupling paths and noise source mechanisms remain largely unchanged at the CPU PCB level. As a result, modifications and measurements were made on the CPU PCB

alone, and models developed for the noise source and coupling path at the board level.

Five models shown in Figure 3 were proposed for the dominant energy coupling path off the CPU board. These models were based on previously demonstrated fundamental mechanisms of radiation from PCBs with attached cables [1]. The source for model Model 1 is a noise voltage source that results from the RF noise on the power bus (switching noise). The source is differential, *viz.*, between two well defined conductor pairs, the noise “signal” and “return”. The arrows in the five models indicate the direction of the common-mode current on the attached power leads. The two dots on each of the leads denote the connector, and the portion of the figure to the left is associated with the CPU board, and the portion to the right, the power leads. In the sub-module testing, the two portions of the antenna are comprised of the power lead (5 V) and extended ground. Power and ground are never perfectly balanced, and can lead to common-mode current on the cable. Typically, on the power supply side, the extent of ground is considerably greater than the power lead, resulting in imbalance and an EMI antenna. For Model 1, the common-mode current is actually the difference of the currents shown on the power leads. The capacitor in dashed lines indicates the displacement current that completes the current path together with the common-mode current on the leads carried by conduction current. In the functioning S-1000, noise coupled off the CPU PCB by the path indicated in Model 1 would be conducted differentially off the board onto the power planes of the motherboard, and from there be conducted throughout the system, coupling to attached cables, exciting apertures, etc. to result in EMI. In this case, only the noise source is on the CPU PCB, but the antenna conductors are not.

Model 2 is very similar to Model 1 in that the noise source is a differential-mode noise voltage on the power planes as a result of device switching. One of the antenna conductors, however, is on the CPU PCB. In this case, signal return or ground are entire planes on the board, and form an effective other portion of the antenna. In the functioning S-1000 the other half of the antenna would be on the motherboard, but one part would be the ground plane on the CPU PCB. While the figure for Model 2 shows the 5 V power lead being driven against ground on the PCB, the antenna conductors could also be  $V_{cc}$  on the PCB driven against ground in the power leads.

The source proposed in Model 3 is a voltage that may be due to noise on the PCB or IC power planes, or a signal, any of which could capacitively couple to large metal structures on the CPU PCB that are not well grounded, and form an effective piece of an antenna. In this case, the heatsink was likely. The other portion of the antenna is the power leads that go off the board. Since power and ground are capacitively coupled over the board through

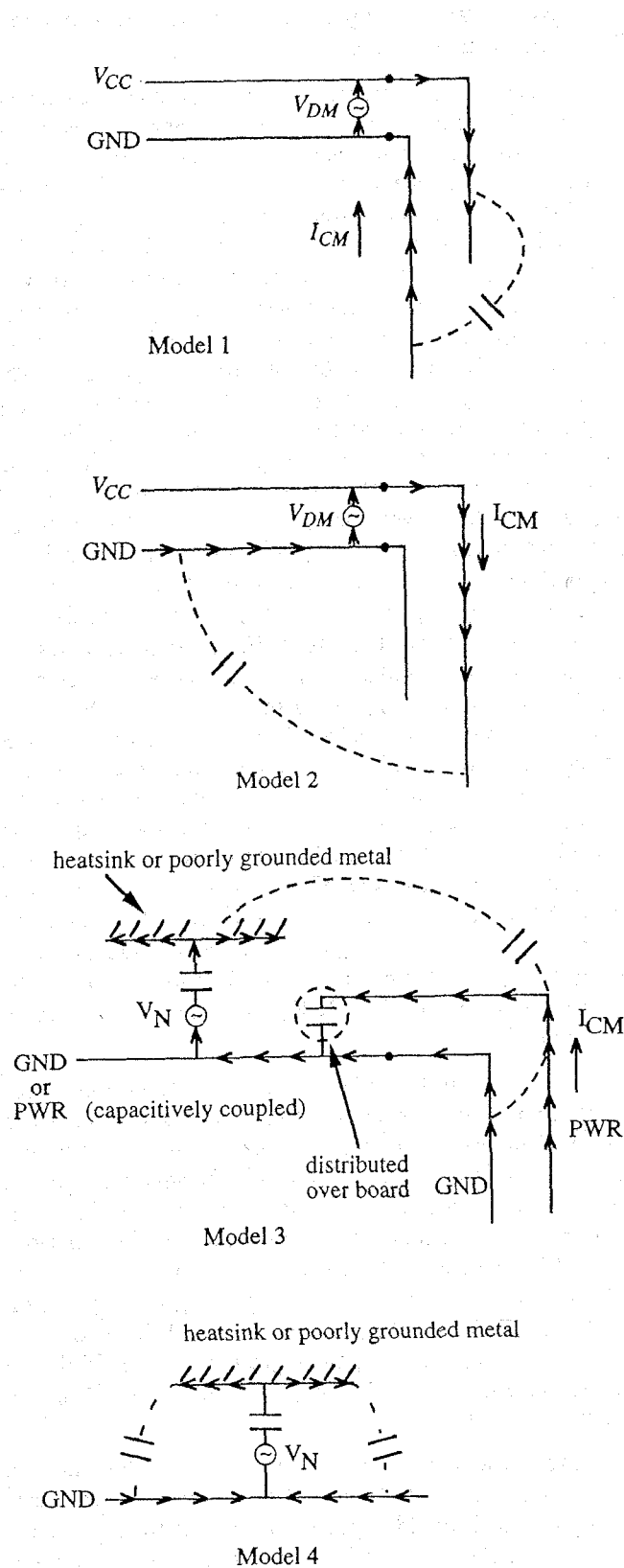


Figure 3. Models for proposed mechanisms by which noise was coupled off the CPU PCB.

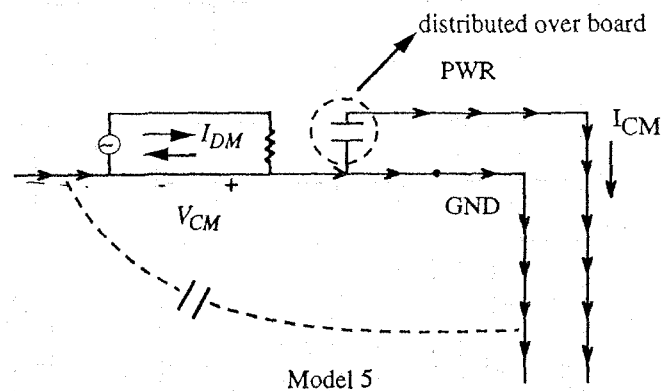


Figure 3. (Continued) Models for proposed mechanisms by which noise was coupled off the CPU PCB.

the closely spaced power planes, this half of the antenna could be ground, power, or both in the cable. A lumped capacitance at the connector denotes this capacitance. In the functioning S-1000, the displacement current path may be from the heatsink to the chassis, and then the current returns back to the mother board and CPU PCB.

Model 4 is nearly identical to Model 3, with the exception that the EMI antenna is entirely contained on the CPU board, e.g., the heatsink being driven against the GND plane. Distinguishing between Models 3 and 4 was not important, since modifications to minimize EMI resulting from them were the same.

Model 5 differs considerably from the previous four models in that the driving source for the noise is a differential-mode current as opposed to a differential-mode voltage. A differential-mode current returning through a finite impedance ground results in a potential difference between two portions of extended ground, denoted  $V_{CM}$  in Figure 3. The two portions of extended ground are then driven against each other by the potential difference [1]. The two parts of the antenna are pieces of ground, one on the CPU PCB, and the other the power/ground leads. While not specifically shown in the figure, the rearmost portion of ground (opposite the connector on the other side of the source) could conceivably capacitively couple to the heatsink.

Models 1-5 do not relate specific layout geometries and/or IC's on the CPU PCB, to the voltage or current sources and coupling path to the EMI antenna indicated in the models. Rather, the models distinguish between the antenna conductors, and the fundamental mechanism by which noise is coupled off the PCB to the EMI antenna(s). Once the mechanisms and coupling paths were determined from the sub-module testing, further, well-focused experiments could be designed to identify specific devices and coupling paths at the PCB level.

Several experiments were conducted to test the proposed models at the sub-module level and determine the noise coupling path off the CPU PCB. The specific modifications to the sub-module and experiments were:

- *Case A:* A shield constructed from copper tape was applied around the entire CPU PCB module. The shield was attached around the heatsink periphery, and was continued down and around the plastic connector where it terminated leaving the connector end open over its mouth. The shield then formed a type of open conducting bag enclosing the module. Care was taken to insure that the shield was insulated from the board.
- *Case B:* The same shield as for Case A was employed, except the shield was continued over the connector mouth to completely enclose the module. Small holes were cut for the power and ground leads. The two ground leads were then soldered to the shield and the holes soldered shut. The two power leads were decoupled with two 805 SMT 0.1  $\mu F$  capacitors from each lead to ground. The power and ground leads entered the shield within several millimeters of each other. The shield was complete, and this case served as a check to show that the noise coupled off the board could be all but eliminated.
- *Case C:* The completed shield, together with the decoupling from the power leads to the shield as described in the previous case was modified by cutting a 1/4" strip around the periphery of the portion of the shield surrounding the plastic connector. As a result, the shield encompassing the CPU PCB was isolated from the portion around the connector mouth. The portion of the shield around the connector mouth was retained to provide an effective filter for differential-mode noise at the connector. The geometry around the connector mouth provided a low-inductance path for the decoupling between the leads.
- *Case D:* The differential-mode filter detailed above for Case C was retained, but the shield covering the board was removed.
- *Case E:* Multiple ferrite sleeves were applied at the connector for the unmodified CPU PCB in the sub-module test. A specially made ferrite around the PCB connector was constructed from flat ferrite pieces for testing in the S-1000.
- *Case F:* The heatsink spanning the processor and cache controller was removed.

It was feasible to conduct some of the tests in the S-1000, and in those cases, the sub-module level testing was corroborated with the functioning S-1000 system.

The anticipated effect on the proposed models for the described modifications on radiated EMI experiments of the CPU PCB with attached power leads is tabulated in Table I. A *Y* indicates that the modification should lower the

radiation for the proposed model, and an *N* indicates that the modification will have no effect or potentially increase the radiation. A question mark indicates that the effect is dependent on the source location on the board, and the test gives no information. Case A should have no effect on Models 1 or 2 in which the noise source is a DM voltage between the power planes. At most, the shield will capacitively couple to the ground or power plane and become part of the antenna structure on the board. The radiation could be potentially worse if the new antenna had a lower impedance. The shield for Case A should lower the radiation from Models 3 and 4 by capacitively loading the source (with a new displacement current path). The effect of the shield on Model 5 is dictated by the effective location of the source  $V_{CM}$  on the board.

The complete shield and DM filter of Case B should decrease the radiation from all the proposed models. The unconnected shield DM filter for Case C should decrease the radiation from Models 1 and 2 because the DM noise voltage that appears at the connector is being loaded by the decoupling. The shield would affect Models 3, 4, and 5 in the same manner as the shield in Case A, improving Models 3 and 4, but having uncertain effects on Model 5. The DM filter (decoupling) would have no effect on Models 3, 4, and 5. The DM filter alone for Case D should affect Models 1 and 2 by loading the source, while having no effect on Models 3, 4, and 5.

A ferrite sleeve as in Case E should have no effect on Model 1, since the series loading is placed on the end of the effective antenna. It could potentially improve Model 2 depending on the effective source and antenna impedance. Similarly, a ferrite sleeve might improve Model 3. However, in this case the source impedance includes the capacitance between the noise voltage source and the other antenna conductor on the board, and a ferrite sleeve may not add sufficient series impedance. An improvement is not necessarily expected for Model 3, but could result. Since the antenna conductors for Model 4 are located on the board, a ferrite sleeve would not reduce the radiation in this case. A ferrite sleeve may reduce the radiation from Model 5 depending on the source and antenna impedance, and the effective location of the source on the board. Finally, a ferrite at 1 GHz may not provide significant series impedance relative to the antenna.

The modifications for Cases A - E were implemented on the CPU PCB and tested with the module alone, and in those cases that allowed, in the functioning S-1000 system as well. In addition, measurements were made on the module with and without the heatsink, denoted Case F. In the latter stages of the testing, when the CPU PCB was considered expendable, Case F was also conducted in the S-1000 chassis. Case F was pursued to determine the role of the heatsink in the coupling path to the slots in the S-1000 chassis. The results of the measurements are

TABLE I  
EFFECT OF CPU PCB MODIFICATIONS ON PROPOSED COUPLING PATHS

Model	Modifications				
	Case A: Shield only	Case B: Shield and filter (CM & DM)	Case C: Shield and DM filter	Case D: DM filter	Case E: ferrite sleeve
1	N	Y	Y	Y	N
2	N	Y	Y	Y	Y
3	Y	Y	Y	N	Y
4	Y	Y	Y	N	N
5	?	Y	?	N	Y

summarized in Table II. Multiple down arrows indicate improvements greater than 5–8 dB over several CPU harmonics. Fewer arrows indicate less improvement. Both up and down arrows indicate mixed results, i.e., an increase at some frequencies and a decrease at others over the entire frequency range. A dash indicates no discernible change, and an X indicates that the modification could not be made in the S-1000 system and no measurements were made. Only changes in excess of 5–8 dB over several harmonics are considered significant for the purposes of model development. The frequency span of the measurements was divided into three ranges, < 500 MHz, 500–1000 MHz, and > 1 GHz, denoted LOW, MEDIUM, and HIGH, respectively.

The experimental results in the HIGH frequency range suggest Models 3 or 4 for the noise coupling path off the CPU PCB. However, at this stage, the results eliminating Model 5 are not entirely conclusive. In either case, the results clearly indicate that the heatsink is part of the coupling path (or antenna in the sub-module tests). For the current-driven mechanism in Model 5, Figure 3 indicates that the portion of the antenna on the CPU PCB might be ground. However, the testing clearly indicates that if Model 5 is the source mechanism, the ground on the PCB must capacitively couple to the heatsink to form the antenna. There is a  $V_{CC}$  layer between ground and the heatsink, and Model 5 was eliminated based on this. The results of the test in the MEDIUM frequency range were in general mixed, with the exception of eliminating Models 1 and 2. These mixed results might be expected if the models in the LOW and HIGH ranges were indeed different.

### III. IC SOURCE AND COUPLING PATH ON THE PCB

Only the noise coupling paths off the CPU PCB have been determined at this stage, however, the noise sources and coupling paths to the EMI antennas at the board level have

not been related to specific layout geometries and components. Efforts were directed toward making these determinations only in the HIGH frequency range.

Testing with the CPU PCB alone was conducted to determine the specific layout attributes and components that comprised the EMI noise source and coupling path (to the EMI antennas) at the printed circuit level. Portions of the circuit were selectively disabled to discern which active components were the primary contributors to the EMI noise source. The significant active components on the CPU PCB were the processor and the cache controller, eight memory ICs, a clock buffer, and oscillator. The processors were powered separately from the clock oscillator buffer and memory through a 5 V DC/DC converter, and the processor 5 V planes are not connected to 5 V at the connector. Power to the processors could be disabled independently from the memory and buffer. Six outputs from the clock buffer were used to clock the memory and processors. Each processor was on a separate clock line, and the remaining four clock outputs were connected to two memory modules per output. All clock lines were run on a single layer that is sandwiched between entire planes in the interior of the board stackup, and were resistively terminated with each line having a 220  $\Omega$  resistor between line and  $V_{CC}$ , and 110  $\Omega$  between line and ground.

Several sequences of selectively disabling clocks and power to the active devices were pursued with similar results. Disabling the clocks to the memory and processors by lifting the clock output pins at the clock buffer IC had little effect on the radiated EMI from the CPU PCB. At this stage, only the clock buffer and oscillator were going through any activity, though the processors and memory were powered. The buffer was disconnected from the oscillator, and the radiated EMI was reduced by 30–40 dB. Consequently, the clock buffer was identified as the IC noise source. The heatsink for the processors also extended over the clock buffer, though it was not in contact, and had no functional

TABLE II  
SUMMARIZED RADIATED EMI RESULTS FOR THE MODIFICATIONS TO THE CPU PCB

Modifications	Frequency Range								
	LOW			MEDIUM			HIGH		
	S-1000	CPU	Models	S-1000	CPU	Models	S-1000	CPU	Models
Case A: shield only	↓	-	1, 2, 5 not 3 or 4	↑↓	↑↓	?	↓↓↓	↓↓↓	3, 4, 5 not 1 or 2
Case B: shield & filtered pwr & gnd (CM & DM)	×	↓↓↓	all	×	↓↓↓	all	×	↓↓↓	all
Case C: shield & DM filter pwr & gnd	×	↑↑	not 1 or 2	×	↑↑	not 1 or 2	×	↓↓↓	
Case D: DM filter	×		not 1 or 2	↓		not 1 or 2	×	-	not 1 or 2
Case E: ferrite sleeves	↓	↓↓	2, 3, 5	↓	-	?	↓↓	-	not 5 ?
Case F: remove heatsink	-	-		↓	↓		↓↓↓	↓↓↓	

purpose for the buffer. Two effective noise sources and coupling paths were proposed. First, capacitively coupling from significant conductor structures on the IC package to the heatsink. Second, capacitive coupling of switching noise on the  $V_{cc}$  plane (Layer 2) to the heatsink.

A third sequence of well-defined tests including adding a dielectric material between specific ICs and the heatsink, better high-frequency grounding of the heatsink, and a local shield over the buffer was proposed and conducted to verify the proposed paths, and to distinguish between them. The results clearly indicated that it was capacitive coupling from a conducting structure on the buffer IC package. While this may be surprising, given the small size of the package, approximately  $8\text{ mm} \times 13\text{ mm}$ , it was nonetheless the case. The clock buffer had a total of five ground pins, two on one side, three on the other. A shield that covered only the top of the buffer package was constructed simply by soldering an  $8\text{ mm} \times 13\text{ mm}$  rectangle of copper tape placed on top of the buffer to all five ground pins. The resulting measured radiated EMI in the S-1000 system shown in Figure 4, can be compared with that in Figure 2. The reduction of the  $60\text{ MHz}$  harmonics (frequency of the oscillator input to the buffer) in the HIGH frequency range is significant.

#### IV. SUMMARY AND CONCLUSION

A method for identifying an EMI noise source in a complex system using tests at the sub-module level has been presented. This approach can aid in developing more focused and well-defined testing than is sometimes possible at the system level to identify and model an effective noise source and coupling path.

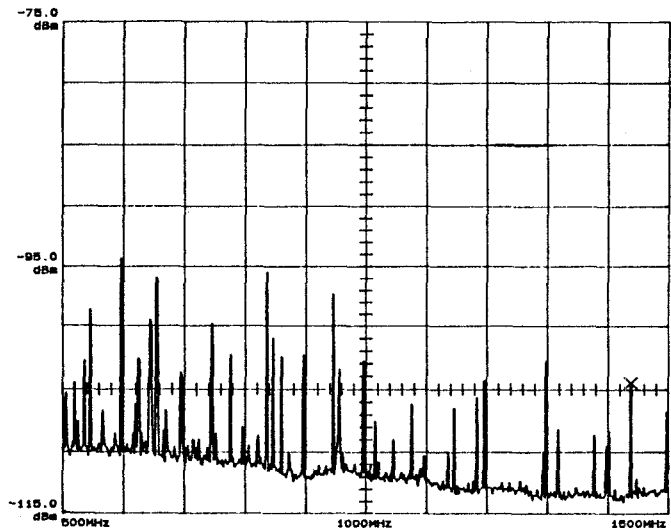


Figure 4. Radiated EMI measurements for the S-1000 system with the clock buffer shielded (500 - 1500 MHz, -75 → -115 dBm).

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