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Full Binary Combination Schema for Floating Voltage Source Multilevel Inverters

Xiaomin Kou, *Student Member, IEEE*, Keith A. Corzine, *Member, IEEE*, and Yakov L. Familiant, *Student Member, IEEE*

***Abstract*—This paper presents schema of operation for floating voltage source multilevel inverters. The primary advantage of the proposed schema is that the number of voltage levels (and thus power quality) can be increased for a given number of semiconductor devices when compared to the conventional "flying capacitor" topology. However, the new schema requires fixed floating sources instead of capacitors and therefore is more suitable for battery power applications such as electric vehicles, flexible ac transmission systems and submarine propulsion. Alternatively transformer/rectifier circuits may be used to supply the floating sources in a similar way to cascaded H-bridge inverters. Computer simulation results are presented for 4-level, 8-level, and 16-level inverter topologies. A 4-level laboratory test verifies the proposed method.**

***Index Terms*—Flying capacitor, multilevel inverters, pulse-width modulation, voltage-source.**

I. Introduction

POWER electronic dc/ac inverters are widely used in motor control systems. The harmonics generated on the ac side greatly influence the power quality of the control system. The multilevel inverter [1]–[20] improves the ac power quality by performing the power conversion in small voltage steps leading to lower harmonics. For this reason, researchers have done considerable work on multilevel inverters in recent years. The floating voltage source multilevel inverter topology, also known as the flying capacitor inverter [7]–[16], is one of the typical methods for reducing the harmonics by increasing the inverter levels. A new method, full binary combination scheme (FBCS), based on the floating source topology is described herein. With the same amount of power switches, FBCS can utilize all the possible switch combinations and generate a higher number of levels compared to the conventional floating source method.

II. The Conventional FS Multilevel Inverter

A. A. The Two-Cell FS Inverter Topology

The conventional floating source (FS) topology for a three-level inverter is shown in Fig. 1. In this topology, two voltage sources and four power switches (IGBTs) are used for each phase. This topology can also be called the two-cell FS topology, where each cell includes one voltage source and two complementary switches. The dc voltage ratio of the conventional two-cell inverter [7] is v_1: $v_2 = 1 : 2$. If $v_2 = E$, the relationship between the switching states and the line-to-ground voltage can be shown in Table I, where x represents phase a, phase b or phase c. From Table I it can be seen that the switches have four possible combinations while the line-to-ground voltage generated on ac side has only three possible values.

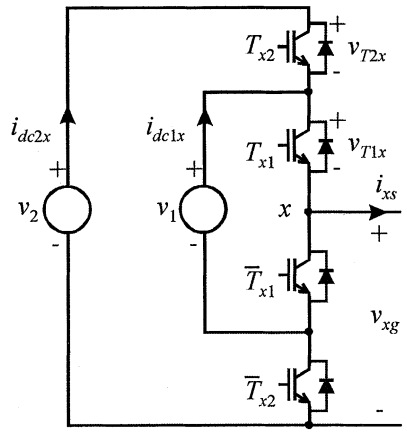

Fig. 1. Two-cell FS topology.

TABLE I
Traditional Two-Cell Inverter

Table I. Traditional two-cell inverter		
T_{x2}	T_{x1}	v_{xg}
0	0	0
0	1	$E/2$
1	0	E/2
1	1	E

B. The Three-Cell FS Inverter Topology

Using the topology shown in Fig. 2, a four-level inverter can be realized, if the dc voltage ratio of the traditional three-cell inverter is $v_1 : v_2 : v_3 = 1 : 2 : 3$. Assuming $v_3 = E$, the relationship between the switching states and the line-to-ground voltage is shown in Table II. Here, it can be seen that the three switches of each phase have $2^3 = 8$ possible combinations while the line-to-ground voltage v_{xg} generated on the ac side only has four possible values. This indicates an underutilization of switching states.

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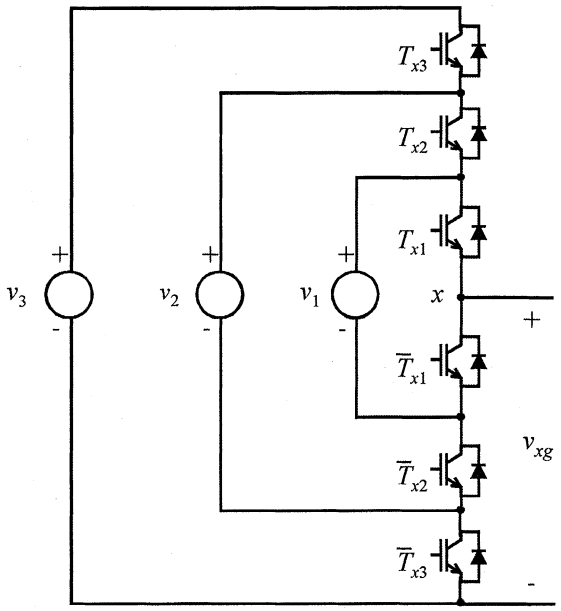

Fig. 2. Three-cell FS topology.

TABLE II
CONVENTIONAL THREE-CELL INVERTER

T_{x3}	T_{x2}	T_{x1}	v_{xg}
0	0	0	0
0	0	1	$E/3$
0	1	0	$E/3$
0	1	1	$2E/3$
1	0	0	$E/3$
1	0	1	$2E/3$
1	1	0	$2E/3$
1	1	1	$1.\ E$

C. The n-Cell FS Inverter Topology

Conventional FS inverters with other cell numbers can be studied when dc voltage sources are set to

$$v_i = \frac{i}{nc} E, \qquad (1 \le i \le nc) \tag{1}$$

where nc is the number of cells. The results are summarized in Table III where

ns number of switches;

sc number of switch combinations;

nl number of voltage levels.

Table III shows that each cell added increases inverter voltage levels by one. It can be seen that the conventional FS topology only uses part of the switching combinations, and $2^n - (n+1)$ switching combinations are not utilized (Fig. 3). Fig. 4 shows that with increasing nc, the unused switching combinations increase dramatically.

TABLE III
SUMMARY OF CONVENTIONAL FS TOPOLOGY ($nc > 1$)

Table III. Summary of conventional FS topology (nc>1)			
nc	ns	sc	nl
2	$2\times2=4$	$2^2=4$	3
3	$2\times3=6$	$2^3=8$	4
4	$2\times4=8$	$2^4=16$	5
.	.	.	.
.	.	.	.
n	$2n$	2^n	$n+1$

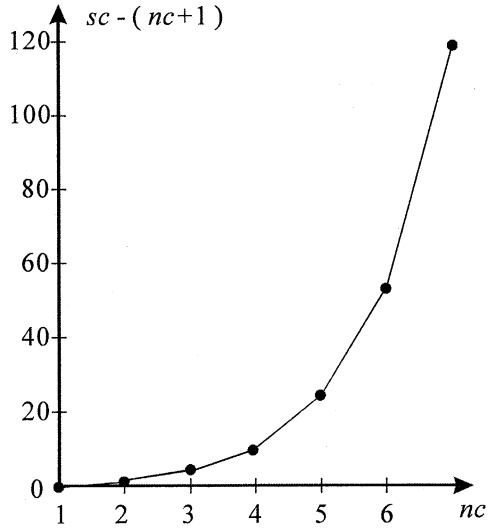

Fig. 3. Unused switch combinations in conventional FS inverter.

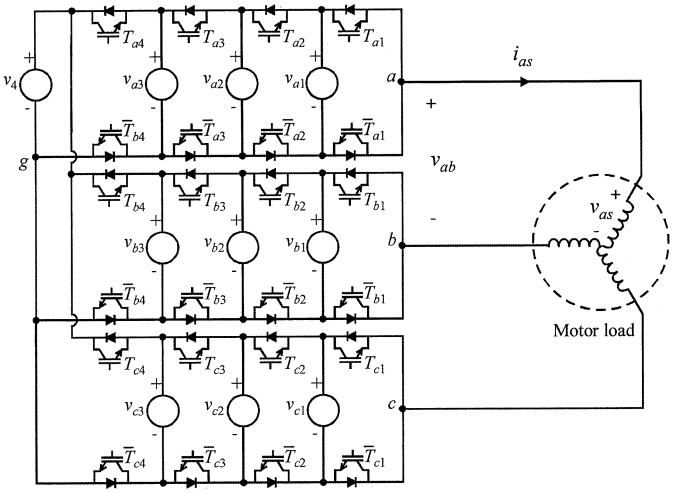

Fig. 4. Four-cell inverter topology.

III. FULL BINARY COMBINATION SCHEMA (FBCS)

A. A 4-Level Design for the Two-Cell Inverter

From Table I and Fig. 1, it can be seen that the circuit generates the same line-to-ground voltage for the "01" and "10" switching combinations. If a new design can refer "01" or "10" switching states to different voltages, a four-level inverter will result instead of a 3-level inverter. Table IV shows the results of a new design for a two-cell inverter by using the same topology

TABLE IV
TWO-CELL 4-LEVEL INVERTER

Table IV. Two-cell 4-level inverter		
T_{x2}	T_{x1}	v_{xg}
0	0	0
0	1	$E/3$
1	0	$2E/3$
1	1	E

TABLE V
THREE-CELL 8-LEVEL INVERTER

Table V. Three-cell 8-level inverter			
T_{x3}	T_{x2}	T_{x1}	v_{xg}
0	0	0	0
0	0	1	$E/7$
0	1	0	$2E/7$
0	1	1	$3E/7$
1	0	0	$4E/7$
1	0	1	$5E/7$
1	1	0	$6E/7$
1	1	1	E

shown in Fig. 1. Here the ratio $v_1 : v_2$ is changed from 1 : 2 to 1 : 3. From Table IV it can be seen that if a suitable ratio of v_1 and v_2 is chosen, all four switching combinations can be utilized, and a 4-level inverter can be created by using the same topology as Fig. 1.

B. An 8-Level Design for the Three-Cell Inverter

Table V shows the results of an 8-level inverter design using the same topology as Fig. 2. The voltage ratio $v_1 : v_2 : v_3$ is changed from 1 : 2 : 3 to 1 : 3 : 7. The relationship between switching states and v_{xg} is shown on Table V. From Table V it can be seen that if a suitable ratio of $v_1 : v_2 : v_3$ is chosen, all the eight switching combinations can be utilized and an 8-level inverter can be created by using the same topology as Fig. 2.

C. General Representation for FBCS

The previous sections have presented examples of how the switching states may be maximized in a floating source inverter. The crux of this method relies on the selection of an appropriate ratio for the dc voltages. This section presents two methods to choose the dc voltages v_i for setting the voltage ratios. The first method, referred to as full binary combination schema 1 (FBCS1), is to set the dc voltage ratio v_i as

$$v_i = \left(\frac{2^i - 1}{2^{nc} - 1}\right) \cdot E \qquad (1 \le i \le nc). \tag{2}$$

On the ac side, the inverter can always generate $nl = 2^{nc}$ levels of line-to-ground voltage, which also equals the entire binary number combinations of the switches. The second method, referred to as full binary combination schema 2 (FBCS2), is to set dc voltage ratio v_i as

$$v_i = \left(1 - \frac{2^{nc-i} - 1}{2^{nc} - 1}\right) \cdot E \qquad (1 \le i \le nc). \tag{3}$$

FBCS 1 and FBCS 2 are two efficient ways to cover the maximum binary combinations of the switches. However, there are still some other possibilities on choosing v_i to cover all the binary combinations. The term AFBCS (Additional Full Binary Combination Schema) is used to represent the other methods for setting dc voltage ratios to obtain the maximum binary combinations of the switches.

D. A Four-Cell FBCS Design

Consider the design of a four-cell FBCS multilevel inverter. In this case, $nc = 4$, $nl = 2^{nc} = 2^4 = 16$. From FBCS 1, the dc voltages for each phase can be set to

$$\begin{cases} v_1 = \left(\dfrac{2^1 - 1}{2^4 - 1}\right) \cdot E = \dfrac{1}{15} E \\ v_2 = \left(\dfrac{2^2 - 1}{2^4 - 1}\right) \cdot E = \dfrac{3}{15} E \\ v_3 = \left(\dfrac{2^3 - 1}{2^4 - 1}\right) \cdot E = \dfrac{7}{15} E \\ v_4 = E. \end{cases} \tag{4}$$

From FBCS 2, the dc voltages for each phase can be set to

$$\begin{cases} v_1 = \left(1 - \dfrac{2^{(4-1)} - 1}{2^4 - 1}\right) \cdot E = \dfrac{8}{15} E \\ v_2 = \left(1 - \dfrac{2^{(4-2)} - 1}{2^4 - 1}\right) \cdot E = \dfrac{12}{15} E \\ v_3 = \left(1 - \dfrac{2^{(4-3)} - 1}{2^4 - 1}\right) \cdot E = \dfrac{14}{15} E \\ v_4 = E. \end{cases} \tag{5}$$

As an AFBCS example, a 4-cell, 16-level inverter can also be generated by setting the dc voltage ratio as

$$v_1 : v_2 : v_3 : v_4 = 1 : 5 : 13 : 15. \tag{6}$$

Table VI shows the relationship between the switching states and the line-to-ground voltage by applying the basic circuit laws and FBCS. It can be seen that FBCS 1, FBCS 2 and the AFBCS example all result in 16 different line-to-ground values, which also means that by applying FBCS, it is possible to generate a four-cell, sixteen-level inverter. The conventional four-cell FS topology design, compared to FBCS, merely yields a five-level inverter. Fig. 4 shows a three-phase version of the 16-level inverter topology.

IV. COMPARISON BETWEEN CONVENTIONAL N-CELL FS METHOD AND FBCS

A. Voltage Levels

The previous sections have demonstrated that FBCS utilizes the full switch combinations to yield 2^n voltage levels. The conventional method uses a dc voltage ratio that results in $n + 1$ voltage levels.

B. Semiconductor Voltages

In designing multilevel inverters, it is convenient to choose all the switches of the same rated voltage. For the conventional FS schema, the blocking voltage of each IGBT is distributed

TABLE VI
FOUR-CELL 16-LEVEL INVERTER APPLYING FBCSa

Table VI. Four-cell 16-level inverter applying FBCS							
T_{x4}	T_{x3}	T_{x2}	T_{x1}	v_{xg} Formulas	v_{xg} (FBCS 1) 1:3:7:15	v_{xg} (FBCS 2) 8:12:14:15	v_{xg} (AFBCS) 1:5:13:15
0	0	0	0	0	0	0	0
0	0	0	1	v_1	$E/15$	$8E/15$	$E/15$
0	0	1	0	$v_2 - v_1$	$2E/15$	$4E/15$	$4E/15$
0	0	1	1	v_2	$3E/15$	$12E/15$	$5E/15$
0	1	0	0	$v_3 - v_2$	$4E/15$	$2E/15$	$8E/15$
0	1	0	1	$v_3 - v_2 + v_1$	$5E/15$	$10E/15$	$9E/15$
0	1	1	0	$v_3 - v_1$	$6E/15$	$6E/15$	$12E/15$
0	1	1	1	v_3	$7E/15$	$14E/15$	$13E/15$
1	0	0	0	$v_4 - v_3$	$8E/15$	$E/15$	$2E/15$
1	0	0	1	$v_4 - v_3 + v_1$	$9E/15$	$9E/15$	$3E/15$
1	0	1	0	$v_4 - v_3 + v_2 - v_1$	$10E/15$	$5E/15$	$6E/15$
1	0	1	1	$v_4 - v_3 + v_2$	$11E/15$	$13E/15$	$7E/15$
1	1	0	0	$v_4 - v_2$	$12E/15$	$3E/15$	$10E/15$
1	1	0	1	$v_4 - v_2 + v_1$	$13E/15$	$11E/15$	$11E/15$
1	1	1	0	$v_4 - v_1$	$14E/15$	$7E/15$	$14E/15$
1	1	1	1	v_4	E	E	E

TABLE VII
THE BLOCKING VOLTAGES OF TWO-CELL INVERTERS

Table VII. The blocking voltages of two-cell inverters		
	Conventional FS ($v_1 : v_2 = 1 : 2$)	FBCS 1 ($v_1 : v_2 = 1 : 3$)
v_{T1x}	$E/2$	$E/3$
v_{T2x}	$E/2$	$2E/3$

evenly; while in FBCS, the blocking voltage of IGBTs are different. For instance, in the design of a two-cell multilevel inverter as shown in Fig. 1, the blocking voltages for T_{x1} and T_{x2} will be different for FBCS as shown in Table VII. From the average cost point of view, there is no difference between the two designs. However, regarding convenience, all switches will be designed to have the same rated voltage, which means that the rated voltage will be chosen as $2E/3$ instead of $E/2$ when applying FBCS. Fortunately, the modulation will result in a desirable split of voltage and frequency when FBCS is applied. In particular, devices in the two-cell inverter with a range of $2E/3$ will switch at a lower frequency than the devices rated at $E/3$. This makes it possible to mix devices such as IGCTs and IGBTs [2]–[4], [9].

C. Floating Source Currents

The conventional FS method can take advantage of the redundancy to force the average dc source currents to be zero. This allows capacitors to be used for the voltage sources. Since the line-to-ground voltage redundancy does not exist in the FBCS methods, positive or negative dc source current results. Fig. 5 shows the simulated dc source current for the two-cell inverter.

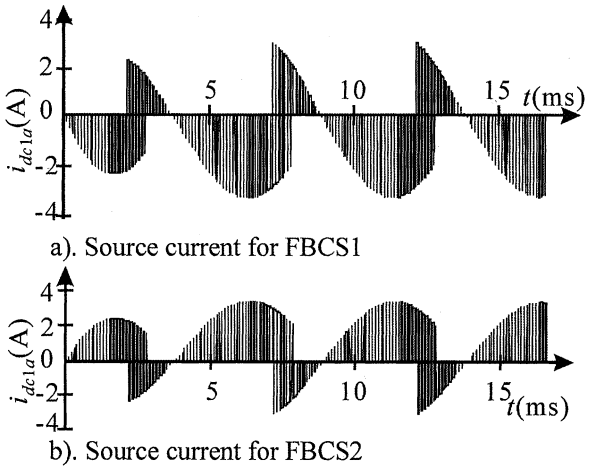

Fig. 5. Two-cell FBCS inverter simulation results.

As can be seen, FBCS1 results in negative average current (into the source as shown in Fig. 1) and FBCS2 results in positive average current. For two-cell inverter operation, FBCS2 is preferred so that the power flow will be out of the dc sources (batteries or transformer/rectifier circuits).

V. DC VOLTAGE RATIO ISSUE FOR OTHER MULTI-LEVEL INVERTER TOPOLOGIES

Fig. 6 shows one phase of the cascaded H-bridge multilevel inverter topology. As can be seen, the inverter phase consists of a number of series cells. Each cell has four power transistors and one isolated voltage source. This structure is popular for medium voltage drives due to its modularity and the fact that the power transistors need only block a fraction of the total voltage. Recent research on this inverter has included a valuable method

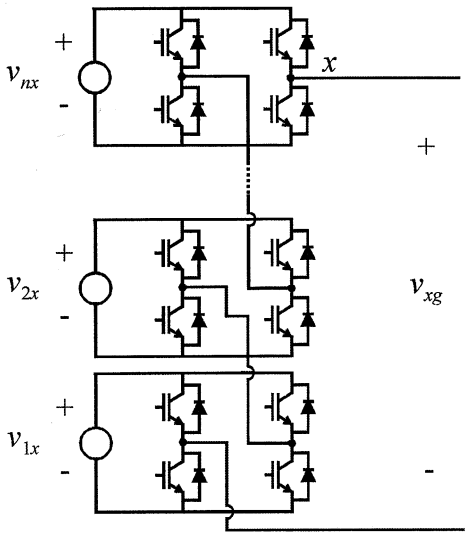

Fig. 6. H-bridge multilevel inverter topology.

of obtaining more voltage levels per member of semiconductor switches [2]–[4]. In particular, it has been shown that if the dc voltage ratio is set according to

$$v_{ix} = 2^{i-1} \times E \qquad (1 \le i \le nc) \tag{7}$$

then a total number of

$$nl = 2^{nc+1} - 1 \tag{8}$$

voltage levels may be obtained. If this is compared to the number of levels obtainable by applying FBCS to the floating source inverter, it can be seen that the cascaded H-bridge inverter produces roughly twice as many voltage levels. However, the cascaded H-bridge inverter also requires twice as many transistors per cell so that the ratio of number of levels to number of transistors is nearly the same. This is especially true for inverters with a high number of cells. Other comparisons between these topologies may be found in the literature [5], [6].

VI. Computer Simulation Results

A computer simulation with a three-phase R–L load has been created to verify the FBCS method. Several methods [17]–[20] are available to trigger the power switches for controlling the voltage levels generated on the ac side of inverters. In this simulation, the multilevel sine-triangle modulation method [18], [19] is adopted. For a n-level inverter system, the duty cycle of phase x with the third harmonics injection can be expressed as

$$d_{xm} = \frac{n-1}{2} \cdot \left[1 + m \cdot \cos(\theta) - \frac{m}{6} \cdot \cos(\theta)\right] \tag{9}$$

where θ is the angle position and m is the modulation index. Triangle waveforms can then be used to generate the switching level states s_x after comparing with the d_{xm}. Fig. 7 shows the duty cycle, triangle waveforms, and resulting comparison for the 4-level inverter. Once the switching level states s_x are generated, one can simply match them to the related switching actions. For instance, by following the above procedure, the switching level states s_x for a 2-cell FBCS2 inverter can range from 0 to

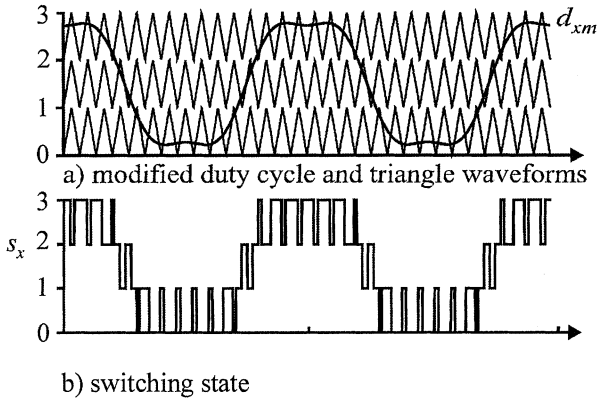

Fig. 7. Four-level sine-triangle modulation technique.

TABLE VIII
Two-Cell FBCS 2 Inverter ($v_1 : v_2 = 2 : 3$)

Table VIII. Two-cell FBCS 2 inverter (v_1 : v_2 = 2 : 3)

S_x	T_{x2}	T_{x1}	v_{xg}
0	0	0	0
2	0	1	2*E*/3
1	1	0	*E*/3
3	1	1	*E*

3. Table VIII shows the matching relationship between s_x and transistor signals. Fig. 8 shows the computer simulation results of the line-to-ground voltage and the line-to-neutral voltage for 4-level, 8-level, and 16-level inverters. The simulations included detailed switching of each cell and demonstrated the operation of FBCS.

VII. Laboratory Validation

A two-cell 4-level FS inverter was constructed in the laboratory. A 3.7 kW induction motor [9] was used as a load. The inverter modulation was accomplished using multilevel sine-triangle modulation with a switching frequency of 10 kHz and a modulation index of 1.13. The commanded fundamental frequency was 60 Hz. The first study involved using batteries for the floating sources in order to demonstrate the negative and positive source currents for FBCS1 and FBCS2, respectively. In this setup, a battery voltage of $v_1 = 24$ V was used. Since the voltage for the battery studies was considerably less than the rated motor voltage, the rotor was blocked and it acted as an R–L load. Fig. 9 shows the laboratory measurements for FBCS1 where $v_2 = 72$ V. Therein, the upper transistor voltages, dc source current, line-to-ground voltage, line-to-line voltage, and line current for the a-phase are shown. As can be seen, the transistors with a high blocking voltage have a low switching frequency and visa versa. This is a common feature that results in maximally distended converters [9] and is desirable since it matches the market reality where higher voltage power switches are lower-rated in switching frequency. The dc source current is negative on average as expected from the simulation results. The voltage and currents exhibit typical 4-level inverter performance. Since the dc voltage is low for this study, the effect of semiconductor drops can be seen in the line-to-ground voltage. Fig. 10 shows the laboratory results for FBSC2 where

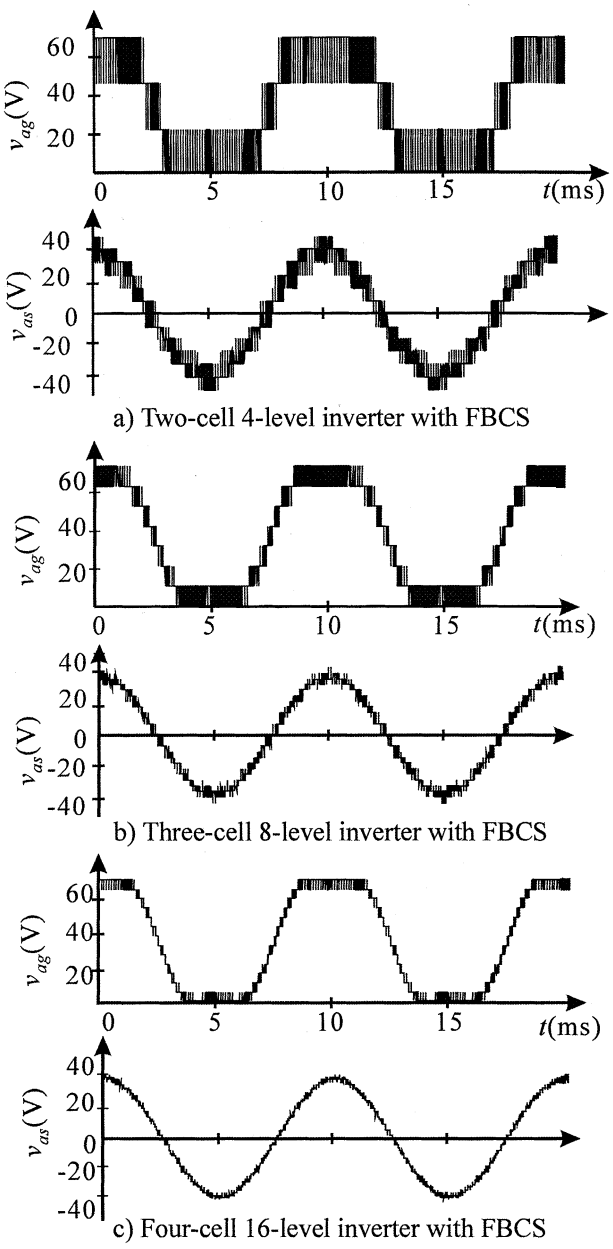

Fig. 8. FBCS simulations.

the dc voltage has been set to $v_2 = 36$ V in accordance with (3). In this case, the dc source current has a positive average value. In the next study, transformer/rectifier sources were used to supply $v_1 = 220$ V in each phase. The dc link voltage was set to $v_2 = 330$ V in accordance with FBCS2 so that the rectifier currents will be positive on average. These voltage levels were chosen since they correspond to rated voltage on the motor. The motor was operated at rated load. Fig. 11 shows the laboratory measurements. It can be seen that, in this study, the semiconductor voltage drops are negligible. The low-frequency harmonics in the current waveform are due to induction motor saturation.

VIII. Conclusion

This paper has presented new full binary combination schema for floating source multilevel inverters. The new schema pro-

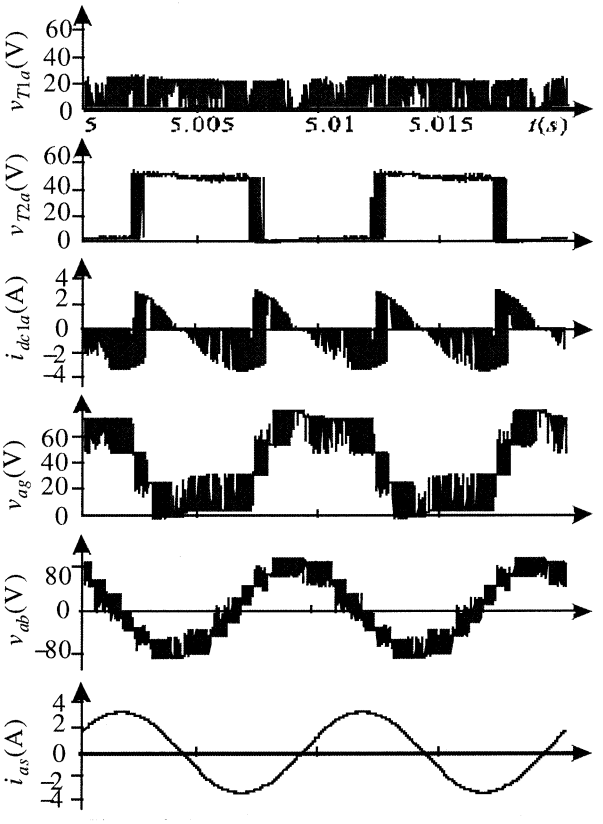

Fig. 9. Test results using FBCS 1 (using battery sources).

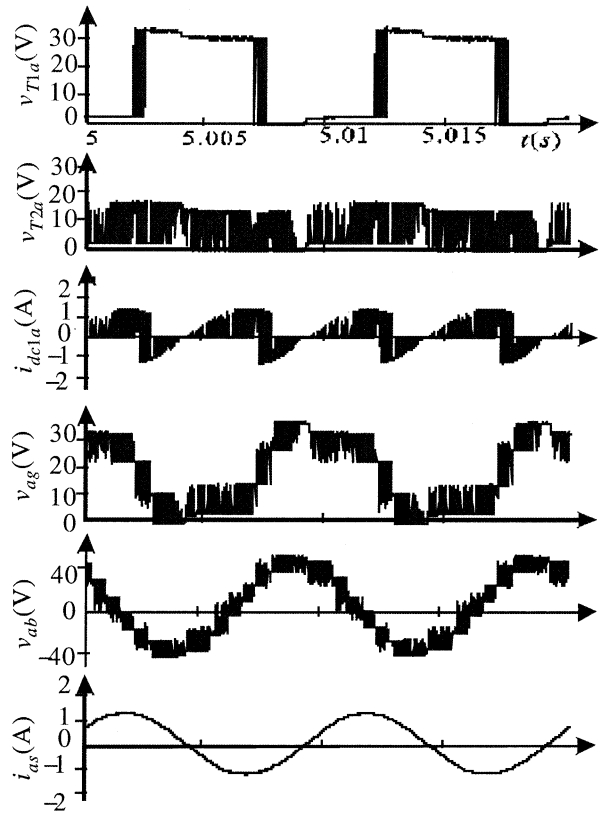

Fig. 10. Test results using FBCS 2 (using battery sources).

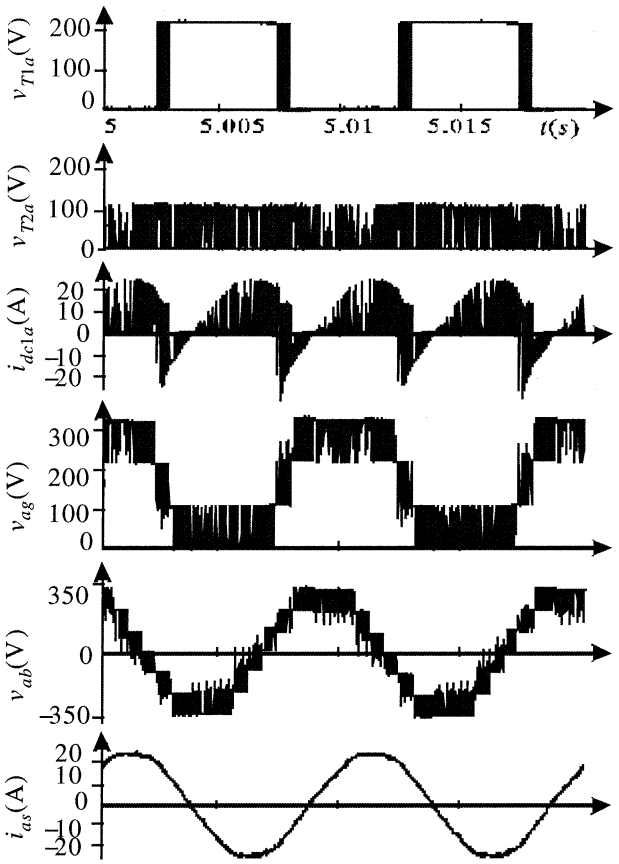

Fig. 11. Test results using FBCS 2 (using rectifier sources).

vides an efficient method for constructing multilevel dc/ac inverters. Comparing this with the conventional FS multilevel inverters, the proposed schema use less power electronic switches while yielding a higher number of voltage levels. The proposed method has been analyzed in terms of voltage levels, device voltage stresses and floating source currents. Computer simulation and laboratory measurements have been presented.

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