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# Extraction of SPICE-Type Equivalent Circuits of Signal Via Transitions Using The PEEC Method

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**Abstract**—Digital devices and discontinuities are typically analyzed by inserting their equivalent circuits into SPICE-type simulators. The partial element equivalent circuit method has been proven to be very useful for electromagnetic modeling. It can be used in both the time and the frequency domain. In this paper, the PEEC technique is employed as an efficient full-wave modeling tool to derive SPICE-type equivalent circuits of signal via transition structures. A nodal analysis technique is utilized in conjunction with the optimization algorithm to extract the equivalent circuits, whose component values are the parameters optimized. The good agreement between different approaches demonstrates that the proposed approach can be a powerful tool for deriving the equivalent circuits of signal via transitions.

**Keywords**- PEEC, signal integrity, circuit extraction.

## I. INTRODUCTION

Signal line routing in multi-layer printed circuit designs is a primary concern in meeting signal integrity (SI) and electromagnetic interference (EMI) requirements [1]. Due to the increasing board design density, signal lines often have to be routed on different planes of a printed circuit board (PCB) using via interconnects. As the clock frequency and board size continue to increase, inductance effects associated with via interconnects have become significant. Since via interconnects limit system performance in high-speed very large integrated circuit design, modeling via interconnects is receiving more attention.

In modeling approaches, microwave devices and discontinuities are typically analyzed by inserting their equivalent circuits into SPICE-type simulators. Many modeling methods have been employed in the development of tools and techniques to extract the equivalent circuits of via interconnects. However, the challenges are not only the complexity of the 3-D structures, but also the accuracy in an increasing frequency range. The models must also be able to handle the equivalent circuit of such complexities as frequency dependent inductances and resistances in the time-domain as well. This is the motivation for developing a fast and accurate modeling technique for extracting the equivalent circuit for complex 3-D structures.

The partial element equivalent circuit (PEEC) [2][3] technique has been applied successfully to model the electrical properties of interconnects. In the PEEC approach, the continuous conductor is subdivided into distributed pieces and then assumes that the current is uniform in each piece. The inductive and capacitive circuit elements and the DC resistance of each piece are computed based on a quasi-static solution of Maxwell's equations. Thus, a circuit is formed with these elements. Finally, the yielded equivalent circuits can be combined with other circuit models (transistors) into an input circuit for a SPICE-type circuit simulator.

A new, general non-orthogonal PEEC model approach was introduced in [4] recently. The formulation uses quadrilateral and hexahedral shapes to represent the different conductors and dielectric regions. The approach retains the flexibility of the orthogonal PEEC approach, and works equally well in the time and frequency domains as well. Moreover, based on the non-orthogonal mesh, the approach can be used to model interconnects in greater detail. In this paper, an improved PEEC approach with the calculations of the coefficients of potential and the partial inductances is employed as a full-wave modeling tool to calculate the Z-parameters of a via transition structure, which is from a microstrip to a coplanar waveguide. Then, a SPICE-type equivalent circuit of via transition structures is derived from the calculated Z-parameters using the nodal analysis technique in conjunction with an optimization algorithm. Numerical results demonstrate that the proposed approach yields good results for the case studied.

In this paper, a brief description of the PEEC method is presented in Section II. The PEEC method is extended to non-orthogonal cases, and the extractions of partial elements are discussed. Section III describes the nodal analysis technique that is applied in conjunction with an optimization algorithm to extract the equivalent circuits of interconnects. In Section IV, the PEEC method is employed as a full-wave modeling tool to calculate the Z-parameters of the via transition structure from a microstrip to a coplanar waveguide. Then, a nodal analysis technique in conjunction with the optimization algorithm is used to derive a SPICE-type equivalent circuit of the via transition structures. The results demonstrate that the PEEC method can be a powerful tool for deriving the equivalent

circuits of via interconnects, which can be inserted into SPICE for the purpose of circuit simulation.

## II. THE PEEC METHOD

Since the PEEC method was developed in 1974 [2], the PEEC circuit formulations have been used widely and successfully for modeling interconnect structures. The PEEC method builds up models of complex interconnect structures from simple rectangular bricks. The DC resistance, partial inductance, and partial capacitance are calculated for each rectangular brick. The partial elements are then assembled into a complete circuit and solved with a circuit simulator. Accuracy improves with finer subdivision of the original geometry.

The PEEC method is based on the circuit interpretation of the Electric Field Integral Equation (EFIE) full wave formulation. The EFIE is interpreted in terms of the capacitive and inductive interactions between the elemental currents and charges in the discretized structure. The unknowns in the circuit interpretation are the current densities within the conductors, and the charges on the surfaces or the potentials (voltages). To compute the partial inductance and the coefficients of potential between brick-type elements, analytical expressions are available for the double volume integral and double surface integral,

$$L_{p\alpha\beta} = \frac{\mu}{4\pi} \frac{1}{a_\alpha a_\beta} \int_{a_\alpha} \int_{a_\beta} G(\bar{r}_\alpha, \bar{r}_\beta) dv_\alpha dv_\beta$$

$$= \frac{\mu}{4\pi} \frac{1}{a_\alpha a_\beta} \int_{a_\alpha} \int_{a_\beta} \frac{\bar{i}_\alpha \cdot \bar{i}_\beta}{|\bar{r}_\alpha - \bar{r}_\beta|} dv_\alpha dv_\beta, \quad (1)$$

$$P_{ij} = \frac{1}{4\pi\epsilon} \frac{1}{a_i a_j} \int_{a_i} \int_{a_j} G(\bar{r}_i, \bar{r}_j) ds'_i ds'_j, \quad (2)$$

where  $a_\alpha$  is the cross section of the cell,  $\bar{i}_\alpha$  is the unit vector in the direction of current flow for the cell, and  $G(\bar{r}, \bar{r}') = \frac{1}{|\bar{r} - \bar{r}'|}$  is the static Green's function in free space.

Most of the early work in PEEC modeling was restricted to a rectangular mesh. However, for many realistic problems such as via interconnects, the elements are not necessarily parallel and can not easily be discretized into brick-shaped elements. A non-orthogonal mesh is required to model these problems. For this reason the PEEC formulations were extended to the case of non-orthogonal elements in [5] [6]. A local non-orthogonal coordinate system  $(a, b, c)$  was introduced into the PEEC approach. Based on the new local non-orthogonal coordinate, the partial inductance and the normalized coefficients of potential are calculated as

$$Lp_{\alpha\alpha'} = \frac{\mu}{4\pi} \int \int \int \int \int \int (\hat{a} \cdot \hat{a}') h_\alpha G[\bar{r}_\alpha(\bar{r}_i), \bar{r}_{\alpha'}(\bar{r}_j)] da' db' dc' h_\alpha da db dc, \quad (3)$$

$$Pn_{\alpha\alpha'} = \frac{1}{4\pi\epsilon} \int \int \int \int G[\bar{r}_\alpha(\bar{r}_i), \bar{r}_{\alpha'}(\bar{r}_j)] da' db' da db, \quad (4)$$

where  $\bar{r}_g$  is the global coordinate, and  $\bar{r}_l$  is the local coordinate, the magnitude of the tangential vector  $h_\alpha = \left| \frac{\partial \bar{r}_l}{\partial a} \right|$  as

well as the unit vector  $\hat{a} = \left( \frac{\partial \bar{r}_l}{\partial a} \right) / h_\alpha$ , where  $a$  can be the local coordinates  $a, b, \text{ or } c$ .

Unfortunately, complete analytical expressions do not exist for such arbitrarily shaped six-sided volumes, and the partial element integral must be computed numerically. Referring to (3) and (4), higher dimensional integrals and higher order quadrature are required to calculate the PEEC coupling terms of arbitrarily shaped elements. Clearly, this approach becomes computationally intractable when the number of elements exceeds several hundred, and this limits the size of the problem that can be analyzed. Based on a derivation for the potential due to a distribution of sources on a flat quadrilateral panel, and a distance adaptive algorithm, an improved PEEC approach has been developed to rapidly extract the partial element parameters of generally shaped six-sided PEEC elements [7]. It can be used to calculate the Z-parameters of discontinuities effectively.

## III. NODAL ANALYSIS IN CONJUNCTION WITH THE OPTIMIZATION ALGORITHM

A nodal analysis technique is employed to derive the SPICE-type equivalent circuit of microwave discontinuities from their Z-parameters. The nodal equations of an N-node circuit can be expressed in the following form,

$$\{V\}_{N \times 1} = [Z]_{N \times N} \{I\}_{N \times 1}, \quad (5)$$

where  $\{V\}$  and  $\{I\}$  are voltage and current vectors at the  $N$  nodes for an equivalent circuit, and  $\{Z\}$  is the impedance matrix. If considered as a two-port network, only two ports contain the accessible nodes. Equation (5) can be manipulated into the convenient form

$$V_{2 \times 1} = Z_{2 \times 2} I_{2 \times 1}, \quad (6)$$

where

$$V_{2 \times 1} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix},$$

$$I_{2 \times 1} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix},$$

$$Z_{2 \times 2} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = M_{11} - M_{12} M_{22}^{-1} M_{21},$$

$$M_{11} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix},$$

$$M_{12} = \begin{bmatrix} z_{13} & z_{14} & \cdots & z_{1N} \\ z_{23} & z_{24} & \cdots & z_{2N} \end{bmatrix},$$

$$M_{22} = \begin{bmatrix} Z_{33} & Z_{34} & \cdots & Z_{3N} \\ Z_{43} & Z_{44} & \cdots & Z_{4N} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{N3} & Z_{N4} & \cdots & Z_{NN} \end{bmatrix},$$

$$\text{and } M_{21} = \begin{bmatrix} Z_{31} & Z_{32} \\ Z_{41} & Z_{42} \\ \vdots & \vdots \\ Z_{N1} & Z_{N2} \end{bmatrix}.$$

The S-parameter matrix of the circuit can then be calculated from

$$S = \left[ \frac{Z_{2 \times 2}}{50} + I \right] \left[ \frac{Z_{2 \times 2}}{50} - I \right]^{-1}, \quad (7)$$

where  $S$  is the S-parameter matrix of the circuit, and  $I$  is the identity matrix.

A lumped circuit model can be constructed for an arbitrary interconnect geometry from basic physics associated with the geometry. Based on this lumped circuit model, the Z-parameters can be calculated. Then an optimization procedure is employed to derive the component values. The optimization procedure considers each of the component values of the circuit as a parameter to be optimized. The objective function  $J$  for the optimization procedure is chosen to be

$$J = \sum_{n=1}^{N_f} \sum_{j=1}^2 \sum_{i=1}^2 |Z_{ij}(f_n) - Z_{ij}^{op}(f_n)|^2, \quad (8)$$

where  $N_f$  is the total number of frequencies of interest,  $Z_{ij}$  is the specified Z-parameters of the equivalent circuit, and  $Z_{ij}^{op}$  is the Z-parameters calculated from the equivalent circuit selected by the optimization procedure. For a given set of specified Z-parameters, the optimization algorithm strives to minimize the objective function  $J$  by selecting the component values of the equivalent circuit. The optimization procedure begins with an initial set of component values. The optimization procedure then iteratively generates a new set of component values, derived from the previous ones, through the application of the objective function. In the process of applying the optimization procedure based on (8), the Z-parameters  $Z_{ij}^{op}$  need to be calculated at each iteration step using the nodal analysis technique.

#### IV. SIMULATION OF A VIA INTERCONNECT

To test the approach, a via transition structure was studied. The structure is a two-layer board with a via transition from a microstrip to a coplanar waveguide, as shown in Figure 1(a). The top layer of the PCB is a microstrip trace, and the bottom layer is a coplanar waveguide structure. The two structures are connected through a via. The dielectric layer is 14 mils thick, with a dielectric constant of 5.2 and loss tangent of 0.01. The width of the 50  $\Omega$  microstrip is 20 mils, and the width of the 50  $\Omega$  coplanar waveguide is 22.5 mils. The via diameter is 13 mils. Figure 1(b) shows a non-orthogonal volumetric mesh for the connected cells used in the PEEC method. The connected cells for the example were approximately 1800. Based on this mesh, the quadrilateral surface mesh for the capacitive cells

and three hexahedral volumetric meshes for the inductive cells were constructed. Thus, a complete circuit of the via transition structure was assembled to calculate the Z-parameters. Since both the inductance and capacitance matrices for the PEEC method usually are dense matrices, this leads to a prohibitively large simulation time and memory requirements. The frequency analysis for the example took approximately two hours, and the memory requirement was approximately 1.2 GigaBytes. Meanwhile, an equivalent circuit of the via transition structure was developed, as shown in Figure 2. The nodal analysis in conjunction with the optimization algorithm was employed to extract the component values of the equivalent circuit. The extracted component values are shown in Figure 2 as well. HSPICE was employed to simulate the frequency response of the equivalent circuit extracted. The PEEC and SPICE simulated results of a frequency domain analysis for the example are plotted in Figure 3. To verify the PEEC and SPICE simulated results, the same structure was simulated using FLOEMC and FDTD. Both FLOEMC and FDTD used a rectangular mesh in the calculations. Both of the simulated results are plotted in Figure 3 as well. The discrepancy between different approaches for the  $|S_{21}|$  is within 0.05 dB. The good agreement demonstrates the utility of the proposed approach.

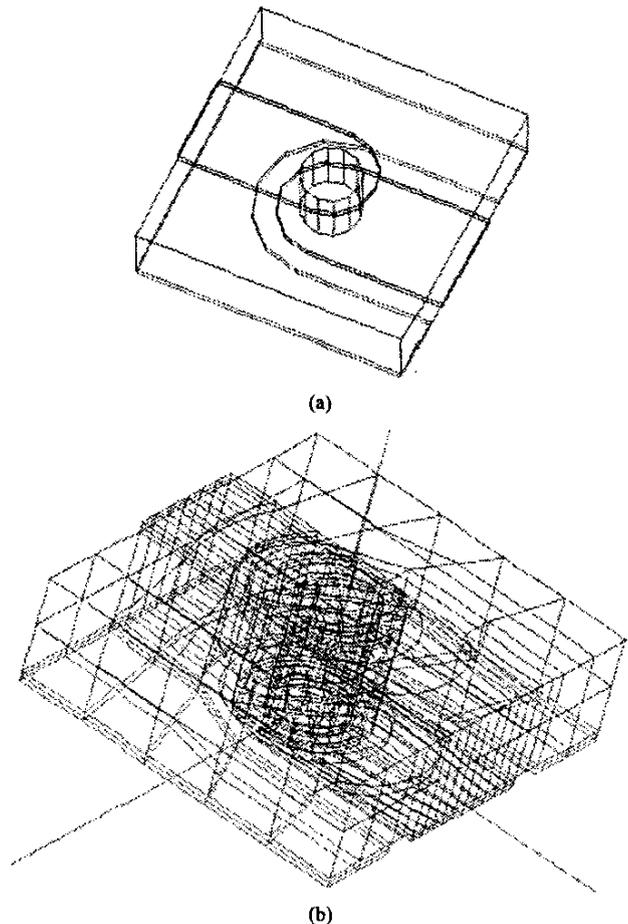


Figure 1. Via transition structure. (a) geometry, and, (b) volumetric mesh.

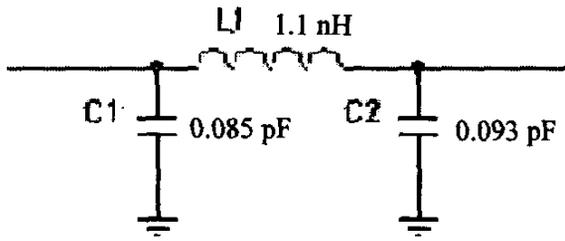


Figure 2. The equivalent circuit of the via transition.

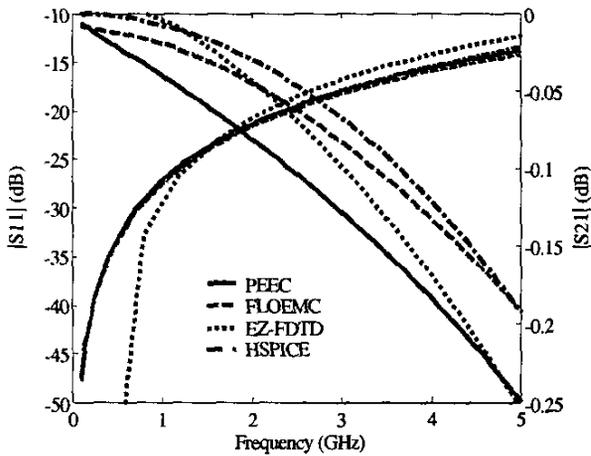


Figure 3. Simulated results for the via transition structure.

## V. CONCLUSION

In this paper, an efficient technique is presented for systematically extracting SPICE-type equivalent circuits of via interconnect structures from computed Z-parameters. Since the

non-orthogonal PEEC method extends the applicability of the PEEC method for analysis of 3D complex structures, it is employed as an efficient full-wave modeling tool to model via interconnects. The advantage of the PEEC method is that the PEEC method extracts an equivalent circuit. The equivalent circuit model can then be implemented in SPICE, and IC device models and PCB trace models incorporated into the overall modeling for signal integrity. This approach is easily implemented, but the size of the equivalent circuit models might be very big due to the fine mesh. A simplified SPICE-type equivalent circuit is required for signal integrity analysis. Herein, using a nodal analysis technique in conjunction with an optimization algorithm, SPICE-type equivalent circuits of via interconnects can be extracted from the PEEC simulated results. The modeled results agree well with the SPICE simulated results.

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