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Distributed Control of Hybrid Motor Drives

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***Abstract*—The hybrid inverter fed motor drive with two cascaded multilevel inverters is an attractive option for high performance high power applications such as naval ship propulsion systems due to a number of unique features. There is a natural split between a higher-voltage lower-frequency "bulk" inverter and a lower-voltage higher-frequency "conditioning" inverter in the cascaded system which matches the availability of semiconductor devices. Furthermore, the bulk inverter may be a commercial-off-the-shelf (COTS) motor drive meaning that only the conditioning inverter needs to be custom made. However, a drive involving a COTS bulk inverter would require a distributed conditioning inverter control which works completely independent of the bulk inverter control. In this paper, a set of distributed control methods are developed for the hybrid inverter drive with cascaded bulk and conditioning inverters, requiring only single dc source. Moreover, a solution to the practical problem of instant synchronization between the two inverters is presented. Laboratory measurements on a 3.7-kW induction motor drive validate the proposed control. Various practical considerations (such as low m-index performance and capacitor precharging options) are discussed and their solutions provided.**

***Index Terms*—Commercial-off-the-shelf (COTS) motor drive.**

I. Introduction

THE HYBRID multilevel inverter has received much attention in the literature during recent years due to advantages of exceptional power quality [1]–[10]. The general concept of this inverter is to split the power conversion between a "bulk" inverter supplying low-frequency higher-voltage and a "conditioning" inverter supplying high-frequency low-voltage. For many systems (including Naval ship propulsion), there is a desire to distribute the control so that the bulk inverter may be commercial-off-the-shelf (COTS)with its stock controller and only the conditioning inverter and control, typically an order of magnitude smaller in power, would be custom made [1]. In order for the distributed control to operate properly, the conditioning control needs to provide voltage harmonic compensation and at the same time be synchronized with the bulk inverter. This paper presents recent development of a distributed control where the harmonic compensation and synchronization issues have been thoroughly addressed. Laboratory results of the new control are included for validation.

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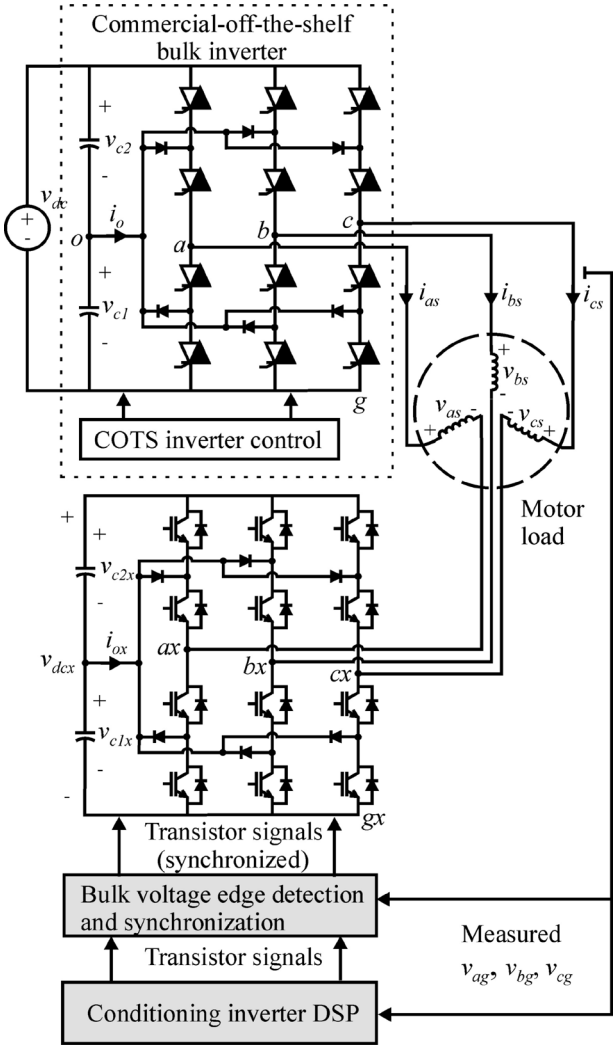

Fig. 1. Hybrid multilevel inverter with distributed controller.

II. Hybrid Inverter; Topology and Modulation

Fig. 1 shows the topology of the hybrid inverter drive formed by cascading two three-level inverters. Therein, a three-level "bulk" inverter supplies the motor load from the dc source $v_{\rm dc}$. The neutral point of the machine is opened and the other end of each phase is connected to a three-level "conditioning" inverter. This topology has been extensively studied in the literature and previous research has shown that this inverter is capable of operating at maximal distension with nine-level inverter performance if the voltage ratio is set to $v_{\rm dc} = 3v_{dcx}$ [1], [4]. For applications such as naval propulsion where only one source is available, the "conditioning" inverter dc source v_{dcx} is supplied by a capacitor bank and its voltage can be regulated using redundant states selection (RSS) control [1]. Referring to Fig. 1,

the line-to-ground voltages of the bulk and conditioning inverter may be expressed as

$$\begin{aligned}\begin{bmatrix} v_{ag} & v_{bg} & v_{cg}\end{bmatrix}^{\mathrm{T}} &= \begin{bmatrix} s_a & s_b & s_c\end{bmatrix}^{\mathrm{T}} \frac{v_{\mathrm{dc}}}{2} \\ \begin{bmatrix} v_{agx} & v_{bgx} & v_{cgx}\end{bmatrix}^{\mathrm{T}} &= \begin{bmatrix} s_{ax} & s_{bx} & s_{cx}\end{bmatrix}^{\mathrm{T}} \frac{v_{dcx}}{2}\end{aligned} \quad (1)$$

where (s_a, s_b, s_c) and (s_{ax}, s_{bx}, s_{cx}) are the switching states of bulk inverter and the conditioning inverter. For three-level inverters, the switching states have the option of 0, 1, or 2. Equation (1) is based on the assumption that the capacitors of the bulk and conditioning inverters are regulated to their ideal values [1]. The phase voltages of the load can be expressed in terms of the line-to-ground voltages as [1]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs}\end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2\end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg}\end{bmatrix} - \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2\end{bmatrix}\begin{bmatrix} v_{agx} \\ v_{bgx} \\ v_{cgx}\end{bmatrix}. \quad (2)$$

The load voltages can be plotted in the q–d stationary reference frame for all possible switching states of both the bulk and conditioning inverter resulting in the vector plot shown in Fig. 2. The bold vectors form a three-level pattern which represents bulk inverter switching states. These will be referred to as "bulk vectors" herein. Each bulk vector is the origin of a smaller three-level sub-hexagon as marked by dotted line and each vector dot in the sub-hexagon represents one or more switching states of the conditioning inverter. Every dot in the vector plot can be further decomposed into the switching states of the bulk and conditioning inverter. First, each vector dot can be affiliated with a sub-hexagon; the origin of which is it's bulk inverter switching states. For example, in Fig. 3 (the zoomed in view of the shaded sub-hexagon in the Fig. 2), the vector v_3 can be regarded as the addition of the bulk vector 220 and its conditioning inverter vector with the switching states (210). The conditioning inverter switching states are vector v_3 projections onto the reversed ax–bx–cx coordinates (shown as $-ax$, $-bx$, and $-cx$ axis in Fig. 3) with the bulk vector 220 as the origin. The reversed coordinates are used here for convenience since the conditioning inverters phase-to-ground voltages have negative contributions to the load phase voltage according to (2).

In previous research, modulation methods were introduced which take into account the switching states of the bulk and conditioning inverter simultaneously. One example is the space vector modulation (SVM) method [3], [4]. Using this modulation method, the nearest vectors to the reference vector are selected and the switching sequence and timing are determined in the vector domain. This method relies on geometric relationships which can be cumbersome. However, recent research has simplified the SVM method [11]–[13]. An alternate method is natural sampling which is performed on a per-phase basis in the time domain. This method was recently simplified for programming multilevel modulation in a DSP control [14]. By combining this method with RSS switching, the capacitor voltages can be regulated and the inverter can operate from one voltage source as a seven-level inverter [1].

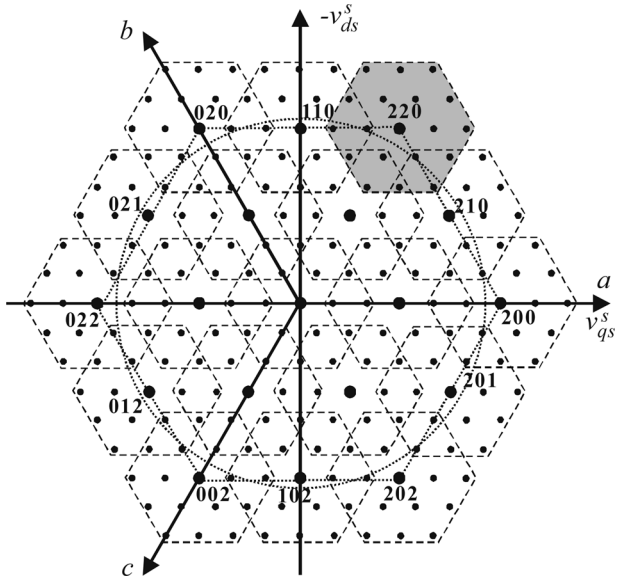

Fig. 2. Cascade-3/3 vector plot for dc ratio 1:3.

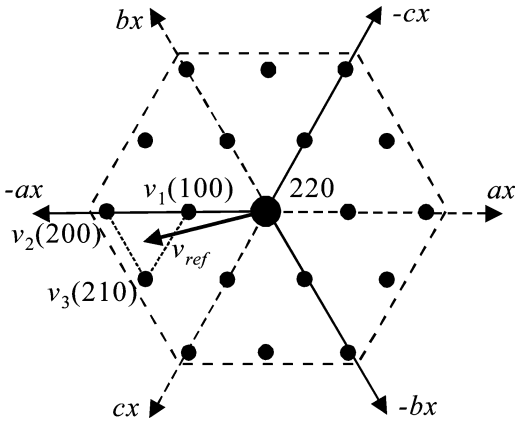

Fig. 3. Reversed ax–bx–cx coordinates for conditioning inverter switching states.

In this paper, a new distributed modulation is proposed. Using this method, the bulk inverter operates by staircase control (block switching) at the fundamental frequency. The control of the conditioning inverter is independently based on real-time harmonic computation and it operates as an active filter. The resulting load voltage output is equivalent to those created by other modulation methods. The details of this method will be described in the next section.

III. Distributed Control of the Hybrid Inverter

The bulk inverter is a commercially available medium-voltage three-level motor drive controlled with its built-in staircase switching. The line-to-ground voltage output is shown in Fig. 4 for the a-phase. The fundamental component can be adjusted by changing the delay angle α. From Fourier expansion, this is

$$|v_{as}| = \frac{2v_{\mathrm{dc}}}{\pi}\cos(\alpha). \quad (3)$$

Although the bulk inverter output has negligible switching losses, large low-frequency harmonics are produced. The con-

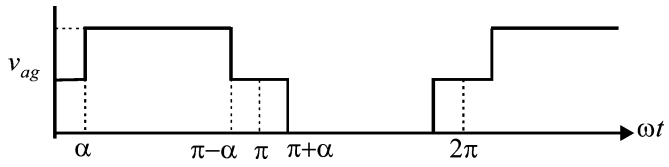

Fig. 4. Bulk inverter a-phase line-to-ground voltage.

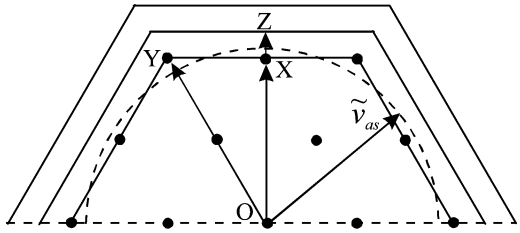

Fig. 5. Maximum modulation index analysis.

ditioning inverter can correct these harmonics by sensing the bulk line-to-ground voltages and computing the required synchronized pulsewidth modulation (PWM) signals for compensation. The control algorithm used by conditioning inverter is to be introduced in Section III-A below. The conditioning control also regulates the dc voltage v_{dcx} through an additional proportional–integral (PI) term which adjusts the commanded average power flow into the conditioning inverter. In Section III-B, the edge detection of the bulk line-to-ground voltages and synchronizing logic is described. Here, the major practical issues in the synchronization are presented and analyzed. The solution to this problem greatly improves the controller performance.

It is insightful to note that the bulk inverter staircase modulation at high modulation index (low α angle) follows the counterclockwise hexagon vector path (as indicated in Fig. 2 by dotted line) traversing all the bulk vectors in the perimeter of the three-level hexagon of the bulk inverter. In the proposed hybrid modulation, the combined output voltage command is exactly the fundamental component of bulk inverter voltage and it's circular vector path is also plotted with dotted line in Fig. 2. It can be seen from the vector plot that when the bulk inverter switching state is at any bulk vector, the reference (circular locus) is always within a sub-hexagon that originates from the bulk vector. Therefore, it's always possible for the conditioning inverter to synthesize the desired locus of commanded vectors with PWM switching.

In order to determine the switching states and duty cycles of the conditioning inverter for any reference vector along the circular path, the nearest vectors must be located. As an example, the reference $v_{\rm ref}$ in Fig. 3 changes to the new origin of bulk vector 220. Then to synthesize the new vector inside the sub-hexagon, it requires the three nearest vectors with certain duty cycles in one PWM cycle. This can be easily accomplished using space vector modulation with non-orthogonal coordinates [11], [12] or the vector in q–d frame can be transform into reversed a–b–c frame and then per-phase duty cycles [14] can be defined. However, the major obstacle is that the controls are distributed and the conditioning inverter controller has no information of the combined output voltage command. Before computing the PWM switching commands, it must locate the reference vector which is in phase with the bulk voltage in real-time. Before detailing this control algorithm, it is instructive to discuss the maximal achievable modulation index of hybrid inverter. In Fig. 5, the circular vector path is the fundamental component for the maximum modulation index (corresponding to $\alpha = 0^{\circ}$). As it turns out, this will yield a maximum voltage of $|v_{as}| = 0.637 v_{\rm dc}$. This peak is between the seventh and eighth level hexagon boundaries which are $OX = 0.577 v_{\rm dc}$ and $OZ = 0.673 v_{\rm dc}$ respectively. This means that the resulting load waveforms will have the performance of an eight-level inverter.

A. Conditioning Inverter Voltage Control

Fig. 6 shows the block diagram for the voltage control in the conditioning inverter. The first step in this control is to convert the bulk inverter line-to-ground voltages into bulk line-to-neutral voltages using

$$\begin{bmatrix} v_{as1} \\ v_{bs1} \\ v_{cs1} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{4}$$

The voltages v_{as1}, v_{bs1} and v_{cs1} represent the bulk inverter contribution to the load voltages and have the shape of load voltages of a typical step inverter. These voltages are then heavily filtered so that the resulting terms $\tilde{v}_{as1}$, $\tilde{v}_{bs1}$ and $\tilde{v}_{cs1}$ will be sinusoidal and used for synchronous reference frame transformation. In particular, the transformation terms can be calculated by dividing out the magnitude of the filter voltages using

$$\cos(\theta_e) = \sqrt{\frac{3}{2}} \frac{\tilde{v}_{as1}}{\sqrt{\tilde{v}_{as1}^2 + \tilde{v}_{bs1}^2 + \tilde{v}_{cs1}^2}} \tag{5}$$

$$\sin(\theta_e) = \sqrt{\frac{1}{2}} \frac{\tilde{v}_{cs1} - \tilde{v}_{bs1}}{\sqrt{\tilde{v}_{as1}^2 + \tilde{v}_{bs1}^2 + \tilde{v}_{cs1}^2}}. \tag{6}$$

These terms can be used to transform the line-to-ground voltages to the q–d synchronous reference frame. Notice that this is equivalent to transforming the line-to-neutral voltages v_{as1}, v_{bs1}, and v_{cs1} to the synchronous reference frame where they would ideally be dc values. Thus by low-pass filtering (LPF) v_{qo}^e and v_{do}^e, the resulting voltages $\widetilde{v}_{qo}^e$ and $\widetilde{v}_{do}^e$ will be ideal (or commanded) values. Note that there will be no attenuation associated with the LPF since the fundamental component is dc in the q–d reference frame. However, the dynamic response will be affected by the additional this LPF filter. Next, the commanded conditioning inverter q- and d-axis synchronous reference frame voltages can be determined by subtracting $\widetilde{v}_{qo}^e$ and $\widetilde{v}_{do}^e$ from v_{qo}^e and v_{do}^e. Before this is done, a PI term needs to be added for regulation of the capacitor voltage v_{dcx} (which will be described in detail below). The output of this control is a new set of voltages $\widetilde{v}_{qo,new}^e$ and $\widetilde{v}_{do,new}^e$ which are subtracted from v_{qo}^e and v_{do}^e. The results can then be transformed back to a–b–c yielding commanded per-phase voltages which will compensate the harmonics from the bulk inverter output. The PWM duty cycles are created using these voltages according to the modulation method described in [14]. Note that the same reference frame transform terms in (5) and (6) are used for the inverse transformation. In this way, the commanded voltages for the conditioning inverter will be in phase with the bulk staircase voltage output, even though a phase delay was introduced by the LPF blocks that formulated the transformation terms.

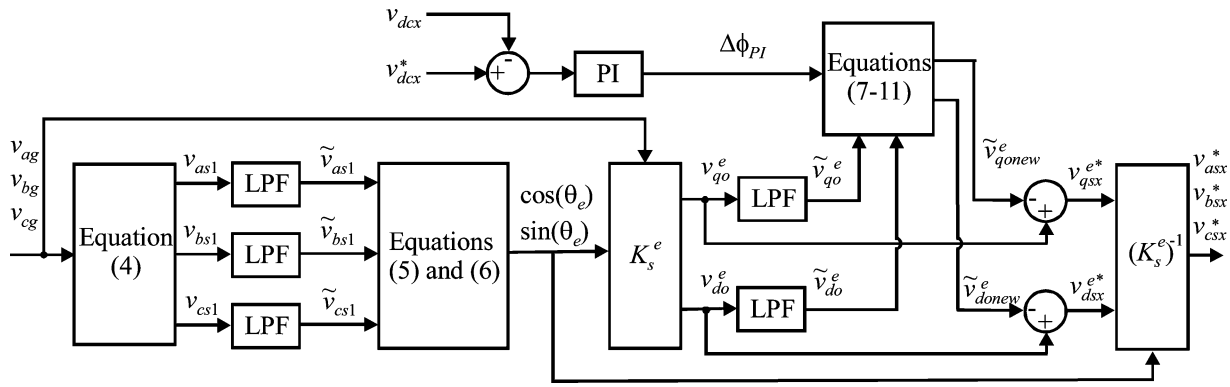

Fig. 6. Conditioning inverter voltage controller block diagram.

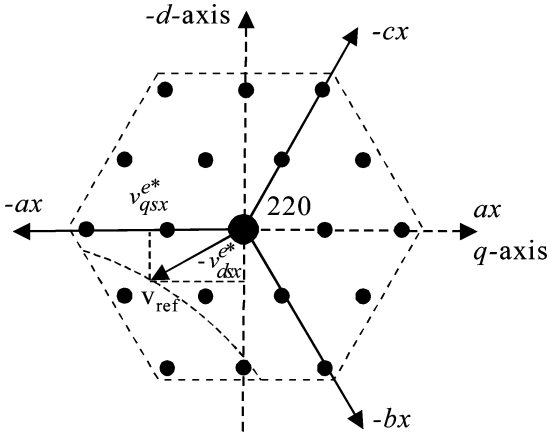

Fig. 7. Conditioning inverter reference.

The vector plot of Fig. 7 will be used to gain a more insightful look at the operation of the hybrid modulation control. This plot is the same shaded sub-hexagon in Fig. 2, when the bulk inverter stays at the switching states 220. The dotted curve represents the circular vector path taken by the fundamental voltage of the bulk inverter. In each DSP cycle, a certain vector in the circular path (such as $v_{\rm ref}$) and its projections onto q- and d-axis in the sub-hexagon will be computed as v^{e*}_{qsx} and v^{e*}_{dsx} by the algorithm just introduced. The origin of $v_{\rm ref}$ is now at vector 220 and for the conditioning inverter, it's switching states and duty cycles within a DSP clock cycle can be determined by first converting the v^{e*}_{qsx} and v^{e*}_{dsx} into the reversed a–b–c coordinates, then using either space vector modulation or its equivalent per-phase duty cycle modulation [14] to find three nearest vectors in the sub-hexagon which can synthesize $v_{\rm ref}$.

Fig. 8 is a graphical representation of the function of the PI control which maintains v_{dcx} at $v_{\rm dc}/3$. Therein, vectors corresponding to the load voltage and current are shown as rotating vectors along with the synchronous reference frame. The effective voltage magnitude and angle from the bulk inverter are first determined using

$$\left|\hat{v}^e_{\rm qdo}\right| = \sqrt{\left(\tilde{v}^e_{qo}\right)^2 + \left(\tilde{v}^e_{do}\right)^2} \tag{7}$$

$$\phi_v = \tan^{-1}\left(\frac{-\tilde{v}^e_{do}}{\tilde{v}^e_{qo}}\right). \tag{8}$$

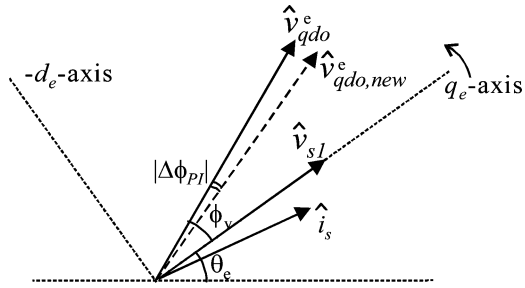

Fig. 8. Phasors in synchronous q–d frame.

Next, the PI regulator term is added to adjust the voltage angle

$$\phi_{\rm v,new} = \phi_v + \Delta\phi_{\rm PI}. \tag{9}$$

Finally, the q–d terms are recombined to form new q- and d-axis voltages (with the same magnitude but with an altered angle) using

$$\tilde{v}^e_{\rm do,new} = -\left|\hat{v}^e_{\rm do}\right|\sin(\phi_{\rm v,new}) \tag{10}$$

$$\tilde{v}^e_{\rm do,new} = \left|\hat{v}^e_{\rm qdo}\right|\sin(\phi_{\rm v,new}). \tag{11}$$

Altering the phase angle as in (9) has the following effect. When the commanded voltage vector $\hat{v}^e_{\rm qdo,new}$ is adjusted to slightly lag the bulk inverter fundamental $\hat{v}^e_{\rm qdo}$ by $|\Delta\phi_{PI}|$, the angle between $\hat{v}^e_{\rm qdo,new}$ and current vector $\hat{i}_s$ is decreased. Therefore, more real power is commanded from the conditioning inverter than is necessary and the average power flow from the conditioning inverter becomes positive since it not only compensates the harmonics in the bulk inverter output (a process which has zero net power flow) it also attempts to provide the difference between the commanded real power and the real power from the bulk inverter. This tends to discharge the conditioning inverter capacitor bank since it has no dc source. When $\hat{v}^e_{\rm qdo,new}$ slightly leads $\hat{v}^e_{\rm qdo}$, the commanded load power is less than that provided by the bulk inverter. Hence, the resulting PWM command of the conditioning inverter tends to absorb the extra real power, and charges its capacitor bank.

It is also possible to regulate the capacitor by adjusting the magnitude instead of the phase angle of $\hat{v}^e_{\rm qdo,new}$ to direct more

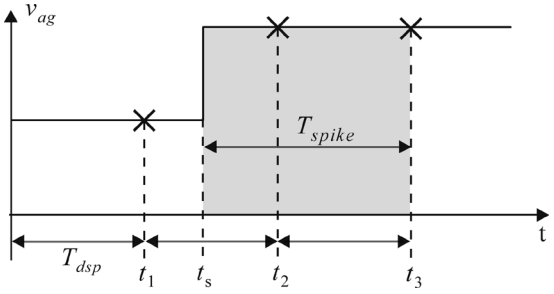

Fig. 9. Un-synchronization due to DSP computation delay.

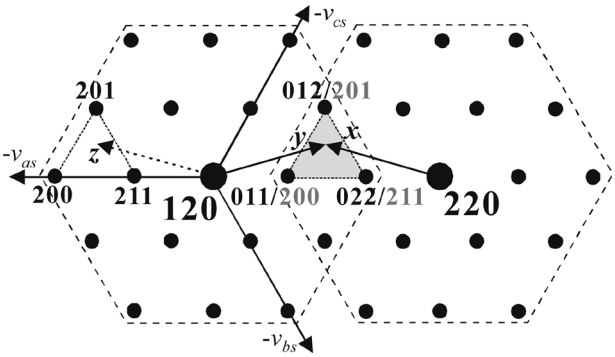

Fig. 10. Visualization of un-synchronization problem and the solution.

or less average power flow into and out of the conditioning inverter. Both methods have been verified in simulation and experiment and the phase angle control was proven to be more effective and used in the final prototype.

B. Conditioning Control Synchronization

The above described control and PWM is computed at every clock cycle of the DSP and cannot instantaneously output the gate signals. In practice, there's always one DSP cycle delay between the bulk output and conditioning inverter output. While this effect is negligible for most of a fundamental cycle, it poses serious un-synchronization problems at the point where one phase of the bulk inverter voltage steps up or down. The delay time in this case will be between one and two DSP cycles as designated by $T_{\rm spike}$ in Fig. 9. Therein, the a-phase bulk line-to-ground voltage is shown at a time when it steps from the mid-point to the full dc voltage. First, the bulk voltage steps up at time t_s, which is an unsynchronized position within a DSP cycle and the time between t_s and the end of the current DSP cycle t_2 is a random number between 0 and a full DSP cycle T_{dsp} (between 0 and 100 μs for 10 kHz sample period). The other part of the delay is one fixed DSP cycle (100 μs for example) starting from t_2. In this cycle, the DSP samples the new bulk voltage and computes the correct conditioning inverter transistor signals and latches them to be output to the inverter gates in the next DSP cycle (starting at t_3).

During $T_{\rm spike}$, the sudden step up (or down as the case may be) of the bulk inverter voltage at one phase needs to be instantly compensated by synchronized three phase conditioning inverter output; otherwise the per-phase load voltage will have a significant leap to an erroneous value. This problem is analyzed in Fig. 10 which is a zoomed-in look at the two neighboring

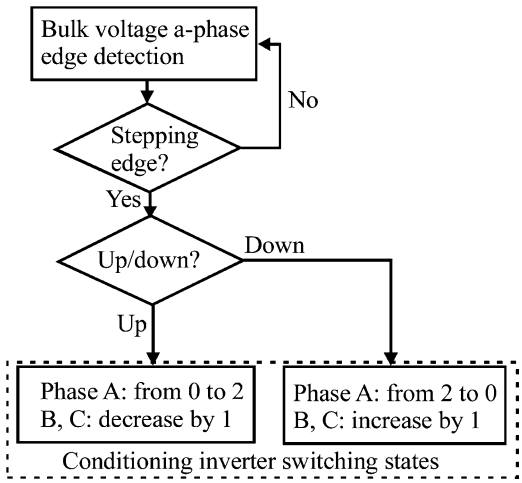

Fig. 11. Flow chart of the edge detection synchronization (a-phase).

sub-hexagons centering at the bulk vectors 220 and 120. The highlighted triangle region is their overlapped area. The three vertices of the three vectors are labeled with the conditioning inverter switching states belonging to each sub-hexagon. It also represents the vector's projection onto the reversed a–b–c coordinates in each sub-hexagon as introduced previously. When the reference vector "x" of the conditioning inverter is inside the triangle and the bulk inverter is at state 220, "x" is synthesized by switching the conditioning inverter at states (201), (211), and (200) with certain timing sequence . Suddenly, the bulk inverter voltage jumps to the state 120 (i.e., the voltage v_{ag} steps down from the top voltage level down to the mid-point). Then with the bulk vector 120 as the new origin, the conditioning inverter should use the new set of switching states of (012), (022), and (011) to synthesize the vector "y," which points to the same combined output as before the bulk inverter transition edge. However, during the time $T_{\rm spike}$ following this transition, the new switching states and timing are not yet computed; the old states (201), (211), and (200) are still being used. The resulting vector "z" and the combined output vector has a large leap towards an erroneous position which amounts to a large voltage spike with considerable time duration of $T_{\rm spike}$ in the phase voltage of the load.

Therefore, the problem is how to find the correct switching states immediately after the bulk transition without DSP calculation. The solution lies in the same Figure. For the three vectors of the overlapped triangles that originated from bulk vector 220, their a-phase conditioning inverter switching states are purely at level 2. For the same set of vectors originated from bulk vector 120, their a-phase switching states are all level 0. So immediately after the v_{ag} step down from the state 2 to 1, the correct conditioning inverter switching states must change from all 2 to all 0 in phase a. Using a similar argument, the b-, c- phases need to be increased by one level from those used right before the bulk phase A step-down occurred. Similar logic can be applied to the other overlapped regions where the bulk voltage step (up or down) occurs in certain phase. The solution is summarized for the a-phase logic in the flow chart shown in Fig. 11.

The discovery above makes instant synchronization between bulk and conditioning inverter possible and practical. Since immediately after the bulk inverter edge, the conditioning inverter

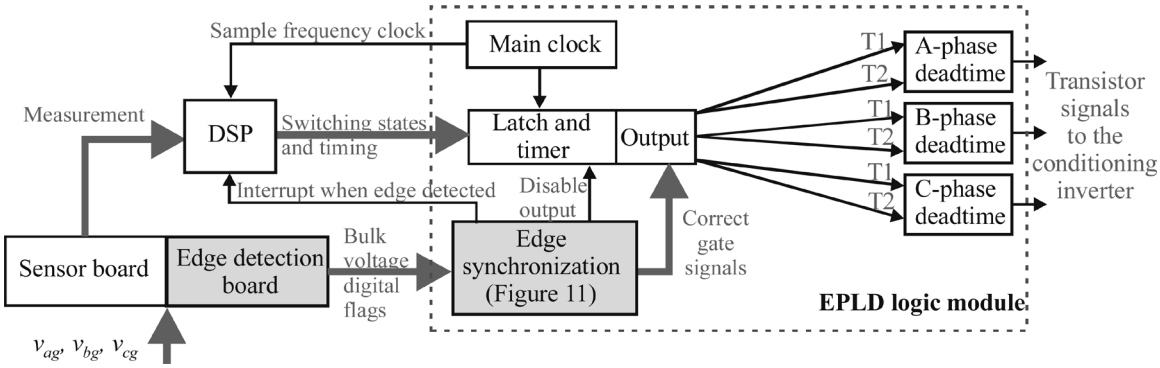

Fig. 12. Hardware implementation block diagram.

TABLE I
INDUCTION MACHINE PARAMETERS

$poles = 4$	$M = 64.4\,\text{mH}$
$r_s = 0.4\,\Omega$	$L_{ls} = 5.73\,\text{mH}$
$r_r' = 0.227\,\Omega$	$L_{lr}' = 4.64\,\text{mH}$

switching states and transistor signals require no DSP calculation and can be programmed into FPGA firmware. Here the only delays of the conditioning inverter output are the propagation delay of FPGA (in the order of nanoseconds) and the dead-time delay in the conditioning inverter PWM which is inherent and not avoidable in the distributed control. However, it will be shown from the lab results that the effect of dead-time delay is negligible and can be handily removed using a light filter at the load.

A block diagram of the implementation is presented in Fig. 12. At the input side, there is voltage sensor and edge detection circuitry constructed in hardware. Whenever the bulk inverter output steps, the edge detection circuit outputs digital flags to disable the gate signal output from the DSP and replace them with (correct) signals programmed in firmware. At the same time, the DSP is interrupted and a new cycle is initiated to calculate the conditioning inverter output with the updated bulk inverter voltages. After this new cycle, the edge handling logic will enable the DSP gate signal output again until the occurrence of the next bulk edge.

IV. LABORATORY VALIDATION

The bulk and conditioning inverters were constructed in the laboratory for validation of the proposed control. The bulk inverter is controlled by a Cypress CY37128P84 CPLD with staircase modulation. A TI TMS320C32 DSP and Flek-10K EPLD were used for the conditioning inverter control.

For the studies presented herein, the bulk inverter dc voltage applied was 320 V. The bulk commanded frequency is 60 Hz and the firing angle was set to $\alpha = 18^\circ$. This will produce a peak fundamental phase voltage of 194 V according to (1). A four-pole 3.7-kW induction machine with parameters listed in Table I was used as the load to test the prototype inverter. The induction machine was operated at 186.9-rad/s with an output torque of 20.9-N · m resulting in an output power of 3.9 kW.

Fig. 13 shows the laboratory measurements. The first two traces show the bulk and conditioning inverter a-phase line-to-ground voltages v_{ag} and v_{agx}. These depict the split between the higher-voltage low-frequency bulk inverter and the lower-voltage high-frequency conditioning inverter. The effect of the conditioning PWM is to compensate the bulk inverter

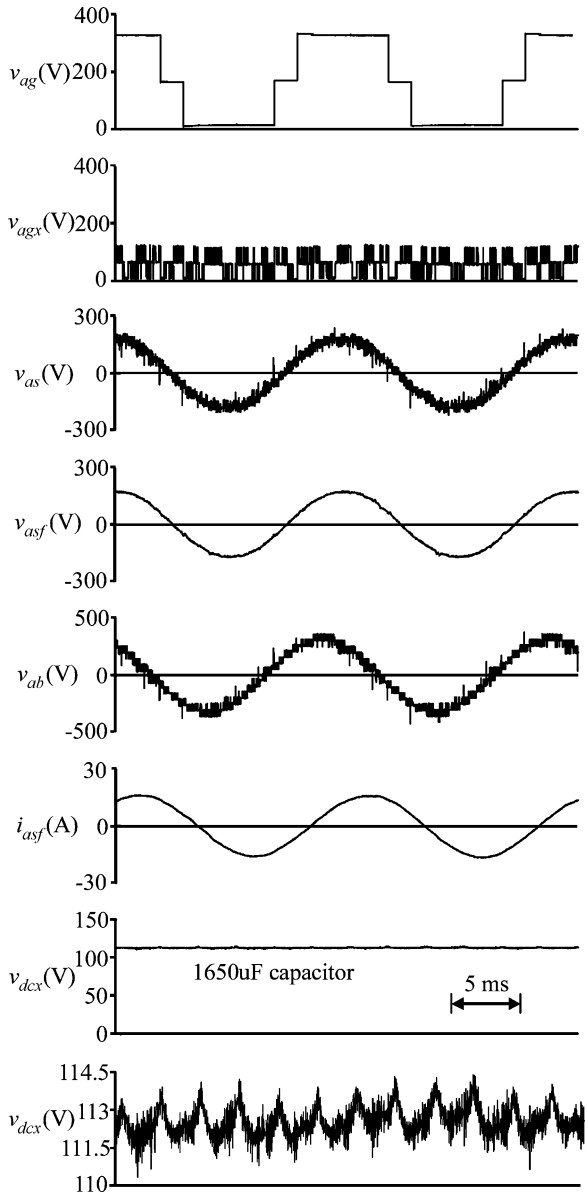

Fig. 13. Distributed control laboratory measurements.

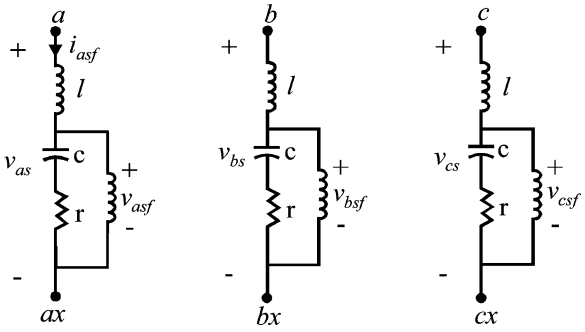

Fig. 14. RLC PWM filter.

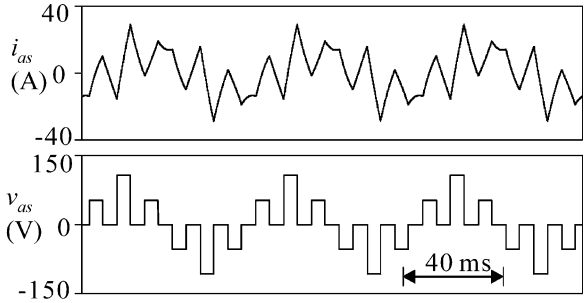

Fig. 15. Bulk inverter phase voltage and motor current at $\alpha = 75.5°$, m =1/4 and f = 15 Hz, without conditioning inverter.

TABLE II
MEASURED THD VALUES

$THD(v_{as}) = 12.2\%$	$THD(v_{asf}) = 5.5\%$
$THD(v_{ab}) = 11.8\%$	$THD(i_{asf}) = 5.3\%$

harmonics. To illustrate this, a small PWM filter with a cut-off frequency of 1-kHz was used in the experiment as shown in Fig. 14. The resulting filtered voltage v_{asf} was applied to the induction motor and is shown as the fourth trace in Fig. 13. As can be seen, the filtered voltage is very smooth. Although the edge detection circuit and EPLD synchronize with the bulk inverter, the transistor dead-time results in some voltage spikes as seen in v_{as}. The dead-time in this circuit was set to 3 μs, but the PWM filter completely removes these spikes. The next trace is the effective line-to-line voltage v_{ab} which is the difference of v_{as} and v_{bs}. This is shown for comparison to a typical multilevel inverter. In this case, the hybrid inverter is operating with eight effective levels. Therefore, the line-to-line voltage will have fifteen distinct levels (seven positive, seven negative, and zero). The fifteen levels can be seen in the v_{ab} waveform. The last three traces are the a-phase motor current i_{asf} and the conditioning inverter capacitor voltage v_{dcx}, and the zoomed in view of v_{dcx} to show voltage ripple. The capacitor voltage v_{dcx} is well regulated at one-third of the bulk voltage by the PI control and the voltage ripple is very small. The THD values are listed in Table II. Herein, the THD is defined as

$$THD(v_x) = \frac{\sqrt{v_{\mathrm{x,rms}}^2 - v_{\mathrm{x1,rms}}^2}}{v_{\mathrm{x1,rms}}} \tag{12}$$

where $v_{\mathrm{x,rms}}$ is the true rms voltage and $v_{x1,rms}$ is the rms value of the fundamental component of v_x. The THD of v_{as} and v_{ab} would typically be around 9% for the hybrid inverter [15]. However, they are increased in the distributed control due to the transistor dead-time after synchronization. With a filtered load voltage having a THD of about 5%, one might expect the load current THD to be much less. However, the motor tooth saturation distorts the current waveform resulting in a current THD which is around 5%.

V. PRACTICAL CONSIDERATIONS

To make the distributed control fully functional in practical motor drive applications, various implementation details are discussed in this section, particularly the set of solutions for low modulation index operation performance degradation. The COTS bulk inverter is an independent motor drive unit which can run the motor without the conditioning inverter. Its design consideration details are beyond the scope of the paper. Generally, to be compatible with the staircase converter modulation, the COTS motor drives to be used are most likely the scalar control (Volts/Hertz), which are suitable for mega-Watt propulsion drives with a relatively slow transient. As discussed in detail below, certain design considerations of the COTS bulk inverter do have impact on the overall system performance. The complete set of distributed control methods (including distributed modulation, capacitor voltage regulation and instant synchronization) were simulated for the wide range of power factors (0.05 to 0.95), speed/frequency (10-Hz to 60-Hz), load (746-W to 75-kW), and phase voltage magnitude (40 to 400 V). Satisfactory results were obtained in all cases.

A. Low Modulation Index Performance Degradation and Improvement Options

Generally, for any multilevel topologies, low modulation index has much lower performance both for PWM and staircase switching schemes. In this specific application with cascaded bulk and conditioning inverters, the modulation index lower than 1/2 (staircase angle $90° > \alpha > 60°$) is defined as low m-index region and its performance degradations can be classified into three categories. For each issue, a solution is briefly introduced as follows. Then an all-in-one solution is discussed which involves bulk inverter control design. Detailed simulations are shown in subsequent sub-section B to illustrate the improvement.

1) Underused Multilevel Potentials: The obvious reason for performance degradation is the reduced number of output voltage levels with lower m-index and smaller circular locus radius in the space vector plot. For example, the m =1/2 results in five levels and m =1/4 results in only a three-level performance.

2) Heavily-Harmonic-Distorted Bulk Inverter Output when $90° > \alpha > 60°$: Another low m-index issue is illustrated in Fig. 15, which shows the phase voltage of the bulk inverter at m =1/4 ($\alpha = 75.5°$). Obviously, considerable amount of low frequency harmonics deform the phase current beyond any resemblance of sinusoidity, requiring much more conditioning inverter reactive power compensation. This implies higher capacitor voltage ripple. Moreover, it poses difficulty for the LPF

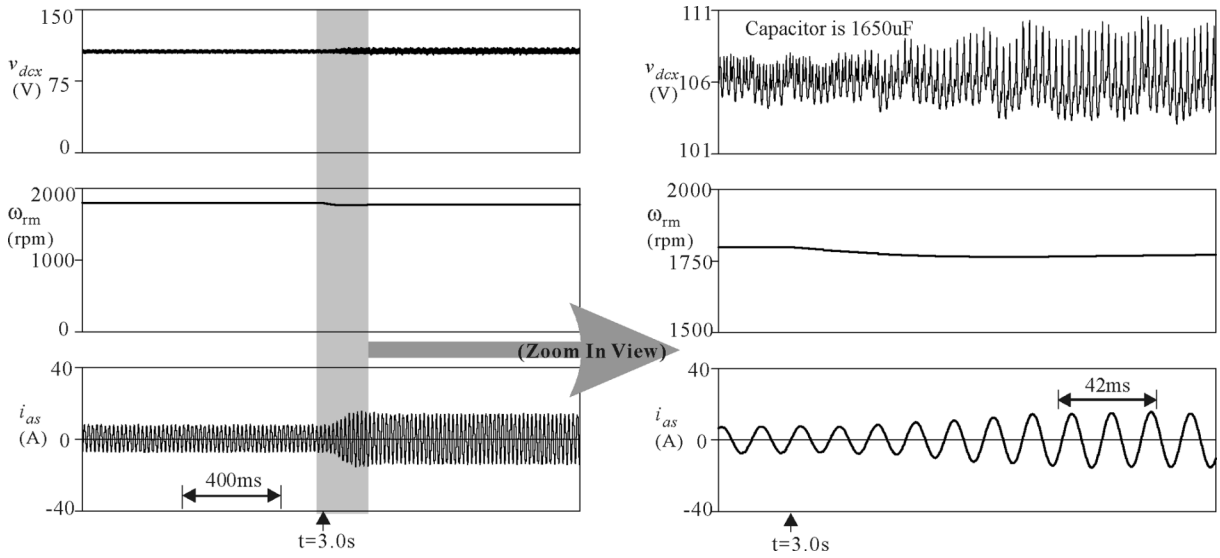

Fig. 16. Motor no-load to full load step simulation at full speed (60 Hz) with $\alpha = 18^\circ$, and $m = 0.951$.

which filters the bulk phase voltage to have a sinusoidal synchronous reference frame (shown in Fig. 6). As verified by simulations, it becomes hard to get pure sinusoidal reference by simple LPF at low m-index, which results in inaccurate extraction of the bulk fundamental component. To solve the problem, a phase locked loop (PLL)block can be added between the LPF block and the synchronous transformation block (in Fig. 6) to obtain the pure sinusoidal reference terms at the same frequency as the bulk inverter voltage. The rest of the control remains the same.

3) The 3:1 Voltage Ratio in Single dc Source Operation: A voltage ratio of 3:1 between the bulk and conditioning inverter cells, also known as "maximal distension" for cascaded inverter topology, gives highest number of output levels. However, as discussed in the literature [16], when operated with single dc source, certain ranges of m-index will result in a non-continuously-sinusoidal phase voltage, which degrades its THD performance from ideal multilevel PWM. The phenomenon is best explained in space vector perspective. First, the bulk vector traversal pattern and timing are fixed, since the bulk inverter fundamental must be fixed as it is the only real power supplier. Then, due to its smaller dc voltage v_{dcx} at 1/3 of the bulk inverter voltage $v_{\rm dc}$, a certain portion of the load voltage vector circular path is beyond the harmonic compensation range of conditioning inverter. Note that such operating range issue is inherent in the single dc source operation of cascaded inverter topologies, no matter if it is distributed controlled or jointly controlled. The detailed analysis and complete mathematical derivation of the operating range issues is described in the literature [17]. It defined quantitatively the m-index ranges with degraded performance. These problematic ranges are expressed in terms of the staircase angle α. They are regions a few degrees around 30° and most of the region between 60° and 90°, which is exactly the low m-index region. For a proximity of $\alpha = 30^\circ$, there is a solution to avoid the problem, however, the low m-index region $(90^\circ > \alpha > 60^\circ)$ has degradation unavoidable by all means. The solution here is to reduce the system into voltage ratio of 2:1, because it is proven that the 2:1 ratio has an ideal operating range for the full range of m-index. Certainly, the number of output levels will be reduced with 2:1 ratio. The dynamic changing of voltage ratio between 3:1 and 2:1, depending on whether m-index is above or below 1/2, is a viable option with robust capacitor voltage regulation control. Or for control simplicity, it might use only a 2:1 voltage ratio to accommodate the low m-index operation.The same set of distributed control methods can be used with either a 3:1 or 2:1 voltage ratio.

4) All-In-One Solution: One solution exist for each type of performance degradation at low m-index, and they can be integrated into the conditioning inverter control; however, the best and all-in-one solution lies in the bulk inverter design itself which could take advantage of an active dc front end. For the phase voltage magnitude $|v_{as}|$ between rated and half rated value, the m-index is adjusted by varying α, then for lower values of $|v_{as}|$, the m-index is fixed at 1/2 ($\alpha = 60^\circ$), and the bulk inverter front end dc voltage $v_{\rm dc}$ can be adjusted accordingly with the rectifier firing angle. Meanwhile the capacitor voltage regulation control can track the change very well and always keep v_{dcx} at 1/3 of $v_{\rm dc}$. If the bulk inverter controller design can satisfy the above description, the low m-index operating range will be simply avoided and the related problems will be solved all at once. It also guarantees that the voltage output has at least five-level performance and the 3:1 ratio can be used without any operating range issue.

B. Step Load Under Various Operating Conditions

To demonstrate the distributed control at different voltage magnitudes (by varying m-index or the dc front end voltage) and output fundamental frequency (for variable speed motor drives), Figs. 16 and 17 show the simulations of the distributed control at different motor speeds with a step change in load torque. Note that for motor drive application, it is more relevant to study the cases where the phase voltage magnitude and frequency output are kept directly proportional. The motor parameters are the same as the ones used previously in lab test.

Fig. 16 shows the motor steps from no-load to the rated load at $t = 3.0$s 3.0 s. The three traces from top to bottom are capac-

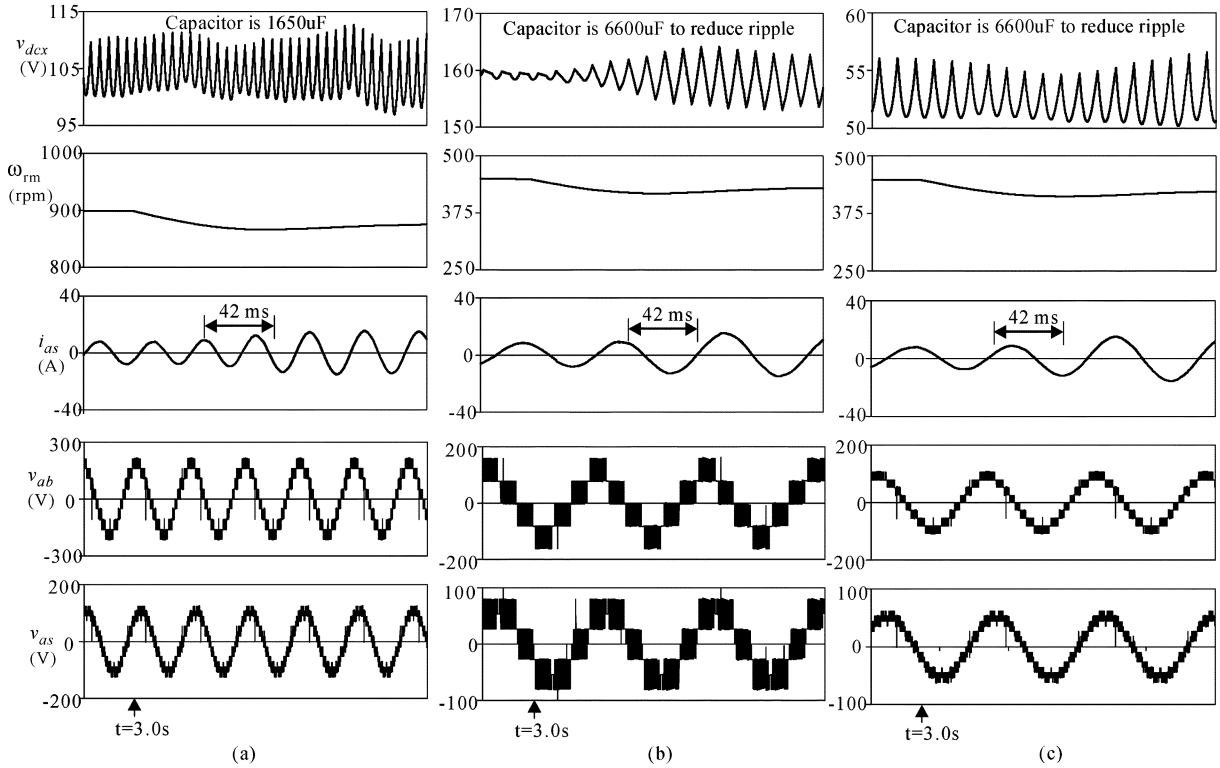

Fig. 17. Motor no-load to full load step simulation at different phase voltage magnitudes/frequencies. (a) At halfspeed (30 Hz), 1/2 rated voltage 1/2 m-index with a $\alpha = 60°$, (b) at 1/4 speed (15 Hz), 1/4 rated voltage 1/4 m-index with $\alpha = 75.5°$, voltage ratio 2:1 used, and (c) at 1/4 speed (15 Hz), 1/4 rated voltage 1/2 m-index. with $\alpha = 60°$; 1/2 Vdc.

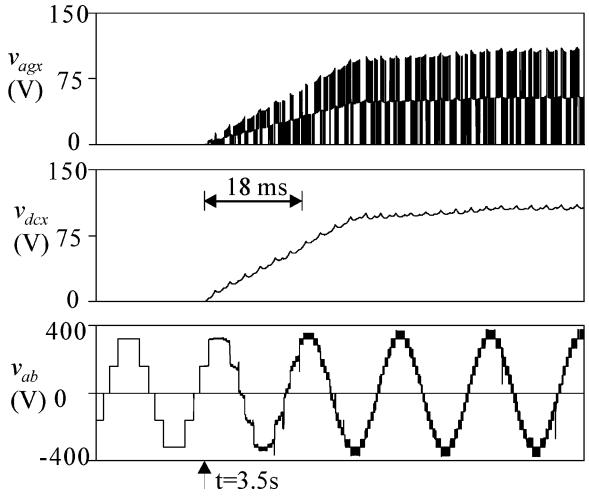

Fig. 18. Conditioning inverter switch-on simulation.

itor voltage, motor speed, and phase current. Then three more cases with lower speed/lower voltage magnitude are presented in Fig. 17. The five traces from top to bottom are respectively capacitor voltage, motor speed, phase current, equivalent line-line voltage and phase voltage. Specifically, Fig. 17(a) shows the half speed operation with 30 Hz frequency. Meanwhile the voltage magnitude is half the rated value by setting bulk staircase angle $\alpha = 60°$. Fig. 17(b) shows the 1/4 speed operation with 15 Hz frequency. Meanwhile the voltage magnitude is at 1/4 of rated value by setting bulk staircase angle at 75.5°. To address the low m-index performance degradation, 2:1 voltage ratio and PLL loop are used. Fig. 17(c) shows the 1/4 speed operation with 15 Hz output frequency. Meanwhile the voltage magnitude is at 1/4 of rated value by setting bulk staircase angle at 60° (half m-index) and bulk inverter dc voltage at half rated value (320 V/2). The m-index lower than 1/2 are simply avoided in this case. In all four cases, with the distributed control operated as a VSI, the phase voltage and line-line voltage are obviously not affected by the load change. It only changes the phase current magnitude and its phase angle. After the short transient, the phase angle between the v_{as} and i_{as} decreases due to the power factor change. The capacitor voltage remains stabilized after the sudden load step; while the voltage ripple change is observable mainly due to the higher level of power flow in and out of the capacitor bank. Another observation from the Fig. 17 is the obvious advantage of using the adjustable bulk inverter dc voltage at low voltage output. Five-level performance is achieved in case (c), compared with the three-level output in case (b) using solely the m-index to adjust the phase voltage magnitude.

The capacitor selection is based on the detailed simulations with various operating speed/voltage/load. It can be geometrically proven that in single dc source operation, the conditioning inverter capacitor voltage ripple frequency and its shape are determined by the bulk inverter m-index. Also, its peak-to-peak value is dependent on factors like the fundamental output frequency, output power, capacitor operating voltage, and capacitance. For 3.7 kW operation, 1650 μF capacitor is selected (as in experiment prototype) when operating at normal frequency and the dc voltage deviation is less than 5%. When operating at low frequency as in Fig. 17(b) and (c), a larger capacitor (6600 μF) is needed for the same performance.

C. Conditioning Inverter Capacitor Initial Charging Options

For initial capacitor voltage build-up with two cascaded inverter cells, certain combinations of bulk/conditioning inverter switching states can form a charging path to the conditioning inverter capacitor. For example, if the conditioning inverter gate signal output is disabled, and the bulk inverter is at state "2,0,0," a charging path to the conditioning inverter capacitor will be created (via parallel diodes of condition inverter and motor windings (see Fig. 1). By commanding the state "2,0,0" with a certain duty ratio (digital hysteresis current control), the voltage vdcx can be charged to the rated value without transient over-current. However, this generic precharging methodology (without extra hardware) only applies in jointly controlled bulk/conditioning inverters. In the distributed control, the COTS bulk inverter is not supposed to be controlled together with conditioning inverter to create the charging path. For the distributed control, the following two capacitor charging options are available.

1) Offline Precharging: Precharging its capacitor before turning on the conditioning inverter requires extra hardware. It is used to form a charging path from the bulk inverter dc source through the conditioning inverter capacitor (such as one IGBT switch and current limiting resistor). After precharging, the IGBT will be turned off to guarantee the voltage sources isolation.

2) Online Charging: Since the bulk inverter can run the motor independently (with considerable low frequency harmonics), the user has the option to switch on the conditioning inverter at any time during motor operation with or without its capacitor precharged. Its capacitor voltage can be built-up and stabilized by the voltage regulation control previously introduced. Fig. 18 shows the simulation of the conditioning inverter start-up and its capacitor voltage build-up process. Initially, the bulk inverter operates alone while the conditioning inverter three-phase switching states are commanded at "0,0,0," as a shorted neutral point for bulk inverter. Then at $t = 3.5$ s, the conditioning inverter is enabled. Computation and gate signal output then start. After a short while (about two fundamental cycles), the PI controller has fully charged the capacitor to 1/3 of the bulk dc voltage. Meanwhile the conditioning inverter output becomes well synchronized with the bulk inverter and equivalent eight-level performance is achieved, in comparison with the staircase shape of v_{ab} before the conditioning unit is switched on.

VI. Conclusion

This paper presented a distributed control for the hybrid inverter. The hybrid inverter is unique in that two three-level inverters are used to drive the motor load. The "bulk" inverter operates at a higher-voltage and low-frequency and provides the power to the machine. The other inverter drives the opposite end of the motor windings with a lower-voltage high-frequency PWM and serves as an active filter or "conditioning" inverter. Since two three-level inverters are used, the resulting waveforms have exceptional power quality. With the proposed distributed control, the bulk inverter can be used with its COTS controller. The conditioning inverter senses the bulk voltages in order to compensate the harmonics of the bulk inverter and also synchronize to the bulk inverter steps. This makes the conditioning inverter control independent of the bulk inverter. Furthermore, a component of the conditioning inverter control regulates it's dc voltage so that it can be supplied from a capacitor. This is useful in Naval drive applications where extra voltage sources at high power levels are difficult to create. The solution to the instant synchronization between two inverters is then proposed. The proposed control was validated in the laboratory on a 3.7-kW induction motor drive. Finally, the reasons and solutions for possible problems in practical implementation are comprehensively discussed.

References

[1] K. A. Corzine, M. W. Wielebski, F. Z. Peng, and J. Wang, "Control of cascaded multi-level inverters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 732–738, May 2004.

[2] K. A. Corzine, S. D. Sudhoff, and C. A. Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. Energy Conv.*, vol. 14, no. 3, pp. 433–439, Sep. 1999.

[3] K. K. Mohaparta, V. T. Somasekhar, and K. Gopakumar, "A harmonic elimination scheme for an open-end winding induction motor drive fed from two inverters using asymmetrical D.C. link voltages," *Eur. Power Electron. J.*, vol. 12, no. 4, pp. 28–35, Sep./Oct./Nov. 2002.

[4] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, A. Pittet, and V. T. Ranganathan, "Space vector PWM control of dual inverter fed open-end winding induction motor drive," *Eur. Power Electron. J.*, vol. 12, no. 1, pp. 9–18, Feb. 2002.

[5] K. K. Mohapatra, K. Gopakumar, V. T. Somasekhar, and L. Umanand, "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1187–1198, Dec. 2003.

[6] Y. Kawabata, M. Nasu, T. Nomoto, E. C. Ejiogu, and T. Kawabata, "High-efficiency and low acoustic noise drive system using open-winding AC motor and two space-vector-modulated inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 783–789, Aug. 2002.

[7] K. Iwaya and I. Takahashi, "Novel multilevel PWM wave control method using series connected full bridge inverters," in *Proc. IEEE Int. Elect. Machines Drives Conf.*, Jun. 2003, vol. 3, pp. 1543–1548.

[8] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 1993, vol. 5, pp. 7–14.

[9] S. Kwak and H. A. Toliyat, "A hybrid solution for load-commutated-inverter-fed induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 1, pp. 83–90, Jan./Feb. 2005.

[10] S. Kwak and H. Toliyat, "A current source inverter with advanced external circuit and control method," in *Proc. IEEE Int. Elect. Machines Drives Conf.*, San Antonio, TX, May 2005, pp. 1327–1334.

[11] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[12] D. Peng, F. C. Lee, and D. Boroyevich, "A novel SVM algorithm for multilevel three-phase converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2002, vol. 2, pp. 509–513.

[13] B. P. McGrath, D. G. Holmes, and T. A. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[14] K. A. Corzine and J. R. Baker, "Multilevel voltage-source duty-cycle modulation: analysis and implementation," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1009–1016, Oct. 2002.

[15] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[16] S. Lu, K. A. Corzine, and T. H. Fikse, "Advanced control of cascaded multilevel drives based on P-Q theory," in *Proc. IEEE Int. Elect. Machines Drives Conf.*, May 2005, pp. 1415–1422.

[17] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, Mar./Apr. 2005.

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