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DC Power-Bus Modeling and Design With a Mixed-Potential Integral-Equation Formulation and Circuit Extraction

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***Abstract*—Application of a circuit extraction approach based on a mixed-potential integral equation formulation (CEMPIE) for dc power-bus modeling in high-speed digital designs is detailed herein. Agreement with measurements demonstrates the effectiveness of the approach. Dielectric losses are included into the calculation of Green's functions, and thus, incorporated into the rigorous first principles formulation. A SPICE model is then extracted from the discretized integral equation. A quasistatic approximation is used for Green's functions to keep the extracted circuit elements frequency independent. Previous work has established a necessary meshing criterion in order to ensure accuracy for a given substrate thickness and dielectric constant to a desired frequency. Several power-bus design issues, such as surface mount decoupling and power-plane segmentation, were investigated using the modeling approach. The results and discussions illustrate the application of the method to dc power-bus design for printed circuit and multi-chip module substrates.**

***Index Terms*—Circuit extraction, dc power-bus design, dielectric losses, mixed-potential integral equation formulation, segmented power plane, surface mount decoupling.**

I. Introduction

A CIRCUIT Extraction approach based on a Mixed-Potential Integral Equation formulation (CEMPIE) is suitable and effective for dc power-bus modeling in high-speed digital designs [1], [2]. The method is an extension of the partial element equivalent circuit approach (PEEC) to a multi-layer printed circuit substrate [3]–[5]. As a PEEC-type method, the CEMPIE formulation results in an extracted circuit. External circuit models, such as sources, loads, or transmission lines, can then be easily incorporated, and thus, an evaluation of the performance of a printed circuit board (PCB) design can be pursued in a more integrated fashion. The formulation of CEMPIE is based on a mixed-potential integral equation (MPIE), which is discretized and evaluated using a method of moments procedure. Instead of using the free-space Green's function, CEMPIE employs Green's functions for a multi-layer medium, *viz.*, all dielectric layers in an arbitrary substrate stackup configuration are incorporated into the calculation of Green's functions. The integral equation is then constructed only on the metallization surfaces of interest. An equivalent circuit is extracted from the moment matrix without solving the matrix equation. In order to ensure that the extracted circuit elements are frequency independent, a quasistatic approximation is applied to Green's functions. Simulation studies can then be performed in SPICE based on the extract equivalent circuit. The CEMPIE formulation is suitable for any multi-layer substrate including PCBs and multichip modules (MCMs).

Recently, many studies have focused on dc power-bus related issues in high-speed digital designs, using experimental and/or modeling approaches [5]–[9]. There are many signal integrity (SI) and electromagnetic interference (EMI) issues associated with the dc power-bus structures used in a PCB design. One of the main concerns is the simultaneous switching noise (SSN) generated in the power-bus structure by switching devices. This noise can propagate among the PCB circuits via the parallel planes of the power bus, thus interfering with susceptible devices causing system malfunctions, and coupling off the PCB resulting in emissions through apertures, slots, cables, and other radiation mechanisms. High-frequency noise decoupling and isolation techniques are extensively used in a practical design. Surface-mount technology (SMT) capacitors are applied between power and ground layers, decoupling or bypassing noise to prevent its propagation. A common concern is the number of capacitors that are sufficient to mitigate the high-frequency noise. Typically, many capacitors are added to a PCB to mitigate noise. However, these capacitors consume a lot of real estate, limit the routing flexibility, and increase cost as well. The locations of the capacitors can have an impact on the effectiveness as well. Correctly distributing decoupling capacitors may reduce the required number. This is an issue of local decoupling versus global decoupling. Generally, SMT decoupling capacitors have an effective frequency range. When the frequency reaches the point where the parasitic inductance associated with the interconnects (vias and traces) dominates the capacitance value, the total impedance is inductive, and the frequency has exceeded the capacitor's effective frequency range. The inter-plane capacitance, intrinsic to the parallel-plane structure, will then dominate the power-bus impedance through the PCBs distributed resonances. Increasing this inter-plane capacitance by using a higher dielectric constant material, or decreasing the

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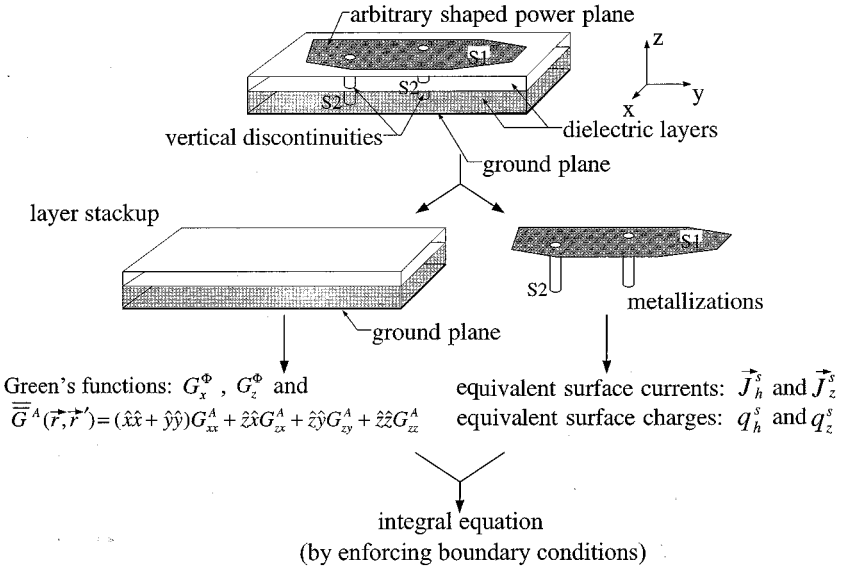

Fig. 1. Power-bus structure with vertical discontinuities.

thickness between power and ground layers, or employing an embedded capacitance layer, is often used in design to mitigate high-frequency noise. However, the utilization of a high dielectric constant material increases the electrical size of the PCB, thus lowering its distributed resonant frequencies. In order to decrease the power-bus impedance at distributed resonant frequencies of the parallel power planes, a lossy material can be used to damp these resonances, and a lower noise voltage on the planes results for the same magnitude of injected noise current.

Segmenting the power plane to prevent noise propagating from its source to susceptible devices is another noise mitigation technique used in digital circuit designs. If a dc connection between two separate portions using the same logic level is necessary, then either a conduction bridge or an SMT ferrite bead is used. This connection and other geometrical dimensions, such as the gap width, location, and shape, impact the isolation that can be achieved. Further, the RF isolation can affect the EMI performance of the PCB as well. All of these issues impact the power-bus design, however, no methodical and proven design guidelines are well established. The CEMPIE approach detailed herein can accommodate various power-bus design features, such as SMT decoupling capacitors, interconnects, arbitrarily-shaped power islands, board thickness and dielectric materials, and losses. It is an effective means for developing power-bus design guidelines, as well as for a specific design evaluation.

An overview of the MPIE formulation of the CEMPIE approach is given in Section II. Dielectric losses are included in the CEMPIE modeling in the examples presented in this paper as well, and the incorporation in the formulation is detailed. Instead of using a real number for the relative permittivity (ϵ_r), a complex number is employed with the imaginary part characterizing the loss behavior of the material. A frequency-dependent conductance results in the extracted circuit model to reflect the dielectric losses. Section III provides comparisons between modeled and measured results. Examples of the application of CEMPIE to dc power-bus modeling are presented in Section IV.

II. Overview of the MPIE Formulation and Treatment of Dielectric Losses

The CEMPIE formulation is based on a mixed-potential integral equation, which is established by applying boundary conditions, as in typical scattering problems. However, it departs from the standard MPIE approach [10], keeping the cell-based scalar potentials as primary unknowns as well as the edge-based currents to derive a standard modified nodal analysis (MNA) circuit equation. The unknown currents are expanded in the Rao–Wilton–Glisson basis functions, and the unknown scalar potentials are related to the charges that can be expressed as a function of the surface divergence of the Rao–Wilton–Glisson basis functions through the current continuity equation. An equivalent circuit is extracted from the discretized matrix equation based on the partial elements. A comprehensive treatment can be found in [1], [2]. An overview is given here for convenience. A typical power-bus structure has two distinct types of metallization surfaces, *viz.*, planar conduction layers (power and ground layers), and surfaces of vertical discontinuities (device vias and test ports). As shown in Fig. 1, all dielectric layers and the ground plane are assumed of infinite size, and Green's functions for the grounded multi-layer medium are calculated. The spectral-domain expressions for Green's functions can be derived based on the concepts of generalized transmission and reflection coefficients [11], since they are fields of a horizontal or vertical electric dipole (HED or VED) embedded in the grounded dielectric slab. These spectral-domain expressions are then approximated into a series of complex exponentials (images), using the generalized-pencil-of-function (GPOF) algorithm [12]–[15]. Every term in the complex exponential series can then be inversely Fourier transformed from the spectral to

spatial domain using the Sommerfeld identity [11]. In this fashion, the spatial-domain expressions for Green's functions are calculated.

The dyadic form of Green's function for vector magnetic potential ($\bar{\bar{G}}^A$), which has four components in a stratified medium [16], is given by

$$\bar{\bar{G}}^A = G^A_{xx}(\hat{x}\hat{x} + \hat{y}\hat{y}) + G^A_{zx}\hat{z}\hat{x} + G^A_{zy}\hat{z}\hat{y} + G^A_{zz}\hat{z}\hat{z} \quad (1)$$

where G^A_{zx}, G^A_{zy} are the induced z-directed vector potentials due to an x-oriented or a y-oriented dipole, respectively, G^A_{xx} is the induced x-directed vector potential due to an x-oriented dipole, and G^A_{zz} is the induced z-directed vector potential due to a z-directed dipole. Green's function for the scalar electric potential is expressed as G^ϕ herein, and is a function of the permittivities of the dielectric layers. Dielectric losses can be accounted for by ascribing a complex permittivity to the material, i.e.,

$$\epsilon = \epsilon' - j\epsilon'' \quad (2)$$

where ϵ' is the real permittivity, ϵ is the equivalent overall permittivity with losses included, and $\epsilon'' = \epsilon' \tan\delta$, where $\tan\delta$ is the loss tangent of the material. Values of loss tangent are experimentally measured or given by the material manufacturer. With the dielectric losses incorporated into G^ϕ, its impact can be rigorously included into the CEMPIE first principles formulation.

The conductor surfaces (excluding the infinite ground plane) are replaced by equivalent surface currents and charges after the dielectric layers and ground plane are accounted for in Green's functions. The total electric field, i.e., the vector sum of the incident electric field and the induced electric field due to the equivalent surface currents and charges, must satisfy boundary conditions on these conductor surfaces. Thus, an electric field integral equation results as

$$\hat{n} \times \left[j\omega \int_{S1+S2} \bar{\bar{G}}^A(\vec{r},\vec{r}') \cdot \vec{J}(\vec{r}')\, ds' + \nabla\phi(\vec{r}) \right] = 0, \quad \vec{r} \in S1 + S2 \quad (3)$$

where

- ϕ induced scalar electric potential;
- $S1$ horizontal planes of concern (power planes);
- $S2$ vertical surfaces of device vias and ports, as shown in Fig. 1;
- $\vec{J}(\vec{r})$ equivalent surface current density.

The incident electric field is assumed to be zero, and is not shown in (3). This is because a circuit extraction approach is used, and excitations can be handled as impressed current sources, which are more straight-forward in the extracted circuit model than the incident electric field is in the first principles formulation.

The integral equation is discretized using the standard method of moments (MOM) procedure. A triangular mesh is generated on the power planes, and the vector basis functions are defined on all the interior edges [17]. The cylindrical vertical discontinuities are approximated by hexagonal cylinders, and a rectangular mesh is applied on their surfaces. The corresponding basis functions are anchored on every horizontal edge, and have the form of one-dimensional linear functions. On the intersections between the triangular and rectangular meshes, current continuity must also be ensured [1]. The current density in (3) is expanded using these two types of basis functions. Then, the integral equation is tested with testing functions that are the same as the basis functions. The inner product of the testing functions with the gradiant of the scalar potential can be expressed as an integral of the divergence of the testing functions times the scalar potential, based on the vector identity. Further assuming that the scalar potential is constant over every mesh cell, a matrix equation results as

$$j\omega[\mathbf{L}][\mathbf{i}] - [\mathbf{\Lambda}][\phi] = 0 \quad (4)$$

where $\mathbf{i}$ is the unknown edge-current vector; ϕ is the unknown cell-potential vector; $\mathbf{\Lambda}$ is the connectivity matrix that relates cell quantities to edge quantities, and whose elements are

$$\Lambda_{\alpha n} = \begin{cases} 1, & \text{if node } n \text{ is the positive end of edge } \alpha \\ -1, & \text{if node } n \text{ is the negative end of edge } \alpha \\ 0, & \text{otherwise.} \end{cases} \quad (5)$$

$\mathbf{L}$ is denoted the *branch-wise inductance* matrix, due to its coefficient $j\omega$ and the relationship between current and voltage. Its elements are

$$L_{\alpha\gamma} \equiv \frac{1}{l_\alpha l_\gamma} \left\langle \vec{f}_\alpha, \int_{S_\gamma} \bar{\bar{G}}^A(\vec{r},\vec{r}') \cdot \vec{f}_\gamma\, ds' \right\rangle \quad (6)$$

where $\vec{f}_\alpha$ and $\vec{f}_\gamma$ are the testing and basis functions, respectively, and l_α and l_γ are the lengths of the edges where the testing and basis functions are anchored.

Let nodal currents $\mathbf{I}$ be defined as the total currents flowing out of the corresponding mesh cells. Then, these nodal currents are related to the edge currents by the connectivity matrix as

$$[\mathbf{I}] = [\mathbf{\Lambda}^T][\mathbf{i}]. \quad (7)$$

Current continuity provides a relationship between charge and current as

$$-j\omega[\mathbf{Q}] = [\mathbf{I}] + [\mathbf{I}^e] \quad (8)$$

where Q_n, I_n, and I^e_n are the charge, the nodal current, and the impressed nodal current associated with Cell n, respectively. The impressed currents are introduced here to accommodate current sources in the circuit simulation.

Since the charge density is constant over each mesh cell, by taking the surface divergence of the selected current basis functions, the unknown cell potentials are related to cell charges as

$$[\phi] = [\mathbf{K}][\mathbf{Q}] \quad (9)$$

where

$$K_{pq} = \frac{1}{A_p A_q} \int_{S_p} \int_{S_q} G^\phi(\vec{r},\vec{r}')\, ds'\, ds. \quad (10)$$

S_p and S_q indicate a surface integration over cell p and q, respectively; and, A_p and A_q are the corresponding cell areas. As

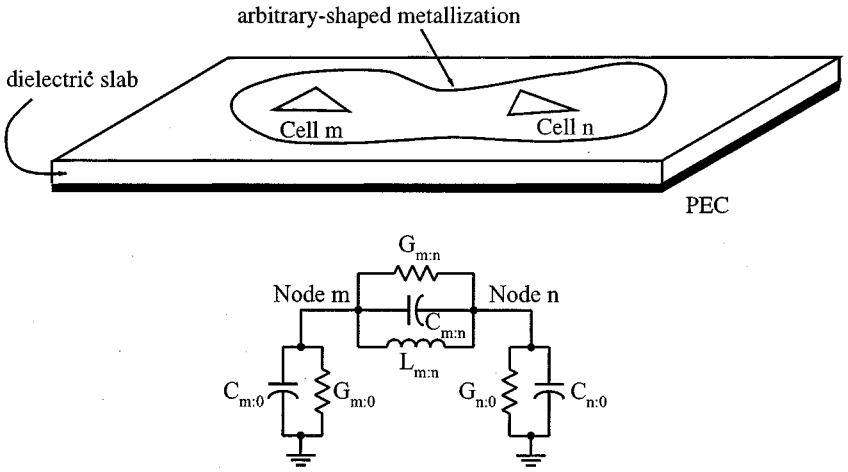

Fig. 2. The equivalent circuit model between any arbitrary pair of two nodes m and n.

mentioned before, G^{ϕ} is a function of material permittivities, which are complex numbers if dielectric losses are included. This makes G^{ϕ}, thus K_{pq} as well, a complex number. Then let

$$[\mathbf{K}^{-1}] = [\mathbf{C}] - j[\mathbf{G_d}] \tag{11}$$

where the $\mathbf{C}$ and $\mathbf{G_d}$ matrices are both real. Due to the relationship between potential and charge, $\mathbf{C}$ is denoted the *cell-wise capacitance* matrix, and $\mathbf{G_d}$ is the *cell-wise conductance* matrix that results from the dielectric losses. Using (4), (8), (7), (9) and (11), a discretized form of a mixed-potential integral equation results as

$$\begin{bmatrix} j\omega\mathbf{L} & -\mathbf{\Lambda} \\ \mathbf{\Lambda}^T & \omega\mathbf{G_d} + j\omega\mathbf{C} \end{bmatrix} \begin{bmatrix} \mathbf{i} \\ \phi \end{bmatrix} = \begin{bmatrix} 0 \\ -\mathbf{I}^e \end{bmatrix}. \tag{12}$$

This equation has the standard form of a Modified Nodal Analysis system of equations that is utilized in many circuit simulators [18].

A relationship between the node (cell) potentials and only the impressed nodal currents can be derived from (12) as

$$[\mathbf{Y}][\phi] = [-\mathbf{I^e}] \tag{13}$$

where the $\mathbf{Y}$ matrix is denoted the *nodal admittance matrix* of the system, and

$$[\mathbf{Y}] = \frac{1}{j\omega}[\mathbf{\Lambda}^T\mathbf{L}^{-1}\mathbf{\Lambda}] + j\omega[\mathbf{C}] + \omega[\mathbf{G_d}]. \tag{14}$$

Instead of directly solving (13), an equivalent circuit model can be extracted from the admittance matrix, by enforcing Kirchoff's Current Law (KCL) at every cell (node) [1]. In order to keep the extracted circuit elements frequency-independent, a quasistatic approximation of Green's functions is employed [2]. This approximation introduces an additional mesh constraint to keep the extracted circuit meaningful and valid for capturing the distributed behavior of the power bus up to a specified upper frequency. This limitation is determined by the highest frequency of interest, layer stackup, and dielectric materials [2].

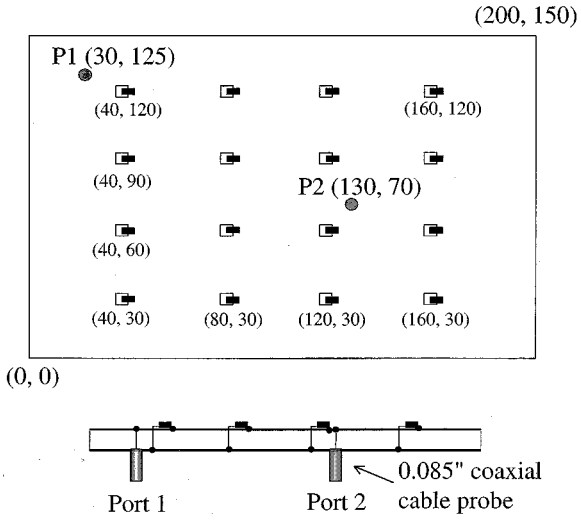

Fig. 3. Two-layer dc power-bus example including SMT capacitor decoupling. Dimensions are in millimeters.

Fig. 2 shows the equivalent circuit between an arbitray pair of Nodes m and n. A parallel LCG branch exists between these two circuit nodes, and there is also a parallel shunt CG between each node and the ground node. For those nodes that are associated with cells that have vertical surface currents flowing into the ground plane, there is an inductance connecting from the node to the ground node as well [1]. The conductance in this model results from the imaginary part of dielectric permittivities, thus, dielectric losses are characterized in the circuit model. The extracted circuit model is then exported into SPICE where well-developed IC source, load, and transmission line models can be incorporated. Various kinds of simulations, such as input impedance, scattering parameters, noise voltage distribution, transient simulations, and so on, can be performed.

III. Comparisons Between Experiments and Modeling

The CEMPIE modeling approach was demonstrated by comparison with experiments. Fig. 3 shows a two-layer PCB test geometry with dimensions of 15 cm $\times$ 20 cm. Sixteen SMT decoupling capacitors, with individual values of 0.01 μF, were uni-

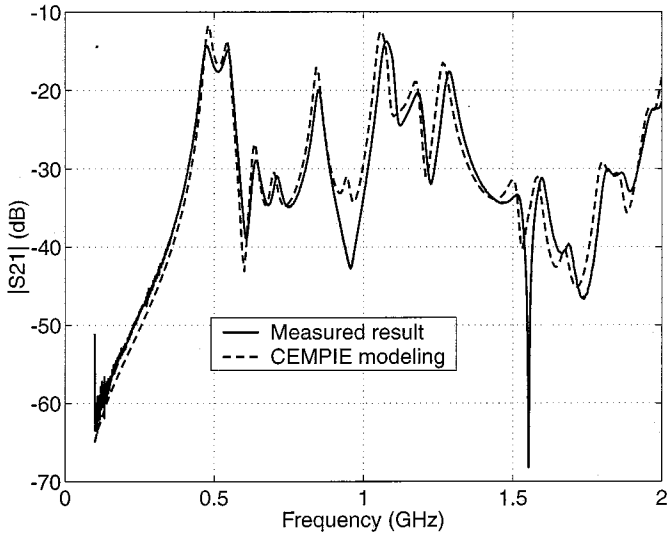

Fig. 4. Comparison between modeled and measured $|S_{21}|$ results for the power-bus structure shown in Fig. 3.

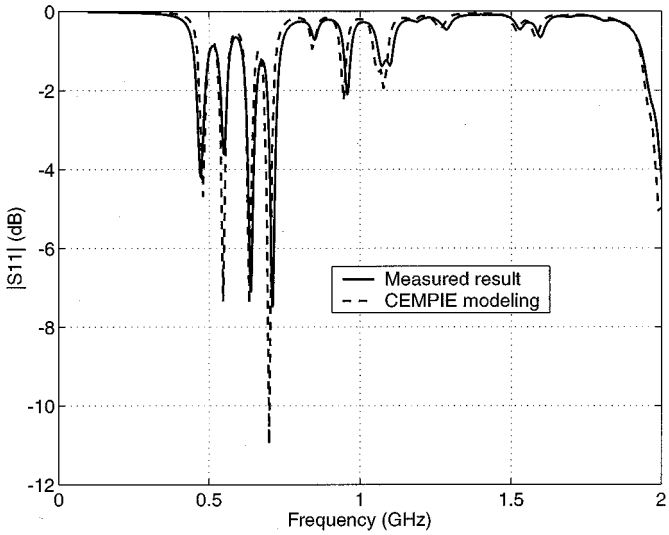

Fig. 5. Comparison between modeled and measured $|S_{11}|$ results for the power-bus structure shown in Fig. 3.

formly distributed over the board. Nominal parasitic inductance (ESL) and resistance (ESR) values associated with the capacitor package used in the modeling were 820 pH and 120 mΩ, respectively, and were measured from one capacitor using an HP4291A Impedance Analyzer. As shown in Fig. 3, one end of every capacitor was soldered directly to the power plane, while the other end was connected to the ground plane through a wire with a diameter of 24 mil. Both the power plane and interconnects were modeled in the first principles formulation, and the SMT capacitors were included as lumped elements. The dielectric thickness between the power and ground planes was 63 mils. The material was FR-4 with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. Two test ports, labeled as P1 and P2 in Fig. 3, were selected. The $|S_{21}|$ between them, and $|S_{11}|$ at P1 were investigated. Two test probes were constructed of 0.085″ semi-rigid coaxial cable with SMA connectors. The center conductors of test probes with diameters of 20 mils that connected to the the power plane were also modeled in the first principles formulation. The measurements were performed using an HP8753D network analyzer. The calibration planes were at the SMA test connectors. A 12-term error correction model using an open, short, and load was used in the calibration. A port extension was used to move the measurement planes to the coaxial cable feed terminals looking into the power bus.

Fig. 4 shows the comparison between modeled and measured $|S_{21}|$ results. The results compare favorably up to 2 GHz. The discrepancies between the modeling and measurements result in part from the nonideal construction of the test board. The wires fitted through the holes to make connections on the bottom board side may not be drilled perfectly straight and located exactly on the grid as shown. Further, values of C, ESR, and ESL measured from only one capacitor were used for all the capacitors. Modeled and measured results of $|S_{11}|$ at P1 are compared in Fig. 5, and they agree well from 100 MHz to 2 GHz as well. The CEMPIE model had 3549 mesh edges, and 2422 mesh cells. The problem took approximately 6 h and 20 min to complete either the $|S_{21}|$ or $|S_{11}|$ simulation with 301 frequency points in a Pentium III PC with a 450-MHz CPU and 512-MB memory. This test geometry includes most typical dc power-bus structures, thus, it well demonstrates the capability of the CEMPIE approach in dc power-bus modeling.

Arbitrarily shaped power planes can also be addressed using the CEMPIE approach, since the triangular mesh is suitable for approximating any arbitrary contour encountered in practical power-bus designs. The example shown in Fig. 6 is a segmented power plane structure. The two-layer test PCB had dimensions of 15 cm $\times$ 9 cm, and the bottom layer was a solid plane representing the ground plane. The top layer, however, as shown in Fig. 6, was gapped with a zigzag pattern, and the two conductor areas were connected by a conducting bridge to provide dc continuity. The board material was FR-4 with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. The layer separation between the power and ground planes was 43 mil. A test port was located in each area of the two gapped portions, and $|S_{21}|$ between them was studied both experimentally and with the CEMPIE modeling. SMA PCB mount jacks with diameters of the inner conductor of 50 mils were used as the test probes. The two test port conductors were modeled in the first principles formulation with the segmented power plane. Similarly, $|S_{21}|$ was measured using an HP8753D network analyzer, and the reference planes were located at the SMA jack terminals. The modeled and measured results from 1 MHz to 2 GHz are compared in Fig. 7, and agree well over the entire frequency range. A mesh with 2239 edges and 801 cells was used in the simulation. It took approximately 55 min to complete 301 frequency points in the Pentium III PC with a 450-MHz CPU and 512-MB memory. The number of unknowns, and the run time was greatly reduced from the previous examples, because the mesh could be coarser as a result of not having to mesh down to small via diameters.

The above two examples with typical dc power-bus structures, as well as other measurements, demonstrate that the CEMPIE approach is suitable for dc power-bus modeling.

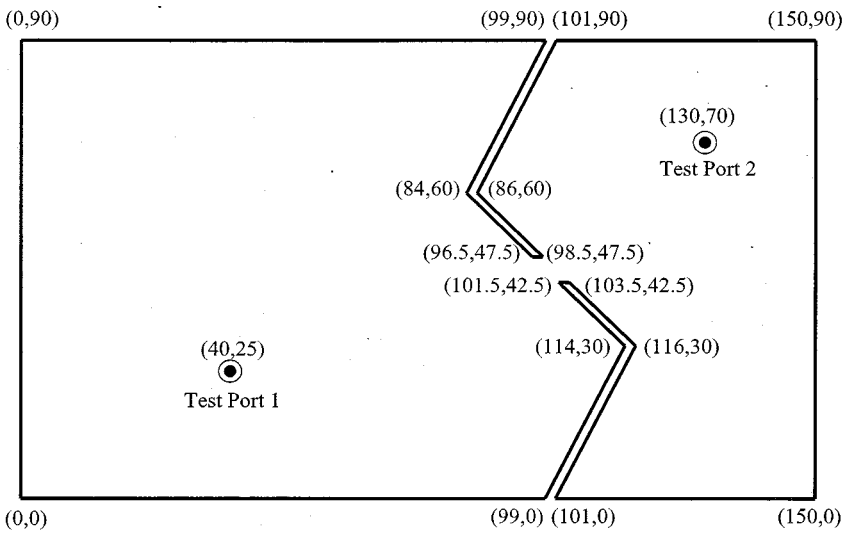

Fig. 6. A segmented power plane test geometry for CEMPIE modeling. All dimensions are in millimeters.

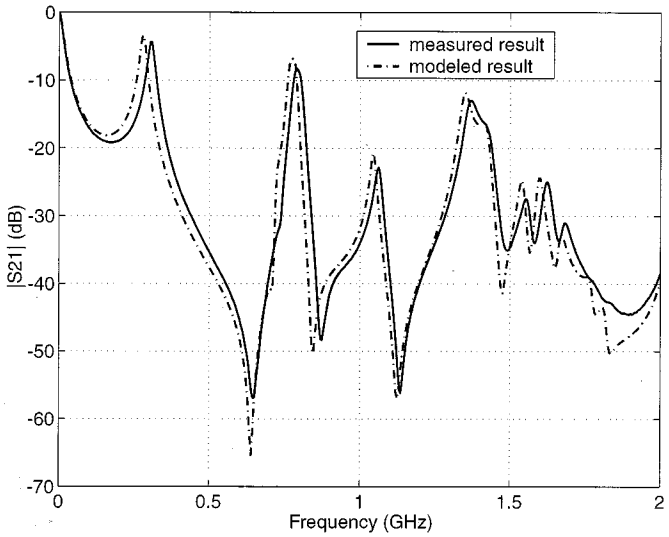

Fig. 7. Comparison between modeled and measured results for the segmented power plane shown in Fig. 6.

Various power-bus design issues can then be addressed using this modeling approach with confidence. The following section details several power-bus design examples.

IV. DC Power Bus Modeling Using the CEMPIE Approach

Issues on dc power-bus design in high-speed digital circuits can be addressed by a suitable and effective power-bus modeling tool more easily and thoroughly than hardware trial-and-error. The CEMPIE approach can handle various design problems on dc power-bus structures and SMT capacitor decoupling issues. Typical power-bus structures with arbitrarily shaped power planes, an arbitrary multilayer medium, as well as vias and test ports, can be formulated and addressed in CEMPIE. The circuit extraction approach enables an interface with SPICE compatible models of IC devices, transmission lines, and other circuit models, easily. Comparisons between modeling and measurements demonstrate its effectiveness. Several power-bus design issues were studied using CEMPIE, and shown below as examples of the application of the CEMPIE approach in dc power-bus design.

A. Local and Global SMT Decoupling Capacitor Placement

SMT decoupling capacitor placement on a PCB is a critical design aspect in high-speed digital designs. Traditionally, the use of local decoupling, namely, placing decoupling capacitors adjacent to an IC device, has been advocated. This view may stem from PCB designs where entire planes were not devoted to power supply and current return. Placing capacitors near the IC devices in this case reduces the parasitic inductance, thus making these decoupling capacitors effective at higher frequencies. More recent studies on dc power-bus structures with power and ground layers have suggested that all decoupling capacitors were shared in the frequency range in which they were effective; hence, the location of the decoupling capacitor on the board was unimportant [19]. This study considered thin power/ground layer separation (10 mils or less) cases. However, for thick power layers (greater than 30 mils), local decoupling can be benificial. Local decoupling capacitors remain effective far beyond the series resonance frequency of the SMT capacitors with the inductance of the interconnects, when all other decoupling capacitors have already lost their effectiveness [20]. This local decoupling effect results from the mutual inductive coupling between closely spaced vias [21].

A power-bus geometry shown in Fig. 8 was used to study the local decoupling effect using the CEMPIE approach. It was a two-layer PCB with a thickness of 43 mils, and dimensions of $6'' \times 9''$. Two solid planes were power and ground layers. The dielectric layer had a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. There were 39 global decoupling capacitors uniformly distributed on the PCB on $1''$ centers. Adjacent to the input test port were 4 local decoupling capacitors placed in a circle centered at the input port. The spacing between the local capacitors and the input port was varied. All SMT decoupling capacitors had individual values

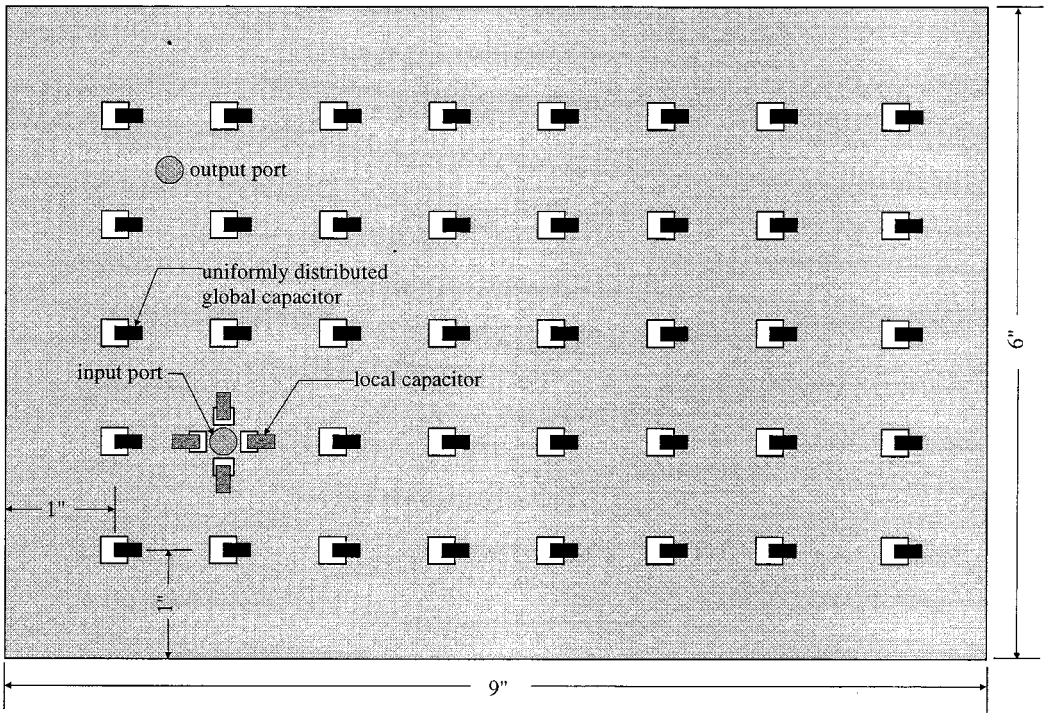

Fig. 8. A power-bus geometry for CEMPIE modeling of local decoupling capacitor effects.

of 0.01 μF, and the respective ESL and ESR values for the capacitor package used in the modeling were 820 pH and 120 mΩ, respectively. One end of the capacitors was connected to the top plane directly, while the other end was connected to the bottom plane through vias with diameters of 30 mils, as shown in Fig. 8. The input port was assumed to be an SMA PCB mount jack with a diameter of inner conductor of 50 mils, and an ideal open-circuited probe was set as the output port. The Z_{21} between the input and output ports was calculated from the CEMPIE modeling, and directly indicates the noise voltage at the output port due to the injected noise current at the input port. Results are compared with the baseline case, where no local decoupling capacitors were present, in Fig. 9, where s is the spacing between the local capacitors and the input port. The modeled frequency range was from 100 MHz to 2 GHz. Beyond a few hundred megahertz, the global decoupling capacitors normally have ceased to be effective. From Fig. 9, the local decoupling capacitors resulted in a $|Z_{21}|$ in excess of 15 dB lower for $s = 50$ mils over the entire freqency range, even to 2 GHz. The smaller the spacing between the local decoupling and the input port was, the lower the Z_{21} magnitude. Further, the $|Z_{21}|$ reduction is nearly independent of frequency. This can be explained by the mutual inductive coupling between the test port via and the decoupling capacitor via, and a hybrid lumped/distributed circuit model can be developed [1].

Modeling indicates that, for a thick power layer (30 mils or greater), local decoupling can be beneficial. It can effectively reduce power-bus noise up to several gigahertz. However, placing decoupling capacitors adjacent to IC devices may occupy space near the devices, thus limiting the routing flexibility. CEMPIE can provide a means of evaluating the benefit from local decoupling, based on the IC/capacitor spacing, and power layer thickness. Tradeoffs between local decoupling and routing flexibility can be made based on the results.

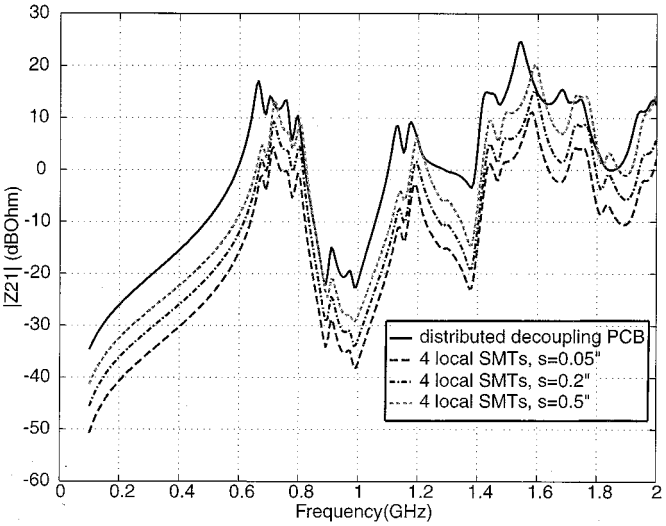

Fig. 9. Local SMT decoupling effect versus spacing.

B. High-Dielectric-Constant Power Layer Materials

The effective frequency range of SMT decoupling capacitors are typically limited by their parasitic interconnect inductance. When the parasitic inductance dominates the total capacitance of the SMT device, the equivalent impedance of the capacitors is much larger than the impedance of the parallel-plate structure of the power and ground layers. The inter-plane capacitance then dominates the PCB's impedance through the board distributed resonances, and serves as a source of high-frequency charge. Increasing the inter-plane capacitance either by using a high-di-

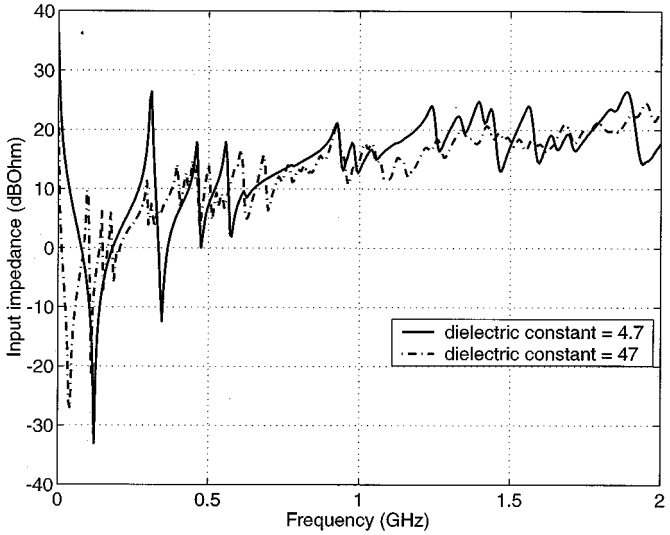

Fig. 10. Power-bus impedance of a bare high-dielectric-constant power layer.

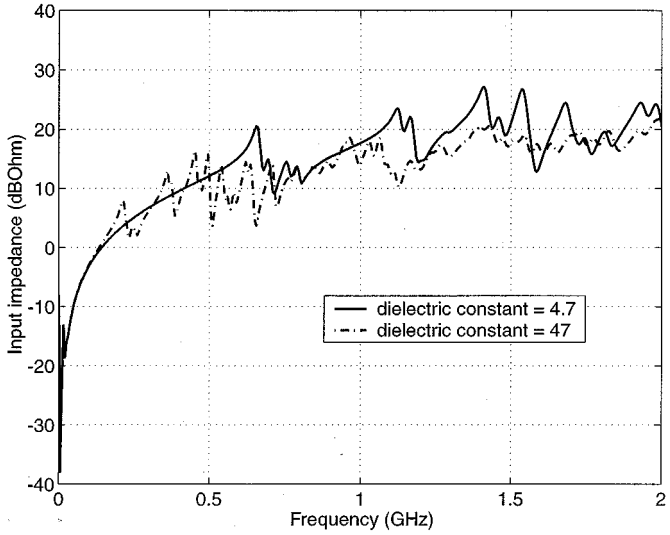

Fig. 11. Power-bus impedance of a high-dielectric-constant power layer populated with SMT capacitors.

electric-constant material or decreasing the layer thickness increases this high-frequency source of charge. Using a high-dielectric-constant material as the power layer was modeled with CEMPIE, and compared with an ordinary FR-4 material as the power layer.

The modeled structure was a $6'' \times 9''$ two-layer PCB, as shown in Fig. 8. The bare board, without the global and local decoupling capacitors, was first studied. The impedance at the input port terminal shown in Fig. 8 was calculated from the CEMPIE modeling for two cases with different board materials over the frequency range from 1 MHz to 2 GHz. One was an ordinary FR-4 material with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. The other was a fictitious high-dielectric-constant material. The only paramenter different from the FR-4 material was its permittivity $(\epsilon_r = 47)$. The layer thickness in both cases was 43 mil. Modeled input impedance results are shown in Fig. 10. The high dielectric constant resulted in a lower impedance at low frequencies due to the dramatically increased interplane capacitance. However, it also increased the electrical size of the PCB, thus decreased the frequencies at which the board exhibited distributed resonances. When the boards exhibited a distributed behavior, the overall magnitudes for two cases were comparable. It can be shown by considering a two-port network that minimizing the input impedance is consistent with reducing the noise voltage over the power bus. The benefit of a high-dielectric-constant material may be limited to frequencies less than the board distributed resonances, though further study is required for reaching a general conclusion regarding high-dielectric power layers.

When all the global decoupling capacitors were present as shown in Fig. 8, the low-frequency improvements due to the high-dielectric-constant material was neglegible, as illustrated in Fig. 11. This result is reasonable since the low-frequency board impedance was dominated by the decoupling capacitors, and the board distributed resonances were so low that the inter-plane capacitance did not have a wide effective frequency range.

C. Using Loss in Power Layers and SMTs

The input impedance of the PCB at any point is dominated by its distributed resonance peaks for frequencies higher than the first board distributed resonance as demonstrated previously. Decoupling capacitors (except for the local capacitors) and the inter-plane capacitance do not impact the overall level of the power-bus noise in this region, though resonant frequencies can shift. Using loss in the power layers can damp the resonance peaks, thus reduce the power-bus noise. The active components themselves will contribute to the power-bus loss, but in the gigahertz frequency range, the dielectric and conductor losses will dominate. Essentially, a lossy material will introduce dielectric losses into the noise propagation, and these losses are proportional to frequency. The higher the frequency is, the more the noise magnitude can be reduced. Since dielectric losses can be addressed by applying a complex dielectric constant in Green's functions, this issue can be modeled using the CEMPIE approach as well.

The test geometry shown in Fig. 8 was again used, including the global decoupling capacitors. The local decoupling capacitors were not placed. An ordinary FR-4 material with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$ was used as a baseline. A fictitious lossy material with the same dielectric constant, but loss tangent of $\tan\delta = 0.2$ was modeled, and compared with the more typical case. The dielectric layer thickness in both cases was 43 mils. The $|Z_{21}|$ between the input and output ports, as well as the input impedance looking into the input port terminal, was modeled from 100 MHz to 2 GHz. The $|Z_{21}|$ results are shown in Fig. 12(a). The lossy material damped the board distributed resonance peaks by as much as 15 dB in the $|Z_{21}|$. This indicates that less noise propagated to the output port using the lossy material than using an ordinary FR-4 material. Fig. 12(b) shows the comparison between the two input impedance results. Again, the lossy material damped the board distributed resonance peaks by as much as 10 dB. In practice, when all IC devices and other circuit components are placed for a populated PCB, these components may introduce losses as well. Therefore, the effect

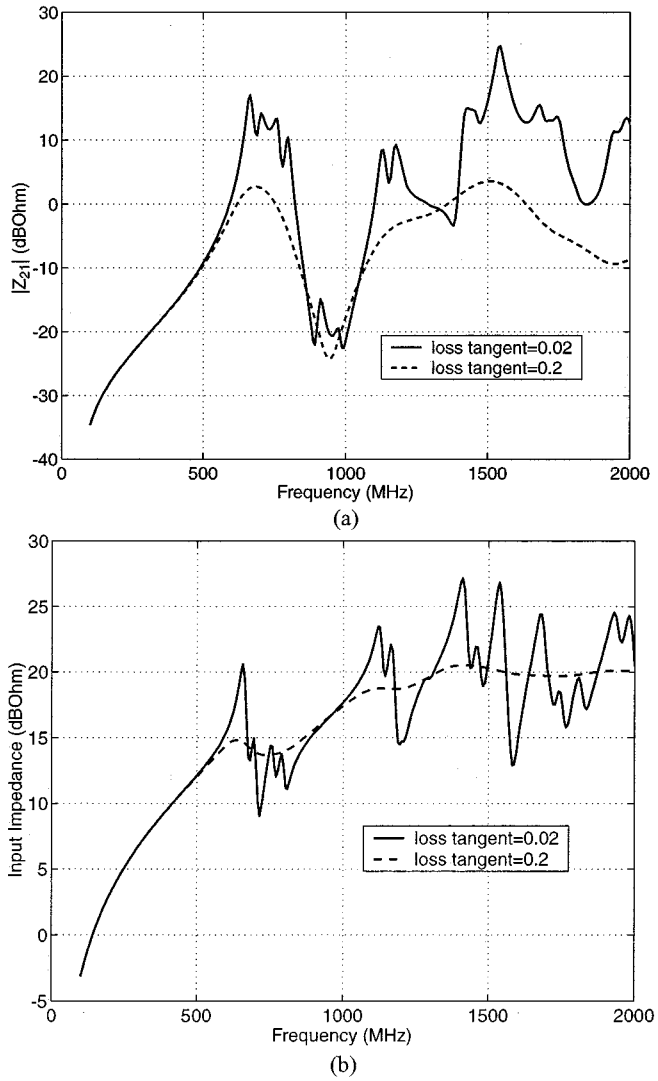

Fig. 12. Using a lossy material in the power layer to damp the resonance peaks. (a) $|Z_{21}|$. (b) Input impedance.

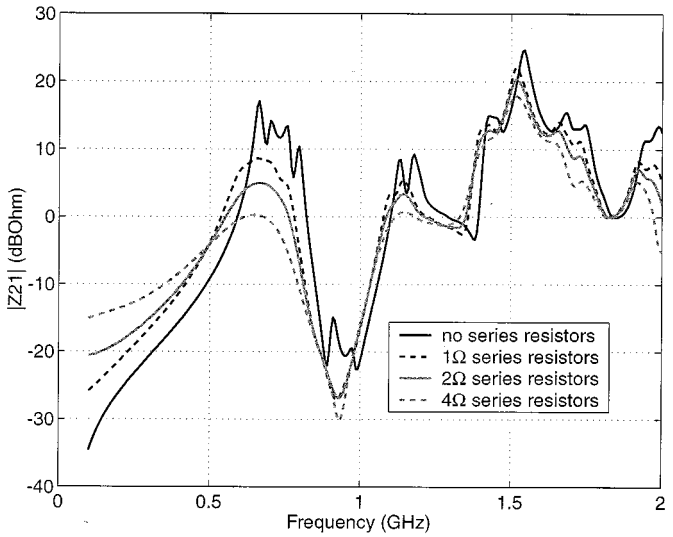

Fig. 13. Modeled $|Z_{21}|$ results when adding resistive losses in the SMT decoupling capacitors.

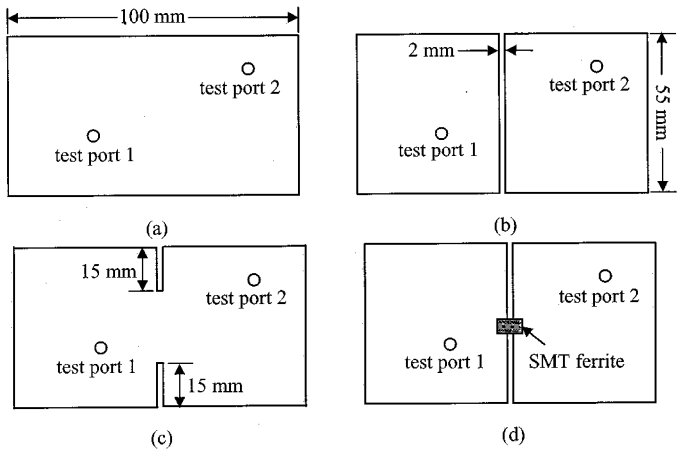

Fig. 14. Power-plane segmentation geometries modeled with the CEMPIE approach.

of losses in the power layers may not be so dramatic, in particular below 1 GHz. The CEMPIE formulation can easily incorporate these device models if available, and, therefore, the effect of using lossy materials as power layers can be evaluated in a more appropriate fashion with suitable device models.

Adding resistive losses in the power-bus structure was studied using the same test geometry as above. A series resistor with an ESL value of 820 pH was added to every SMT decouping capacitor, and $|Z_{21}|$ between the input and output ports was determined. Three different resistor values of 1, 2, and 4 Ω were investigated, and modeled results are compared with the case without the series resistors in Fig. 13. Adding resistive losses damped the first several resonance peaks between 600–800 MHz, and the larger the series resistors were, the more these magnitudes were decreased. However, higher-frequency resonance peaks had only slight changes. Further, with the increase of the resistor values, the low-frequency magnitudes increased, which may greatly reduce the noise margins at these frequencies. Adding resistive losses affects the first several resonances, and the specific value of loss must balance the low-frequency performance against the improvements at these resonant frequencies.

D. Power-Plane Segmentation

Segmented power planes are often employed in high-speed digital designs for minimizing the propagation of high-frequency noise on dc power buses. The rationale is based on introducing a series impedance in the power plane to provide isolation of a noise source from the rest of the PCB design. A lumped equivalent circuit model based on the segmented structure and dimensions can be established, and is useful at frequencies lower than the board distributed resonant frequencies [22]. However, the RF performance of power-plane segmentation into the gigahertz frequency range requires a full-wave approach. CEMPIE is suitable for this modeling, since an arbitrarily shaped power plane can be handled with no extra effort.

Four power-plane structures shown in Fig. 14 were studied as an example. All PCBs had dimensions of 10 cm $\times$ 5.5 cm, and a thickness of 43 mil. The board materials were the same as previously, with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. The only differences were in the power planes. A continuous power plane was used as a baseline case.

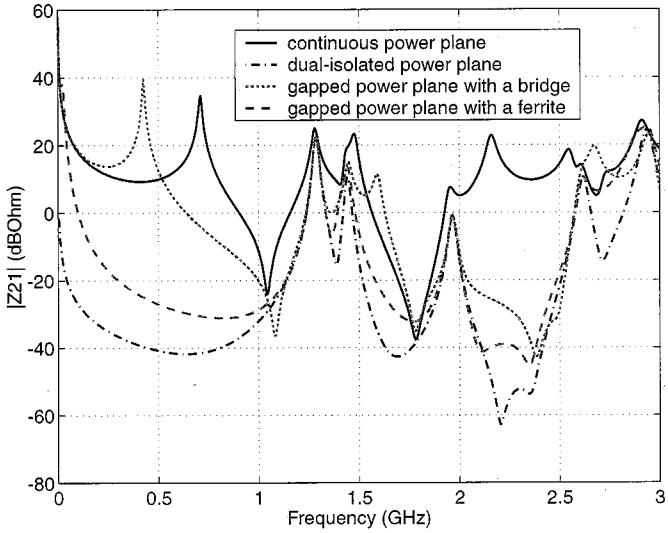

Fig. 15. Comparisons of $|Z_{21}|$ due to different segmented power-plane structures.

A dual-isolated power plane, a gapped power plane with a conducting bridge, and a gapped power plane with a ferrite connection were modeled as three common segmentation structures. All gaps were located in the center of the longer edge with gap widths of 2 mm for the latter three cases. Two test ports were chosen. In the segmented power-plane configurations, they were located in the two gapped portions. The modeled $|Z_{21}|$ results between the two test ports are shown in Fig. 15. Compared with the continuous power plane, the dual-isolated plane had better isolation over nearly the entire frequency range, except at distributed board resonances where the gap did not affect the current distribution of the modes associated with these resonances. However, when the conducting bridge was present to provide a dc connection, the gapped plane did not decrease $|Z_{21}|$ at frequencies lower than 500 MHz, and the conducting bridge compromised the isolation achieved by the gap. An alternative was to use a ferrite to provide RF impedance but dc continuity. An equivalent parallel *RLC* circuit with $R = 300\ \Omega, L = 7\ 00$ nH, and $C = 0.65$ pF was used to represent an SMT ferrite. The modeled results show that the gapped plane with the ferrite connection had almost the same degree of isolation as the dual-isolated plane in the entire frequency band, except that the ferrite model also provided dc continuity.

The isolation as a function of geometry factors, such as gap and bridge dimensions and location, gap shape, and other factors can be studied using the CEMPIE approach by performing various what-if scenarios. Then, specific power-plane segmentation designs can be facilitated and guided using this method.

V. Conclusion

A modeling approach formulated from first principles and extracting a SPICE model was used to study several dc power-bus issues critical in high-speed digital designs. The comparisons between measured and modeled results demonstrated its effectiveness and application. The compatibility of the CEMPIE approach with SPICE type circuit models, its capability of modeling vertical discontinuities and planar areas in multiple layers, and easy handling of arbitrarily shaped planes make it a powerful modeling tool for PCB and MCM power-bus design, where power is distributed using planar areas.

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