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R. Lee Hill

Thomas Van Doren
Missouri University of Science and Technology, vandoren@mst.edu

Todd H. Hubing
Missouri University of Science and Technology

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1494

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COMMON MODE CURRENTS INDUCED ON WIRES ATTACHED TO MULTILAYER PRINTED WIRE BOARDS WITH SEGMENTED GROUND PLANES

R. Lee Hill, T. Van Doren, T. Hubing, J. Drewniak
Department of Electrical Engineering
Electromagnetic Compatibility Laboratory 208/ERL
University of Missouri-Rolla
Rolla, Missouri 65401

Franz Gisn
ROLM (A Siemens Company)
4900 Old Ironsides Drive M/S 658
P.O. Box 58075
Santa Clara, California 95052

Abstract

An investigation has been undertaken to further study the fundamental mechanisms responsible for inducing high frequency common mode currents on wires attached to multilayer printed wire boards (PWBs). Previous work reported in the EMC literature [1], [2], [3], [4], [5], [6] has demonstrated that the presence of unintended common mode currents on the external cables of electronic equipment is often the primary source of radiated EMI at frequencies above 30 MHz. In an attempt to reduce the magnitude of these currents to yield "quieter" electronic products, many EMC engineers have implemented segmented or "gapped" ground plane geometries in mulilayer PWB designs. The objective of this study is to explore and develop a better understanding of the underlying electrical properties of such geometries. The establishment of a theoretical basis and empirical validation for such methods could then be used to construct a set of fundamentally sound EMC design guidelines for PWBs operating at high frequencies with attached cables.

Introduction

Recent investigations of the fundamental mechanisms responsible for establishing common mode currents on wires attached to PWBs have focused primarily upon 1) demonstrating that these common mode currents are the primary source of radiated EMI from electrically small electronic products, 2) establishing a linkage between partial inductance in signal return "ground" circuits and the induced common mode currents, and 3) validating the use of ground planes to reduce the magnitudes of induced common mode currents. The objective of this study is to investigate and develop a better understanding of the electrical properties and corresponding effects of segmented "ground" planes in multilayer PWBs. While many EMC engineers implement such structures as a means of reducing the emissions from PWBs and their attached cables, scant analytical information exists to fundamentally describe and demonstrate the often claimed effectiveness of such design techniques. Towards an ultimate goal of establishing fundamental information and practical PWB EMC design guidelines, this paper details Part I of the investigation to determined an approximate model for the inductance introduced by a finite gap in a microstrip "ground" plane and verified the model's predictions with empirical measurements. Part II of this study, which is still in progress at the time of this writing, will utilize this model to examine the common mode currents induced on the attached wires of four PWB's with various power and "ground" plane segmentations.

To provide a vehicle for empirical tests, two sets of PWBs were designed and built. For Part I of the study, a single section of shorted microstrip transmission line was implemented on the first set of two boards as shown in Figures 1a and 1b. Of these two boards, one was built with a continuous "ground" (return) plane beneath the strip conductor, while the other was built with a gap inserted in the return plane. These boards were examined using a network analyzer to study the inductance introduced by the insertion of the finite gap in the return plane.

For Part II of the investigation, a second set of PWBs was designed with a four layer signal-power-ground-signal construction and identical component placements. Each PWB contained a quartz crystal controlled square wave oscillator IC, a 74AC00 type oscillator buffer IC, and an identical 74AC00 "load" buffer IC. Four identical circuit traces were designed on each PWB, each including selectable jumpers to allow the oscillator signal to be independently activated or deactivated on each of the four traces. A subminiature type "D" connector was also installed on each assembly to provide a port for attaching an external wire(s) to the PWB ground plane, power plane, and/or the oscillator signal. Each of the four boards had a power and "ground" plane structure distinct from the others, as shown in Figures 3-6. Board #1 implemented a continuous, non-segmented set of planes. Board #2 was designed with a single "gap" in both the power and return planes that was oriented with its long dimension perpendicular to the long dimension of the "D" connector. Board #3 was built with a single power and return plane gap oriented parallel to the long dimension of the "D" connector. Board #4 was designed with a pair of identical gaps in each plane near and oriented parallel to the "D" connector. Power was supplied by an electrically small battery pack connected through wires electrically short over the frequency range of interest (30-200 MHz). A high sensitivity current probe and spectrum analyzer were used to record the magnitude of common mode currents induced on the wire(s) attached to a board via the its "D" connector. A second set of common mode current measurements was made on boards 1 through 4 using a swept frequency oscillator to drive a differential voltage on to the PWB power and "ground" planes. This setup eliminated the uncertainty in resulting experimental data associated with the unknown loaded power output spectrum of the on board square wave oscillators.

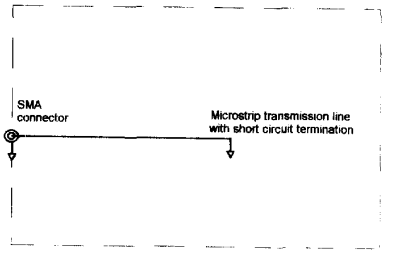

Figure 1 (a): PWB with microstrip line, short circuit termination, unsegmented return plane beneath microstrip line

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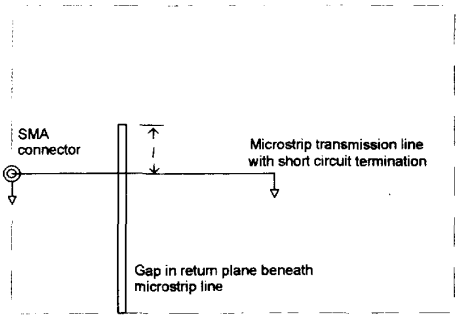

Figure 1 (b): PWB with microstrip line, short circuit termination, and gap in return plane beneath microstrip line

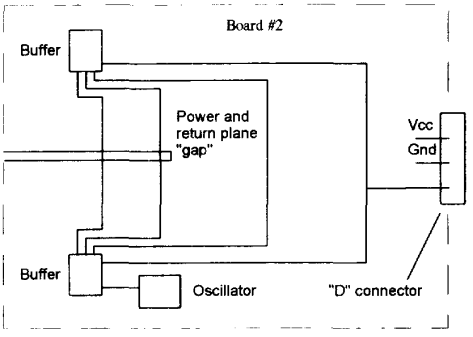

Figure 3: Multilayer PWB with power and return plane gap perpendicular to long dimension of "D" connector

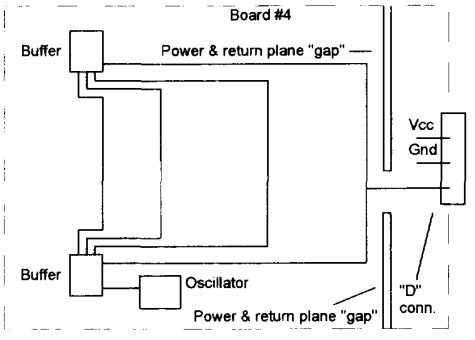

Figure 5: Multilayer PWB with power and return plane "gaps" parallel to "D" connector

Split Power and "Ground" Planes

Design and EMC engineers frequently debate the merits of introducing finite sized gaps into the power and/or return ("ground") planes of multilayer PWBs. Such structures have been used successfully in low frequency analog and power control circuits, where large low frequency current paths can be readily identified and planned to avoid common impedance coupling through the PWB power network. At frequencies above 100 KHz, however, signal and signal return currents form tightly coupled signal loops, establishing paths of least possible inductance. Despite that many high frequency noise sources on PWBs occupy well defined and identifiable physical paths, EMC engineers have developed many "split" or "gapped" ground plane design strategies. These strategies seek to divide PWB assemblies into high frequency sections (containing oscillators, microprocessors, etc.), and low frequency I/O (input/output)

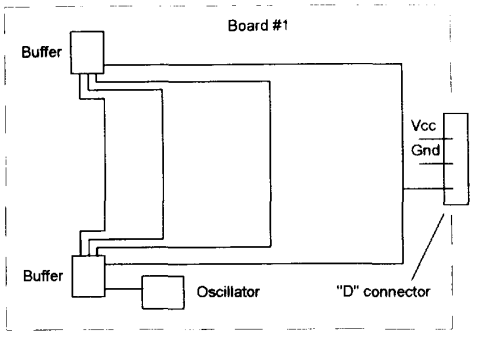

Figure 2: Multilayer PWB with unsegmented power & return planes

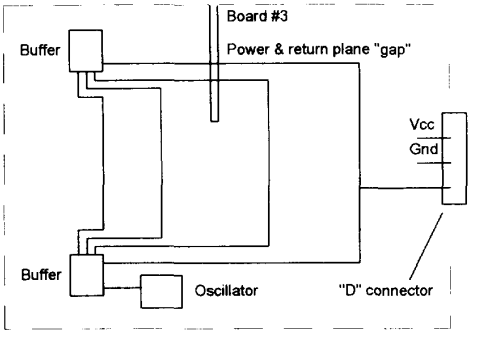

Figure 4: Multilayer PWB with power and return plane "gap" parallel to "D" connector

sections. One goal of such strategies is to reduce the common mode current induced on cables attached to the PWB, thus reducing radiated EMI from the PWB/cable assembly. [The PWB designs shown in Figures 2-5 were created to model and investigate the nature of these design techniques.]

Part I - Theoretical Model of Gap Inductance

To provide a sound basis for the analysis of the gapped plane structures, a simple electrical equivalent circuit model for the gapped microstrip board of Figure 1b was postulated. The model, shown in Figure 6, consists of three partial inductances; 1) the inductance associated with the interconnect between the SMA connector and PWB, 2) the inductance associated with the portion of the microstrip having an unsegmented return plane, and 3) the inductance associated with the portion of the microstrip crossing the return plane gap. By sketching the high frequency current path that must exist on the segmented return plane of Figure 1 (b), a shorted transmission line segment can be visualized along the path from points "a" to "b", as shown in Figure 7.

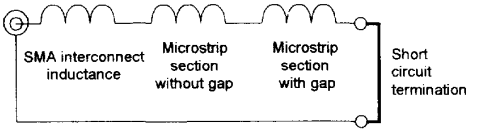

Figure 6: Equivalent circuit model showing partial inductances of shorted gapped microstrip PWB of Fig 1(b)

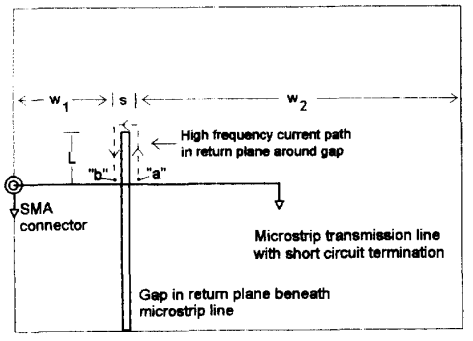

Figure 7: PWB with microstrip line, short circuit termination, and current path around gap

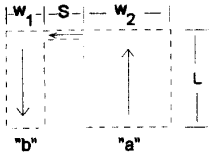

Figure 8: Current path around gap in return plane modeled as shorted section of coplanar strip transmission line

The shorted transmission line segment can be approximated as a coplanar strip type line, as shown in Figures 8 and 9. Closed form expressions for the characteristic impedance and per unit length capacitance are available in the literature [7], but only for symmetrical structures where $w_1 = w_2$. If the smaller width dimension of an asymmetrical structure is used in these expressions, then intuitively the result will yield a per unit length inductance and a characteristic impedance slightly larger than for the actual case. Using a line width of w_1 in the expression for the symmetrical case could thus be expected to yield an upper bound for the partial inductance associated with the gap in the return plane.

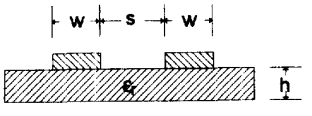

Figure 9: Coplanar strip transmission line

The characteristic impedance of a pair of symmetrical coplanar strips [7] is:

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{re}}} \frac{K(k)}{K'(k)} \ \Omega \qquad (1)$$

where:

$$\varepsilon_{re} \approx \frac{\varepsilon_r + 1}{2}, \quad \text{for } \frac{h}{W} << 1$$

$$k = \frac{S}{S + 2w}, \quad k' = (1 - k^2)^{1/2}$$

$$\frac{K(k)}{K(k')} = \frac{\pi}{\ln\left[2\frac{1+\sqrt{k}}{1-\sqrt{k'}}\right]} \quad \text{for } 0 \le k \le 0.707$$

For the gapped microstrip structure (Figure 1b) that was constructed:

$s = 0.12$ in. $\quad w_1 = 0.95$ in.
$\varepsilon_r = 2.3 \quad h = 0.065$ in.

The effective permitivity, ε_r, of the perforated plastic dielectric substrate ("perfboard") used to construct the shorted microstrip lines in this investigation was determined by building and measuring the capacitance of a large, closely spaced parallel plate capacitor of known dimensions.

Using equation (1) and the given parameters,

$Z_o \approx 143\ \Omega$

The input impedance of a lossless transmission line of length l, characteristic impedance Z_o and terminated in load impedance Z_l can found using:

$$Z_{in} = Z_o \frac{Z_l + jZ_o \tan\beta l}{Z_o + jZ_l \tan\beta l} \ \Omega \qquad (2)$$

Equation (2) can be used to calculate the impedance seen at the input (points "a" and "b") of the shorted coplanar strip line shown in Figure 7. For a section of line of length $l < \lambda/4$, this input impedance will be a pure inductive reactance. Equation (2) can then be rewritten as:
where:

$$j\omega L = jZ_o \tan\beta l,$$

$$L = \frac{Z_o \tan\beta l}{\omega} \ \text{(Henries)} \qquad (3)$$

L = inductance seen at terminals "a" and "b"
β = propagation constant of the coplanar strips
l = length of the shorted line, corresponding to distance between the edge of the microstrip conductor and the far edge of the plane gap

This inductance can be interpreted as the partial inductance introduced by the gap in the signal return plane. Using equation (3) with the values determined earlier of Z_o and ε_r, and the line length l of 0.95 in. ("L") shown in Figure 1(b), we find:

$L_{gap} \approx 18$ nH

Part I - Empirical Validation of Gap Inductance Model

Two methods were employed to verify the results of the theoretical gap inductance model for the structure of Figure 1b:

Method 1

The total inductance of the "ungapped" and "gapped" microstrip PWB assemblies shown in Figures 1(a) and 1(b) was derived from network analyzer measurements of the one-port input reflection coefficient $\Gamma = S_{11}$.

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o}$$

for a short circuit with $Z_L = 0 + j\omega L$,

$$\Gamma = \frac{j\omega L - 50}{j\omega L + 50}$$

and

$$\angle \Gamma = (180 - \alpha) - (\alpha)$$

where

$$\alpha = \tan^{-1}\left[\frac{\omega L}{50}\right]$$

Solving for L,

$$L = \frac{25\tan\left[\frac{180 - \angle\Gamma}{2}\right]}{\pi f} \text{ (Henries)} \qquad (4)$$

The interconnect inductance associated with the SMA connector - PWB interface on each PWB was similarly derived by placing a short at the input to the microstrip line and again measuring the inductance of the PWB assembly. The gap partial inductance was then found to be:

L_{gap} = L_{total} (PWB with gap) - $L_{interconnect}$ (PWB with gap) - L_{total} (PWB no gap) - $L_{interconnect}$ (PWB no gap)

The above expression assumes the two PWB s have identical microstrip line lengths and ε_r, but allows for unequal interconnect inductances.

Method 2

The second empirical technique derived the equivalent gap partial inductance by introducing a capacitor and recording the resonant frequency as observed on the network analyzer S_{11} phase display. The physical placement of the capacitor and resulting equivalent circuit are shown in Figures 10,11, & 12.

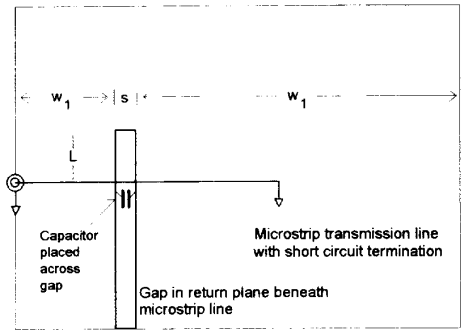

Figure 10: Capacitor added across return plane gap directly opposite microstrip line

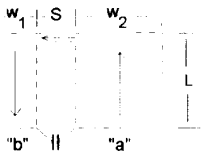

Figure 11: Capacitor added across return plane gap at input of coplanar strip transmission line

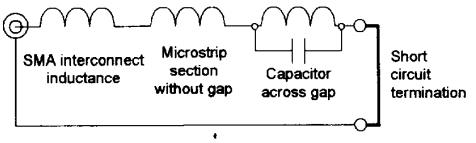

Figure 12: Equivalent circuit model with external SM capacitor added across gapped section of mictrostrip PWB

The partial inductance introduced by the gap is then found by observing the first resonance indicated by the network analyzer S_{11} display and using:

$$L = \frac{1}{4\pi^2 f^2 C} \text{ (Henries)}$$

where f = parallel resonant frequency of gap inductance and capacitor

C = capacitor value chosen such that $\lambda_{resonance} >> $ effective length "L" of gap

Comparison of Results - Part I

The one theoretical and two experimental values found for the gap partial inductance of the microstrip PWB are summarized in Table 1 below:

Partial Inductance Associated with Return Plane Gap		
Theoretical	Experimental Method 1 (input impedance)	Experimental Method 2 (resonance)
18 nH	15 nH	16 nH

Table 1: Summary of Theo. & Exp. Gap Inductance Data

As predicted, the theoretical result establishes an upper bound on the actual measured values. The quantitative analysis establishes a valuable benchmark for the actual inductance introduced by an approximately one inch long "effective" gap length. Note that it is the maximum gap to microstrip conductor separation distance "L" (shown in Figure 9) that determines the magnitude of the inductance, NOT the total length of the gap. The inductance introduced by a similar size effective gap length on a fiberglass-epoxy FR-4 type PWB would be less, due to the higher dielectric constant and the resulting lower coplanar strip characteristic impedance.

Part II of this work will study the relationship between the gap partial inductance and the common mode current induced on externally connected PWB wires.

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Acknowledgments

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