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Vittorio Ricchiuti

Antonio Orlandi

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

Francesco de Paulis

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Vittorio Ricchiuti[(1)], Antonio Orlandi[(2)], James L. Drewniak[(3)] and Francesco De Paulis[(3)]

[(1)] Technolabs S.p.A., L'Aquila, Italy
Email: vittorio.ricchiuti@technolabs.it
[(2)] UAq EMC Lab, University of L'Aquila, 67100, Poggio di Roio, L'Aquila, Italy
Email: orlandi@ing.univaq.it
[(3)] UMR EMC Lab – ECE Department University of Missouri-Rolla, Rolla, MO, USA
Email: {drewniak, fd8b4}@umr.edu

Abstract—**Nowdays the fast and increased demand for bandwidth in the telecommunication world translates into the design of complex boards exchanging data at high bit rate in reduced design cycle. Sometimes it is impossible to spent time in setting pre-layout simulations, because they are not compatible with the design time schedule. In this scenario it is better to design the boards using experience and then make simulations in conjunction with measurements, using customized numerical tools which don't need complex models.**

Keywords - differential serial link; Printed Circuit Board; time domain measurements; frequency domain measurements; dielectric losses

I. INTRODUCTION

The telecommunication market in the last years has been characterized by an ever increasing demand for bandwidth. This calls for designing digital equipments with boards interconnected by backplanes on which digital signals flow at very high bit-rate. The paper illustrates some key issues for the design of an electro/optical Add-Drop Multiplex (ADM) functioning at a nominal bit-rate of 10Gbps, which multi(demulti)plexes data fluxes according to the Gigabit Ethernet (GbE) and Synchronous Digital Hierarchy (SDH) protocols. In this design the backplane (the large board functioning as backbone for the system) exchange data at 5.5Gbps. At the increased complexity and data rate of the equipments corresponds a reduced design cycle, which translates into the so called "first time right" design. It's superfluous to remember that the costs of the design and products have to be as low as possible. In this scenario it is very difficult to find time in the project's flow to perform electromagnetic simulations for optimizing the design, because they are time consuming and require significant efforts for setting the correct models. The only possibility for the designer is to use specific software tools oriented at the analysis of the signal link path supported by measurements and its own experience.

In this paper it will be analyzed the design of a backplane in FR4 used for transmitting digital signals at 5.5Gbps. The FR4 has been chosen for its reduced cost, in spite of its dielectric losses that can impact the quality of the signal transmission.

The paper is organized as follows: in SECTION II the geometric details of the backplane are briefly described; SECTION III illustrates the significant measurement performed on the backplane for characterizing its electrical properties. SECTION IV briefly describes the software tool used for simulating the signal paths, while SECTION V considers the analysis of the differential traces used for signal transmission. SECTION VI offers some design remarks.

II. BACKPLANE DESIGN

The first step in designing a high speed backplane, from the electrical point of view, is choosing the proper dielectric material, taking into account the operating bit-rate of the transmitted data, the maximum length of the traces, the electric permittivity and dielectric losses of the material and, last but not least, the cost. In the present case the daughter cards with transceivers, connected through the backplane, exchange data at 5.5Gbps. The total length of the link path card-to-card is of 19 cm: 5cm on the transmitting card, 7cm on the backplane, 7cm on the receiving card. These reduced lengths allows the designer to use the common FR4 with nominal characteristics $\varepsilon_r = 4.5$ @ 1MHz and $tg\delta = 0.02$ @ 1MHz for manufacturing the boards.

The backplane is a 427mm x 130mm board. It has 8 layers, for a total thickness of 1914μm. The stuck-up is in Fig. 1a. The backplane connects 16 cards. Several 100Ω differential striplines, whose cross-section is in Fig. 1b, are laid out on the high speed signal layers (L2 and L7). The traces are designed as wide as possible to decrease the skin effect losses (200μm), taking into account the maximum allowed clearance among the pins

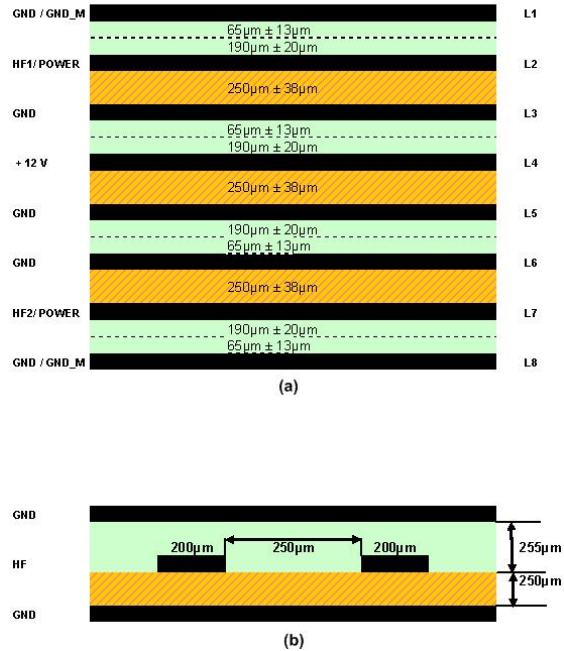of the pin-field HF connectors used in the project, as shown in Fig. 2.

(a)

(b)

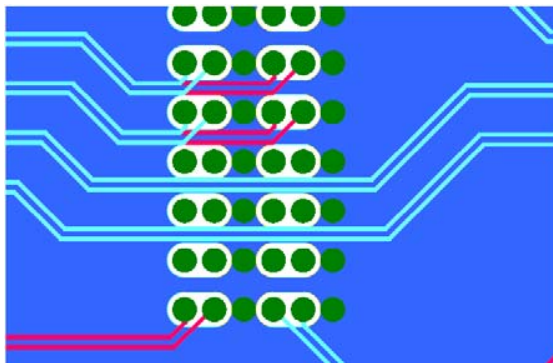Figure 1.   (a) Stack up of the backplane and (b) crossection of the differential traces.

Figure 2.   Differential stiplines are routed among the pins of the HF connectors.

III.   BACKPLANE MEASUREMENTS

In order to characterize the transmission properties of the differential traces routed on the backplane, the backplane itself should be connected to the measurement equipment. The two test daughter cards shown in Fig. 3 have been designed for this purpose. Particular care has been used in the design of these cards in order to reproduce all the significant features of the signal path: length of the link, female/male connectors, length of the unavoidable vias stubs. Measurements on a differential

trace on L2 have been performed in both time and frequency domain, by using a Time Domain Reflectometer (Tektronix CSA800 with TDR sampler 80E04) and a Vector Network Analyzer (Anritsu 37257C with 4-ports extension). A standard full two-ports calibration procedure (Short-Open-Load-Thru calibration) in the frequency range 40MHz-18GHz has been made at the ends of the test probes for calibrating the network analyzer with high quality calibration standards [1].
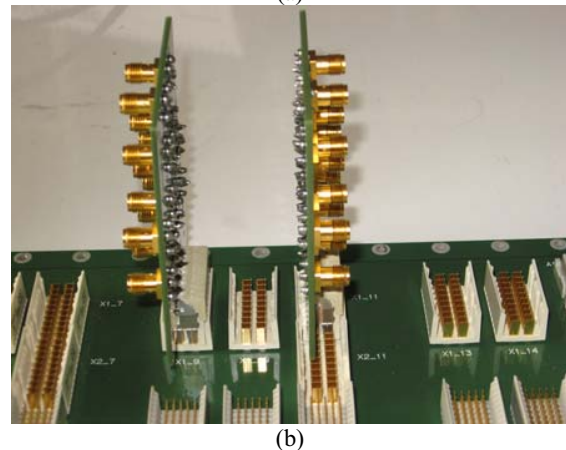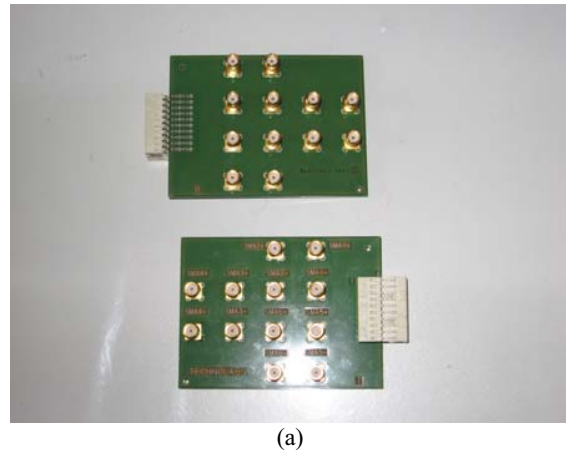

(a)

(b)

Figure 3.   (a) Test daughter cards for connecting the backplane to the measurement instruments; (b) Test cards connected to the backplane.

At the connector's pins on L2 the differential trace is impacted by the presence of long stubs, generated from L2 to the bottom layer by the through vias in which the connector's pins are soldered.

Fig. 4 shows the odd mode impedance of the two traces in the differential pair, measured with the TDR. The impedances of the traces on the test board used for connecting the backplane to the TDR are also highlighted. As it is evident, the odd mode impedances of the two traces are equal to 50Ω, which means that the used stack up guaranties a differential impedance equal
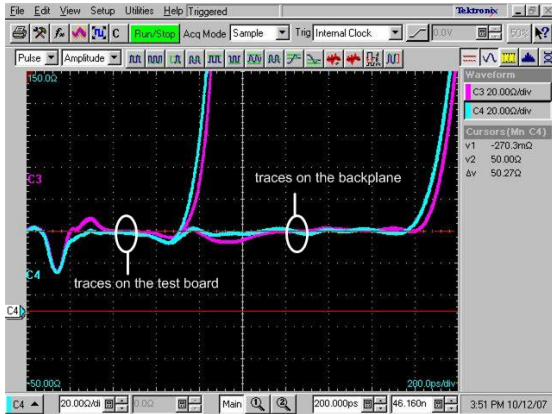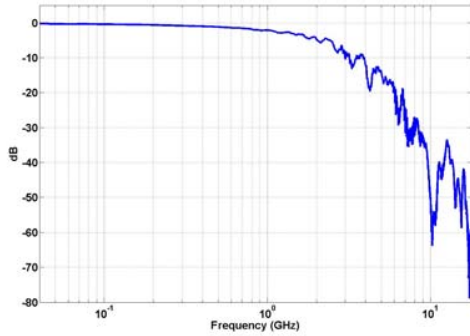
Figure 4.   TDR measurement.


Figure 5.   Transfer funtion of the differential trace.

to 100Ω. Fig. 5 shows the magnitude of the mixed mode scattering parameter S_{DD21}.

At 2.5GHz the insertion loss due to the trace is equal to 7dB, while at 5.5GHz is almost 17dB. Moreover at 10.27GHz there is a dip due to the through via where the connector's pins are soldered.

Fig. 6a shows the eye diagram of the differential signal at the input of the first test board connecting the backplane to the eye pattern generator, while Fig. 6b shows the same eye diagram at the end of the second test board connecting the traces on L2 of the backplane to the scope. We used a PRBS 2^7-1 NRZ input data pattern at 5.5Gbps with amplitude equal to 500mV. The Maximum Eye Opening (MEO) at the end of the trace is 232mV, about one half of the MEO at the input of the trace (460mV) [2]. The Maximum Eye Width (MEW) is 180ps at the input and 150ps at the end of the trace. Note that the eye opening is not affected by the dip at 10.27GHz (Fig. 5). Fig. 6b shows that the component of the PRBS signal at 5.5Gbps is enveloped by the component at 2.5Gbps. This means that the component at 5.5Gbps is attenuated more than the component at 2.5Gbps, as it is also evident from the insertion loss in Fig. 5.
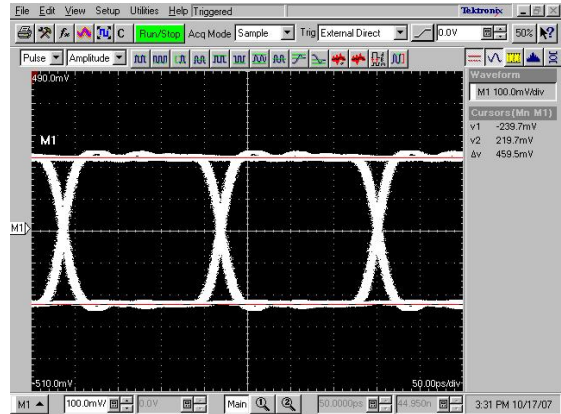
(a)
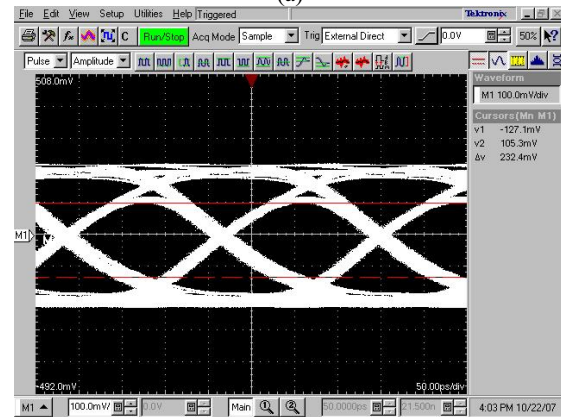
(b)

Figure 6.   (a) Eye pattern at the input of the test board connected to the differential trace on L2 of the backplane; (b) Eye pattern at the end of the test board connecting the differential trace on L2 of the backplane to the scope.

Because the minimum possible signal at the input of the used receiver is 200mV, we have not enough margin with a measured eye opening of 232mV.

One technique to improve the link performances is the pre-emphasis. The next section employs this method and the link performances with and without pre-emphasis will be compared.

IV. THE LINK PATH ANALYZER

To study the effects of the pre-emphasis we use the numerical simulation tool named Link Path Analyzer (LPA) [7] which, starting from the files obtained with the VNA measurements, allows to simulate the eye diagram at the end of the differential trace. LPA gives fast and effective information without setting complex simulation environment.

It allows to simulate link path composed by multiple sections, such as transmission lines, vias, connectors etc. The S-parameter data of each single piece are cascaded together to obtain the S-parameter data set of the overall link. Then the obtained S-parameter is employed to

simulate the eye pattern and the eye parameters such as eye width, eye height and jitter are computed. These parameters help the designer judging the goodness of the link.

An effective procedure for investigating the performances of a link path is to analyze each single section. The designer can easily identify the worst section through the LPA, i.e. recognizing the one that reduces the most the eye opening and generates most of the jitter. Measuring the S-parameter data for each piece is not always easy; sometimes the only way to obtain the data of the unknown section is to de-embed it, procedure widely used for example in the error correction procedure included in the VNA [6]. The LPA is able to extract an S-parameter data set of an embedded section starting from the S-parameter of all the other single pieces and the one of the overall link.

Furthermore the tool allows to check the 'goodness' of the imported data through the check of the causality and passivity. The former extracts the causal imaginary part from the real part and compares it to the original imaginary part according to the procedure shown in [3,4]; the latter gives information about the passivity of the data at each frequency computing the 2-norm of the S-parameter matrix [5].

V. BACKPLANE SIMULATIONS

The first step to obtain meaningful simulations is to make sure that the input data are correct and that they represent properly the system under test.

The passivity and causality features of the LPA briefly described in Section IV are used for this purpose.

The passivity check result is shown in Fig. 7 for the overall card-to-card link path. The 2-norm of the 4-port S-parameters is computed and it is compared to one that is the limit for a passive system.

The norm of the S-parameter matrix passes this limit three times at low frequency reaching a maximum value of 1.017686. This kind of response allows to state that the measured data represent a passive system since the computed 2-norm is below one for almost the whole frequency range.

Fig. 8 presents the results of the causality check for the differential transfer function S_{DD21}. This parameter includes the information about the propagation of the differential signal launched at the driver, therefore it is needed for link path analysis through the eye pattern simulation. The causal imaginary part of the S_{DD21} parameter is extracted and it is compared to the original one. The two curves are completely overlapped, therefore one can concludes that the parameter that is being employed in the simulation characterizes a causal system.
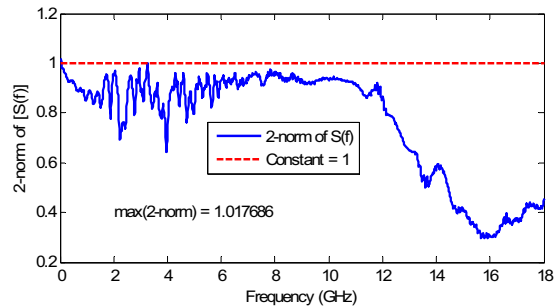

Figure 7. 2-norm of the S-parameter data set related to the overall card-to-card link.
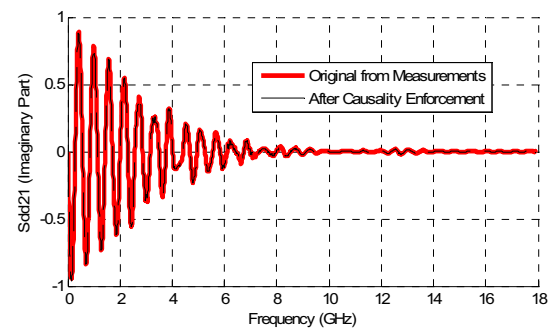

Figure 8. Causality check for the differential transfer function S_{DD21}.

Next step is calibrating the simulation, comparing the measured eye diagram at the end of the differential trace and the simulated one with the same PRBS signal at its input. Fig. 9 shows the eye diagram simulated with LPA. The MEO and MEW are 209mV and 159ps respectively. They are very close to the measured one (MEO = 232mV, MEW = 150ps).

The pre-emphasis technique allows to boost the high frequency components of the signal at the input of the trace, compensating the losses in the transmission medium. Fig. 10 shows how the pre-emphasis acts on the signal in the time domain and how calculating its percentage. The LPA provides a simulated eye pattern as in Fig. 11 by setting the pre-emphasis at 30%,. The value of the eye opening is now 306mV, that means almost 50% more than the signal without pre-emphasis.
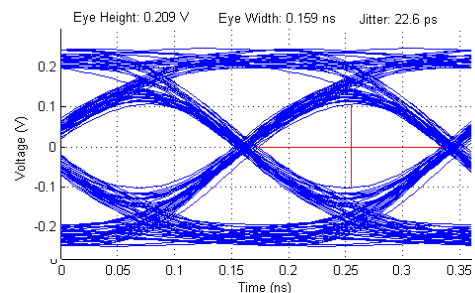

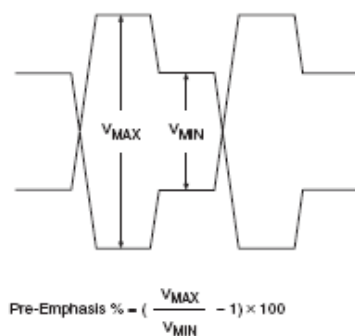Figure 9. Simulated eye pattern at the end of the differential trace.
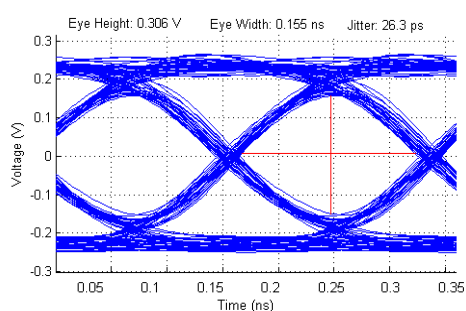
Figure 10. Pre-emphasis technique.

$$\text{Pre-Emphasis } \% = (\frac{V_{MAX}}{V_{MIN}} - 1) \times 100$$

Figure 11. Simulated eye pattern at the end of the differential trace with pre-emphasis setted at 30%.

Figure 12. Simulated eye pattern at the end of the differential trace with pre-emphasis setted at 30% and input signal at 400mV.

The simulation shows that the pre-emphasis is needed because it increases the signal eye opening, also considering that the minimum signal at the input of the trace can be 400mV. Setting the amplitude of the input signal at 400mV and the pre-emphasis at 30%, the simulated signal at the end of the differential trace is in Fig. 12. The pre-emphasis guaranties a MEO = 220mV at the end of the link, which is the minimum eye opening for correct transmission with a receiver threshold equal to 200mV. Consequently the simulation shows that the length of the laid out link is the maximum possible at 5.5Gbps and with input signal amplitude equal to 400mV.
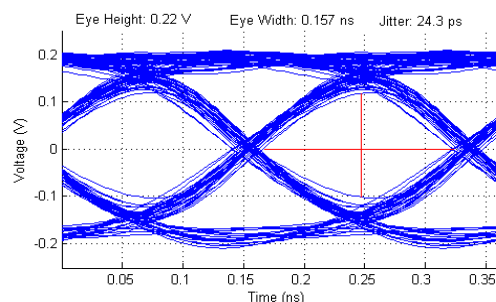
VI. CONCLUSIONS

The paper characterizes a serial link at 5.5Gbps laid out on a board in FR4 using both measurements and simulations. The novelty is that, for speeding up the design cycle, the PCB has been designed using guidelines due to the experience, while the simulations have been made as a second step starting from files obtained from measurements. The method resulted effective, allowing to set the link without spending a lot of time in complex pre-layout simulations.

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