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Application and Limits of IC and PCB scanning methods for immunity analysis

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***Abstract*— Immunity scanning methods can be used to locate sensitive areas on PCBs and ICs. For the analysis of emissions near field scanning is used to determine the local field strength. Both methods have many similarities and differences. For both methods it is difficult to correlate between board level scanning and system level test results as neither method shows the coupling path directly. The paper shows the implementation of an immunity scanning system and analyzes the advantages and limitations of immunity near field scanning.**

I. INTRODUCTION

Immunity scanning has been used by different researchers for analyzing PCB and IC immunity [1-5]. It is able to identify sensitive traces, Pins and ICs. After locating sensitive areas, in-circuit probing while performing ESD testing allows analysing the reaction of the integrated circuit and can provide feed back to the IC or PCB designers. However, the system designers and integrators are interested in system level test results, such as those achieved using IEC 61000-4-2, -4-3 or similar tests. The difficulty resides in correlating system level tests to local injection tests. A local scanning test can reveal a multitude of sensitive nets but those nets may not form good antennas. Or expressed in form of system analysis: The transfer function between the external noise and the sensitive net may need to be known to estimate if the sensitive net will lead to a system level problem. It is obvious that two boards connected by a flex cable will form a much better antenna than a trace on a board. This paper compares the events that unfold in system level ESD testing relative to the local injection as it is done during immunity scanning of PCBs. Using this insight the reader may be guided in using near field immunity scanning with greater success.

II. SCANNING SYSTEM

The scanning system used for performing this work has been described in [1,5]. A local electric, magnetic or direct injection probe is moved to a set of predefined locations. At each location pulses from a transmission line pulser, or other RF signals are injected while the performance of the DUT is observed. For each point a sensitivity threshold is determined such that a sensitivity map is created. These maps are plotted as an overlay to the PCB layout or a photo of the system.

III. TYPICAL TEST RESULTS

Test results that show differences between the E-field and the H-field scanning have been selected to emphasis the difference in coupling mechanisms discussed in this paper. Displays are known to be ESD sensitive. Figures 1 and 2 show scan results of a display for the magnetic field and the electric field respectively. As seen from Fig. 1 the magnetic field couples mainly directly into the DIE of the glass mounted driver IC.

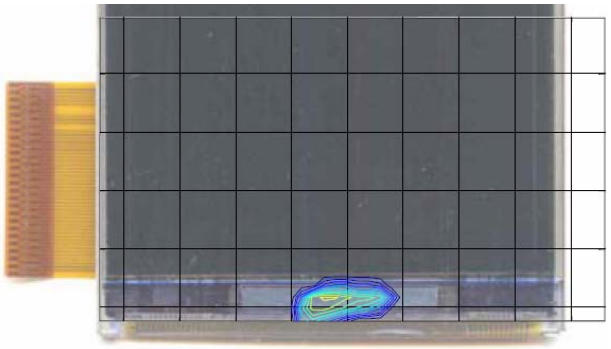

Fig. 1: Scanning result for magnetic field coupling (vertically oriented) on a display module.

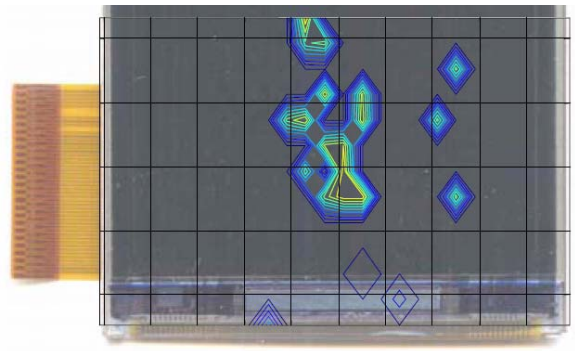

Fig. 2: Scanning result for electric field coupling at positive polarity.

The DIE has been mounted directly to the glass using flip-chip technology. Multiple coupling mechanisms exist: If the conductivity of the substrate is low, it becomes transparent to the magnetic field. This allows direct coupling into the IC. However, the structures, even the metallization layers are relatively small (at most about 6 mm long). Another coupling mechanism is the induction of pulses on the connecting traces on the glass. However, the location of the most sensitive

region is directly above the DIE. In both cases narrow pulses are used to cause a disturbance. These disturbance pulses are relatively narrow, compared to the pulse length and the rise and fall time of the pulses seen during operation of the display. This indicates that a slower I/O may perform better in a system level test.

If the same display is subjected to a rapidly varying local E-field (Fig. 2), most of the sensitive areas can be seen on the display area. The rapidly varying E-fields will couple into the matrix of wires and active elements within the glass. For reducing current consumption they form high impedance circuits which typically are sensitive to E-fields. Another possible coupling mechanism, only existing for the E-field is the return current. The return current will flow from the display via the flex cable. Those flex cables often have no shielding layer, thus the common mode current can easily lead to differential voltages that can disturb the driving IC. This coupling mechanism was not observed in this case, but it has been often observed in displays driven by LVDS connections.

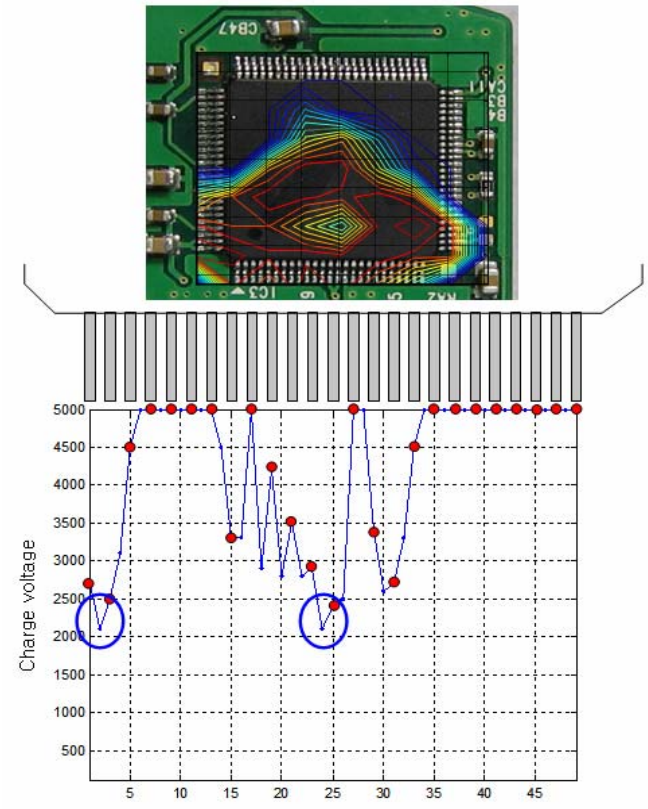

Fig. 3: Scan result (top) and sensitivity of pins determined by direct injection (via 1 pF capacitance) using 250ps rise time transmission line pulser.

Once sensitive areas are determined, voltages at the IC pins can be measured. The localized injection during the scanning greatly simplifies the measurement of voltages on traces during ESD testing. Another option for the next step of the root cause analysis is the use of direct injection into the Pins. The result of pin by pin testing is shown Fig. 3

IV. Coupling during system level testing

System level tests differ in the injected signal and in the injection method. On one extreme IEC 61000-4-2, radiated immunity, uses a far field injection method. On the other extreme IEC 61000-4-6 uses a highly localized injection on cables. ESD testing is in between. On one side the ESD generator will inject a current at the discharge point, on the other side fields radiated from the ESD generator and fields created by the current in the ground return will lead to a more general excitation of the EUT.

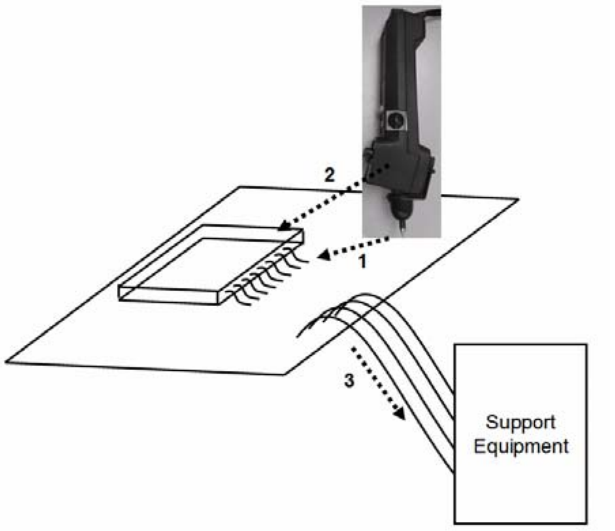

Fig. 4: ESD discharge to a PCB being connected to a second module.

Fig. 4 shows a scenario that might happen in a consumer electronic system like a video phone. Holes in the plastic enclosure allow direct discharges to grounded areas on the PCB. Distinguishing three main coupling mechanisms can assist in understanding the system response and the relationship to local scanning results.

- Path 1. The current spreads after the discharge on the board's ground structure. The current wave will be reflected at the edges of the board and cause the board to ring at its natural resonance frequency. The magnetic field associated with the current density and the displacement current associated with the (moving) charge density couple to traces, possibly leading to bit errors.
- Path 2. The transient fields of the ESD generator can couple directly into the IC's lead frame, Pins and bond wires. Especially in very dense boards, e.g., cell phones this seems to be a dominant mechanism.
- Path 3: The current will spread on the board and flow onto attached cables as common mode current. The common mode current will contain parts of the fast rising initial peak current and spectral components caused by the even faster rising transient fields of the generator and the slower body waveform. The common mode current can be converted into differential mode disturbance currents by any geometrical or electrical asymmetry.

If scanning is performed on such a board the injection is very local. The injection does not scale with the length of a trace (as the real coupling does) and it does not change with the position of a trace (e.g., edge or middle of the board). For a system level test a trace that is close to the edge will couple more strongly to the external noise as the mutual inductance between the trace and the ground structure is much larger for traces at the edge than for traces in the center of a board.

V. INJECTION PROBES

As both, the E and the H-field lead to disturbances one needs to scan using both probes to reveal the relevant sensitivities. In contrast to the current injection caused by the E-field, an H-field probe will induce a voltage in a trace. This is illustrated in Figs. 5 and 7.

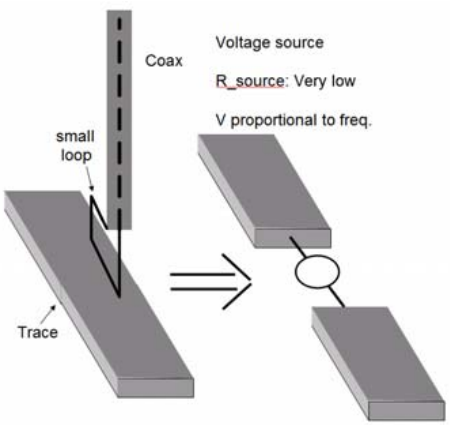

Fig. 5: A loop probe placed above a trace causes a series voltage source being inserted into the trace. The voltage is proportional to the derivative of the inducing magnetic field.

The magnitude and wave shape of the voltage is determined by the time derivative of the pulse injected into the loop as long as the magnetic coupling dominates over the often unwanted electric coupling of a loop probe. An example is shown in Fig. 6. In system level testing the induction is distributed: The longer the trace the larger the voltage, while the induced voltage in local scanning stays constant with trace length.

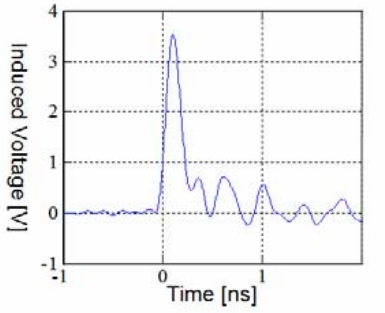

Fig. 6: Induced voltage by placing a 1 x 1 mm loop above a 7 mil wide 50 Ohm trace. The loop is attached to a transmission line pulser having an open circuit voltage of 500 V and a rise time of approximately 250 ps.

A narrow pulse is induced. Its width is only a few hundred picoseconds. For a TLP setting of 500 V about 3.5 V are induced for the typical trace arrangement selected. If this pulses reaches an IC input and if the IC input can react fast enough, such voltage levels can lead to soft-errors.

The electric field injection differs in two regards:

- A current is injected into the trace
- The return current will distribute over the PCB and partially (mainly at higher frequencies) return to the probe as displacement current. Other parts of the injected current will return via the cabling system.

The important difference is: E-field probing will lead to common mode currents, while H-field probing will lead to common mode currents to a far lesser extent.

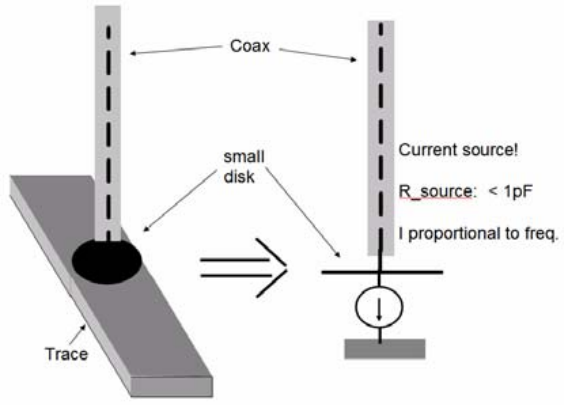

Fig. 7: A small disk connected to the centre conductor of a cable injects a current into a trace.

After inspecting the injection methods one may ask which circuit reacts to the E-field coupling, which ones to the H-field coupling?

It is well known that high impedance circuits are sensitive to the electric field and low impedance circuits are sensitive to the magnetic field. Let us illustrate this in a circuit example. Such examples are often seen during PCB scanning using the susceptibility scanning method.

As example, imagine an IC input that is either connected to a capacitor (for filtering and RF grounding) or to a pull-up resistor. There are four cases:

a) 1 kΩ Resistive pull up with H-field coupling
b) 1 kΩ Resistive pull up with E-field coupling
c) Capacitor to GND with H-field coupling
d) Capacitor to GND with E-field coupling

In case (a) the voltage induced by the magnetic field will be shared by the 1 kΩ resistor and the input capacitance of the IC (typically: a few pF). The TLP induces a narrow pulse. Most of the voltage will be dropped at the 1kΩ consequently the IC may not be disturbed. For case (b) the current injection will change the voltage on the input, thus it may lead to a disturbance. In case (c) a capacitor is mounted to ground. Let us further assume there is some trace length between the capacitor and the input of the IC. The magnetic field causes a voltage source. The capacitor forms a low impedance for a narrow pulse, thus the voltage will drop at the input of the IC.

In case (d) the injected current will flow through the capacitor to ground, the IC will not be disturbed.

The other question posed above is in regards to the return current. Isn't there any return current in current injection?
In our testing we do not connect the shield of the coax cable to the PCB. Thus, there are two returns: A return by displacement current from the shield of the coax to the planes of the board and a low frequency return via the grounding of the board and the grounding of the transmission line pulser.
The important consequence is: In E-field injection there is a common mode current on the PCB and the attached cables, in H-field injection there is no or very little common mode current. For H-field coupling the disturbance effects are highly localized, but in E-field testing the common mode current may cause disturbances at locations far away from the injection points. Is this realistic? Yes, in system level testing a local injection of current takes place. This can couple locally in a manner similar to the scanning system. However, the current will spread on the system being tested and may lead to problems far away from the injection points. An example is the coupling into a LVDS cable connecting an LCD display to a controller IC. If the ESD is applied to the display, a non local disturbance will occur. In scanning, the display may show immunity, while the LVDS cable may show a lack of immunity.

VI. Application of Scanning

Acceptable field performance, often, more or less well expressed as passing system level ESD testing, is the ultimate goal of EMC. However, system level testing often suffers from reproducibility problems. This has been shown in a variety of papers and a larger series of round robin tests has been conducted by the IEC TC77b ESD working group (partial results will be published in the IEEE EMC Symp. In Hawaii, 2007). As listed below, a variety of reasons contribute to the variations.

COMPARISON OF SYSTEM LEVEL AND LOCAL TESTING

	Comparing system testing and local scanning	
	System level	**Local scanning**
Time dependence of the sensitivity	Enough pulses need to be applied. Testing if the observed sensitivity level and its reproducibility is a function of the number of applied pulses will show if enough pulses are being applied	
Brand to brand variability of ESD generator fields and currents	Can cause 1:3 test result variations	Both pulse source and coupling are well defined. The induced voltages can be characterized by measurements on traces
Excitation	Complete system excitation by fields and common mode currents	Very local excitation for H-field probes, mainly local excitation for E-field probes
Level of automation	Often performed by hand (ESD)	Fully automated

Using immunity scanning a much better reproducibility can be achieved, see Fig. 8. This allows a test to determine if a circuit modification improved a design or not.

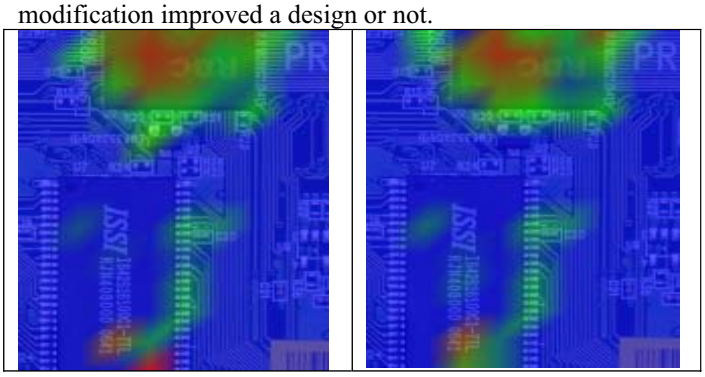

Fig. 8: Scanning results for repeated scanning showing the reproducibility of immunity scanning using 250 ps rise time TLP.

Other applications of scanning are:

- Reduce production risk due to prequalification for soft errors.
- Increased component flexibility in second sourcing without full system immunity tests.
- Provide soft-error specifications to manufacturer.
- Pass responsibility onto IC manufacturer by well repeatable quantified data.
- Sensitive Pins, or coupling into the bond wires can be identified.
- Layout and PCB guidelines and specifications can be created on known sensitivities.

VII. Conclusions

Relative to system level one can conclude the following advantages (+) and disadvantages (-):

+ Detailed information on the source of a problem, system testing provides no reason for a problem
+ Module and PCB level testing possible
+ Applied to second source qualification: Helps avoid system level testing
- System testing is closer to formal qualification testing
- System testing is closer to the customer environment
- Interpretation of test scanning results is not always easy
- Scanning may find sensitive nets that do not show up in system level testing.

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