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An Impact of Layer Stack-up on EMI

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Abstract: *Investigation of a server shows the heatsink of the CPU module as a primary component of the EMI coupling path. In order to identify the specific noise source and coupling path to the heatsink, a series of experiments were defined to provide support for one source and eliminate others. Based on experiments with two different versions of the CPU module, a stack-up related design guideline is proposed: a ground layer should be the first entire plane (as opposed to V_{cc}) on the active component side of the board. If there are known IC sources that switch significant currents with the outputs unloaded at nanosecond rise and fall times on both sides of the board, then ground should be the first entire plane on both sides of the board when feasible.*

I. INTRODUCTION

The importance of the stack-up for a successful high-speed PCB design is well known. For example, one proposed solution is to minimize power bus noise by increasing the interplane capacitance [1], [2], [3]. Even if this is a primary criteria for a good stack-up design, in some cases supplementary criteria may be necessary. In a previous paper, an investigation of a server was presented [4], showing the heatsink of the CPU module as a primary component of the EMI coupling path. In the simplified schematic presented in Figure 1 the parasitic current path is shown. Sources at the PCB level drive the heatsink against the CPU module ground, or the extended ground in the motherboard. Two CPU modules, denoted CPU #1 and CPU #2 were available for the investigations. The two modules were functionally equivalent, but from an EMI point of view CPU #2 had significantly lower emissions above 900MHz. There were differences in routing as a result of the change in memory and clock distribution, but these aspects proved to be minor from an EMI perspective. The clock buffer (a FAST CMOS, 1- to -10, with switching times under 1.5 ns) was the same in the two designs. The CPU #1 module had 2MB of cache memory, while CPU #2 module had 1MB. The clock distribution in CPU #2 module used only two outputs of the clock buffer, one to the processor and four cache memory modules, and one to the cache controller and other four cache memory modules. Each clock line was terminated in a diode clamp. The clock distribution in the CPU #1 module employed six outputs of the clock buffer, one to the processor, one to the cache controller, and four to the cache memory (one per two memory modules). The clock lines in the CPU #1 module were resistively terminated with 220 Ω to ground and V_{CC}. In both designs the clock layer was between a set of power planes, and the heatsink was identical.

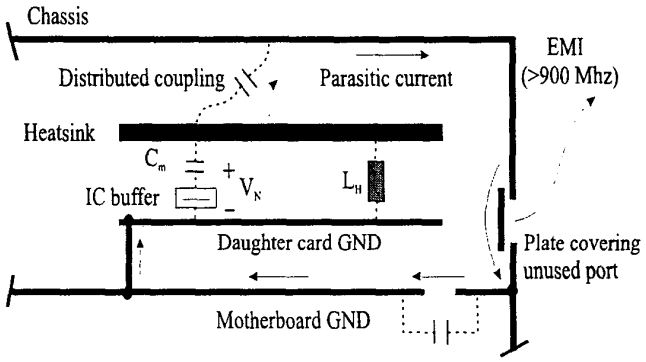

Figure 1. Schematic representation of the noise coupling path from the PCB source to the slot in the enclosure.

A significant difference between the CPU #1 and CPU #2 PCBs was the layer stack-up. Each was a twelve layer board, as shown in Figure 2 and Figure 3. The first solid layer in the CPU #2 design was a ground plane (GND), and physically this was the second layer. In the CPU #1 design the first solid layer was a power plane (V_{cc}), and physically was also the second layer. At frequencies above 500MHz, the dimensions of the structures involved such as the heatsink are a significant fraction of the wavelength. The field and current distribution is than behaving in a distributed fashion, and radiation from the heatsink, or enclosure excitation by the heatsink can result [5]. The heatsink on the CPU #1 and CPU #2 modules was grounded to the PCB ground through the chips, but not directly. The inductance L_H in Figure 1 denotes the impedance associated with this connection.

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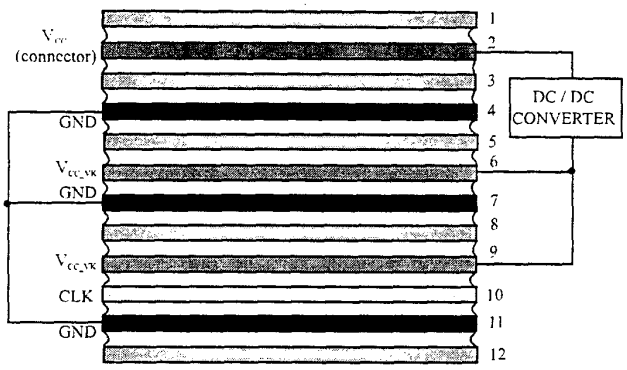

Figure 2. Layer stack-up for the CPU #1 PCB module.

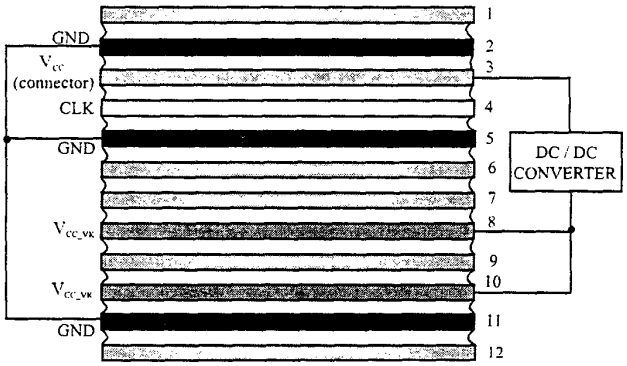

Figure 3. Layer stack-up for the CPU #2 PCB module.

II. THE COUPLING PATH

In order to identify the specific noise source and coupling path to the heatsink, a series of experiments were defined to provide support for one source and eliminate the others. The specific experiments were conducted with the CPU #1 PCB both in the functioning server, as well as with the PCB out of the chassis [4]. These experiments are summarized in Table 1. All the tests were radiated EMI measurements, with the exception of #3, which was noise measurements on the power planes V_{cc} and GND.

The first experiment was to add a dielectric material with $\varepsilon_r \approx 5\text{-}10$ between the buffer and heatsink. The radiated EMI increased for this configuration. If the noise coupling were from the buffer package, the dielectric material would increase the capacitance to the heatsink and result in increase. Likewise the dielectric material would increase the capacitance to the heatsink if the noise were coupling from the power plane V_{CC}. The dielectric material was also placed above the memory modules to test coupling from another area of the power plane, as well as to test if the noise coupling from the memory modules could be the path, since this was one significant change between the CPU #1 and CPU #2 module designs. There was no change in the radiated EMI in this case, indicating that coupling from the memory modules is not a likely candidate. It does not by itself provide evidence against coupling from the V_{CC} plane to the heatsink, since, as discussed below the noise on the V_{CC} power planes was greater in the vicinity of the clock buffer.

The third experiment measured the power bus noise on the V_{CC} and ground planes powering the clock buffer and memory, as well as on the $V_{CC\text{-}VK}$ and ground planes powering the processor and the cache controller. The measurements were made by connecting an 0.085" coaxial semi-rigid cable probe across the terminals of decoupling capacitors and measuring the output on a spectrum analyzer. The measured noise voltage on the V_{CC} planes was approximately 10 dB greater at the buffer location than elsewhere on the V_{CC} power planes. The measurement locations were distributed over the board including at the connector. The measurements on the $V_{CC\text{-}VK}$ planes were in general approximately 10 dB less than the average level on the V_{CC} planes, though the DC current draw by the processor and the cache controller was much greater. The total DC current draw by the CPU #1 module attached only to a bench power supply was 4 A. With the $V_{CC\text{-}VK}$ power planes disabled, the current was under 1 A. The high-frequency current drawn by the processor and cache controller was expected to be greater than by the combined memory and clock buffer, however, the noise on the planes powering the processor and the cache controller was less. This difference in the measured RF noise on the V_{CC} power planes versus the $V_{CC\text{-}VK}$ planes could result from the decoupling added on the processor and controller packages, or the greater interplane capacitance of the $V_{CC\text{-}VK}$ power planes.

The heatsink for the processor and controller modules spanned the length of the PCB, including over the memory ICs on the top board side, and was extended over the clock buffer in both CPU #1 and CPU #2 designs. There were several millimeters of space between the heatsink and the buffer package though, and the heatsink was not intended for any cooling of the buffer package. The portion of the heatsink extending over the buffer was cut away in the fourth test. There was a decrease in the radiated EMI for the CPU #1 module out of chassis, though no significant change was measured in the functioning system.

A shield was placed over the clock buffer in the fifth experiment. The shield, a small piece of copper tape, was flat and covered only the top surface of the buffer, and did not overhang the buffer package. The shield was soldered through wide connections (low inductance) to all five ground pins of the buffer. There was an appreciable decrease at the 60MHz clock harmonics in the radiated EMI as shown in Figure 4. Initially the connections to the buffer ground pins were through relatively thin strips and connected to only one or two ground pins. An increase in radiated EMI was measured. The increase could have resulted from an increase in the capacitance between the buffer

package and the heatsink. If the noise were coupled from the V_{CC} plane an increase in capacitance to the heatsink would also increase the EMI. However, the measured decrease for a shield connected through low inductance to the IC ground pins would result only if the noise coupled from the buffer package to the heatsink. This is a critical experiment to distinguish between the buffer or the power planes as the specific noise coupling path to the heatsink.

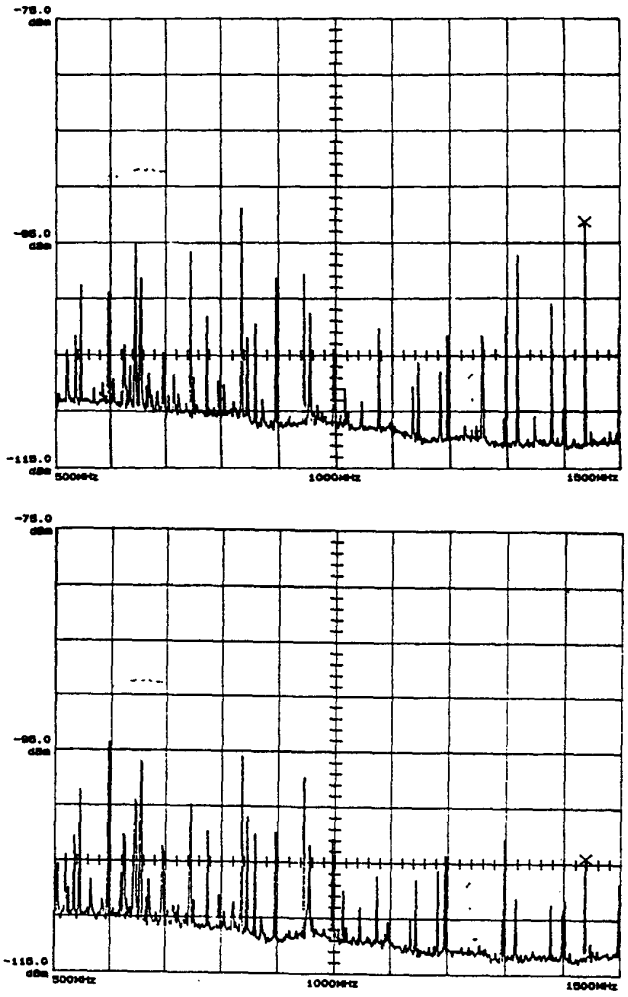

Figure 4. Radiated EMI for one CPU #1 module in the functioning server a) original configuration, and b) with a shield on the top of the clock buffer package.

Experiment 6 was a "sanity" check on the heatsink as a significant contributor to the EMI coupling path, and for comparison and contrast to Experiment 7. The heatsink was well grounded through wide copper tape strips from the heatsink to the PCB ground at points around the entire periphery of the heatsink. While the grounding was far from ideal, it did provide a lower impedance path to the PCB ground than the connection through the processor and controller packages. The radiated EMI measurements for this case are compared in Figure 5. There is a significant decrease for the harmonics above 900MHz, with little or no effect at lower frequencies. Experiment 7 connected the heatsink at multiple points to the V_{cc} plane. If the coupling path were noise on the V_{cc} plane, the radiated EMI should increase.

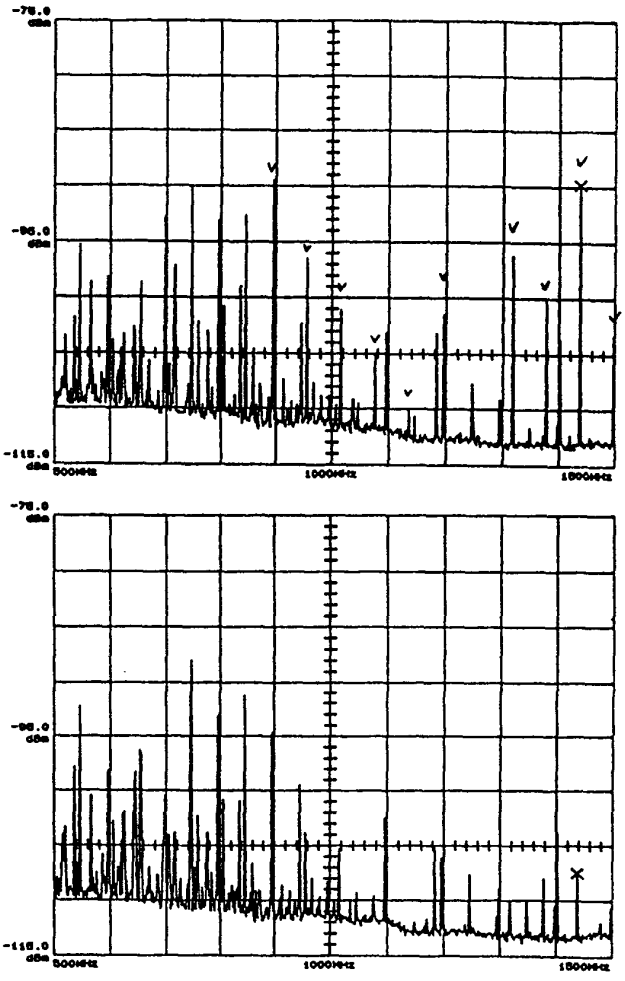

Figure 5. Radiated EMI for one CPU #1 module in the functioning server a) original configuration, and b) with the heatsink grounded around its periphery.

However, the radiated EMI decreased. This decrease is indicative of a lower impedance path back to the reference planes on the buffer package as a result of a direct connection to the V_{cc} plane versus "capacitance" between the heatsink and the plane.

A final set of experiments to determine the coupling path was to provide a better antenna for the coupling path with the module out of chassis and powered only by a bench supply. With the

Table 1. Experiments and results for Identifying the Noise Source - Radiated EMI

Experiment	Server	Module	Noise Source	
			Power planes	IC Buffer
1. ε_r material above buffer (between heatsink & card)	⇑	X	Y	Y
2. ε_r material above memory	-	X	?	?
3. Noise voltage on power planes (10dB greater @ buffer location)	X	*	Y	Y
4. Heatsink cut away around buffer	- ⇓	⇓	Y	Y
5. Partial shield over buffer	⇓	X	N	Y
6. Improved GND on heatsink	⇓	X	Y	Y
7. Heatsink tied to V_{cc} (insulated from GND)	⇓	X	N	Y
8. No heatsink, 1"x1" Copper tape on buffer	X	⇑	?	Y
9. 1"x1" Copper tape on PCB near buffer	X	-	N	Y
10. Extended GND and PWR on PCB (no heatsink)	X	-	N	?

⇑ ⇓ 5-10 dB increase or decrease for f>1GHz
– No change in radiated EMI
X Test not conducted
Y Test supports indicated noise source
N Test rejects indicated noise source
? Test yields no information
* Not a radiated test, noise measurements on power bus

heatsink removed, the EMI antenna for the buffer coupling path was the reference plane on the buffer package being driven against the PCB reference plane and cable. The small size of the buffer package makes this a particularly poor antenna. If the coupling path were from noise on the V_{cc} power planes, the size of the PCB reference plane driven against the cable is of resonant dimensions and will have an input impedance on the order of 100 Ω. Thus, adding electrical extent or length would result in little significant change. First 1" x 1" square of copper tape was bonded to the top of the buffer chip, and an increase in radiated EMI resulted. When the same square was attached on the back edge of the PCB adjacent to the buffer, there was no change in the EMI. The electrical length of the PCB reference plane was extended with a length of wire approximately 0.5 m with no change in the EMI as well.

The set of experiments detailed in Table 1 have eliminated noise coupling from the power planes as a possible path, in particular Experiments 5 and 7. Although the size of the buffer chip was only approximately 8 x 12 mm^2, the noise coupling path was switching noise coupling from the buffer power bus to the heatsink. High-frequency currents on the heatsink were driving cavity modes of the enclosure, and radiation was occurring through perforations. In particular slots associated with the plate-covered connector aperture as illustrated in Figure 1 were primary leakage points.

III. SIMPLIFIED MODELS

Models for the coupling path from the buffer to the heatsink are proposed in Figure 6 and Figure 7 for the CPU #1 and CPU #2 designs. These models assume that the reference structure on the IC is of greater electrical extent than the V_{cc} conductors. This is often the case in IC design. Further, it is assumed that the coupling results from the "crowbar" current effect, during the short interval of the LO to HI (or HI to LO) transition when both transistors of the output stage of a gate are conducting. Though the heatsink is grounded through the processor and cache controller modules, this connection is a relatively high impedance and proved to be ineffective above 1 GHz, and is not shown in the model. For simplicity only V_{cc} and GND are shown schematically in the figure. The inductance shown in the V_{cc} and GND connections of the IC to the PCB planes represents the parasitic package inductance.

The current through the parasitic package inductance cannot change instantaneously when the switch opens as a result of energy storage in the magnetic field. In both the case of CPU #2 and CPU #1 PCB there are two parallel paths for the current through the parasitic package inductance to complete a closed path. One path couples to the heatsink through parasitic capacitance between the buffer reference plane and heatsink, then couples to the chassis, and returns through chassis connections and parasitic capacitance to the PCB reference plane and buffer. This path is the same in both the CPU #2 and CPU #1 designs. The other current path is first capacitively coupled to the heatsink, but then returning through capacitance between the heatsink and the solid copper plane on Layer 2 in the specific design. In the CPU #1 design it is V_{cc}, and in the CPU #2 design it is GND. For the CPU #1 PCB, the currents capacitively coupled from the heatsink to the V_{cc} plane in Layer 2 must return to the buffer reference plane beginning on the upper side of the V_{cc} plane (because of the skin effect) to the holes for the ground vias of the buffer, through these holes to the bottom side of the V_{cc} plane, and then through the interplane capacitance of the power planes to GND, and finally to the buffer package pins. Most of the current will take the holes in the V_{cc} plane through which the buffer pins pass, because the inductance is minimized through this path. The impedance of this path is significant at

frequencies above 1 GHz as a result of the inductance of the circuitous current path from V_{cc} on the PCB back to the ground pins on the buffer. The second current path for the CPU #2 design by contrast is very direct. Currents on the heatsink are capacitively coupled to Layer 2, PCB GND, and then return directly to the ground pins on the buffer. The impedance of this path is considerably less than in the case of the CPU #1 design. As a result, the current or energy coupled to the chassis is considerably greater for the CPU #1 design than for the CPU #2.

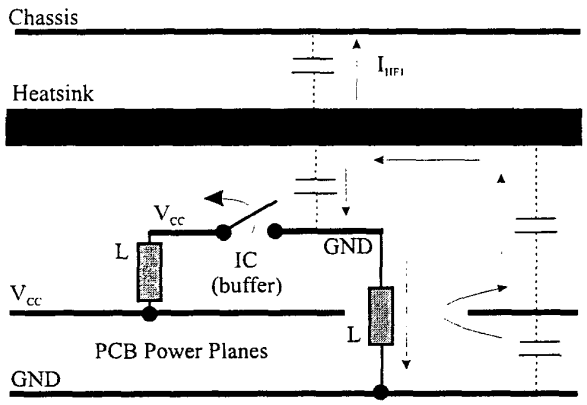

Figure 6. Model for the coupling path from the clock buffer chip to the heatsink for the CPU #1 design ($I_{HF2}<I_{HF1}$).

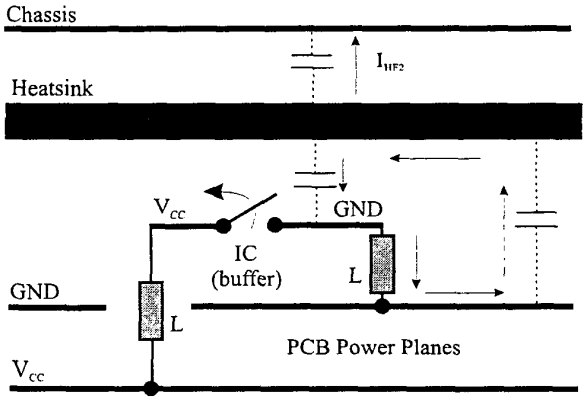

Figure 7. Model for the coupling path from the clock buffer chip to the heatsink for the CPU #2 design ($I_{HF2}<I_{HF1}$).

The influence of the layer stack-up was also checked in another functioning design, denoted below as DUT. In this case the product is a single PCB board design with four layers in a metal enclosure. The radiated emissions were significant up to 1 GHz. Starting with the component side (Layer 1), the stack-up was: Signal - GND - V_{CC} - Signal. Because of the component height, the distance between the GND layer and the metal case (top) was about 1". The distance between the V_{CC} layer and the metal case was only 1/8". Consequently, the capacitance of GND - case was much smaller than the capacitance of V_{CC} - case. The digital ground was ineffectively connected to chassis to limit the radiated emissions from attached cables. With only the power cable present, the tests show the cable driven against the chassis through the V_{CC} - chassis capacitance.

An additional layer on the bottom side, was fashion with copper tape through multiple connections to ground. Even though these

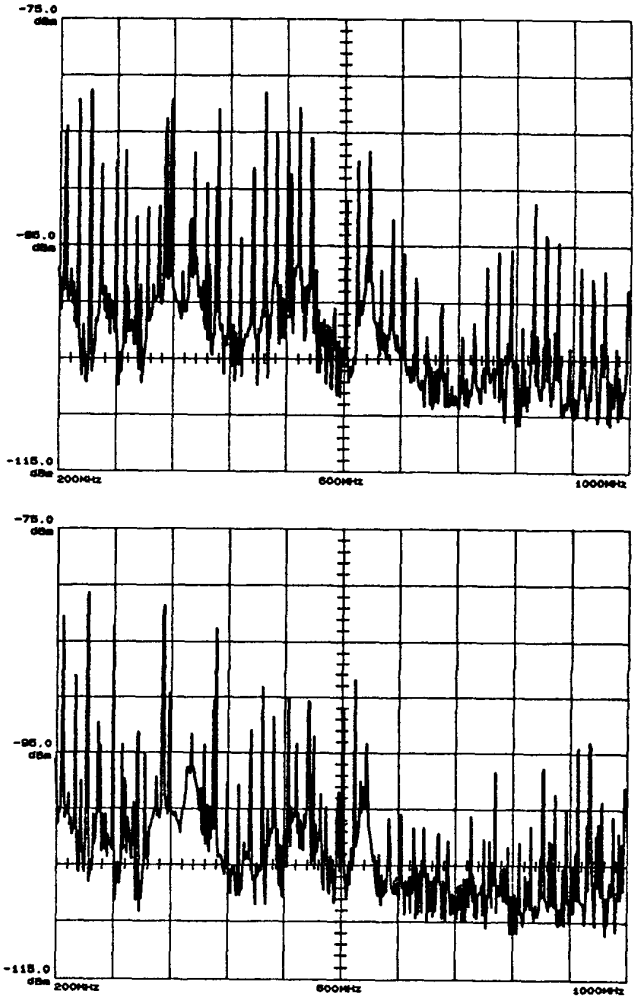

Figure 8. Radiated EMI for the DUT a) original configuration, and b) with a supplementary ground plane between the PCB and the enclosure wall.

connections were imperfect, greater than 5 dB reduction in radiated EMI resulted, in particular for frequencies above 400 MHz, as shown in Figure 8.

IV. SUMMARY AND CONCLUSIONS

Radiated EMI problems in two functioning PCB designs were shown experimentally to be related to the layer stack-up. The influence of layer stack-up on EMI is well-known in practice, and one mechanism has been demonstrated experimentally. Capacitive coupling from IC packages to significant metal structures including heatsinks and nearby shielding enclosure walls can lead to significant radiated EMI. This coupling can be exacerbated or minimized by different choices for the layer stack-up.

The study presented indicates that a ground layer should be the first entire plane (as opposed to V_{cc}) on the active component side of the board. If there are known IC sources that switch significant currents with the outputs unloaded at the nanosecond rise and fall time on both side of the board, then ground should be the first entire plane on both sides of the board if feasible. The two CPU modules differed principally in layer stack-up, one in which the stack-up proceeding from the side with the clock buffer was S GND etc., and the other with S V_{cc} etc.. The testing demonstrated that the first case was clearly superior for EMI design, in particular, for minimizing coupling to the heatsink. While the heatsink was necessary in the coupling path that was studied, as the size of IC packages continues to increase, the to source enclosure modes. An outer ground layer could benefit reference planes may themselves be of sufficient electrical extent these cases as well.

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