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An Estimative Current Mode Controller for DC-DC Converters Operating in Continuous Conduction Mode

Mehdi Ferdowsi
Missouri University of Science and Technology, ferdowsi@mst.edu

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Mehdi Ferdowsi, *Member, IEEE*

Power Electronics and Motor Drives Laboratory
University of Missouri-Rolla
Rolla, MO 65409, USA
Phone: (573) 341-4552; Fax: (573) 341-6671
E-mail: ferdowsi@umr.edu

***Abstract*—A new digital average-current-mode controller for converters operating in continuous conduction mode is introduced. The principal idea of the proposed control scheme is to estimate the required value of the duty ratio based on the dynamic of the converter using the measured samples of current and voltage signals. The proposed control scheme is stable for any value of the duty ratio without employing an external ramp. Furthermore, it is robust, accurate, and has a fast dynamic response.**

Keywords-continuous conduction mode; DC-DC power converters; digital control; switch-mode power supplies.

I. Introduction

Current mode control technique, in which the output voltage of a converter is controlled by choice of the peak or average value of its inductor current, has wide applications in switching power converters [1]-[5]. The major advantages of current mode control over the conventional single-loop voltage mode control scheme can be summarized as [6]: a) Failures due to the excessive switch current can simply be prevented by monitoring the data obtained via measuring the inductor current. b) Load sharing of several converters operating in parallel is more convenient. c) The design of the feedback network is easier due to the removal of one pole from the characteristic equation of the system. Most importantly, this results in a faster transient response of the converter.

Numerous current mode control techniques have been developed during the past three decades [7]. They are mainly suffering from sub-harmonic oscillations when the duty ratio is greater than 0.5 [8]. Adding an external ramp to the measured current signal would resolve the problem; however, the slope of the external ramp is constant and pre-selected with respect to the maximum value of the output power. Therefore, overcompensation of the converter in lighter loads deteriorates the speed of response of the converter.

In this paper, a new average current mode control algorithm is introduced. The basic idea of this control scheme is to estimate the required value of the duty ratio based on the measured samples of the current and voltage signals in order to make the inductor current track the control input signal [9-11]. This control scheme operates in fixed frequency and does not require an external ramp and is stable for the entire range of the duty cycle. The proposed control technique is robust against the variations of the circuit parameters and enjoys a very fast dynamic response. Furthermore, it is digital in nature and hence can easily be programmed in a digital signal processor (DSP) among the other required functions such as voltage compensation or power factor correction (PFC).

Section II briefly describes current mode control technique in continuous conduction mode (CCM). The proposed estimative current mode controller is presented in Section III. Section IV investigates the stability of the proposed control scheme. Simulation results are depicted in Section V. Effects of the error in the inductance estimation is studied in Section VI. Experimental result of applying estimative current mode control on a buck converter is presented in Section VII. Finally, Section VIII draws conclusions and presents an overall evaluation of this new control technique.

II. Current Mode Control

A simplified block diagram of a peak current mode controller is illustrated in Fig. 1. The *control input signal* is proportional to current $i_c(t)$, and the control network switches the transistor such that the peak or average inductor current follows $i_c(t)$. From this point on, in this paper, $i_c(t)$ is going to be referred to as *current command signal* (CCS). Current command signal can be a) the output of the voltage compensator circuit to regulate the output voltage, or b) the load sharing command signal to equalize the power that is being generated by the converters operating in parallel, or c) proportional to the input voltage to provide power factor correction.

The current mode controller illustrated in Fig. 1 is unstable whenever the steady-state duty cycle is greater than 0.5. To avoid this stability problem, the control scheme is usually modified by adding an external ramp to the sensed inductor current waveform [8]. However, due to the fixed value of the external ramp, the converter is overcompensated for most of the load values resulting in a slower dynamic response. Estimative current mode control, proposed in this paper, is a

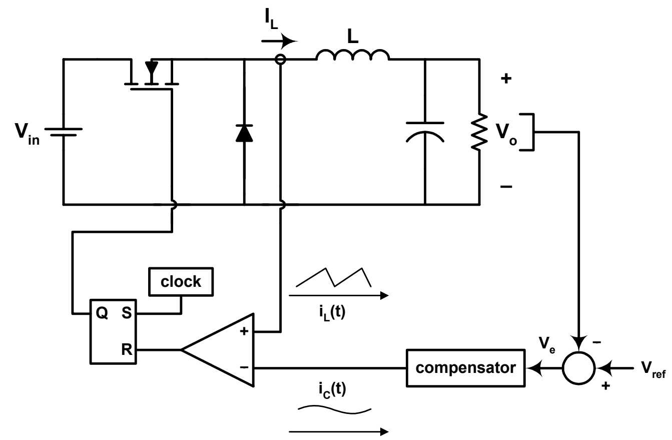


Fig. 1. Block diagram of a typical current mode controller.

new digital control method, which doesn't require an external ramp for compensation and is stable for the entire range of the duty cycle variations.

Without loss of generality, buck converter will be used to present the new current mode controller. This converter, Fig. 1, is a well-known switched-mode converter that is capable of producing a dc output voltage less than the dc input voltage. Typical transient and steady state current waveforms of inductor L during a single switching period, while operating in CCM, are shown in Figs. 2(a) and (b), respectively.

In Fig. 2(a), assuming that the ac ripple of V_{in} has a frequency much less than the switching frequency of the converter and the output capacitor is large enough to filter out the output voltage ripple, final value of the inductor current at the end of the switching cycle I_f can be written as:

$$I_f = I_i + TDm_1 - T(1-D)m_2 \tag{1}$$

where, in a buck converter, $m_1=(V_{in}-V_o)/L$, $m_2=V_o/L$, D is the duty cycle, T is the switching period, and I_i is the initial value of the inductor current at the beginning of the switching interval (Fig. 2(a)).

By simplifying (1) using the corresponding expressions for m_1 and m_2 in a buck converter, one obtains:

$$I_f = I_i + (T/L)(DV_{in} - V_o) \tag{2}$$

Solution for D yields:

$$D = L(I_f - I_i)/(TV_{in}) + V_o/V_{in} \tag{3}$$

Equation (3) specifies the required value for the duty cycle in order to have the desired final value for the inductor current.

In the steady-state operating mode, as shown in Fig. 2(b), there are two conditions that need to be satisfied; a) $I_f = I_i$ and b) the average value of the inductor current needs to be equal to the desired load current. Having the first condition in mind, equation (3) results in:

$$D_{ss} = V_o/V_{in} \tag{4}$$

The *ss* subscript is used to denote the steady-state operating mode. In the steady-state condition, the average value of the inductor current during the switching interval is given by:

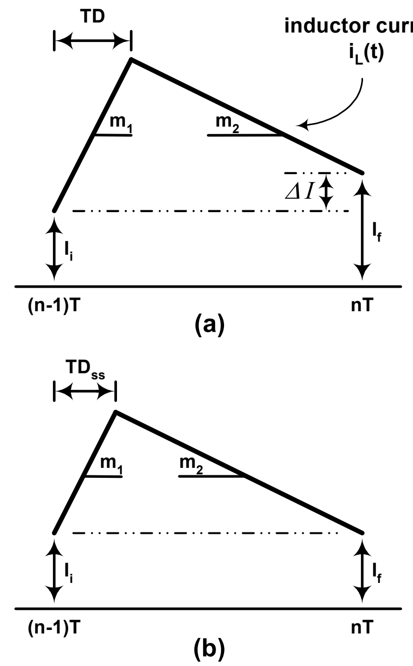


Fig. 2. Typical waveforms of the inductor current in a buck converter; (a) transient and (b) steady state.

$$\langle i_L \rangle_{ss} = I_f + (TD_{ss}m_1)/2 \tag{5}$$

III. Estimative Current Mode Control

In order to make the inductor current track the *current command signal* and reduce the tracking error, equation (5) needs to be retained in each single switching period. Since the average value of the inductor current will be delivered to the load, the desired tracking characteristic is to use *current command signal* (CCS) as the desired average value of the load and force the average value of the inductor current to follow this signal. Using equation (5), the desired value of I_f, which yields to attain the zero steady state tracking error can be obtained. In equation (5), by replacing $\langle i_L \rangle_{ss}$, by CCS, the required value of I_f is calculated as:

$$I_f^* = CCS - (TD_{ss}m_1)/2 \tag{6}$$

Now that the required final value of inductor current I_f^* is calculated, equation (3) can be used to compute the required value of duty cycle D^*, which makes the final value of the inductor current equal to I_f^* at the end of the switching interval.

$$D^* = L(I_f^* - I_i)/(TV_{in}) + D_{ss} \tag{7}$$

Therefore, at the beginning of each switching interval, input and output voltages and initial value of the inductor current I_i, as well as CCS, if it is not already a digital signal, are sampled. Then, using equation (6), the controller computes the *required* final value of the inductor current at the end of the switching cycle (I_f^*). After that, using equation (7), the controller computes the *required* value of the duty cycle which leads to have I_f^* at the end of the switching cycle. Applying this computed value of duty cycle to the converter makes the average value of the inductor current ($i_{L(av)}$ measured at the end of the switching cycle) follow CCS. The required mathematical computation (equations (6) & (7)) can be easily programmed in a DSP. Fig. 3 shows the block diagram of the controller. Based on the specific application, CCS can be obtained using the same DSP, or another DSP with a higher level, or an analog circuit.

IV. Stability Analysis

Instability and sub-harmonic oscillations of the current loop occurs when the desired duty cycle is not stable. Most of the current mode control techniques are unstable when the duty cycle exceeds 0.5. If the programmed current waveform is perturbed, in other words, if the initial value of the current is disturbed by ΔI_i, based on equation (7) the perturbed value of the duty cycle is:

$$\Delta D^* = -(\Delta I_i L)/(TV_{in}) \quad (8)$$

Using equation (2), such a disturbance in D^* will result in:

$$\Delta I_f = \Delta I_i + (T/L)\Delta D^* V_{in} \quad (9)$$

Combining equation (8) and (9) leads to:

$$\Delta I_f = \Delta I_i - \Delta I_i = 0 \quad (10)$$

Equation (10) shows that any kind of current disturbance will be depressed to zero after only one switching cycle. It is worth mentioning that large disturbances will result in D^* out of the feasible range of $0<D^*<1$. In this case, it takes more than one switching cycle to damp down the disturbance.

V. Simulation Results

Figs. 4(a) and (b) show the simulation results of the transient response of the converter to the step down and up changes of CCS. Simulation parameters are presented in Table I. As can be observed, the inductor current immediately follows CCS. In Fig. 4(a), before the step change the duty ratio is greater than 0.5 while after the step is less than 0.5. There are not sub-harmonic oscillations in any of the step changes. Fig. 5 shows the transient response of the converter to the step change of the load resistance while keeping CCS constant (at 5 Amps). Instability and sub-harmonic oscillations do not appear in any of the simulation results.

VI. Error in Inductance Estimation

As it can be observed, the numeric value of the inductor (L) appears in (6) and (7). Equation (7) does not really depend on the numeric amount of L. The control goal is to depress the first part of equation (7) (in which L appears) to zero. Therefore, a slight error in the estimation of the value of the inductor does not change the transient behavior of the control scheme. The error in L estimation, on the other hand, does affect the steady state response. Equation (6) can be written like:

$$I_f^* = CCS - \frac{TD_{ss}}{2}\frac{V_{in} - V_o}{L} \quad (11)$$

If ΔL represents the error in the numeric value of L, applying $L+\Delta L$ into this equation yields:

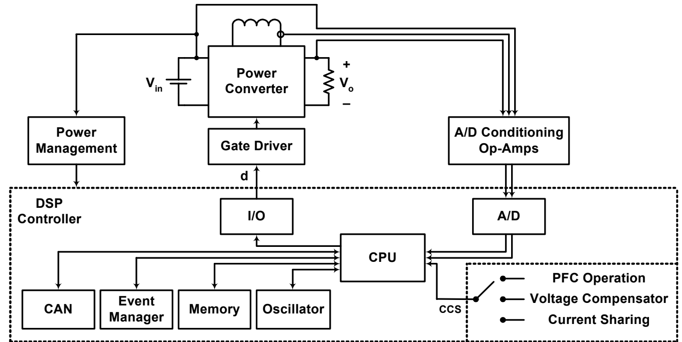
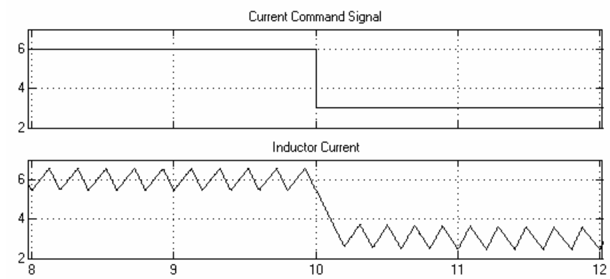
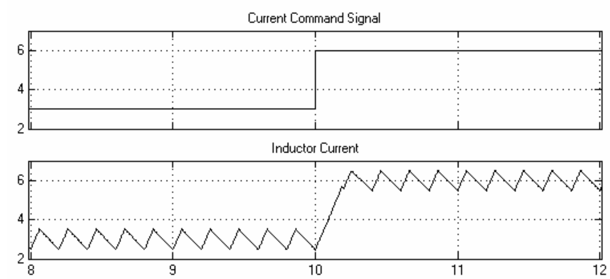


Fig. 3. Block diagram of the digital current controller.



(a)



(b)

Fig. 4. Simulation results of the converter transient response to the step change of the current command; (a) step down and (b) step up.

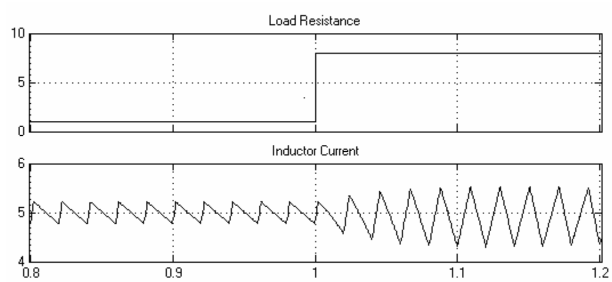


Fig. 5. Simulation results of the converter transient response to the step change of the load resistance.

TABLE I
SIMULATION PARAMETERS

Input Voltage	V_{in}	48 V
Inductor	L	200 μH
Output Capacitor	C	5 μF
Load Resistance	R	5 Ω

$$I_f^* = CCS - \frac{TD_{ss}}{2}\frac{V_{in} - V_o}{L + \Delta L} \quad (12)$$

Equation (12) can be rewritten like:

$$I_f^* = CCS - \frac{TD_{ss}}{2}\frac{V_{in} - V_o}{L} + \frac{TD_{ss}}{2}\frac{(V_{in} - V_o)\Delta L}{L(L + \Delta L)} \quad (13)$$

The third term in (13) can be interpreted as an error CCS. So the generated current will be slightly different from CCS. Since the variation of L is basically temperature or age dependent and is very slow, even a very slow voltage control loop can easily damp this error to zero. Fig. 6 depicts the simulation results of the response of the buck converter if a 30% step error happens in the assumed value of inductor L. As it can be observed from (13) and the simulation results, even applying a 30% estimation error doesn't greatly affect the operation point of the converter.

VII. Experimental Results

The TMS320LF2407A has been employed for the experimental implementation of the new estimative current mode controller. This DSP is designed to meet a wide range of embedded control applications and real-time signal processing.

This DSP is based on a 16-bit, fixed-point, low-power CPU, and uses new combinations of on-chip memory with a wide range of peripherals. These include; Analog-to-Digital converters (ADC), controller area network (CAN), event manager, serial communications ports, and safety features such as watchdog timers and power drive protection. In addition, most of the instructions of this DSP are single cycle. Therefore, multiple control algorithms can be executed at high speed, thus making it possible to achieve the required high sampling rate for a fast dynamic response.

Fig. 7 shows the experimental results of the buck converter being controlled with the estimative digital current control. This figure depicts the transient response of the inductor current after a step change applied to CCS. The vertical arrow marks the time instant at which the step change is applied. The experimental results highly agree with the simulation results and the system has a very fast dynamic response without any sub-harmonic oscillations.

VIII. Conclusion

The estimative current mode control technique that has been introduced in this paper enjoys the following advantages: I) Due to not being overcompensated, it has a very fast transient response. II) It is stable for any value of the duty cycle. III) It is easy to be implemented by a digital processor. IV) It is not sensitive to the circuit parameter variations.

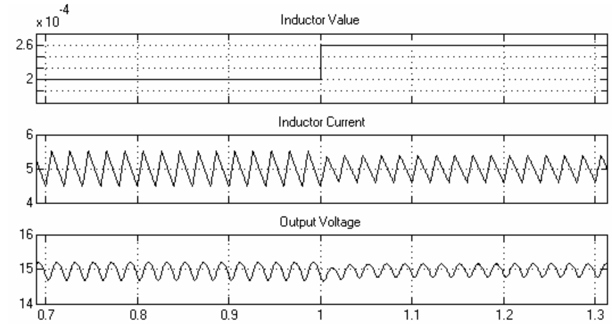


Fig. 6. Simulation results of the converter response to the 30% step change of assumed inductor value.

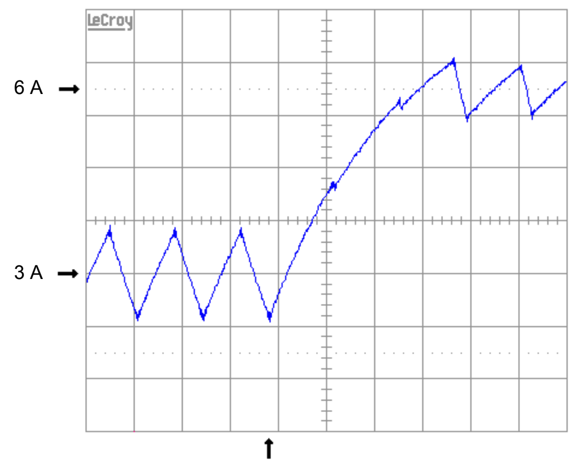


Fig. 7. Experimental results of the inductor current after a step up change in CCS.

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