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A Novel Seven-Level Shunt Active Filter for High-Power Drive Systems

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***Abstract* - In high-power adjustable speed motor drives, such as those used in electric ship propulsion systems, active filters provide a viable solution to mitigating harmonic related issues caused by diode or thyristor rectifier front-ends. To handle the large compensation currents and provide better thermal management, two or more paralleled semiconductor switching devices are often used. In this paper, a novel topology is proposed where two active filter inverters are connected with tapped reactors to share the compensation currents. The proposed active filter topology can also produce seven voltage levels, which significantly reduces the switching current ripple and the size of ripple filters. Based on the joint redundant state selection strategy, a current-balancing algorithm is proposed to keep the reactor magnetizing current to a minimum. It is shown through simulation that the proposed active filter can achieve high overall system performance. The system is also implemented on a real-time digital simulator to further verify its effectiveness.**

I. Introduction

Adjustable speed motor drives (ASDs) have found extensive application in a variety of high-power systems. One example is the electric propulsion system used in modern naval ships, the power ratings of which can be tens of megawatts. Typically the front-ends of such ASDs employ a diode or thyristor rectifier. In spite of their simple control and robust operation, these devices can result in serious power quality issues. They can generate voltage and current harmonics that might affect the operation of other devices in the same ac system. Conventionally, passive *L-C* filters are used to mitigate harmonic related problems. However, due to their large size and inflexibility, passive filters are gradually being replaced by active filters that utilize power electronic inverters to provide compensation for harmonics [1].

Among various active filter configurations, the shunt active filter systems have a number of advantages and constitute the optimal harmonic filtering solution for ASD rectifier front-ends [2]. Compared with the series and hybrid configurations, the shunt active filters do not need an additional coupling transformer and require much less protection and switchgear. They operate as three-phase controlled harmonic current sources and are not affected by harmonic distortions in supply voltages. In general, the ratings of shunt active filters are based on the rms compensating current and the rms filter terminal voltage. For high-power applications such as ship propulsion systems, the large compensation current often requires parallel operation of two or more switching devices or active filters.

In recent years, multilevel converters have shown some significant advantages over traditional two-level converters [2-3], especially for high power and high voltage applications. In addition to their superior output voltage quality, they can also reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower dv/dt is achieved, which greatly alleviates electromagnetic interference problems due to high frequency switching. Over the years most research work has focused on converters with three to five voltage levels [4-5], although topologies with very high number of voltage levels were also proposed [6]. In general, the more voltage levels a converter has the less harmonic and better power quality it provides. However, the increase in converter complexity and number of switching devices is a major concern for multilevel converter. It has been shown that although more voltage levels generally mean lower total harmonic distortion (THD), the gain in THD is marginal for converters with more than seven levels [7].

This paper presents a shunt active filter configuration that uses tapped reactors for harmonic current sharing. It reduces current stress of the switching devices by distributing the compensation current between two parallel legs of a H-bridge topology. It also reduces voltage stress across the switches by utilizing a conventional three-level flying capacitor topology. Overall, the configuration is capable of producing seven distinct voltage levels and thus greatly reduces switching ripple in the compensating currents.

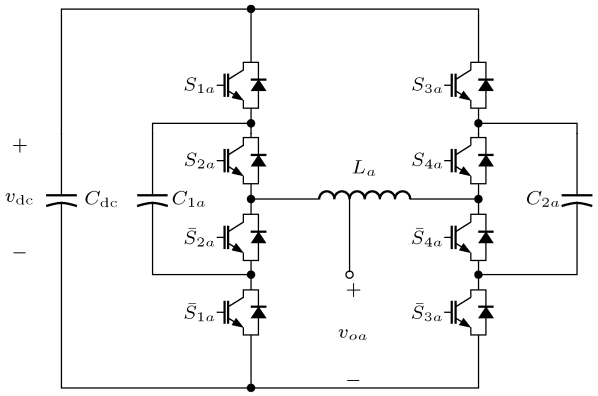

Fig. 1. Phase *a* of the seven-level active filter topology.

II. Active Filter Topology

The *a*-phase of the proposed active filter topology is

shown in Fig. 1.It consists of an H-bridge configuration made from three-level flying capacitor branches. Essentially, it is a voltage-source-inverter (VSI) with capacitive energy storage (C_{dc}) shared by all three phases. A total of eight switching devices are used in each phase. A tapped reactor is used to connect the two legs of the H-bridge, and the output terminal is at the one-third tap of the reactor.

III. Tapped Reactor Model

Unlike the center-tapped inter-phase reactor used in [8-11], the reactor in the proposed topology has a tap terminal at its one-third position. For the convenience of analysis, the reactor can be divided into two parts. As shown in Fig. 2, part one, denoted as L_1, consists of the portion from terminal 1 to the tap and has a number of turns $N_1 = N$; part two, denoted as L_2, consists of the portion from the tap to terminal 2 and has a number of turns $N_2 = 2N$. Terminals 1 and 2 are defined as the input terminals while the tap terminal is defined as the output terminal, O.

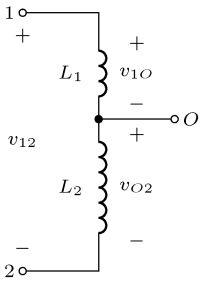

Fig. 2. Ideal tapped reactor model.

A. Analysis of an Ideal Tapped Reactor

To derive the relationship between the input voltages and the output voltage, an ideal model of the tapped reactor is considered first in which there are no losses and no leakage flux. The following assumptions are made:

- The core of the reactor is highly permeable in a sense that it requires vanishing small magnetomotive force to set up the flux.
- The core does not exhibit any eddy current or hysteresis loss.
- All the flux is confined in the core so there is no leakage flux.
- The resistance of the reactor is negligible.

Suppose that voltage v_1 and v_2, with respect to a common ground, are applied to the input terminals 1 and 2 respectively. The voltage across the two input terminals is denoted as $v_{12} = v_1 - v_2$. For this ideal model it is straightforward to determine the voltage between the output terminal O and terminal 2:

$$v_{O2} = \frac{N_2}{N_1 + N_2} v_{12} = \frac{2}{3}(v_1 - v_2) . \quad (1)$$

The voltage at the output terminal with respect to the common ground is thus

$$v_O = v_{O2} + v_2 = \frac{2}{3} v_1 + \frac{1}{3} v_2 . \quad (2)$$

Each leg of the H-bridge has a voltage-clamping capacitor and the voltages at the two input terminals of the reactor can be 0, $v_{dc}/2$, or v_{dc}, where v_{dc} is the nominal voltage of the capacitor C_{dc}. For each phase there are nine different switching states, corresponding to nine terminal voltage combinations (v_1, v_2). These combinations can produce a line-to-ground voltage v_o at the output terminal that has seven distinct voltage levels, as shown in Table I.

Table I. Voltage relationship for tapped reactors.

State	v_1	v_2	v_O
0	0	0	0
1	0	$v_{dc}/2$	$v_{dc}/6$
2	$v_{dc}/2$	0	$v_{dc}/3$
2'	0	v_{dc}	$v_{dc}/3$
3	$v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$
4	$v_{dc}/2$	v_{dc}	$2v_{dc}/3$
4'	v_{dc}	0	$2v_{dc}/3$
5	v_{dc}	$v_{dc}/2$	$5v_{dc}/6$
6	v_{dc}	v_{dc}	v_{dc}

Note that there are two redundant states 2' and 4' that produce the same voltage as states 2 and 4, respectively. However, these are not desirable because the voltages applied across the reactor are twice as in other states. The output current is shared by the two legs of the H-bridge, with one having one-third of the current and the other having two-thirds. Therefore, the switching devices can be rated at either one-third or two-thirds of the required compensating current level, depending on the reactor terminal these are connected to.

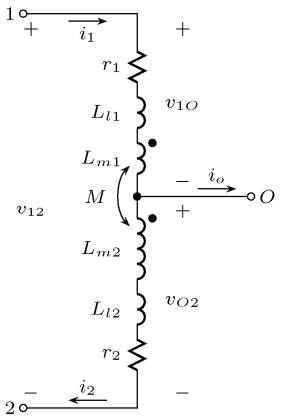

Fig. 3. Detailed model of the tapped reactor.

B. Non-ideal Reactor Model Analysis

The ideal reactor model demonstrates that with three-voltage levels at the input terminals, the output voltage can have seven distinct levels. In practice, winding resistance, leakage inductance, and magnetizing inductance should be taken into account to obtain more accurate voltage and current relationships for the purpose of analysis and simulation.

As shown in Fig. 3, the detailed reactor model consists of two inductors that are coupled via a common core. The following quantities are defined:

N_1, N_2: number of turns of each inductor, $N_1 = N$, $N_2 = 2N$
r_1, r_2: winding resistance
L_{l1}, L_{l2}: leakage inductance
L_{m1}, L_{m2}: self inductances
M: mutual inductance between the two inductors

For simplification, it is reasonable to assume that the winding resistance and leakage inductance of an inductor are proportional to its number of turns. Hence

$$\begin{aligned} r_1 &= r & r_2 &= 2r \\ L_{l1} &= L_l & L_{l2} &= 2L_l \end{aligned} . \tag{3}$$

It can be shown that the relationship between the self inductances and mutual inductance is

$$L_{m1} = \frac{M}{2} \qquad L_{m2} = 2M . \tag{4}$$

Let the current through inductor L_1 be i_1 and the current through L_2 be i_2, then the voltage across L_1 is

$$v_{1O} = L_l \frac{di_1}{dt} + \frac{M}{2}\frac{di_1}{dt} + M\frac{di_2}{dt} + ri_1 , \tag{5}$$

and the voltage across L_2 is

$$v_{O2} = 2L_l \frac{di_2}{dt} + 2M\frac{di_2}{dt} + M\frac{di_1}{dt} + 2ri_2 . \tag{6}$$

By Kirchhoff's voltage and current laws, (5) and (6) can be re-written as

$$\begin{aligned} v_{1O} &= \frac{1}{3}v_{12} + \frac{2}{3}L_l\frac{di_o}{dt} + \frac{2}{3}ri_o \\ v_{O2} &= \frac{2}{3}v_{12} - \frac{2}{3}L_l\frac{di_o}{dt} - \frac{2}{3}ri_o \end{aligned} . \tag{7}$$

If L_l and r are negligible one would obtain the same results as in (1). The derivatives of inductor currents can be determined as

$$\begin{aligned} \frac{di_1}{dt} &= -\frac{2}{3}\frac{-2L_l\frac{di_o}{dt} - 3M\frac{di_o}{dt} - v_{12} + ri_o + 3ri_2}{2L_l + 3M} \\ \frac{di_2}{dt} &= -\frac{1}{3}\frac{2L_l\frac{di_o}{dt} + 3M\frac{di_o}{dt} - 2v_{12} + 2ri_o + 6ri_2}{2L_l + 3M} \end{aligned} . \tag{8}$$

Equations (7) and (8) can be used to build a detailed model of a tapped reactor for simulation. It should be noted that since the output terminal is always connected to another inductor, the three currents i_1, i_2 and i_o are not independent and only two of them can be chosen as system states.

C. Active Filter Interface

As shown in Fig. 4, the active filter is connected to the power system via a three-phase inductor L_f. The filtering function is achieved by injecting a compensating harmonic current into the point of common coupling of the utility-load interface, which in this case is the secondary side of the rectifier load transformer. The reference harmonic currents are extracted from the load currents so that the sum of the load currents and the injection currents has a total harmonic distortion that meets the required specifications. The seven-level inverter can produce an output voltage that contains much less switching frequency ripple than a conventional two-level inverter, thus the generated injection currents are smoother. In addition, the size of the switching frequency passive filter can be significantly reduced.

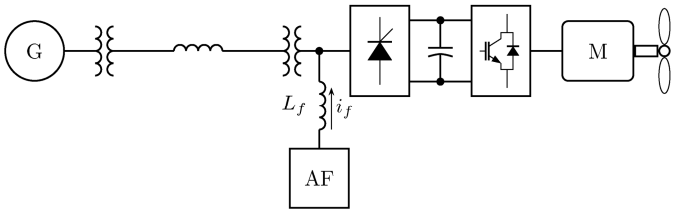

Fig. 4. Active filter connection to a shipboard power system.

IV. Active Filter Control

To effectively compensate the load harmonic currents, the active filter controller should be designed to meet the following three goals:

- Extract and inject load harmonic currents
- Maintain a constant dc capacitor voltage
- Avoid generating or absorbing reactive power with fundamental frequency components

A. Harmonic Current Extraction

For diode or thyristor rectifier loads, the most common harmonic currents are of the 5th, 7th, 11th, and 13th order. Although a high-pass filter can be used to extract these components directly from the line currents, it is not feasible to obtain high attenuation at the fundamental frequency due

to the high current amplitude. The synchronous *q*-*d* reference frame controller developed for shunt active filter systems is used to generate the reference compensating current [12]. As shown in Fig. 5, the load phase currents (i_{aL}, i_{bL}, and i_{cL}) are first transformed into the synchronous reference frame to obtain i_{qL} and i_{dL}. Low-pass filters are then used to extract the dc components, which correspond to the fundamental frequency components in the load currents. High-pass filters are implemented by removing the extracted dc components from i_{qL} and i_{dL}.

B. DC Capacitor Voltage Control

For the active filter to operate effectively it is important to maintain the dc capacitor voltage at a constant value. Since the active filter topology is essentially identical to that of an active rectifier, similar control strategies for the active rectifier are applicable.

The dc capacitor voltage is directly affected by the real power transferred across the active filter. To keep the voltage constant, ideally no real power should be transferred. However, due to losses in switching devices and other components, a small amount of real power is needed. In the synchronous reference frame with the *q*-axis aligned with the voltage at the point of common coupling, the real power transferred can be expressed as

$$P = \frac{3}{2} v_{qs} i_{qf} , \tag{9}$$

which means that by adjusting the *q*-axis filter current the real power can be effectively controlled. The controller diagram is shown in Fig. 5.

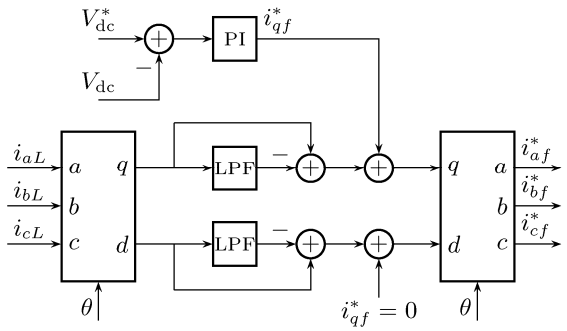

Fig. 5. Active filter control diagram.

C. Reactive Power Control

In most cases the active filter is rated based on the harmonic components. Although the active filter is capable of generating or absorbing reactive power, it is not intended to be used as a reactive power compensator. Therefore, a unity power factor for fundamental frequency components is required at the active filter terminals. Since the reactive power can be expressed as

$$Q = \frac{3}{2} v_{qs} i_{df} , \tag{10}$$

this goal can be achieved by keeping the *d*-axis current at zero, as shown in Fig. 5. The combined control of dc capacitor voltage and reactive power uniquely determines the fundamental frequency component of the active filter output current. This current is then superimposed onto the commanded harmonic currents, and the commanded filter currents i_{af}^*, i_{bf}^* and i_{cf}^* can be obtained.

D. Harmonic Current Regulator

A current regulator is needed to generate the commanded compensation current. Generally, a hysteresis control provides fast response and is suitable for non-sinusoidal current tracking. However, it suffers from some serious disadvantages such as variable switching frequency and phase interaction problems [1]. In addition, to fully take advantage of the benefits of a multilevel converter, a current regulator that uses a voltage-source PWM modulation is desirable.

In this paper, a predictive current regulator is implemented to track the harmonic currents. Given the system voltages and filter inductor currents, the required *a*-phase filter voltage can be calculated based on estimated values of the filter inductance

$$v_{af}^* = \hat{v}_{as} + \frac{(\hat{i}_{af}^* - i_{af})\hat{L}_f}{\Delta t}, \tag{11}$$

where Δt is the switching period, $\hat{v}_{as}$ is the predicted source voltage and can be calculated as

$$\hat{v}_{as} = v_{as}(t) + 1.5\Delta t[v_{as}(t) - v_{as}(t-\Delta t)], \tag{12}$$

and $\hat{i}_{af}^*$ is the predicted reference harmonic current

$$\hat{i}_{af}^* = i_{af}^*(t) + 2\Delta t[i_{af}^*(t) - i_{af}^*(t-\Delta t)]. \tag{13}$$

For accurate current tracking, the prediction takes into account the controller delay due to data acquisition and calculation. The active filter interface inductance L_f can be estimated online.

E. Multilevel Voltage Modulation

Once the commanded voltages v_{af}^*, v_{bf}^* and v_{cf}^* are calculated, the next step is to determine the switching signals that generate these voltages. The active filter can generate seven distinct voltage levels (0 to 6). The immediate levels below and above v_{af}^* can be determined by

$$ll_a = \text{int}(d_{am}) \qquad ul_a = ll_a + 1, \tag{14}$$

where the function int(.) truncates d_a to an integer and

$$d_{am} = \left(\frac{v_{af}^*}{V_{dc}} + 0.5 \right) \times 6 . \tag{15}$$

ll_a should be limited in the range from 0 to 5.

The switching time is then calculated as

$$t_a = (d_{am} - ll_a)\Delta t . \tag{16}$$

To generate v_{af}^* in a switching period Δt, the active filter should generate voltage level ul_a for time duration t_a, and generate level ll_a for duration $\Delta t - t_a$.

To generate a specific output voltage level, Table I is first used to determine the voltage levels that should be applied to the reactor input terminals. Switching signals can then be determined for the two flying-capacitor converter legs to generate the required voltage levels.

V. Magnetizing Current Minimization

A. Reactor Magnetizing Currents

The current through the reactor consists of two components. One is the compensating current that flows out of the center tap and is shared by the two parts of the reactor. The other is the magnetizing current that is generated when a dc voltage is applied across the reactor input terminals. The magnetizing current does not contribute to the filtering function and should be minimized to reduce current ratings of the switching devices and to avoid reactor saturation. Ideally, the magnetizing current has a zero dc component. In practice, however, the dc current tends to drift away from zero if uncontrolled because of the differences in component parameters and controller errors. Therefore, it is necessary to monitor and control the magnetizing currents of the three-phase reactor so that its value is within the required range.

Let the magnetizing current in phase a be i_{am}, then the following relationship holds

$$\begin{aligned} i_{am} + \frac{2}{3} i_{ao} &= i_{a1} \\ i_{am} - \frac{1}{3} i_{ao} &= i_{a2} \end{aligned} \tag{17}$$

Either equation can be used to calculate the magnetizing current.

B. Magnetizing Current Minimization

The magnetizing current can be minimized by balancing the voltage applied across the tapped reactor. Among the seven switching states in Table I, states (0, 0), ($v_{dc}/2$, $v_{dc}/2$), and (v_{dc}, v_{dc}) have no effect on the magnetizing current, while the other four states can either increase or decrease the magnetizing current. Since states 2' and 4' are not used, there is no usable per-phase redundant state. Thus, the magnetizing current of each phase cannot be adjusted independently. In this paper, a technique similar to the joint-phase redundant states selection (JRSS) method proposed in [7] is used to minimize the magnetizing currents.

The concept behind JRSS is that for a three-phase inverter, the line-to-ground voltages of all phases may be changed simultaneously without affecting the load voltages since the terms that are common in all phases will cancel when looking at the line-to-neutral voltages or line-to-line voltages.

The current minimization procedure is as follows. At the beginning of each switching period, the magnetizing current for each phase is calculated. Suppose the commanded voltage levels are s_i, where $i = a, b, c$, and $0 \le s_i \le 6$. The number of available joint redundant states is

$$k = \min(s_i) + 6 - \max(s_i) . \tag{18}$$

Each redundant state specifies the three-phase active filter voltage levels. Based on Table I, the voltage applied across the reactor for each phase, and whether the magnetizing current increases, decreases, or does not change can be determined. If the magnetizing inductance L_m is known, the change in the current (for phase a) can be calculated as

$$\Delta i_{am} = \frac{v_{a1} - v_{a2}}{L_m} \delta t , \tag{19}$$

where δt is the duration of the state. The switching state that results in the minimum three-phase total magnetizing current is selected.

VI. Simulation Results

Numerical simulations have been conducted to validate the proposed topology. The example system has a rated line-to-line voltage of 306 V and a three-phase six-pulse diode rectifier with a 50 Ω dc load. The rated dc capacitor voltage of the active filter is 500 V. The three-phase tapped reactor has a leakage inductance of L_l = 50 μH, winding resistance r = 0.1 Ω, and mutual inductance M = 100 mH. The active filter interface inductance is 1 mH.

Figs. 6 and 7 show the a-phase operation of the active filter with the rectifier load. As can be seen, the load current i_{aL} contains a significant amount of harmonics. The active filter produces multilevel voltages that generate a current i_{af} to cancel the harmonic contents. The compensated source current i_{as} contains much less harmonics than i_{aL}. It can be seen that there are periodical spikes in the compensated current, which is a result of the predictive current regulation. These spikes are high frequency components and can be removed by passive filters.

The effectiveness of the magnetizing current control is illustrated in Fig. 8. The top part of Fig. 8 shows whether the JRSS current balancing algorithm is turned on or off, and the bottom part shows the magnetizing current in phase a. Initially the balancing is on and it can be seen that the magnetizing current is kept within a small range with a very low dc component. At time $t = t_{off}$, the balancing algorithm is turned off, and the magnetizing current drifts away from zero and keeps decreasing. In practice a large magnetizing current can cause the iron core to saturate and eventually damage the reactor and switching devices. When the balancing method is turned on again at $t = t_{on}$, the magnetizing current returns to its minimum value. Similar results are obtained for phase b

and phase *c*.

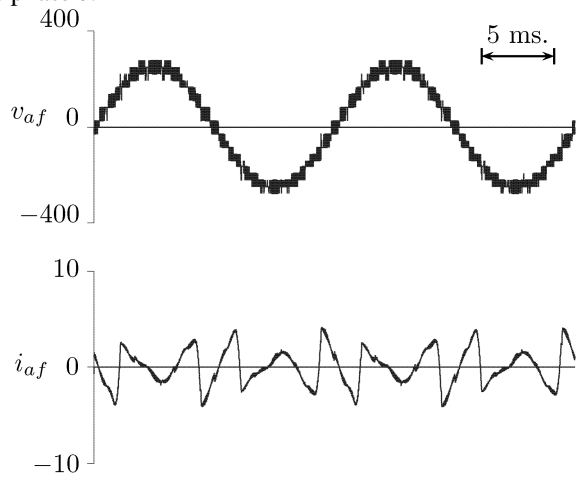

Fig. 6. Active filter output voltage and current.

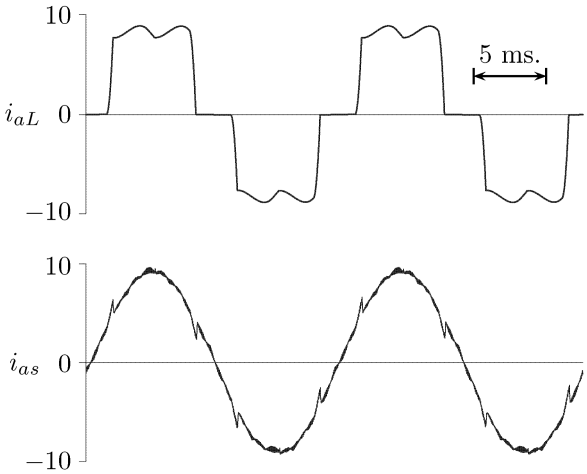

Fig. 7. Load current and compensated current.

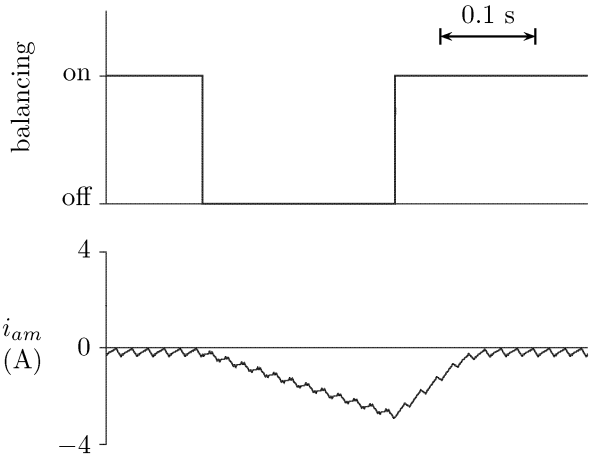

Fig. 8. Magnetizing current with and without balancing algorithm.

VII. Conclusions

In this paper, tapped reactors are used for the parallel operation of active filters. The proposed topology can achieve seven output voltage levels and significantly reduce switching frequency harmonics. A detailed model of the tapped reactor is analyzed to show the relationship between reactor input and output voltages. To minimize reactor magnetizing currents, a joint redundant state selection method is used to balance the voltage across the reactor. Simulation results confirm the effectiveness of the proposed topology and control strategies.

References

[1] B. Singh, K. Al-Haddad, and A. Chandra, "A Review of Active Filters for Power Quality Improvement," *IEEE Transactions on Industrial Electronics*, volume 46, number 5, pages 960-971, October 1999.

[2] M.E. Ortuzar, R.E. Carmi, et al., "Voltage-Source Active Power Filter Based on Multilevel Converter and Ultracapacitor DC Link," *IEEE Transactions on Industrial Electronics*, volume 53, number 2, pages 477-485, April 2006.

[3] Z. Du, L.M. Tolbert, and J.N. Chiasson, "Active Harmonic Elimination for Multilevel Converters," *IEEE Transactions on Power Electronics*, volume 21, number 2, pages 459-469, March 2006.

[4] M.E. Ortuzar, R.E. Carmi, et. al., "Voltage-source active power filter based on multilevel converter and ultracapacitor DC link", *IEEE Transactions on Industrial Electronics*, volume 53, number 2, pages 477-485, April 2006.

[5] B.R. Lin and T.Y. Yang, "Analysis and implementation of a three-level active filter with a reduced number of power semiconductors", *IEE Proceedings on Electric Power Applications*, volume 152, number 5, pages 1055-1064, September 2005.

[6] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage", *IEEE PESC 04*, volume 4, pages 2572-2576, 2004.

[7] J. Huang and K.A. Corzine, "Extended Operation of Flying Capacitor Multilevel Inverters," *IEEE Transactions on Power Electronics*, volume 21, pages 140-147, January 2006.

[8] F. Ueda, K. Matsui, et. al., "Parallel-connections of pulsewidth modulated inverters using current sharing reactors", *IEEE Transactions on Power Electronics*, volume 10, number 6, pages 673-679, November 1995.

[9] H. Mori, K. Matsui, et. al., "Parallel-connected five-level PWM inverters", *IEEE Transactions on Power Electronics*, volume 18, number 1, part 1, pages 173-79, January 2003.

[10] K. Matsui, Y. Kawata and F. Ueda, "Application of parallel connected NPC-PWM inverters with multilevel modulation for AC motor drive", *IEEE Transactions on Power Electronics*, volume 15, number 5, pages 901-907, September 2000.

[11] S. Ogasawara. J. Takagaki, et al., "Novel Control Scheme of a Parallel Current-Controlled PWM Inverter," *IEEE Transactions on Industry Applications*, volume 28, number 5, pages 1023-1030, September 1992.

[12] S. Bhattacharya, T.M. Frank, et. al., "Active Filter System Implementation," *IEEE Industry Applications Magazine*, volume 4, number 5, pages 47-63, September 1998.