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A Four-Level Crossing dc/dc Converter Based Drive System

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Abstract **- This paper introduces a novel crossing front-end dc/dc converter for a four-level drive system which provides a voltage boost as well as dc capacitor bank voltage regulation. The primary advantage of the proposed converter is that it simplifies the control of the four-level diode-clamped inverter since capacitor voltage balancing is not required by the inverter control. Furthermore, the inverter modulation index can be varied up to its physical limitation. An average-value model of the converter is derived and used for insight and analysis of the converter operation. Detailed simulations of the four-level drive system demonstrate the effectiveness of the proposed system.**

Key words: dc/dc converter, multilevel inverter, multilevel converter, drives, capacitor balancing, average-value model.

I. INTRODUCTION

Multilevel drive systems have gained popularity in recent years since they offer advantages of higher voltage operation, higher power quality, lower switching losses, and better electromagnetic compatibility [1-17]. The general structures of multi-level drive systems are typically based on one of the three fundamental topologies; diode-clamped, flying capacitor, and series H-bridge. Although the diode-clamped multilevel inverter (DCMI) is arguably the most popular topology, it's use is limited beyond three levels due to voltage balancing problems on the series bank of input capacitors [3,4,10-17]. Researchers have sought several solutions to this problem including isolated voltage sources, multi-level active front ends [3], and dc/dc converters [10-17]. The unique aspect of the crossing dc/dc converter solution proposed in this paper is that the voltage level can be boosted at the same time. A voltage boost may be necessary for a drive system, which interfaces with a low-voltage source such as a fuel-cell, battery, or superconducting magnetic energy storage (SMES). This front-end configuration also provides good regulation of the capacitor bank, which allows a straightforward inverter control based on multi-level sine-triangle modulation without regard to redundant state selection typically added for capacitor voltage balancing purposes [3,4]. To maintain balanced capacitor voltages, the maximum modulation index of the four-level DCMI is limited to around 0.6 for a typical motor load with a 0.8 power factor [3,4]. By utilizing the proposed boost converter, the modulation index can be set to the maximum physical limitation of 1.15 for duty-cycles with third harmonic injection. Detailed simulations demonstrate the effectiveness of the proposed drive system.

II. FOUR-LEVEL CONVERTER ANALYSIS

Figure 1 shows the structure of a drive system involving a front-end dc/dc boost stage feeding the dc capacitor bank of a four-level DCMI. The details of the four-level inverter are shown in Fig. 2. The operation of the four-level inverter has been well established in the literature [3,4]. In summary, by switching the three phases to the four capacitor junctions $d_0 \sim d_3$, the four-level DCMI provides four unique line-to-ground voltage levels resulting in high power quality. However, the inverter current will discharge the center capacitor if no external balancing provisions are included. From Fig. 1, it can be seen that the dc/dc converter section solves this problem by connecting the external source directly to the center capacitor. The remaining circuitry forms two boost converters. For example, the switch T_3 and adjacent inductor and diode form a boost converter from the input voltage to the sum of the center and upper capacitor voltages. Since the center capacitor is fixed, this converter can regulate the uppermost capacitor. Likewise, the switch T_1 and the adjacent inductor and diode regulate the lowermost capacitor voltage. Ideally speaking, by setting the duty cycle of the upper boost converters to 0.5, the voltage between d_3 and d_1 can be regulated to $2v_{dc}$. Similarly, the voltage between d_2 and d_0 will be regulated to $2v_{dc}$. Considering that the middle capacitor is directly connected to v_{dc}, the total voltage between d_3 and d_0 can be boosted to $3v_{dc}$ and all of the three capacitor voltages are maintained at v_{dc}. A buck converter may be added in front of the proposed boost converter for systems that require control of the dc voltage to a specific value or for maintaining consistent drive

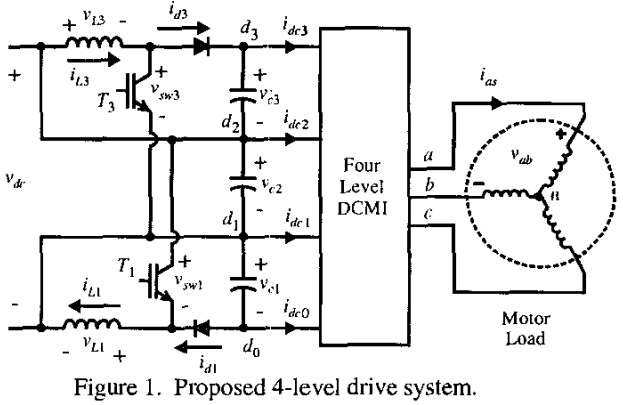

Figure 1. Proposed 4-level drive system.

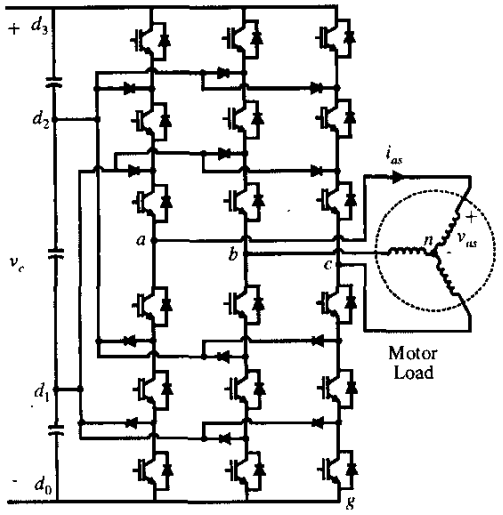

Figure 2. Four-level inverter topology.

voltage while providing ride-through capability [8]. Also, as with other multilevel dc/dc converters, a bidirectional configuration is possible if freewheeling diodes are placed across the transistors and additional transistors are connected in anti-parallel with the converter diodes.

The two switches of the crossing front-end boost converter form four switching states, which are shown in Fig. 3. Therein, the center capacitor is not shown since the input source directly determines its voltage. The first state "00" is the off state for both converters where the inductor is supplying the capacitor and inverter. The next state "01" shows the on-state for the upper converter for building up energy in the inductor. The remaining

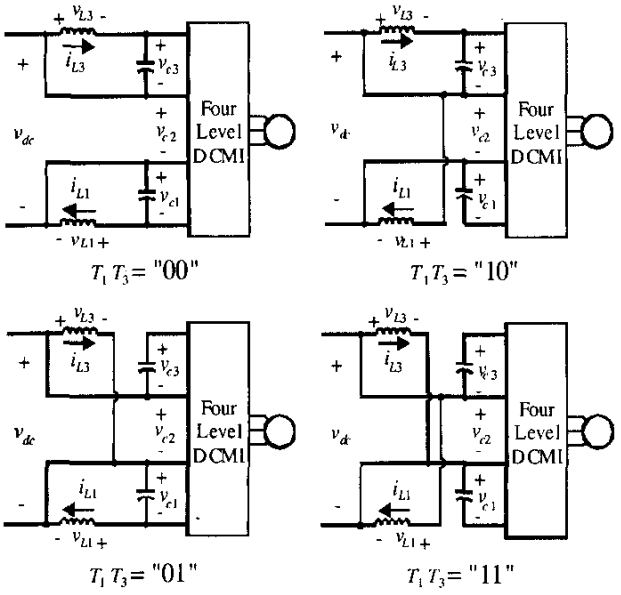

Figure 3 Four-level crossing converter switching states.

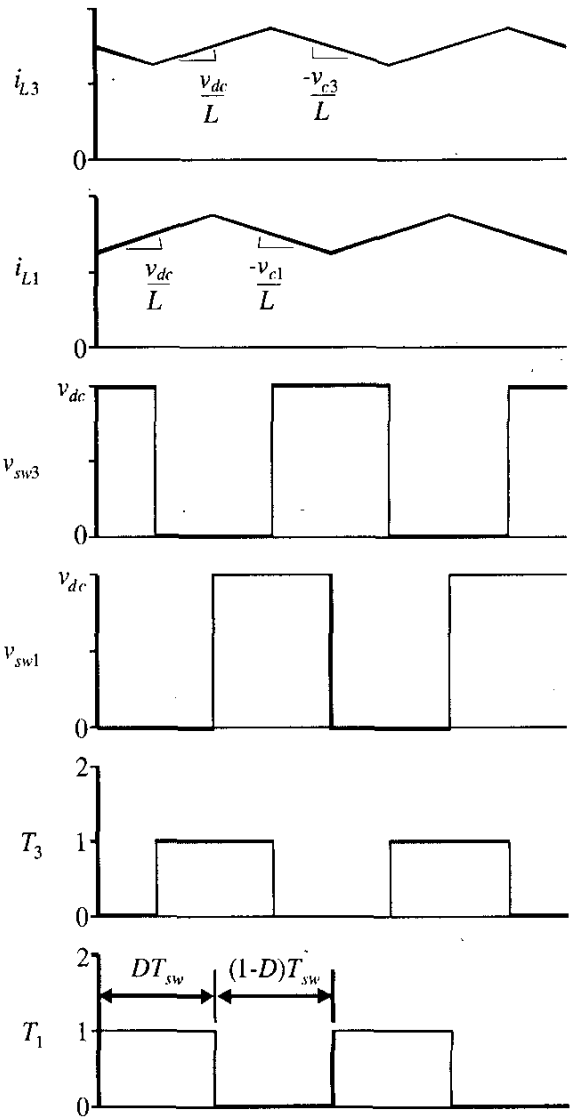

Figure 4. Idealized boost converter waveforms.

states "10" and "11" depict the on-state of the lower converter and the on-state of both converters respectively. One may operate the upper and lower dc/dc converter separately, or follow an interleaving sequence such as "00", "10", "11", then "01"; the latter of which results in smoother dc source current. Figure 4 shows idealized converter waveforms for the interleaved sequence. As can be seen, the lower converter is switched with period T_{sw} and duty cycle D. The upper converter transistor signal is delayed from the lower by a quarter period to form interleaved voltages v_{sw1} and v_{sw3}. The resulting voltages determine the slopes of the inductor currents as shown in Fig 4.

III. AVERAGE VALUE MODEL

To depict the effective operation of the proposed crossing dc/dc boost converter, it is instructive to study its dynamic average-value model. This model predicts the drive's salient performance while neglecting the converter switching and is therefore faster than a detailed model when performing computer simulation [16-19]. This can be useful for drive design where a large number of simulation studies need to be performed. The symbol ^ is used to mean fast average-value or the average of the variable over one switching period of the converter. The average-value model can also be used to gain insight into the operation of the converter and for steady-state calculations.

Referring to Figs. 1 and 4, the upper converter transistor voltage and diode current over one switching period T_{sw} are

$$v_{sw3} = \begin{cases} V_Q & 0 \le t < DT_{sw} \\ v_{dc} + v_{c3} + V_D & DT_{sw} \le t < T_{sw} \end{cases} \quad (1)$$

$$i_{d3} = \begin{cases} 0 & 0 \le t < DT_{sw} \\ i_{L3} & DT_{sw} \le t < T_{sw} \end{cases} \quad (2)$$

where D is the converter duty cycle and V_Q and V_D are the transistor and diode on-state voltage drops respectively. In this analysis, it is assumed that the same duty cycle is used for both converters. Taking the average value of v_{sw3} and i_{d3} over one switching period T_{sw} yields

$$\hat{v}_{sw3} = DV_Q + (1-D)(v_{dc} + \hat{v}_{c3} + V_D) \quad (3)$$

$$\hat{i}_{d3} = (1-D)\hat{i}_{L3}. \quad (4)$$

Using Kirchhoff's voltage law and including the inductor resistance r_L, the average inductor voltage for the upper converter current can be calculated as,

$$\hat{v}_{L3} = -\hat{v}_{sw3} - r_L\hat{i}_{L3} + \hat{v}_{dc} \quad (5)$$

Substituting (3) into (5) yields,

$$\hat{v}_{L3} = D\hat{v}_{dc} - DV_Q - (1-D)V_D - r_L\hat{i}_{L3} - (1-D)\hat{v}_{c3} \quad (6)$$

Equation (4) and the last term in (6) suggest that an ideal transformer model can be used to model the converter coupling [18]. The input side of the converter may be referred through the transformer by first defining

$$\hat{v}_{L3}' = \frac{\hat{v}_{L3}}{(1-D)} \quad (7)$$

$$\hat{i}_{L3}' = (1-D)\hat{i}_{L3} \quad (8)$$

$$r_L' = \frac{r_L}{(1-D)^2} \quad (9)$$

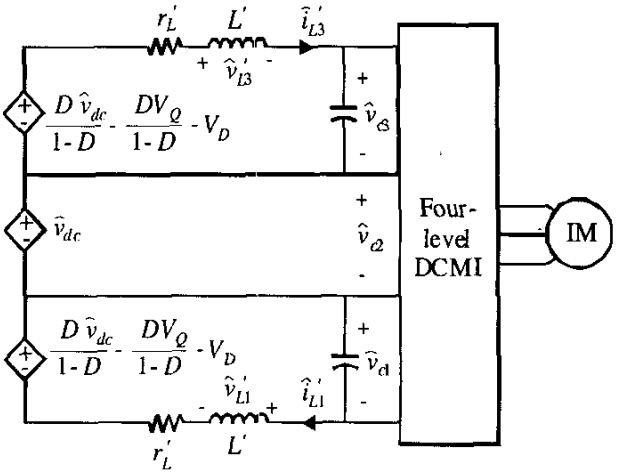

Figure 5. Converter average-value model.

$$L' = \frac{L}{(1-D)^2} \quad (10)$$

where L is the converter inductance. Using these definitions, (6) may be rewritten as

$$\hat{v}_{L3}' = L'\frac{d\hat{i}_{L3}'}{dt} = \frac{D\hat{v}_{dc}}{1-D} - \frac{DV_Q}{1-D} - V_D - r_L'\hat{i}_{L3}' - \hat{v}_{c3}. \quad (11)$$

Since these referred terms match the secondary side of the converter, the equivalent average-value circuit model shown in Fig. 5 can be generated. As can be seen, the effect of the dc/dc converters is to provide three sources to the four-level inverter drive. In addition, some dynamics are included from the referred converter inductance.

Considering that the average inductor voltage is zero in the steady-state and the average capacitor voltage should ideally equal to the source voltage v_{dc}, one can solve the duty cycle D from equation (11) as,

$$D = \frac{r_L\hat{i}_{L3} + \hat{v}_{dc} + V_D}{2\hat{v}_{dc} + V_D - V_Q}. \quad (12)$$

If the inductor resistance and the semiconductor voltage drops are neglected in (12), the duty cycle can be calculated as

$$D = \frac{\hat{v}_{dc}}{2\hat{v}_{dc}} = 0.5 \qquad r_L = 0,\ V_Q = V_D = 0. \quad (13)$$

If only inductor resistance is neglected,

$$D = \frac{\hat{v}_{dc} + V_D}{2\hat{v}_{dc} + V_D - V_Q} \qquad r_L = 0 \quad (14)$$

The same expressions can be derived by considering the switching of the lower converter. Certainly (13) represents the

ideal duty cycle and (14) gives an approximation. Equation (12) is exact, but could be more complete since the inductor current is a function of the drive and motor load. To complete the expression, first, substitute (4) into (12) to get

$$D = \frac{r_L \dfrac{\hat{i}_{d3}}{(1-D)} + \hat{v}_{dc} + V_D}{2\hat{v}_{dc} + V_D - V_Q} \tag{15}$$

Solving for the duty cycle yields

$$D = \frac{3\hat{v}_{dc} + 2V_D - V_Q}{2(2\hat{v}_{dc} + V_D - V_Q)} - \frac{\sqrt{(3\hat{v}_{dc} + 2V_D - V_Q)^2 - 4(2\hat{v}_{dc} + V_D - V_Q)(r_L\hat{i}_{d3} + \hat{v}_{dc} + V_D)}}{2(2\hat{v}_{dc} + V_D - V_Q)} \tag{16}$$

To maintain balanced capacitor voltages the capacitor junction current must be zero. Which implies $\hat{i}_{d3} = \hat{i}_{dc3}$. Therefore, the computation of an accurate dc converter duty cycle eventually depends on the average dc current flowing into the inverter. This current can be calculated by using a four-level inverter average value model. The structure of the average-value model of the four-level DCMI is shown in Fig. 6. For the analysis herein, the average capacitor junction current $\hat{i}_{dc3}$ will be of interest. Due to drive symmetry, only the a-phase contribution to this junction current need be considered. In the inverter control algorithm, the a-phase modified duty cycle of the four-level DCMI can be represented as a function of the modulation index and the inverter electrical angle

$$d_{am} = \frac{3}{2}\left(1 + m\cos(\theta) - \frac{m}{6}\cos(3\theta)\right). \tag{17}$$

The duty cycle defined above ranges from 0~3 and can be classified into three regions, which range from 0~1, 1~2, and 2~3. The duty cycle is then modulated with three sine-waves [3] in order to obtain switching states for the a-phase which range from 0~3. To compute the average current, it is helpful to define the switching function which represents the conditions under which the a-phase is connected to d_3. As a function of the duty cycle, this is

$$S_3 = \begin{cases} 0 & d_{am} < 2 \\ d_{am} - 2 & \text{otherwise} \end{cases}. \tag{18}$$

The dc average current that the inverter draws from junction d_3 can then be calculated by evaluating

$$\bar{i}_{dc3} = \frac{3}{2\pi}\int_0^{2\pi} S_3\, i_{as}\, d\theta \tag{19}$$

where the overscore symbol represents the average over one fundamental cycle of d_{am}. This average can by used in place of

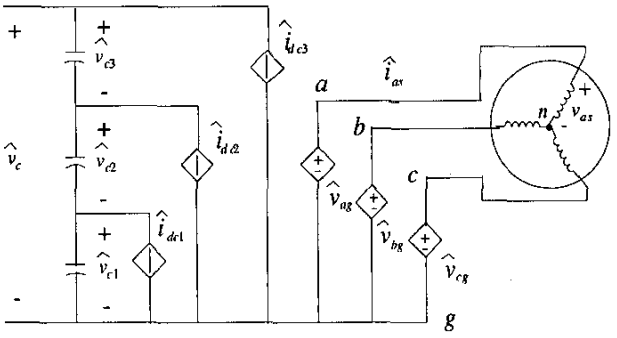

Figure 6. Four-level inverter average-value model.

the fast-average for steady-state calculations. The phase current can be expressed

$$i_{as} = \sqrt{2}\, i_s \cos(\theta + \phi_i) \tag{20}$$

In (20), the current magnitude i_s and angle ϕ_i can be related to the motor steady-sate impedance by

$$i_s = \frac{v_s}{|Z|} \tag{22}$$

$$\phi_i = -\angle Z\,. \tag{23}$$

The voltage magnitude in (22) is determined by the inverter dc voltage and modulation index as

$$v_s = \frac{m \cdot v_c}{2\sqrt{2}}\,. \tag{24}$$

Assuming balanced capacitor voltages,

$$v_c = 3v_{dc}\,. \tag{25}$$

The procedure for determining the correct steady-state

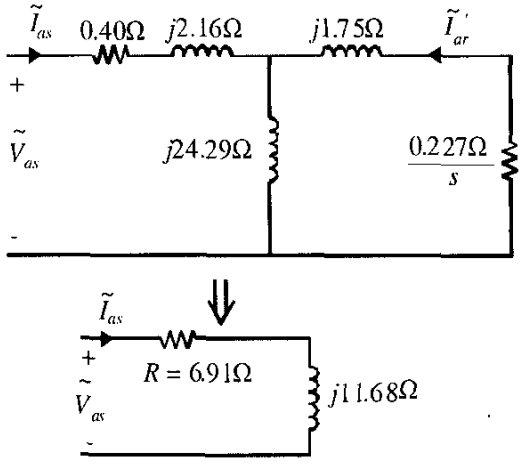

Figure 7. Motor steady-state equivalent circuit.

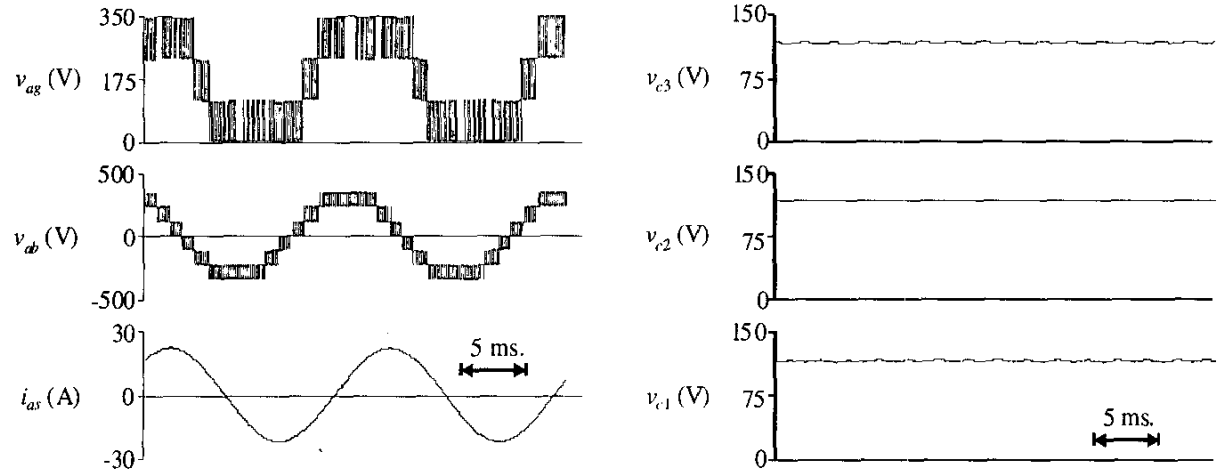

Figure 8. Simulated performance of the four-level drive system.

converter duty cycle is as follows. The magnitude and phase of the load current are computed from the motor load impedance, the dc input voltage, and the modulation index using (22-25). Using these values, an expression for the a-phase current is formed from (20) which is then used along with (17-18) to solve the integral (19). The dc current calculated from this integral can be used in (16) to solve for the duty cycle.

As a numerical example, consider a 4-pole 3.7kW standard NEMA type B induction motor with a steady-state model [19] and parameters shown in Fig. 7 for operation at 60Hz and 183.3 rad/s. The equivalent load impedance can be represented as an R-L load with the parameters shown in Fig. 7. In this example, the power factor is 0.763 lagging. Let the inverter modulation index be m = 1.13 and v_{dc} = 110V. The diode and transistor voltage drops are V_D = 1.2V, V_Q = 2.5V and the inductor resistance is $r_L = 0.2\Omega$. The average dc current $\bar{i}_{dc3}$ can then be computed as 12.54A. Substituting this value into (16) results in D = 0.533. This duty-cycle is calculated based on the upper dc/dc converter, which is also used for the lower dc/dc converter due to the symmetrical structure.

IV. Simulation Results

A detailed simulation of the drive system was created to demonstrate the converter performance. For this study, the dc/dc converter inductance was L = 2mH and converter was switched with a period of T_{sw} = 100μs., The input dc voltage was v_{dc}=110V and the capacitance was set to $C_1 = C_3 = 6{,}600$ μF. The induction motor was the 3.7kW example machine from the previous section. The duty cycle was set to 0.533 as per the previous calculations. Figure 8 shows the inverter waveforms in steady-state with the machine operating at 183.3 rad/s. As can be seen, the inverter exhibits typical four-level drive performance showing four steps in the line-to-ground voltage v_{ag}. As a result, the line-to-line voltage v_{ab}, and phase current i_{as} have low harmonic content. As with other four-level inverters, an average current is drawn from the center capacitor which would tend to discharge the voltage. However, the dc input voltage holds v_{c2} at 110V. The outer capacitor voltages v_{c1} and v_{c3} are regulated by the crossing dc/dc boost converter. Figure 9 shows the dc/dc converter waveforms. In this study, the transistor signals T_1 and T_3 were interleaved in order to reduce the instantaneous current draw from the source. The inductor current waveforms exhibit a triangular shape as expected.

Following the steady-state simulation, a vector control and PI speed loop were added for a dynamic study. Figure 10 shows the

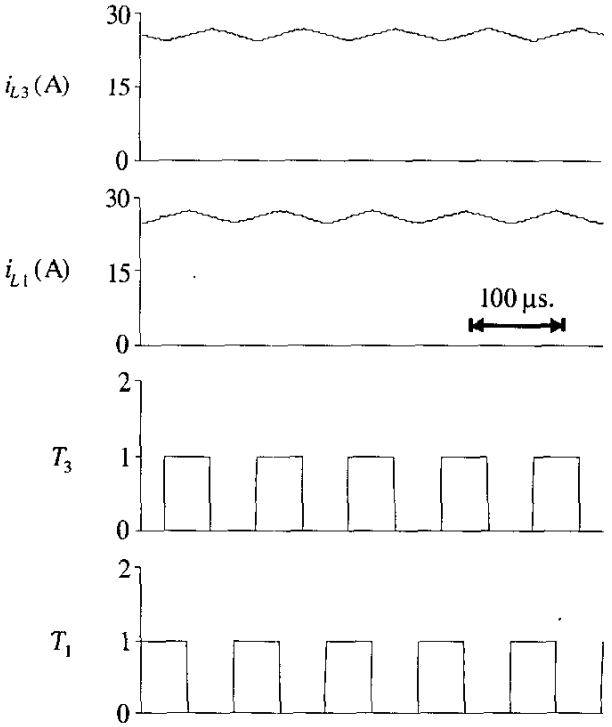

Figure 9. Drive system converter simulation waveforms.

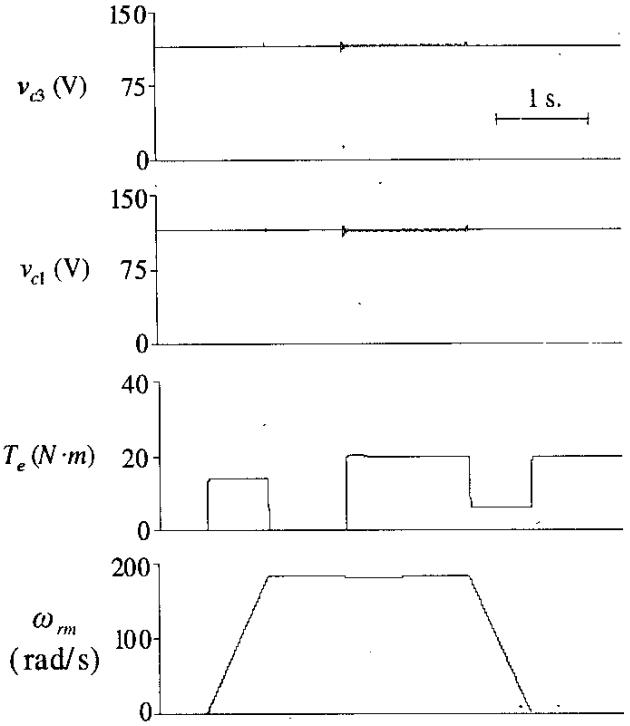

Figure 10. Drive system transient performance.

simulation results where the speed is commanded to ramp from zero to 183.3 rad/s. The load torque is then stepped to its rated value of 20N·m and the motor speed is commanded to zero with the rated load applied. As can be seen, the dc/dc converter provides regulation during the entire transient study.

V. CONCLUSION

Drive systems based on the diode-clamped inverter topology have always had limited application due to the difficulty of regulating the capacitor voltages. The specific problem is that the center capacitors tend to discharge due to the manner in which the load is connected to the capacitor bank. In this paper, a four-level dc/dc converter is introduced which provides a voltage boost and regulates the capacitor voltages making the four-level topology practical for drive applications that interface to low voltage sources (such as batteries of fuel cells). An average-value model for the proposed converter was developed which gave insight into the converter effective operation and allowed the development of duty cycle equations which compensate for the semiconductor voltage drops and inductor resistance. Steady-state and dynamic simulations were carried out on an example four-level drive system in order to verify the converter operation.

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