

01 Jan 1993

Modeling of Intra-Cell Defects in CMOS SRAM

Waleed K. Al-Assadi

Missouri University of Science and Technology, waleed@mst.edu

Y. K. Malaiya

A. P. Jayasumana

Follow this and additional works at: https://scholarsmine.mst.edu/ele_comeng_facwork



Part of the [Electrical and Computer Engineering Commons](#)

Recommended Citation

W. K. Al-Assadi et al., "Modeling of Intra-Cell Defects in CMOS SRAM," *Records of the 1993 IEEE International Workshop on Memory Testing, 1993*, Institute of Electrical and Electronics Engineers (IEEE), Jan 1993.

The definitive version is available at <https://doi.org/10.1109/MT.1993.263145>

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

Modeling of Intra-Cell Defects in CMOS SRAM

W. K. Al-Assadi, Y. K. Malaiya[†], and A. P. Jayasumana
Electrical Engineering Department
[†] Computer Science Department
Colorado State University
Fort Collins, CO 80523

Abstract

The effect of defects within a single cell of a static random access memory (SRAM) is examined. All major types of faults, including bridging, transistor stuck-open and stuck-on, are examined. A significant fraction of all faults cause high IDDQ values to be observed. Faults leading to inter-cell coupling are identified.

1. Introduction

With the increase of cell density, not only does the probability of memory failures increase, but the nature of the failure modes becomes more complex and subtle [1, 2]. Many RAM test algorithms based on different fault models have been proposed. Activeness of test algorithms depends on the accuracy of the fault model, which is used to represent the physical failures [2, 3]. A widely used fault model for RAM devices was proposed by Nair et. al [4]. In this model, defects in the address decoder and the Read/Write logic are mapped onto functionally equivalent faults in the memory array. The advantage of this model is that

all the faults can be considered to be stuck-at-0/1 in the memory array, with the addition of state transition faults and data retention faults. Test algorithms for SRAMs, based on physical spot defects, which are modeled as local disturbances in the layout of an SRAM cell and translated to defects in the corresponding transistor diagram, have been proposed.

In this paper, we examine fault models for the SRAM cell at the transistor level. We consider both functional and IDDQ monitoring. All major transistor faults are considered assuming hard shorts for the bridging faults.

2. Faults in Register Storage Elements

Recent studies have shown that the traditional stuck-at fault model is insufficient for modeling faults in storage elements. Reference [2] shows that a significant fraction of faults cannot be modeled as input/output stuck-at-0/1 for elementary register storage elements. Consider for example, the transmission-gate latch in Figure 1. Some faults cause the cell to ex-

hibit *data-feed-through* behavior, i.e. the input data D or \bar{D} is propagated to the output. Other faults cause the cell to exhibit *clock-feed-through*, i.e. CLK or \bar{CLK} is propagated to the output. These effects are discussed in [5] shows in detail. Besides the *feed-through* behaviors, some faults cause logic non-retention problems, always (NR) or conditionally (CNR). This means that cell works properly in the transparent phase, but not in the latching phase. Indeterminate faults are regarded to be parametric because they can be detected only by monitoring the quiescent supply current (IDDQ). Table 2 summarizes the faulty behavior of the cell in Figure 1.

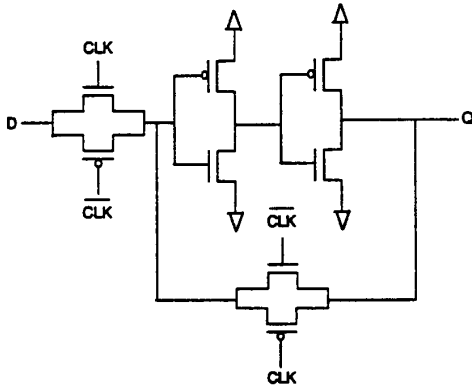


Figure 1: The Transmission-gate latch

Behavior	% of testable faults
stuck-at	45%
Feed-through	18%
NR/CNR	9%
Complex behavior	2%
Fault-free with delay	10%
Parametric	16%

Table 1: Behavior of the transmission-gate latch

3. Detailed Examination of the SRAM Cell

The static cells used in memory chips also use feedback to retain the latched signal. However a new logical value is forced in using a higher strength signal on the bit or \bar{bit} , rather than gating it in using a clock signal.

The common CMOS SRAM cell is shown in Figure 2. Two pMOS transistors are used as pull-up loads for the bit and \bar{bit} lines. The pull-down transistors of the cross-coupled inverters are chosen to be two or three times wider than the pass transistor in order to avoid charge sharing during *read* operation. The two pull-up transistors of the inverters have minimum size to retain charge lost due to leakage current [6]. Although this cell is a storage element, the observations given in [3] for the fault analysis of the elementary storage elements cannot be applied for SRAM cells. This is because the SRAM is a symmetric structure with complimentary bidirectional inputs/outputs and the cell is only indirectly observable via the read circuitry. Here we consider all possible transistors stuck-on, stuck-open and bridging faults. Behavior of the cell under stuck-on/open faults is given in table 2. The results presented depend on the transistor sizing and the read circuitry. 'I' corresponds to IDDQ testable and 'i' corresponds to indeterminate behavior, which depends on the signal strength. Possible inter-cell coupling is indicated using the cx notation. For example 'cb' corresponds coupling involving the bit line. In the table, 'b', ' \bar{b} ', and 'w'

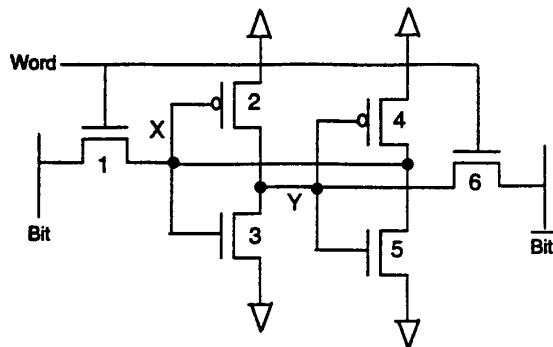


Figure 2: The SRAM cell

Consider stuck-open fault in transistor 1. This fault isolates node X from the bit line. The *write* operation is not affected because of the signal received from \overline{bit} . During the *read* operation, the bit line is pulled-up, while the \overline{bit} functions properly. This suggests that observing this fault depends on the read circuitry of the sense amplifier. If the design is such that the circuit responds to the variations in bit line faster than that of the \overline{bit} , then this fault appears as stuck-at-1. The sense amplifier may cause high IDDQ when both bit and \overline{bit} signal are 1. Similarly stuck-open fault in transistor 6 can be modeled as stuck-at-0. Stuck-on fault in transistor 1 connects the bit line with node X. The behavior of the fault is dependent on the logic value of node X and the relative strengths of the signals and is thus termed indeterminate. This fault can cause coupling between this cell and other cells through the bit line (cb). The same

is true for the stuck-on fault in transistor 6. Stuck-open faults in transistors 2 and 4 cannot affect the functional behavior of the cell. Stuck-on faults in transistors 3 and 5, not only change the functional behavior, but cause increase in IDDQ due to the path between V_{dd} and V_{ss} when the fault is activated.

Transistor	Stuck-on	Stuck-open
1	i, cb	SA1
2	fault-free, I	read circuitry dependent
3	SA1, I	SA0
4	fault-free, I	fault-free
5	SA0, I	read circuitry dependent
6	i,cb	SA0

Table 2: Behavior of the SRAM cell under Stuck-on/open faults

The behavior of the cell under all possible shorts is also examined. Results in Table 2 show that most faults change the functional behavior with increase in IDDQ during the *write* cycle. Some shorts causing the cell to be stuck-at may be dependent on the transistor dimensions. Shorts involving power nodes V_{dd} and V_{ss} With each X and Y nodes can enhance the IDDQ drawn by the cell.

4. Conclusions

In this paper, we present a detailed examination of the SRAM cell. The results show that a large fraction of faults cause increase in IDDQ, which suggests that current testing can be very effective for SRAMs [7]. Some faults may not be detected without using IDDQ monitoring. The cost of testing can be reduced by designing the memory ar-

ray for high current testability. The results presented here can be extracted by considering defects that affect multiple cells. Using inductive fault analysis, or using industrial data from actual faulty chips, probabilities can be assigned to different failure modes. This can be used for optimization of test strategies.

1st. node	2nd. node	Effect
V_{ss}	word	i, I, cw
	bit	SA0, I, cb
	\overline{bit}	SA1, I, $c\overline{b}$
V_{dd}	word	i, I
	bit	SA1, I, cb
	\overline{bit}	SA0, I, $c\overline{b}$
word	bit	SA1, I, cbw
	\overline{bit}	SA0, I, $c\overline{b}w$
	bit	i, I, $cb\overline{b}$
bit	V_{dd}	SA1, I
	V_{ss}	SA0, I
	Y	i, I
X	word	SA1, I, cw
	bit	i, cb
	V_{dd}	SA0, I
Y	V_{ss}	SA1, I
	word	SA1, I, cw
	\overline{bit}	i, $cb\overline{b}$

Table 3: Behavior of the SRAM cell under bridging faults

Acknowledgment

This work was supported by SDIO/IST funded project monitored by ONR.

References

[1] C. A. Papachristou and N. B. Sahgal, "An Improved Method for Detecting Functional Faults in Semiconductor Random Access Memories," *IEEE Trans. on Computers*, vol. c-34, no.

2, pp. 110-116, February 1985. 98-112, October 1992.

- [2] W. K. Al-Assadi, Y. K. Malaiya, and A. P. Jayasumana, "Use of Storage Elements as primitives for Modeling faults in Sequential Circuits," *Proceedings of the 1993 VLSI Design Conference*, pp. 118-123, January 1993.
- [3] R. Dekker, F. Beenker, and L. Thijssen, "A Realistic Fault Model and Test Algorithms for Static Random Access Memories," *IEEE Transaction n Computer-Aided Design*, vol. 9, no.6, June 1990.
- [4] R. Nair, S. M. Thatte, and J. A. Abraham, "Efficient Algorithms for Testing Semiconductor Random Access Memories," *IEEE Trans. on Computers* vo. C-27, no. 6, pp. 572-576, June 1978.
- [5] W. K. Al-Assadi, Y. K. Malaiya, and A. P. Jayasumana, "Detection of Feed-Through Faults in CMOS Storage Elements," *Proc. NASA Symposium on VLSI Design*, pp. 7.2.1-7.2.5, October 1992.
- [6] K. Anami, M. Yoshimoto, H. Shinohara, Y. Hirata, and T. Nakano, "Design Consideration of a Static Memory Cell," *IEEE Journal of Solid-State Circuits*, vol. sc-18, no.4, pp. 414-414, August 1983.
- [7] P. Meershoek, B. Verhest, R. McInerney, and L. Thijseen, "Functional and IDDQ Testing on a Static RAM," *Proceedings of the IEEE International Test Conference 1990*, pp. 929-937.