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Xiaoning Ye

Geping Liu

James L. Drewniak

Missouri University of Science and Technology, drewniak@mst.edu

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Investigation of PCB layout parasitics in EMI filtering of I/O lines

Xiaoning Ye, Geping Liu, James L. Drewniak

Electromagnetic Compatibility Laboratory
Department of Electrical and Computer Engineering
University of Missouri - Rolla
Rolla, MO 65409

Abstract

EMI filters are often utilized on I/O lines to reduce high-frequency noise from being conducted or coupled off the PCB and resulting in an EMI problem. However, layout parasitics are usually inevitable in practical circuit design, and the filtering performance may vary. In this study, the impact of the board layout on the filtering performance is investigated by $|S_{21}|$ measurements of sample PCB boards with different filter layouts. The finite-difference time-domain method is applied to model the boards, support the experimental work, and can be used to provide a means for conducting "what-if" engineering studies.

I. Introduction

Electronic devices continue to operate at increasing speeds and consume more power, which significantly increases EMI concerns and makes it more challenging to meet radiated emissions requirements. One important radiation mechanism is high-frequency noise on the I/O lines that may be conducted or coupled to the attached cables and result in EMI problems [1]. Many lines that come off a high-speed digital design to peripherals are nominally low speed. However, as the clock speeds and edge rates of device technologies continue to increase, increasingly higher-frequency noise is unintentionally coupled to the low-speed I/O lines [2]. EMI filters are often inserted on the I/O lines to suppress the high-frequency noise.

The relevant design features that affect the EMI performance of I/O line filtering found on a typical electronic product are illustrated in Fig. 1. Shunt capacitors are often used to "divert" the high-frequency noise back to its source. However, due to the inherent equivalent series inductance (ESL) and equivalent series resistance (ESR) of the surface mount technology (SMT) capacitor, the EMI filtering performance is compromised at frequencies higher than the series resonance of the capacitance and the ESL. Further, when the EMI filter is mounted on the PCB in practical design, layout parasitics, such as connecting traces and vias, introduce additional inductance in the shunt filtering branch. The filtering performance is further

compromised, and far from ideal. The open literature on the design and application of EMI filters is extensive [3], [4], [5], [6]. Other EMI coupling paths that result in high-frequency common-mode current on low-speed cables can be characterized by a noise voltage between a shielding enclosure and the I/O line as shown Fig. 1. The connection between the PCB reference plane and the conducting shielding enclosure or chassis at the connector can also profoundly impact the EMI performance of any filtering at the connector. The PCB/chassis connection has some non-zero impedance that is schematically represented with an inductor symbol in Fig. 1.

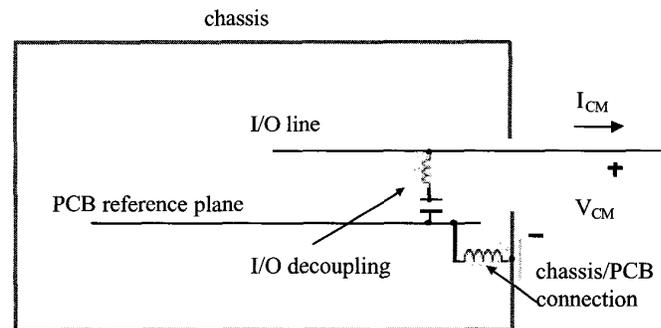


Fig. 1. Schematic representation showing the I/O filtering and chassis/PCB connection parasitics.

In this study, the impact of the board layout on the filtering performance is investigated by $|S_{21}|$ measurements of sample PCB boards with different filter layouts. T-type I/O line filters built with lumped-element resistors and lumped ferrites are used as the test bed. The finite-difference time-domain method is applied to model the boards, and support the experimental work. The algorithm includes passive networks that are characterized as two-ports into the FDTD method. The network can include the nonlinear behavior of ferrite components.

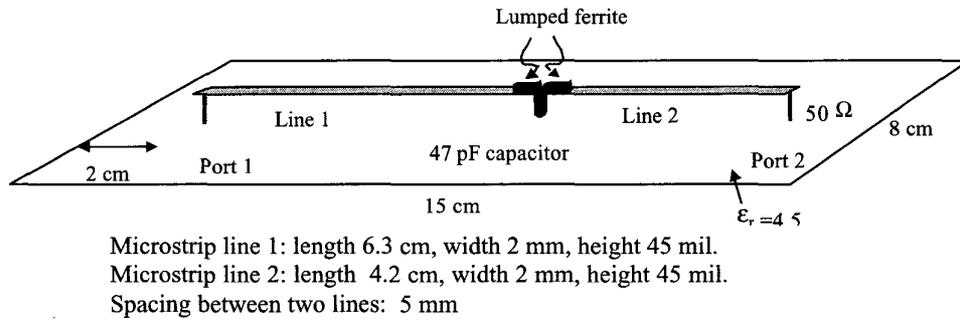


Fig. 2. Schematic of Board A.

II. Layout Parasitics in EMI Filtering of I/O Lines

A simple microstrip circuit shown in Fig. 2 (denoted as Board A) was constructed. Two sections of microstrip lines were connected by a low pass filter, which was formed by two SMT lumped-element ferrites and one SMT capacitor. The PCB dimension was 8 cm × 15 cm, and the dielectric was a 45-mils. thick FR-4 material. The width of the microstrip was 2 mm, and the length of each section of microstrip line was 6.3 cm and 4.2 cm respectively. The characteristic impedance of the microstrip line was 52 Ω, as calculated using the empirical equations provided in [7]. The impedance of one individual 0805 package size SMT ferrite was measured using an HP 8753D network analyzer, and the result is shown in Fig. 3. The 0805 SMT capacitor had a capacitance of 47 pF, which was verified by measurement using an HP 4291 impedance analyzer. One end of the capacitor was soldered to the ground plane directly by cutting a hole in the dielectric substrate, and "burying" the capacitor vertically into the dielectric substrate. The other end of the capacitor was soldered to the end of both SMT ferrites. The layout parasitics were then minimized. The $|S_{21}|$ was then measured using the HP 8753D network analyzer.

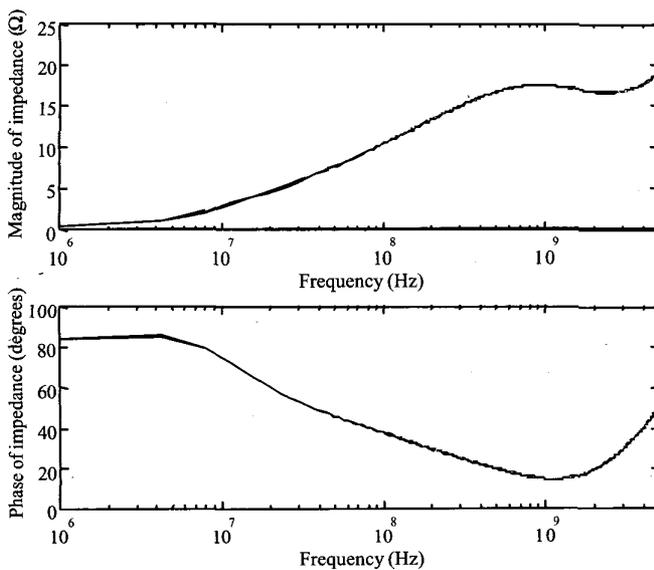


Fig. 3. Measured impedance of an 0805 package size SMT ferrite.

Fig. 4 shows the measured $|S_{21}|$ for the constructed low-pass filter. Although the layout parasitics were minimized, the effect of the shunt capacitor was limited by the parasitic inductance of the component itself. The equivalent circuit for the filtering capacitor is basically an inductor in series with an ideal capacitor and an effective series resistor. Beyond the series resonance of the equivalent circuit (approximately 920 MHz in this example), the shunt capacitor branch begins to look inductive, consequently the impedance between the microstrip line and the reference plane increases with frequency, resulting in an increase in $|S_{21}|$.

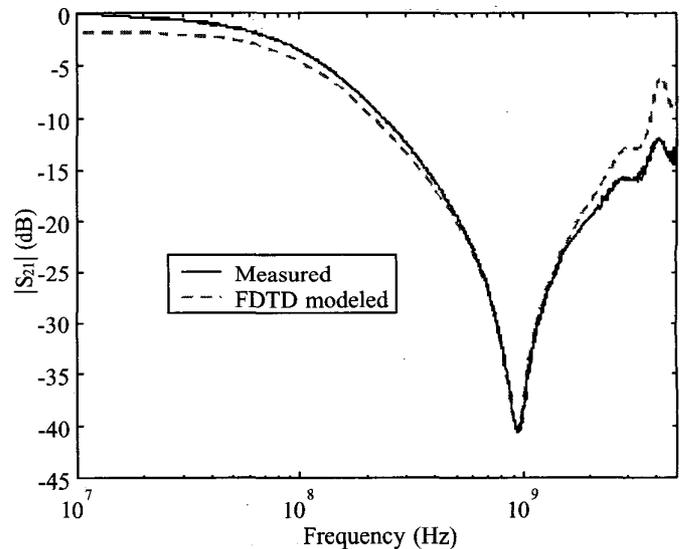


Fig. 4. Measured and FDTD modeled $|S_{21}|$ of Board A.

The finite-difference time-domain method was applied to model Board A. The two-port FDTD algorithm, which incorporates the time-domain Y-parameters of the two-port lumped-element network into the FDTD algorithm, was utilized [8]. Characterization of the two-port lumped element network was then necessary. A simple equivalent circuit of the network is shown in Fig. 5. The parasitics are included in the circuit, where R_p is the ESR of the capacitor, L_{p2} is the ESL of the capacitor, and L_{p1} is the parasitic inductance associated with the discontinuity in the transmission line at the SMT ferrite part.

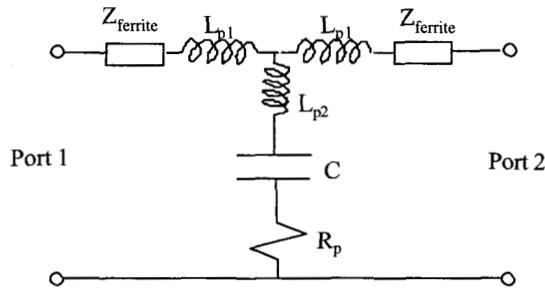


Fig. 5. A simple equivalent circuit model of the local lumped element T-network with $L_{p2} = 0.58 \text{ nH}$, $C = 47 \text{ pF}$, and $R_p = 0.4 \Omega$.

Although the ESL and ESR of the capacitor can be measured using the impedance analyzer, the actual parasitics of a component mounted on the PCB board may differ from the measurement of an individual component. An alternative approach was employed herein to determine the parasitics. The two ferrites shown in Fig. 2 were removed, and the transmission line made continuous with two short sections of copper tape with the same width of 2 mm. Therefore, the I/O line was continuous and the filter consisted of only a shunt capacitor. The $|S_{21}|$ was then measured using an HP 8753D network analyzer. The measured $|S_{21}|$ has a resonance at approximately 960 MHz. The minimum of the measured $|S_{21}|$ results from the series resonance of C and L_{p2} , and L_{p2} is then readily determined to be 0.58 nH. At the resonance, the impedance of the capacitor is purely resistive, and the ESR can be easily calculated from the $|S_{21}|$ at the minimum, which is approximately 0.4 Ω . The impedance of one individual 0805 package size SMT ferrite was measured using the HP 8753D network analyzer, and the result is shown in Fig. 3. Determination of the L_{p1} is difficult since it is related to the redistribution of the current when it flows from the transmission line through the ferrite, and can only be characterized by measurement. There are other approaches to characterize the two-port network, e.g., an overall measurement of the two-port parameters, to characterize the two-port network, as opposed to the approach described above. Once the Y-parameters are determined, the two-port network can be incorporated into the modeling using the algorithm presented in [8].

The FDTD cell size for the modeling was $0.5 \text{ mm} \times 0.5 \text{ mm} \times 0.381 \text{ mm}$. The smallest dimension was used for the board thickness. A sinusoidally modulated Gaussian pulse was applied at Port 1, and Port 2 was terminated with a 50 Ω resistive load.

The feeding probe at Port 1 and Port 2 were modeled using a thin-wire algorithm [9]. Eight perfectly matched layers (PML) were placed at each boundary plane of the computational domain [10], and seven white space layers were placed between the PML and the test board. The dielectric loss of the FR-4 material was included in the FDTD modeling using a Debye model to approximate the dispersive nature of the material [11]. Y-parameters were calculated for the filter model shown in Fig. 5, and incorporated into the FDTD modeling. In this particular case though, though three cells were used to model the thickness of the dielectric, the network port spanned only one cell. A connection was made to the trace and ground plane by adding two wires to span the other two cells of the board thickness to ensure current continuity. The connecting wires were modeled with a thin-wire algorithm. This approximation introduced additional parasitics in the modeling, since current had to neck down from the relatively wide trace to the thin wire. The parasitics can also be represented by an inductance that is similar to L_{p1} . However, these additional parasitics only affected the results at very high frequencies, in part because of the substantial series impedance of the ferrites, as shown by the comparison of the measured and modeled result in Fig. 4. Good agreement was achieved between the measurement and the modeled result for $L_{p1} = 0.5 \text{ nH}$.

The minimum layout parasitics of Board A are usually impractical in actual circuit design. It is hard to "bury" the SMT capacitor into the substrates, and fabrication typically limits the distance between the capacitor and the signal line or the reference plane. This physical distance results in a parasitic inductance, which may have a significant impact on the filtering performance at high frequencies. A second PCB board (denoted as Board B) was constructed to investigate the layout parasitics. The schematic of the board is shown in Fig. 6. The circuitry of Board B was the same as that of Board A except that a 1.8-cm long and 2-mm wide trace was introduced between the SMT capacitor and the I/O line. The length of the trace was chosen exceptionally long to demonstrate the effects of layout parasitics, and also the utility of FDTD modeling for doing engineering studies. The measured $|S_{21}|$ is shown in Fig. 7, and compared to the measured result of Board A. Board B has a better filtering performance from 100 MHz to 400 MHz due to the resonance shift. However, for higher frequencies, the layout parasitics dominates the effectiveness of the SMT capacitor, and the filtering performance of Board B is considerably worse than that of Board A. The results indicate that layout parasitics can significantly impact the performance of the EMI filter.

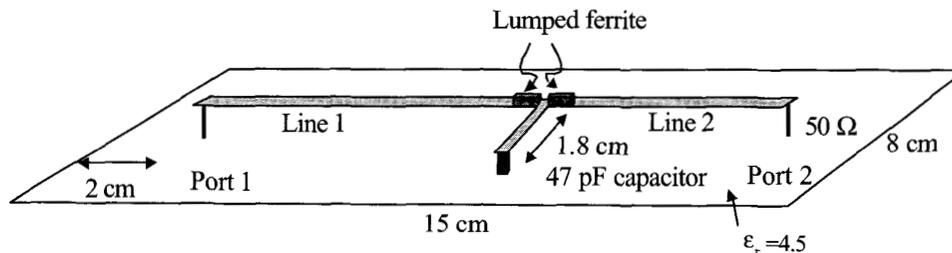


Fig. 6. Schematic of Board B.

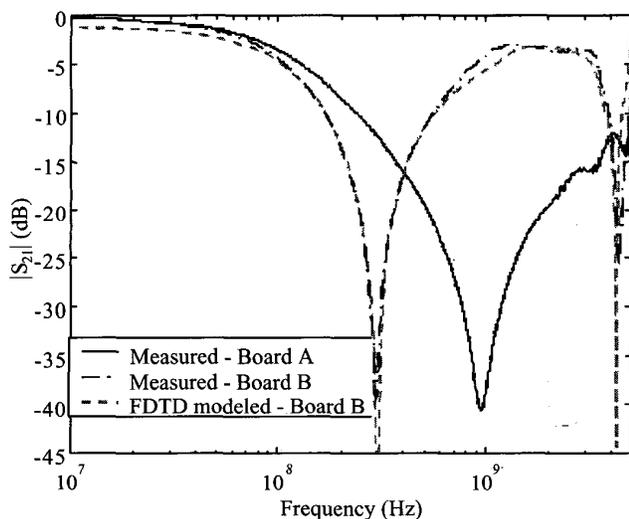


Fig. 7. Measured $|S_{21}|$ of Board A and Board B and FDTD modeled $|S_{21}|$ of Board B.

FDTD modeling of Board B was also conducted. The 1.8-cm long trace was included in the two-port network by considering the impedance looking into the capacitor from the T-junction of the trace as an equivalent lumped impedance, and then the same two-port network modeling approach as that for Board A was used. The 1.8-cm long trace was approximated as an ideal lossless transmission line with characteristic impedance of 52 Ω , and the equivalent lumped impedance was readily calculated from transmission-line theory [7]. Other FDTD modeling details were the same as those for Board A. The modeled result is also shown in Fig. 7, and good agreement was achieved again between the modeled and measured results over most of the frequency range. The $|S_{21}|$ is nearly flat between 1 GHz and 3.5 GHz because over this frequency range, the impedance of the 1.8-cm transmission line terminated with the 47 pF capacitor is relatively large, and the 50 Ω load resistance at Port 2 works as a voltage divider with the two series SMT lumped ferrites. There is some discrepancy above 4 GHz, which results in part from neglecting the dispersion and loss of the FR-4 in the length of the trace connecting the SMT capacitor. This discrepancy also illustrates the importance of including dispersion and loss for the signal propagation in the FR-4.

III. Conclusions

Layout parasitics in EMI filtering on I/O lines were investigated by $|S_{21}|$ measurements of sample PCB boards with different filter layouts. T-type I/O line filters built with lumped-element resistors and lumped ferrites were studied. It was demonstrated that the layout parasitics may have significant impact on the filtering performance of the EMI filter. An algorithm for including passive networks characterized as two-ports into the FDTD method was applied in this work. The method can also include the nonlinear behavior of ferrite

components. The two-port filtering networks were included in the modeling by incorporating the time-domain Y-parameters into the FDTD algorithm. Agreement between the measured and modeled results are favorable. The method also works using any network parameters that can be converted to Y-parameters, and, at least theoretically, for any number of ports.

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