01 May 2002

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## Recommended Citation

S. Luan and J. Fan and W. Liu and F. Xiao and J. L. Knighten and N. W. Smith and R. Alexander and J. Nadolny and Y. Kami and J. L. Drewniak, "Extracting CAD Models for Quantifying Noise Coupling Between Vias in PCB Layouts," *Proceedings of the 52nd IEEE Electronic Components and Technology Conference (2002, San Diego, CA)*, pp. 343-346, Institute of Electrical and Electronics Engineers (IEEE), May 2002.
The definitive version is available at https://doi.org/10.1109/ECTC.2002.1008118

# Extracting CAD Models for Quantifying Noise Coupling between Vias in PCB Layouts

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**Abstract**

A method to extract a lumped element prototype SPICE model is used to study noise coupling between non-parallel traces on a PCB. The parameters in this model are extracted using a PEEC-like approach, a Circuit Extraction approach based on a Mixed-Potential Integral Equation formulation (CEMPIE). Without large numbers of unknowns, the SPICE model saves computation time. Also, it is easy to incorporate into system SPICE net list to acquire the system simulation result considering the coupling between traces on the printed circuit board (PCB). A representative case is studied, and the comparison of measurements, CEMPIE simulation, and SPICE modeling are given.

## Introduction

Electromagnetic coupling or crosstalk between transmission lines is a critical issue that can affect circuit performance. Rules established to minimize crosstalk can reduce routing flexibility making the task more difficult. Prior work has focused on the theoretical analysis, and methods to reduce crosstalk between coupled transmission lines that were parallel [1], [2]. Noise in digital systems is often due to coupling between different digital nodes. In practice, noise coupling between non-parallel transmission lines is common. In this paper, the coupling mechanism of two transmission lines is presented in which the dominant portion of the coupling is between the vias of two different circuits, which are in proximity.

The full-wave modeling approach used in this work is a mixed-potential integral equation formulation with circuit extraction, denoted CEMPIE [3]. It is an application of the partial element equivalent circuit (PEEC) method in multi-layer dielectric media [4], and very suitable for DC power bus and other multi-layer planar circuit modeling. The approach extracts a SPICE compatible equivalent circuit from the first principles Maxwell-equation formulation. The non-parallel transmission lines can be modeled by CEMPIE directly [5], however, a simplified SPICE model can decrease the number of unknowns, save computation time and give accurate results. Also it is easy to incorporate into a system SPICE net list to acquire system simulation results considering coupling between traces on a PCB.

A lumped element prototype SPICE model is developed that adequately encompasses the coupling physics of the two via structures, *viz.*, a transformer that accounts for the magnetic flux from the aggressor circuit that penetrates the loop of the victim circuit, a mutual capacitance resulting from capacitance between the via pads, and capacitors for the capacitance of the via pads to ground, as shown in Figure 1. A procedure has been developed to determine the element values of the simple lumped element prototype circuit from the large SPICE model that results from the CEMPIE modeling [6], [7]. The physics-based models were then used to study noise coupling between non-parallel printed circuit traces.

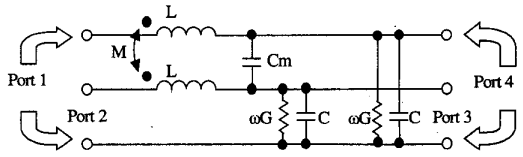


Figure 1. Lumped circuit model for parameter extraction.

The approach is more general, and also applicable to extracting physics-based, or behavioral SPICE models from more complex geometries, e.g., via signal transitions of a differential signal pair.

## Approach

The full-wave formulation of the CEMPIE approach is similar to the formulation of the integral equation method for the scattering problem. An incident electric field is assumed and Green's functions are generated for the infinite multi-layer dielectric media. Then conducting surfaces are replaced by induced surface currents and charges. By enforcing boundary conditions on these conducting surfaces for the vector sum of incident and induced electric fields, an integral equation is obtained. This equation is discretized and tested. Based on the concept of partial elements, field quantities are transformed into circuit quantities. By further assuming the electric potential over each mesh cell is constant, a final system matrix equation is established as [3]

$$[Y][\phi] = -[I^e] \qquad (1)$$

where $[I^e]$ is the impressed node current vector; $[Y]$ is the system admittance matrix and $[\phi]$ is the node based scalar electric potential vector.

If the number of external nodes is N and the total number of nodes is M, the equation (1) can be written as

$$\begin{bmatrix} Y_{11} & \cdots & Y_{1N} & Y_{1(N+1)} & \cdots & Y_{1M} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{N1} & \cdots & Y_{NN} & Y_{N(N+1)} & \cdots & Y_{NM} \\ Y_{(N+1)1} & \cdots & Y_{(N+1)N} & Y_{(N+1)(N+1)} & \cdots & Y_{(N+1)M} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{M1} & \cdots & Y_{MN} & Y_{M(N+1)} & \cdots & Y_{MM} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_N \\ V_{(N+1)} \\ \vdots \\ V_M \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_N \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (2)$$

A lumped circuit model can be constructed for an arbitrary interconnect geometry from basic physics associated with the geometry. For an N-port network, Kirchhoff's Voltage Law (KVL) gives a matrix equation that relates the port voltages to port currents as

$$[Y_{lumped}] \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} \quad (3)$$

where $[Y_{lumped}]$ is the admittance matrix for the lumped circuit prototype with unknown element values. $[V_1 \ V_2 \ \cdots \ V_N]^T$ is the port voltage vector, and $[I_1 \ I_2 \ \cdots \ I_N]^T$ is the port current vector.

Comparing equations (2) and (3), it is possible to relate the CEMPIE based admittance matrix and the admittance matrix of the proposed lumped circuit prototype,

$$[A - BD^{-1}C] = [Y_{lumped}] \quad (4)$$

where

$$[A] = \begin{bmatrix} Y_{11} & \cdots & Y_{1N} \\ \vdots & \ddots & \vdots \\ Y_{N1} & \cdots & Y_{NN} \end{bmatrix}, [B] = \begin{bmatrix} Y_{1(N+1)} & \cdots & Y_{1M} \\ \vdots & \ddots & \vdots \\ Y_{N(N+1)} & \cdots & Y_{NM} \end{bmatrix}$$

$$[C] = \begin{bmatrix} Y_{(N+1)1} & \cdots & Y_{(N+1)N} \\ \vdots & \ddots & \vdots \\ Y_{M1} & \cdots & Y_{MN} \end{bmatrix}$$

$$[D] = \begin{bmatrix} Y_{(N+1)(N+1)} & \cdots & Y_{(N+1)M} \\ \vdots & \ddots & \vdots \\ Y_{M(N+1)} & \cdots & Y_{MM} \end{bmatrix}$$

Then the values of the lumped circuit elements in the physics-based model can be extracted [6].

**Case Study**

The angle of neighboring traces on a PCB is varied. The relative position of two traces varies from parallel to vertical, to along a line. Figure 2 shows main coupling areas for different patterns.

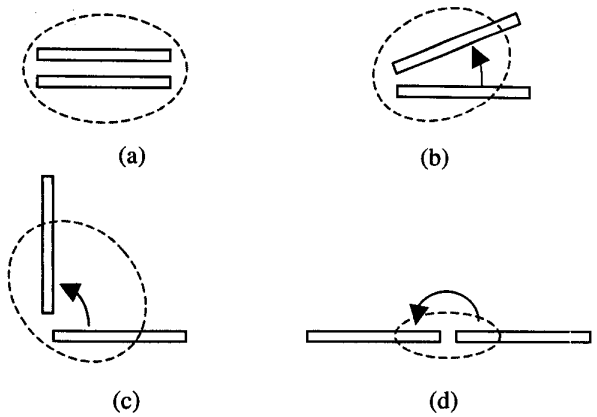


Figure 2. Coupled traces and their main coupling areas.

For the non-parallel cases the coupling mechanism has a common character, the noise coupling occurs in the main coupling area and propagates along the victim traces. The representative and the simplest case is that two traces are co-linear. In this case the coupling area is the smallest. In general, many traces have vias to connect to another layer of the board. The main coupling area is around the adjacent vias. The pattern shown in Figure 3 was selected to demonstrate the lumped element extraction method. A two-layer PCB board was made. The top layer is shown in Figure 3, and the bottom layer is the entire ground layer. The thickness of the board is 41 mils, and the substrate is FR4 with $\varepsilon_r = 4.3$. Two 3 mm wide, 60 mm long traces are put along a line. A via of diameter 1.27 mm is located at the both ends of each traces. The distance between the center of the neighboring vias is 13 mm.

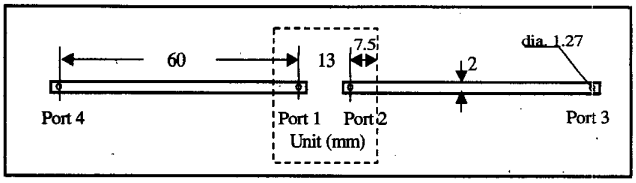


Figure 3. Typical case of non-parallel coupled traces.

A lumped circuit model for the coupling between the two ports in proximity can be constructed as shown in Figure 1. Mutual capacitance between two traces are modeled as $C_m$. Mutual inductance M is modeled for the magnetic flux from the aggressor circuit that penetrates the loop of the victim circuit. Frequency dependent dielectric loss of the trace is modeled by $\omega G$. When Port 3 and Port 4 are shorted, the admittance matrix of the lumped circuit is

$$[Y_{lumped}] = \begin{bmatrix} j\omega L & j\omega M \\ j\omega M & j\omega L \end{bmatrix}^{-1} \quad (5)$$

Comparing (5) with the CEMPIE based admittance matrix , the inductance of the trace and mutual inductance between two traces can be extracted.

Similarly, when Port 3 and Port 4 are open, at low frequency, f = 100 kHz , the dielectric loss can be ignored. The admittance matrix of lumped circuit is

$$[Y_{lumped}]=\begin{bmatrix} j\omega L+\frac{Cm+C}{j\omega(2CmC+C^2)} & j\omega M+\frac{Cm}{j\omega(2CmC+C^2)} \\ j\omega M+\frac{Cm}{j\omega(2CmC+C^2)} & j\omega L+\frac{Cm+C}{j\omega(2CmC+C^2)} \end{bmatrix}^{-1} \quad (6)$$

Then the capacitance of the trace and the mutual capacitance between two traces are obtained. Furthermore, when Port 3 and Port 4 are open,

$$Z_{lumped\,11} \approx j\omega L+\frac{G+j(Cm+C)}{-2\omega CmC-\omega C^2} \quad (7)$$

From equation (7) the dielectric loss G can be calculated.

Two modeling approaches were then used: SPICE modeling with/without trasmission lines. The SPICE model without the transmission lines is shown in Figure 4. To expand the operational frequency range, the inductance and capacitance of the trace are split into 10 segments, and the mutual inductance and mutual capacitance are put in the first segment only.

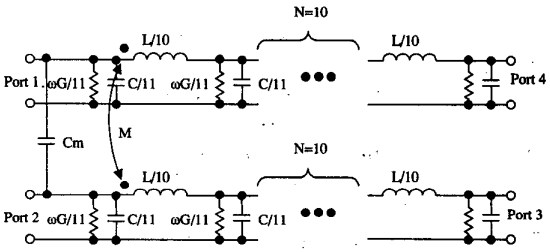


Figure 4. SPICE model without transmission line.

To decrease the computational complexity and simulation time further, the interaction outside the main coupling area can be neglected. The geometry used for the lumped element extraction is reduced to the estimated main coupling area, inside the dashed line, as shown in Figure 3. The lumped circuit model used for comparison with the CEMPIE admittance matrix is the same as shown in Figure 1. The only difference is that the two nodes are specified at the ends of the traces instead of at the vias for Port 3 and Port 4 in the CEMPIE model, as shown in Figure 5. The traces outside the main coupling area can be modeled as uncoupled transmission lines. The characteristic impedance and loss-tangent of transmission line are calculated by 2D cross sectional analysis. Figure 6 shows the SPICE model with lumped elements extracted from main coupling area.


Figure 5. Mesh pattern for CEMPIE.

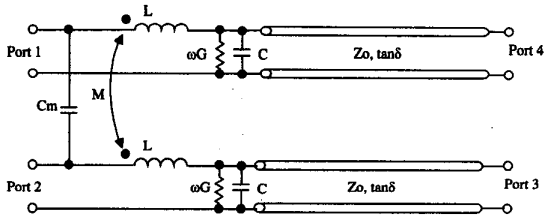


Figure 6. Transmission line including the SPICE model for the coupled vias.

**Result Comparison**

To verify the lumped SPICE model, four-port S-parameters were measured and compared with modeling results. An Agilent 8720 network analyzer was used in the measurements and a vertical SMA PCB mount jack was mounted at each port. Figure 7 shows the comparison of experimental results and the SPICE modeling results without the transmission line. The agreement is demonstrated up to 5 GHz, the deviations are less than 5 dB , except for $S_{31}$ at frequencies below 2.2 GHz and $S_{21}$ at frequencies below 0.5 GHz, when the magnitude is lower than –70 dB which is close to the limit of calibration precision of the network analyzer. Figure 8 shows that when the coupling outside the main coupling area is neglected, the result approximately agrees with the experimental curve. The deviations are less than 10 dB. The bigger the area that is considered as the main coupling area at low frequencies, the better the agreement of the simulation with the measurements.. But the computational complexity increases at the same time. So there is a balance to consider between the tolerance of error and acceptable simulation time.

Due to the limit of the measurement precision of the network analyzer, especially for the frequencies below 500 MHz, the solution of the CEMPIE simulation is also used to compared with the results of SPICE model. Figure 9 shows the comparison between the measurement and CEMPIE simulation. Figure 10 shows that the results of CEMPIE and SPICE model agree favorably in the entire frequency range. The deviations at the frequencies below 1.5 GHz are less than 2dB and they are increasing to about 10 dB when frequency is increasing from 2 GHz to 5 GHz.

**Conclusions**

This paper presents a procedure to extract simple SPICE models for quantifying noise coupling between vias in PCB layouts. Compared with a full wave method, the simple SPICE model saves computation time, provides controllable accuracy and can be easily used in system-level simulation. Approximate agreement among the SPICE model, CEMPIE solution and experimental results have been shown for a typical case. For the typical case examined, where the coupling was dominated by the coupling between vias, results were within 5 dB of measurements. For the more simplified model, where the inclusion of a transmission line section forced all coupling to occur near the vias, results were within 10 dB of measurements.

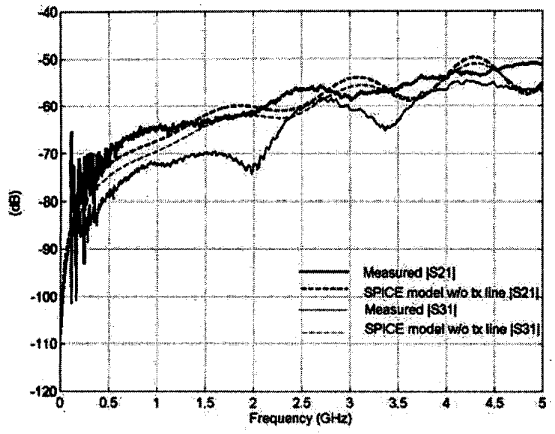


Figure 7. Comparison of experimental results and SPICE model without transmission line.

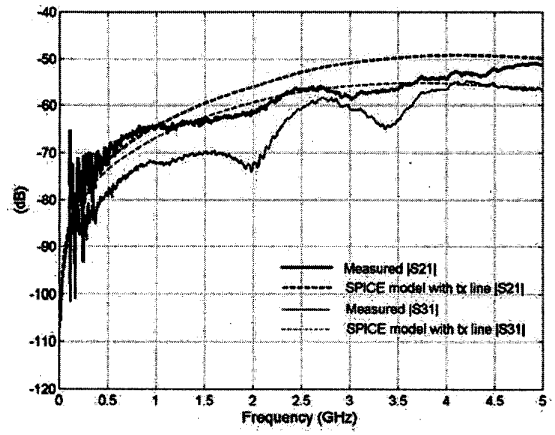


Figure 8. Comparison of experimental results and SPICE model with transmission line.

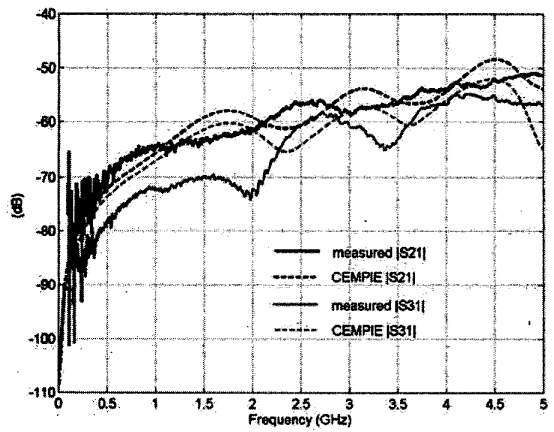


Figure 9. Full-wave CEMPIE simulation vs. experimental.

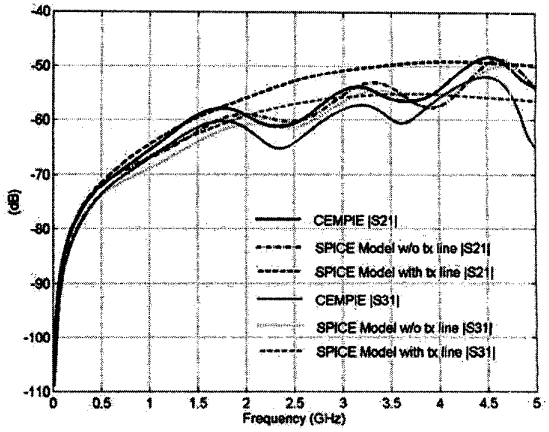


Figure 10. Full-wave CEMPIE simulation vs. SPICE model with transmission line.

**References**


1. Eged, B. *et al*, "Reduction of Far-end Crosstalk on Coupled Microstrip PCB Interconnects", *IEEE Instrumentation and Measurement Technology Conference, 1994 IMTC/94 Conference Proceedings. 10th Anniversary. Advanced Technologies in I & M.* Vol. 1 (1994), pp. 287-290.
2. Dai, S. *et al*, "The Analysis and Reduction of Crosstalk on Coupled Microstrip Lines Using Nonuniform FDTD Formulation", *Microwave Symposium Digest. IEEE MTT-S International.* Vol. 1 (1996), pp. 307-310.
3. Fan, J. *et al*, "Modeling DC Power-Bus Structures with Vertical Discontinuities Using a Circuit Extraction Approach Based on a Mixed-Potential Integral Equation Formulation", *IEEE Transaction on Advanced Packaging*, Vol. 24, No. 2 (2001), pp. 143-157
4. Ruehli, A. E., "Equivalent Circuit Models for Three Dimensional Multiconductor Systems" *IEEE Trans. on Microw. Theory and Techn.*, MTT-22(3) (1974), pp. 216-221.
5. Luan, S., *et al*, "Noise Coupling from Non-parallel PCB Trace Routing", *IEEE Int. Symp. Electromagn. Compat. 2002*, to be published.
6. Fan, J., Modeling and Design of DC Power Buses in High-Speed Digital Circuit Designs, Ph. D thesis, University of Missouri-Rolla, 2000.
7. Fan, J., *et al*, "Calculation of Self and Mutual Inductances Associated with Vias in a DC Power Bus Structure from a Circuit Extraction Approach Based on a Mixed-Potential Integral Equation Formulation", *Proceedings of the 14th International Zurich Symp. And Technical Exhibition on EMC*, Zurich, Switzerland, Feb. 2001, pp. 521-526.