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Experimental Evaluation of Power Bus Decoupling on a 4-Layer Printed Circuit Board

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Abstract: The switching of active devices on printed circuit boards (PCBs) can cause a momentary surge or drop in the power bus voltage. Decoupling capacitors are often utilized to alleviate this problem. They help to stabilize the power bus voltage by supplying transient current to active devices. The decoupling strategy, including where to place the high-frequency decoupling capacitors, is often a topic of debate. This paper examines the effect of decoupling capacitor placement on a 4-layer printed circuit board. Some design guidelines are provided.

power plane was divided into two power islands, Region 1 and Region 2. The testing locations in Region 2 are illustrated in Figure 1. In Region 1, 7 bulk decoupling capacitors and 29 high-frequency decoupling capacitors were employed. In Region 2, 4 bulk decoupling capacitors and 24 high-frequency decoupling capacitors were employed. The values of the bulk decoupling capacitors were 100 μF , 22 μF , or 10 μF . The values of the high-frequency decoupling capacitors were 0.1 μF , 0.47 μF , or 1 μF .

Introduction

The purpose of a power bus in a printed circuit board is to distribute current at a constant voltage to all of the active devices. Due to the power bus impedance, the switching of integrated circuits (ICs) on a PCB can cause momentary surges or drops in the power bus voltage. This phenomenon, called ground bounce or delta-I noise, can be a problem in high-speed PCB designs because the voltage shifts can be large enough to interfere with the normal operation of other components connected to the same power bus. Decoupling capacitors help to stabilize the power bus voltage by supplying transient current to ICs when they switch. Decoupling strategies for multi-layer printed circuit boards were examined by T. H. Hubing et al. [1]. An investigation of power bus decoupling in 4-layer populated printed circuit boards was described in [2]. The effects of decoupling capacitors as a function of location in both populated and unpopulated 4-layer PCBs are further investigated in this study. In addition, the special case of a noise source and decoupling capacitor sharing the same connections to a power or ground plane is examined.

Experimental Setup

The test board was a 4-layer fully populated personal computer motherboard as shown in Figure 1. The top and bottom layers were signal layers, the second layer was the ground plane and the third layer was the power plane. The

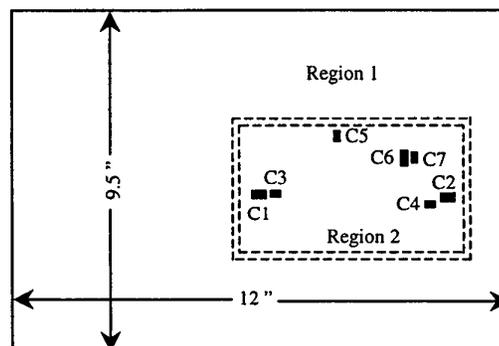


Figure 1. Board Layout

For the S-parameter measurements, two low impedance semi-rigid probes were attached to the testing locations through the bonding pads of existing decoupling capacitors, as shown in Figure 2. An HP8753D network analyzer was connected to the test ports and used to measure S parameters. A signal was injected at Port 1 and the amplitude of the transmitted signal at Port 2 was measured. $|S_{21}|$, the ratio of the transmitted signal to the injected signal, was plotted versus frequency. The lower the $|S_{21}|$ level, the better the isolation and the more effective the decoupling capacitors.

Decoupling on Populated Board

To illustrate the effect of the high-frequency decoupling capacitors, some of them were removed in stages from the populated board while monitoring the measured transfer coefficient. The results at three different stages are shown in Figure 3. The measurement ports were located at C1 and C2 in

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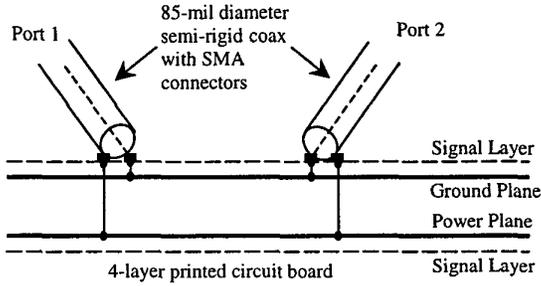


Figure 2. Test Configuration

Region 2. The measured $|S_{21}|$ with all decoupling capacitors in place is indicated by the lowest solid curve in Figure 3. Two 100 nF decoupling capacitors were then removed from locations C3 and C4 near Ports 1 and 2, respectively. The board was re-measured and the result is shown by the middle dashed curve, which is 3-7 dB higher than the solid curve at almost all frequencies. This indicates that the decoupling capacitors near the ports are effective throughout this frequency range. Next, another five decoupling capacitors distant from both ports in Region 2 were removed from the board. This time only a slight increase in the $|S_{21}|$ response was observed, primarily below 200 MHz. This increase is mainly due to the increase in the interconnection inductance of the parallel decoupling capacitor array. Since there were about 22 high-frequency capacitors left in Region 2, pulling five capacitors out increased the overall interconnection inductance by about 23%, which accounts for a 2 dB increase in the $|S_{21}|$ response. Individually, decoupling capacitors far from the ports have almost no effect on the power bus noise.

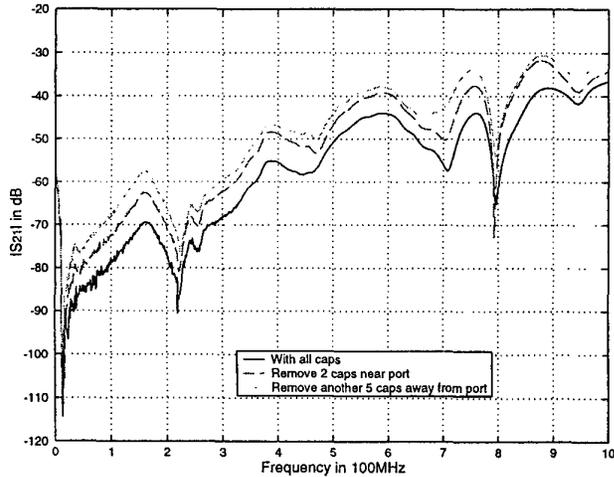


Figure 3. $|S_{21}|$ of the Populated Board when Removing Decoupling Capacitors

This observation was further demonstrated by measurements of the power bus noise spectrum. A Tektronix 2712 spectrum

analyzer was connected to the probe at C1 to measure the power bus voltage spectrum. Again capacitors were removed in the same three stages used in the $|S_{21}|$ measurements. The results are shown in Figures 4, 5, and 6. Compared to Figure 4, the spectrum in Figure 5 increased 3-7 dB for almost all harmonics, which indicates the two decoupling capacitors near the measurement ports were very effective in the measured frequency range. However, Figure 6 shows little or no further increase in the power bus spectrum when the other five capacitors were removed, indicating that the five capacitors distant from the measurement ports had little effect. Notice that the changes in the $|S_{21}|$ measurements show good agreement with the change in the power bus spectrum measurements, therefore, $|S_{21}|$ can be used as a good indication of power bus decoupling effectiveness.

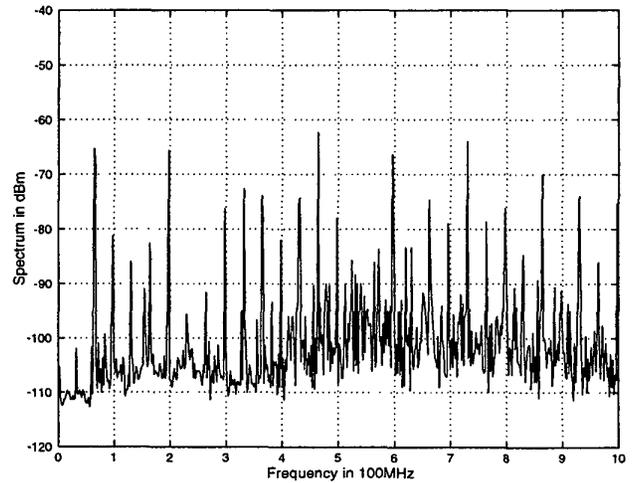


Figure 4. Power Bus Spectrum of the Populated Board with all Decoupling Capacitors

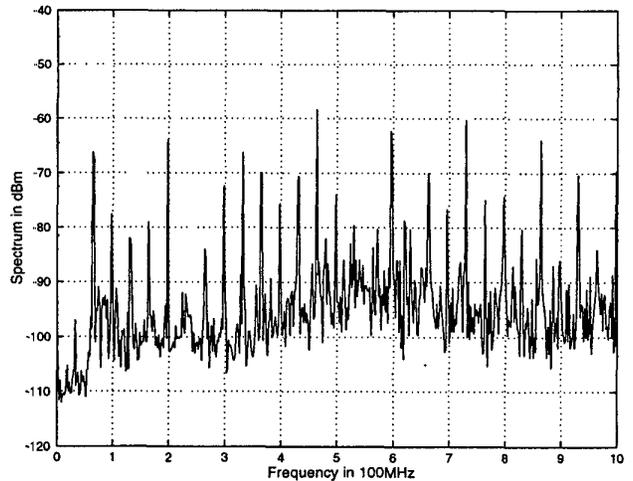


Figure 5. Power Bus Spectrum of the Populated Board with two Capacitors near Ports Removed

Mutual Inductance in 4-Layer PCBs

Mutual inductance between component vias and decoupling capacitor vias plays a significant role in 4-layer board decoupling. For boards with closely spaced power and ground planes, the ICs initially draw transient currents from the plane rather than individual decoupling capacitors. As a result, the locations of decoupling capacitors are not critical [1] and high-frequency decoupling capacitors can be evenly distributed over the board. However, the plane spacing in 4-layer boards is often 40 mils or larger. With this much space between the planes, the magnetic coupling between component vias and capacitor vias is significant, causing the ICs to draw transient current from the closest decoupling capacitors rather than from the planes [2].

In general, on 4-layer boards, the closer the decoupling capacitor is to the noise source, the higher the mutual inductance and the more effective the decoupling. If the decoupling capacitor shares the Vcc or ground via of an IC that pulls current between the planes, the mutual inductance between them will be maximized.

Figure 8 illustrates the power bus decoupling when the decoupling capacitor shares a Vcc or the ground pad with the noise source. The measured $|S_{21}|$ for a distant capacitor is included for reference. Port 1 was mounted at location C6 and Port 2 at C1. A 100nF decoupling capacitor was soldered between the power pad of C6 and ground pad of C7. Port 1 and the decoupling capacitor share the same connection to the power plane as illustrated by Figure 9a. Then, the capacitor was soldered between the ground pad of C6 and power pad of C7 and the board was measured again. Port 1 and the decoupling capacitor share the same ground connection as shown in Figure 9b. As shown in Figure 8, when the capacitor shares the ground pad with Port 1, the $|S_{21}|$ level is 7 dB lower than the reference level. When the capacitor shares the power pad with Port 1, the $|S_{21}|$ level is 15 dB lower than the reference. As expected, the configuration that maximizes the mutual inductance is the most effective.

Summary

The measured data presented in this paper demonstrates power bus decoupling in a 4-layer PCB as a function of capacitor location. Mutual inductance plays an important role in power bus decoupling above the parallel resonant frequencies of high-frequency decoupling capacitors. When the decoupling capacitors and the IC are in close proximity, mutual inductance between their vias encourages the active device to draw most of the transient current from the nearest decoupling capacitors when switching. Moving the decoupling capacitor closer to the active device increases the mutual inductance and therefore increases the effectiveness of power bus decoupling. Therefore, in 4-layer boards or boards that don't have closely spaced power-ground plane pairs, it is important to locate

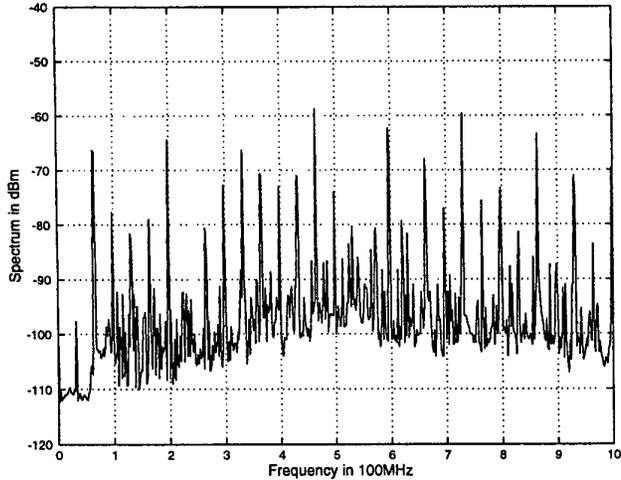


Figure 6. Power Bus Spectrum of the Populated Board with Another Five Capacitors Distant from Ports Removed

Decoupling on an Unpopulated Board

As shown in Figure 3, the decoupling capacitors near the test ports are effective at nearly all frequencies, while the capacitors away from the ports do not have much effect above 200 MHz. This observation can be verified by adding capacitors one at a time to an unpopulated version of the test board. Again Port 1 was located at C1 and Port 2 was located at C2. A 100 nF capacitor was attached at Location C3 and then C4. As shown in Figure 7, when the decoupling capacitor is far from Port 1, it is only effective below its parallel resonant frequency at around 100 MHz. Above 100 MHz, it has little effect. However, when the capacitor is attached near Port 1, it is effective to the upper end of the measured frequency range.

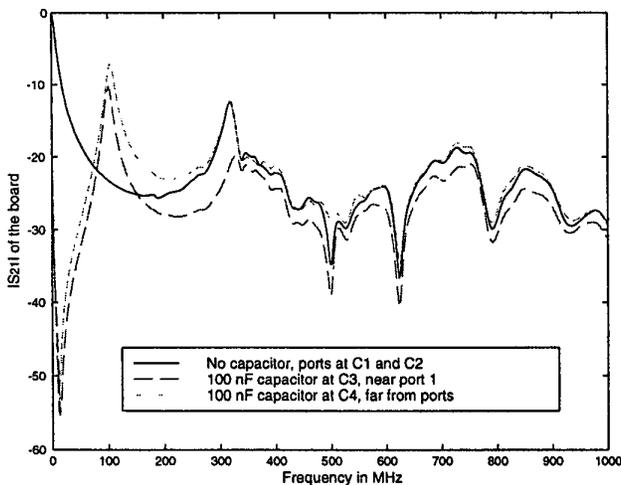


Figure 7. $|S_{21}|$ of the Unpopulated Board when Adding Decoupling Capacitors

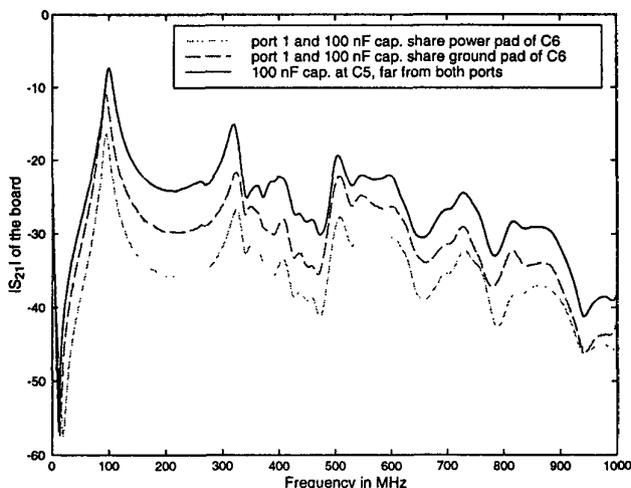


Figure 8. $|S_{21}|$ when Capacitor Sharing Pads with Port 1

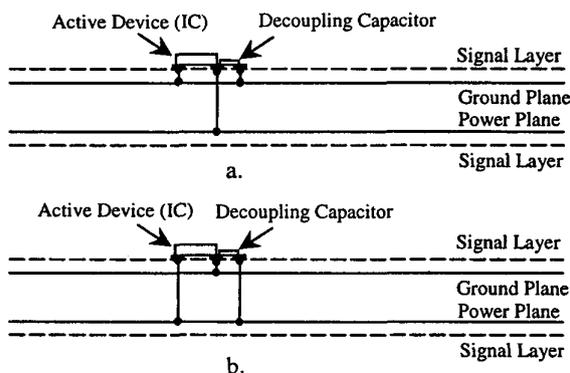


Figure 9. Active Device and Decoupling Capacitor Sharing the Same Power or Ground Pad

decoupling capacitors near ICs. Decoupling is maximized when the capacitor via that draws current from the farthest plane is located nearest the IC power or ground via that draws current from the farthest plane.

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