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EMI Resulting From a Signal Via Transition Through DC Power Bus — Effectiveness of Local SMT Decoupling

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Abstract

Signal vias are commonly used in multi-layer printed circuit board (PCB) design. For a signal via transitioning through the internal power and ground planes, the return current has to jump from one reference plane to another reference plane. The discontinuity of the return current at the via excites the power and ground planes, and results in power bus noise, and can produce an EMI problem as well. Numerical methods, such as finite-difference time-domain (FDTD), Moment Methods (MoM), and partial element equivalent circuit (PEEC), were employed herein to study this problem. The modeled results were supported by the measurements. In addition, the EMI mitigation approach of adding decoupling capacitors was investigated with the FDTD method.

I. Introduction

Routing a signal trace on different planes is widely used in multi-layer PCB design due to increasing board density. The DC power bus is usually placed as entire internal planes, and the inter-plane capacitance is beneficial for EMC purposes. A typical routing of the signal trace with a via transition on a 4-layer board is shown in Figure 1. The signal transitions through a via that penetrates the internal DC power bus, and the signal trace is referenced to dif-

ferent planes on the opposite board sides. At high frequencies, the signal return current at the via has to make a transition from the lower reference plane to the upper reference plane. Since the interplane capacitance of the reference planes provides a nominally low-impedance path (except at certain resonance frequencies), the current may return by displacement current. As a result, this return displacement current excites the power planes, and results in an EMI problem. Similar problems were studied with the via parameters extracted from the analysis of via interconnects [1]. In addition, the waveforms at the source and load for a signal trace with via transitions were previously studied for signal integrity purposes [2]. In an effort to mitigate the EMI resulting from a signal via transition, decoupling capacitors might be placed near the via to provide a low-impedance path for the return current. However, the impedance of the decoupling capacitor interconnect will limit the effectiveness of this strategy. The EMI resulting from the DC power bus due to the signal transition through vias, and placing decoupling capacitors to mitigate the problem are studied herein with numerical methods. The modeled results were supported by measurements on the constructed experimental boards.

II. EMI modeling and measurements

EMI resulting from the DC power bus with a via transition was studied by modeling

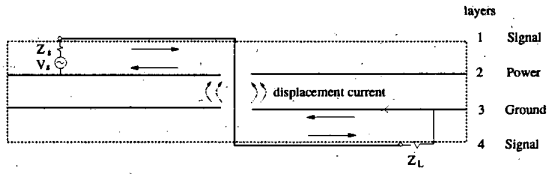

Figure 1. A signal via transitioning through internal power and ground planes.

and measuring an experimental board. For this purpose, the 4-layer test board was constructed to have internal power and ground planes, and a signal via transition. The configuration of the board is shown in Figures 2 and 3. A signal trace was routed on the top and bottom planes, and connected by a via penetrating the power and ground planes. The line-width of the signal trace was 10 *mils.*, and the trace had a microstrip line structure. The characteristic impedance of the singal trace was 88 Ω, and the bottom trace was terminated with a 91 Ω resistor. The length of the signal trace on the top and bottom planes was 5 *cm.* The test board had a dimension of 15 *cm* $\times$ 10 *cm*, a dielectric constant of 3.5, and a layer spacing of 45 *mils.* For investigating the EMI from the power planes, probes were attached to the power planes, and S-parameters were measured. An HP8753D network analyzer was used to measure the $|S_{21}|$ of the test board. Port 1 of the network analyzer was connected to the signal trace on the top plane, and Port 2 was connected to the power planes, as shown in Figure 3. Two 0.085" semi-rigid coaxial ca-

ble probes were built and soldered to the test board to make the $|S_{21}|$ measurements. The same configuration was modeled with FDTD to calculate the $|S_{21}|$. In the FDTD modeling, the signal trace was modeled with one PEC cell in width, and the dielectric layer was modeled with three cells. The cell size was 1 mm $\times$ 0.254 mm $\times$ 0.356 mm, and the total number of cells was 3.4 million. A thin-wire algorithm was used for modeling the signal via [3]. A modulated Gaussian source with 50 Ω impedance was placed at Port 1, and Port 2 was modeled with a 50 Ω load so that the ports of the network analyzer were correctly modeled. The time step was 5.7 $\times$ 10^{-13} sec, and 40,000 time steps were used to record the time history of the voltages and currents at Port 1 and Port 2. In addition, the dielectric loss of the board was modeled with an effective conductivity [4]. The effective conductivity was 4 $\times$ 10^{-5} S/cm in the modeling from 100 MHz to 2 GHz. Other numerical methods, such as MoM [5] and PEEC [6], were used to model this test board, and $|S_{21}|$ calculated. For MoM modeling, the patch size was approximately 1/10th of the shortest wavelength, and 3000 unknowns were used and solved. The power and ground planes were modeled as zero-thickness conductors. For PEEC modeling, the cell size was approximately 1/12th of the shortest wavelength, with an unknown number of 4500. The modeled and measured results of $|S_{21}|$ are shown in Figure 4. In general, the results agree well from 100 MHz to 2 GHz. The peaks of the $|S_{21}|$ are due to the TM_{mn} modes of the DC power bus. In particular, the peaks at 790 MHz and 1.06 GHz correspond to the TM_{01} and TM_{20} modes. The results indicate that the power bus is excited by the via transition.

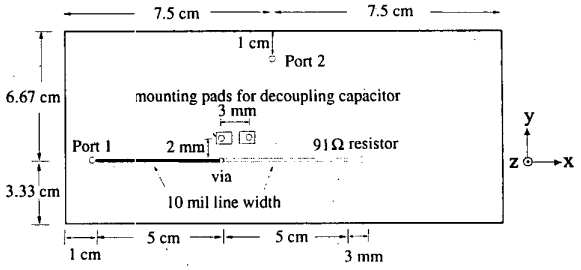

Figure 2. The top view of the test board with a signal via transition.

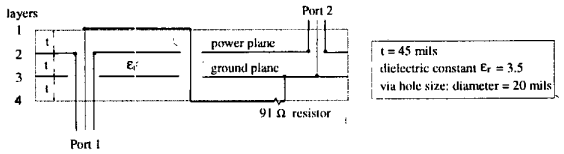

Figure 3. The configuration of the two port measurements on the power planes.

Decoupling capacitors are often used as an EMI mitigation strategy. To test the effect of a local decoupling capacitor, an SMT decoupling capacitor was placed near the via transition on the test board, and was modeled with FDTD. For the same 4-layer PCB geometry, the decoupling capacitor was placed 2 mm away from the via, as shown in Figure 2. The capacitor was 0.01 μF, and had a 0.1 Ω resistance in series. The values of the capacitor were determined from measurements. The interconnections

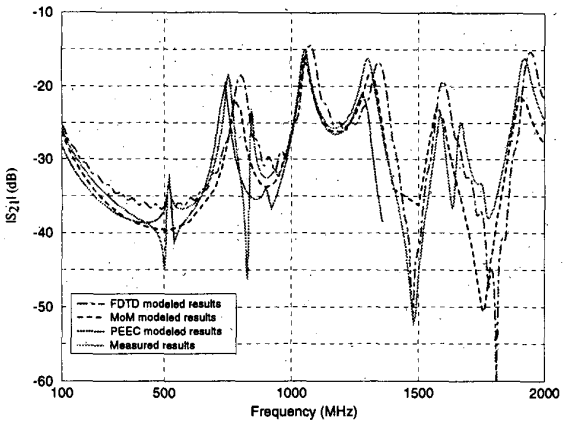

Figure 4. The modeled and measured results of $|S_{21}|$ of the test board.

of the capacitor with the power bus were also modeled in the FDTD modeling. Both the modeled and measured results of $|S_{21}|$, as shown in Figure 5, showed little improvement with this decoupling capacitor present on the board. This suggests the impedance of the SMT capacitor interconnect was significant compared with the impedance of the DC power bus parallel planes. The interconnect inductance in this study was significant in part due to the thickness of the test board. Therefore, at high frequencies, the return current primarily takes the displacement current path. To further study the use of the decoupling capacitor for EMI mitigation, four decoupling capacitors were placed around the via symmetrically. The location of the capacitors, and the FDTD modeled $|S_{21}|$ are shown in Figure 6. Two values of decoupling capacitors, 0.01 μF and 0.1 μF, were chosen, and the results of $|S_{21}|$ are identical above 100 MHz. The peak at 250 MHz is due to the interconnect inductance of the capacitors resonanting with the power bus inter-plane capacitance. Although a decrease of 2 to 8 dB in $|S_{21}|$ is found at the peaks above 700 MHz, placing multiple capacitors for every via transition is difficult to implement in a high-density PCB design. Other EMI mitigation approaches, such as placing capacitors uniformly on the board, and adding losses in series with the decoupling capacitors, must be used to mitigate the EMI resulting from the via transitions.

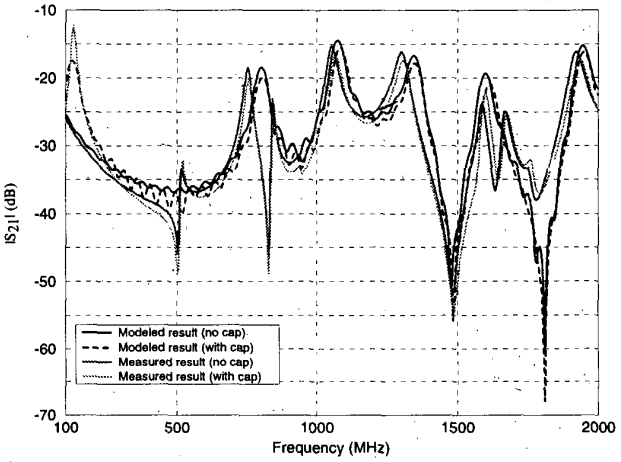

Figure 5. The modeled and measured results of $|S_{21}|$ with a local decoupling capacitor.

III. Conclusions

Signal via transitioning through the DC power bus can result in significant EMI problems. This EMI problem can be studied and modeled with numerical methods. The numerical modeling is accurate and facilitates the analysis of the resulting EMI from the PCB with varying board thickness, di-

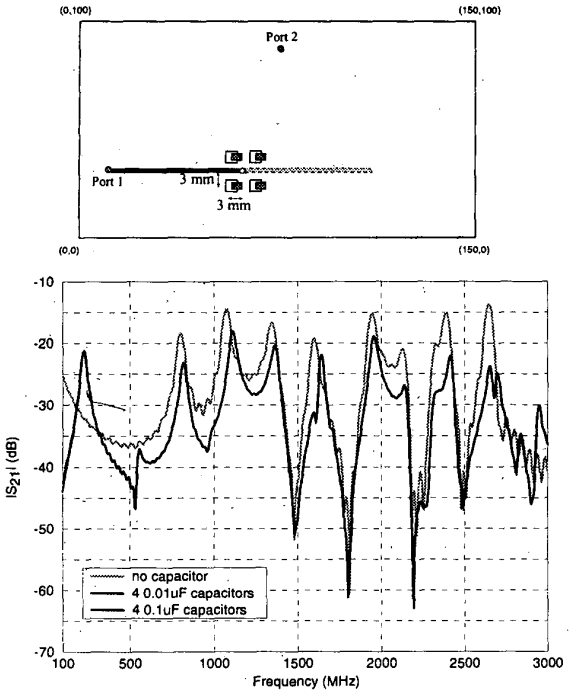

Figure 6. The modeled results of $|S_{21}|$ with four local decoupling capacitors.

electric constant, and decoupling capacitor location. The effect of the local SMT decoupling is dependent on the interconnects of the capacitors. Therefore, minimizing the interconnect inductance is useful to mitigate the EMI from the power bus. In addition, a low inter-plane impedance of the power bus can help the current return. This can be achieved by using a small layer spacing, and a proper dielectric constant.

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