01 Aug 2000

EMC Analysis of an 18" LCD Monitor

Theodore M. Zeeff

Todd H. Hubing
Missouri University of Science and Technology

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

Richard E. DuBroff
Missouri University of Science and Technology, red@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1005

Recommended Citation

T. M. Zeeff et al., "EMC Analysis of an 18" LCD Monitor," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2000, Washington, D.C.)*, vol. 1, pp. 169-173, Institute of Electrical and Electronics Engineers (IEEE), Aug 2000.
The definitive version is available at https://doi.org/10.1109/ISEMC.2000.875557

EMC Analysis of an 18" LCD Monitor

Theodore M. Zeeff, Todd H. Hubing,
James L. Drewniak, Richard E. DuBroff, Thomas P. Van Doren

Electromagnetic Compatibility Laboratory
Department of Electrical and Computer Engineering
University of Missouri-Rolla
Rolla, MO 65409

Abstract: This paper describes a case study covering the evaluation and reduction of the radiated EMI from an 18" Liquid Crystal Display (LCD) monitor. The evaluation was completed in two parts: first potential EMI sources at the Printed Circuit Board (PCB) level were identified, then the EMI antennas driven by these sources were analyzed. Methods for reducing the EMI were described in detail, and where applicable, those modifications were applied. Radiated measurements demonstrate the effectiveness of these recommendations.

I. Introduction

This EMC case study focuses on the evaluation of the 18" LCD monitor depicted in Figure 1. The LCD monitor consists of an LCD module, a Main PCB and a few auxiliary PCB's. The LCD module contains a liquid crystal array, a few interfacing PCB's and a fluorescent light. The Main PCB translates display information coming from a personal computer into a digitally processed signal that can be used by the LCD Module. The auxiliary PCB's generate power for the fluorescent light and relay information from push buttons on the front of the monitor to the Main PCB.

Four shields were used to encase different parts of the LCD monitor. Shield #1 encloses the LCD Module. Shield #2 surrounds the Main PCB. Shield #3 fits over Shield #2 and attaches to Shield #1. Shield #4 covers one of the auxiliary PCB's, the inverter PCB, which powers the fluorescent light of the LCD module.

Circuits inside the LCD monitor operate at a range of clock frequencies. The analog input RGB data is digitized with a clock rate ranging from 35 MHz to 138 MHz depending on the display resolution. In addition, memory chips used by the main processor are clocked from 80 MHz to 101 MHz depending on the display resolution. The digital display data is processed at the same clock rate as the A/D converters, but the output from the main processor is clocked at a fixed 42.5 MHz.

Figure 2 shows the radiated spectrum of the LCD from 0 MHz to 1000 MHz. In this measurement, the output clock is running at 42.5 MHz, the A/D clock is running at 78 MHz, and the memory clock runs at 80 MHz.

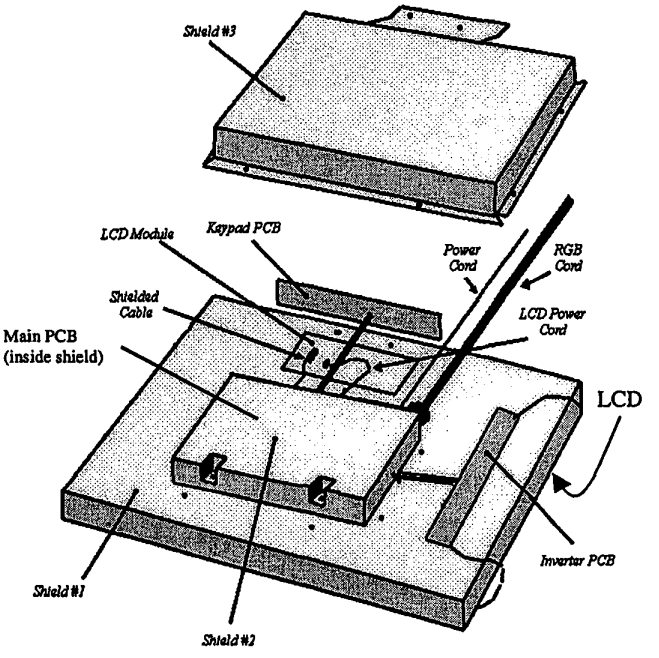

Figure 1: A depiction of the 18" LCD Monitor

II. EMI Improvements for the LCD Monitor

The EMI analysis quickly focused on the Main PCB since frequency harmonics generated exclusively on this PCB dominated the radiated spectrum. All EMI improvements on the Main PCB can be grouped into three broad categories: decoupling, trace routing, and power island placement.

Decoupling: In the time domain, decoupling capacitors behave like charge sources, supplying current that opposes change in the power bus voltage. In the frequency domain, decoupling capacitors lower the impedance of the power source. In either case, attention must be given to how the capacitors are connected. If there is too much inductance in the decoupling path (interconnect inductance), the capacitor will not be able to supply current fast enough and the impedance looking into the power bus will rise. Excessive interconnect inductance

0-7803-5677-2/00/$10.00 ©2000 IEEE

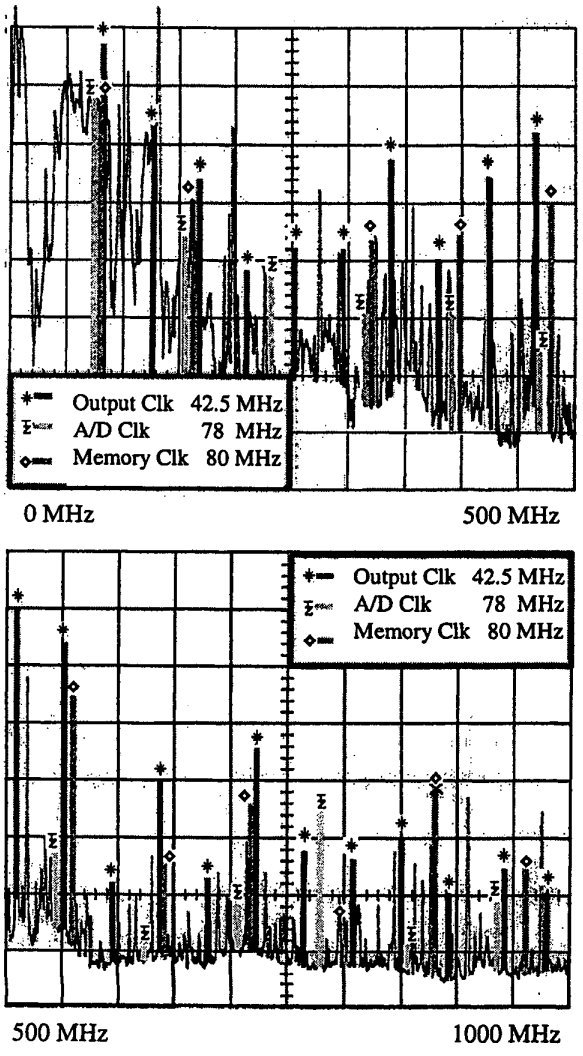

Figure 2: Radiated EMI from the 18" LCD Monitor

will reduce a capacitor's effectiveness and may lead to noisy power planes capable of driving EMI antennas.

Decoupling capacitance can be divided into three different categories: bulk, local and interplane. Bulk decoupling capacitors provide charge at low frequencies (sub-MHz range). Local decoupling capacitors provide charge at higher frequencies (up to many 100's of MHz). At very high frequencies, the capacitance between the power and ground planes, called interplane capacitance, becomes the primary source of decoupling current.

The decoupling scheme on the original design of the Main PCB needed improvement. For instance, the bulk capacitors were not optimally placed. Bulk decoupling capacitors can be placed wherever it is most convenient on a PCB with power planes because at the low frequencies the bulk capacitors operate, the extra inductance in the power bus is negligible[1].

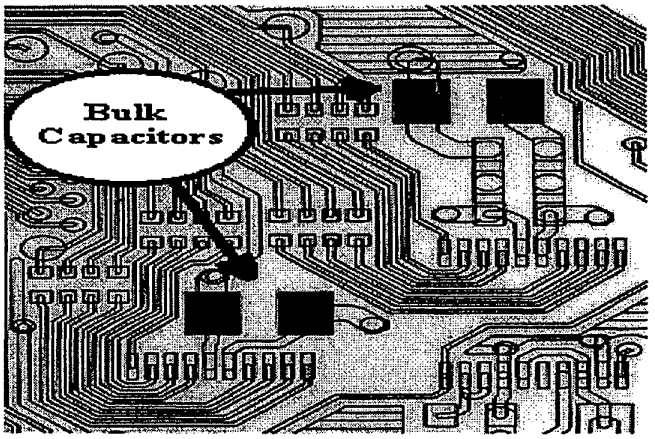

Figure 3: Bulk capacitors placed in a region of high trace density

In this design, the bulk decoupling capacitors on the Main PCB were placed close to IC's where the trace density was high. Moving the bulk decoupling capacitors out of this area does not degrade low-frequency decoupling and allows more room on the PCB for routing critical signal traces. Figure 3 shows how bulk decoupling capacitors were placed in regions of high trace density.

Local decoupling capacitor connections were in need of improvement too. Local decoupling capacitors need to be close to the IC's on PCB's with power planes separated by more than roughly 30 mils [2]. Additionally, the interconnect inductance between the local decoupling capacitors and the power bus needs to be minimized for best results. For the most part, local decoupling capacitors on the Main PCB were placed close to the IC's. However, many local decoupling capacitors were connected to the power bus poorly. In many instances multiple local decoupling capacitors were connected to the power and ground planes through a shared trace. Each of these shared traces had only one via to ground or power meaning all capacitors on the traces shared one via. Local decoupling capacitors connected in this manner have too much interconnect inductance. Figure 4 shows how some of the local decoupling capacitors were placed on the PCB. A better way to connect local decoupling capacitors would be to provide each capacitor with 2 vias at the pads; one via connected directly to the ground plane and the other via connected directly to the power plane. Additionally, decoupling capacitors and IC's should not share power or ground vias if this means running a trace to the decoupling capacitor. To achieve the best results, the vias from the decoupling capacitors and IC's should be positioned to maximize the mutual inductance between the vias. To maximize mutual inductance, the longer of the power or ground vias on both devices should be placed next to one another. In this case, both decoupling capacitor and IC were placed on the topside of the PCB and the stackup from the top to bottom was Signal-Ground-Power-Signal. The longest via from the topside would be the power via for both capacitor

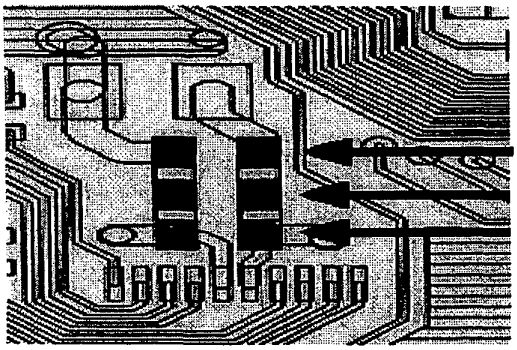

Figure 4: Three capacitors in parallel sharing the same traces and vias to power and ground

and IC. Therefore the power vias from the decoupling capacitor and the IC should be placed as close as possible to one another. If the capacitor were on the opposite side of the board, as shown in Figure 5, then the power via of the IC and the ground via of the capacitor would be placed as close as possible to one another.

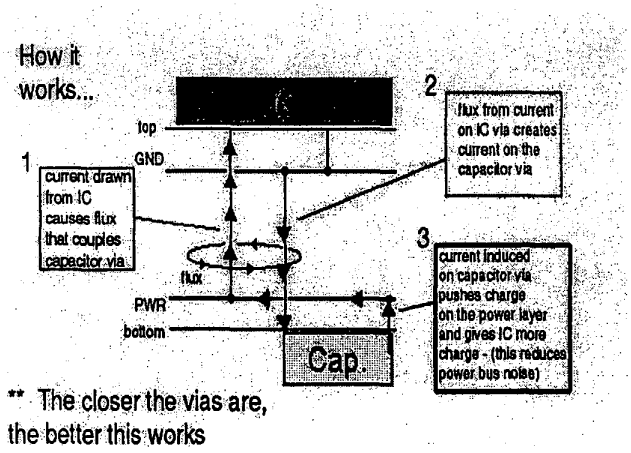

Figure 5: Mutual capacitance between a ground via of a decoupling capacitor and the power via of an IC

Interplane capacitance can be increased by maximizing the mutual surface area between the power and ground layers. In this design, several patches of ground were routed on the power layer. By removing those patches of ground and replacing them with existing power islands on the power layer, the interplane capacitance was increased.

Trace routing: Designers are often tempted to place gaps in the ground layer of printed circuit boards. These gaps may be the result of high-speed clock lines or other traces routed in the ground layer. Sometimes gaps are put in the ground layer to isolate low-frequency areas of the board from high-frequency circuitry. Gaps may inadvertently result due to keep-out areas for connector pins. When return currents are forced to flow around gaps in the ground layer, a potential difference develops across the gap. This potential difference can be an EMI liability.

On the Main PCB, there were several places where traces on the signal layer crossed gaps on the adjacent ground layer. For instance, high-speed data and address lines on the signal layer crossed over a gap in the ground layer created by a clock trace routed on the ground layer. This is shown in Figure 6.

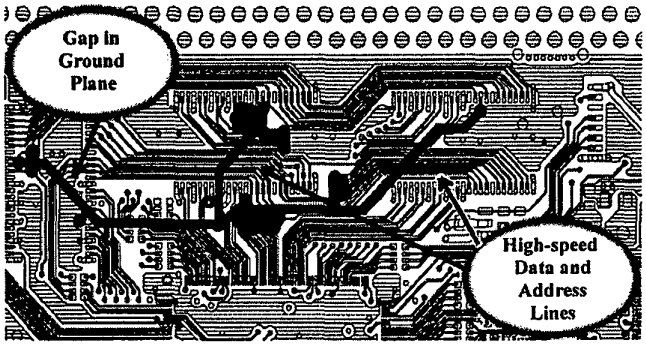

Figure 6: High-speed traces on the top layer crossing a gap in the adjacent ground layer

An isolation gap in the ground layer was used to isolate power circuitry from digital circuitry. However, any advantage to creating this gap will be lost if high-speed traces on an adjacent layer cross over it [3]. In an earlier prototype, the isolation gap was too long, and consequently, several analog RGB traces on an adjacent layer crossed over the gap. Figure 7 shows how RGB traces crossed the gap in the ground plane. Shorting the isolation gap or routing the RGB traces around the gap eliminates a potential EMI source.

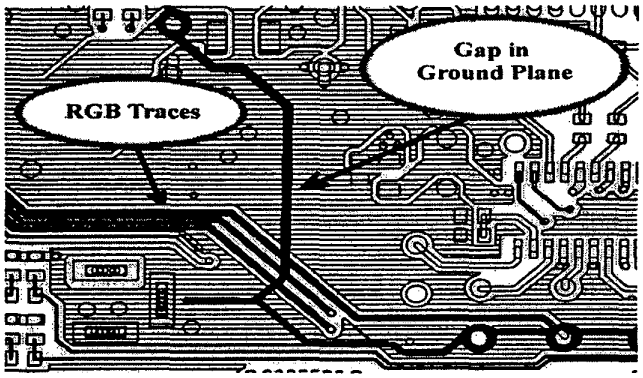

Figure 7: Input RGB traces crossing a gap in the ground plane

Power island placement: The power layer of the Main PCB was divided into many different power islands. As a result, there were many gaps on the power layer. These gaps become a potential EMI liability when return currents from signal traces on the adjacent layer flow around these gaps [4]. To

minimize the potential EMI sources, the number of traces in adjacent layers crossing these gaps was reduced by moving or restructuring power islands. For instance, in Figure 8, a 12-volt power plane that ran the entire length of the PCB should have been routed on the signal layer. In Figure 9, a power island could be moved so RGB signals do not cross any gaps. To further reduce the number of potential EMI sources, only low-speed signal traces were routed on the adjacent signal layer

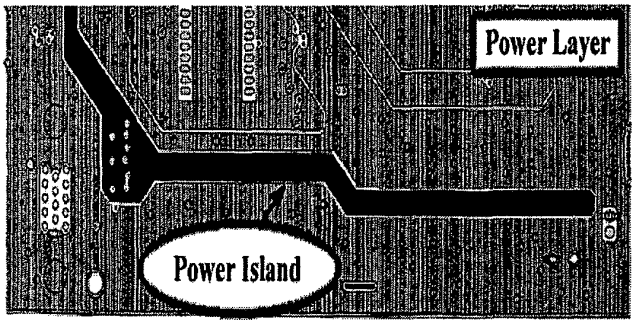

Figure 8: Power island that should be routed on the signal layer to avoid creating a large gap in the power plane

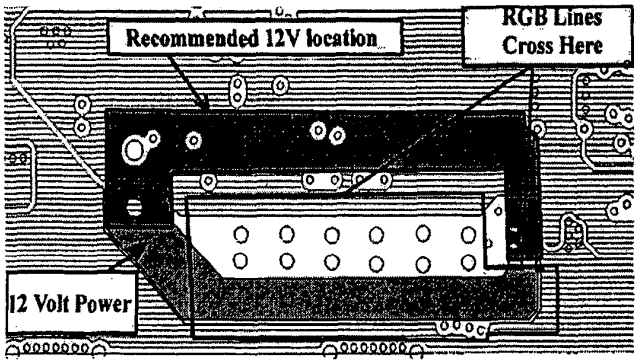

Figure 9: Moving a 12-volt power island so RGB traces on an adjacent layer will not cross the gap created by the power island

III. Locating EMI Antennas

There were many possible EMI antennas on the LCD monitor. To find out which of the possible EMI antennas is the largest contributor to EMI, the method of selective shielding was used. Selective shielding involves shielding all possible antennas with Cu-tape or Al-foil and then selectively exposing one of the possible antennas at a time. Using this method, the contribution of each antenna was quantified.

The most significant EMI antenna was found to be Shield #1 being driven against Shield #2. This antenna is shown in Figure 10. While Shield #1 and Shield #2 are connected to one another by 4 screws, at high frequencies these screws do not provide a good electrical connection. The poor connection between these two shields created an antenna. To eliminate this antenna, fingerstock was placed between both shields. EMI tests showed an average decrease of 2-3dB below 500 MHz, and an average decrease of 5-10 dB above 500 MHz with the fingerstock in place.

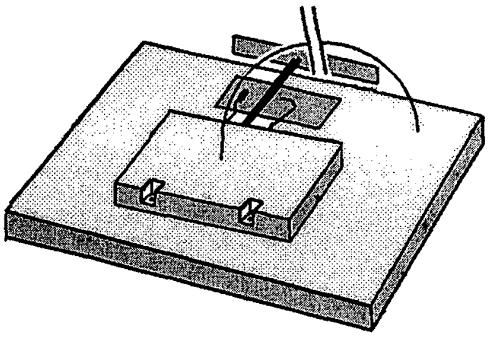

Figure 10: EMI antenna between Shield #1 and Shield #2

Another EMI antenna, shown in Figure 11 was identified as Shield #2 driven against the inverter PCB, the auxiliary PCB that powered the fluorescent light. To reduce emissions from this antenna, a ferrite was wrapped around the cable between the two structures. Measurements showed a slight decrease in the radiated EMI of 2-3 dB from 800 MHz to 1000 MHz. Although the reduction was low, using a ferrite was justified since the monitor required additional attenuation at those frequencies.

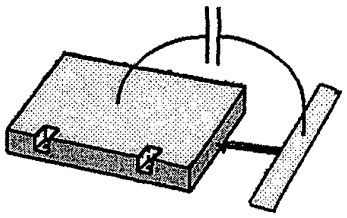

Figure 11: EMI antenna between Shield #2 and the auxiliary PCB

Several other low-speed cables required ferrites to reduce EMI. The bundle of wires between the Main PCB and the keypad PCB, and the cable supplying power to the LCD Module PCB from the Main PCB carried enough noise currents to justify adding ferrites to the cables.

The shielded cable carrying high-speed display data between the Main PCB and the LCD Module was not connected to Shield #2 at the point where it left the shield. Leaving the cable shield unconnected to Shield #2 allowed noise current

from the Main PCB to exit Shield #2 and be radiated. Therefore, a connection between the high-speed data cable's outer shield and Shield #2 was established. Radiated measurements indicated a large decrease for one harmonic of the 42.5 MHz output clock and a modest decrease in frequencies around 800 MHz when this connection was established.

The RGB cable and the power cable that both entered Shield #2 and connected to the Main PCB did not contribute significantly to the radiated EMI and required no modification.

IV. Results of Recommendations

When all of the methods of reducing radiated EMI were implemented, additional radiated measurements were made. Figure 12 shows the radiated measurements before changes were made to the EMI antennas and Figure 13 shows the radiated EMI after changes were made to the EMI antennas.

Below 500 MHz, all clock harmonics were down 3-5 dB, some were down 10 dB. Above 500 MHz, most clock harmonics were down 5 dB. Several were down by more.

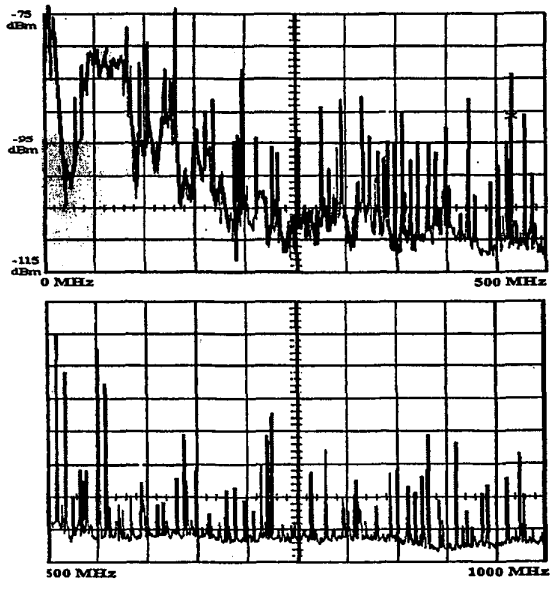

Figure 12: Radiated EMI measurement without any modifications to the EMI antennas

IV. Conclusions

The most significant EMI sources in the LCD monitor did not originate from the LCD panel itself, but from the Main PCB that processed and converted analog RGB data into a digital signal used by the LCD panel. The primary EMI sources were

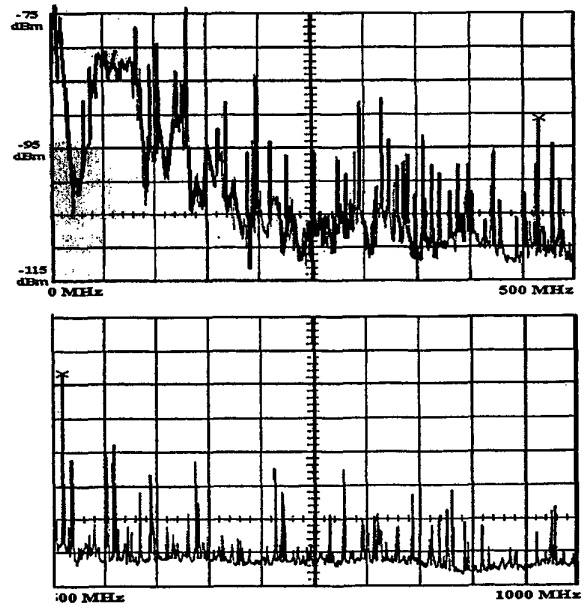

Figure 13: Radiated EMI measurement after changes were made to the EMI antennas

the differential clocks used by the A/D converter, main processor and memory chips. Potential EMI sources, such as the output from an LVDS IC, did not significantly contribute to EMI as was initially thought. EMI antennas consisted primarily of shields that were not adequately bonded to one another, while others consisted of PCB's connected by poorly filtered cables. Modest design changes resulted in 3-5 dB or more reduction in radiated EMI over a wide range of frequencies.

References

[1] T. Hubing, T. Van Doren, F. Sha, J. Drewniak and M. Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility, Atlanta, GA, August 1995, pp. 308-312.

[2] T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," IEEE Transactions on Electromagnetic Compatibility, vol. EMC-37, no. 2, May 1995, pp. 155-166.

[3] S. Britt, D. Hockanson, F. Sha, J. Drewniak, T. Hubing, and T. Van Doren. "Effects of Gapped Ground Planes and Guard Traces on Radiated EMI," Proceedings of the 1997 IEEE International Symposium on Electromagnetic Compatibility, Austin, TX, August 1997, pp. 159-164

[4] Ge Chang, *Investigation of Current Return Paths in Four Printed Circuit Board Configurations*, University of Missouri-Rolla M.S.E.E Thesis, August 1999.